Intel® Server Board S815EBM1

Technical Product Specification

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Date	Revision Number	Modifications
August 2001	-001	First release of the Intel® Server Board S815EBM1 Technical Product Specification
March 2002	-002	Updated document to reflect addition of serial port header. Added Errata section.

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1. Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for Intel® Server Board S815EBM1.

1.1 Intended Audience

The TPS is intended to provide detailed, technical information about the S815EBM1 board and it's components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

1.2 What This Document Contains

- Chapter 2: A description of the hardware used on the S815EBM1 board
- Chapter 3: A map of the resources of the board
- Chapter 4::The features supported by the BIOS Setup program
- Chapter 5: The contents of the BIOS Setup program's menus and submenus
- Chapter 6: A description of the BIOS error messages, beep codes, and POST codes

2. Product Description

2.1 Overview

2.1.1 Feature Summary

Table 1 summarizes the major features of the S815EBM1 server board.

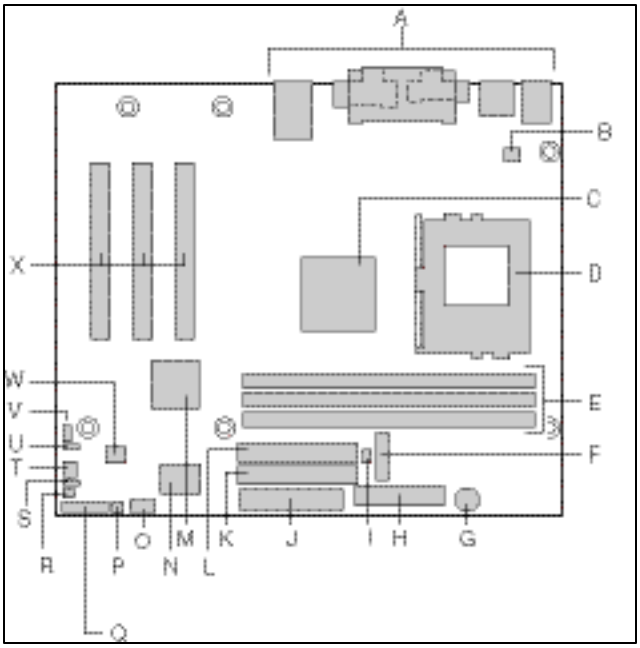
Table 1. Feature Summary

Form Factor	**microATX (9.6 inches by 8.2 inches)**
Processor	Support for either an Intel® Pentium® III processor in a Flip Chip Pin Grid Array (FC-PGA or FC-PGA2) package or an Intel® Celeron™ processor in an FC-PGA package
Memory	• Three 168-pin SDRAM Dual Inline Memory Module (DIMM) sockets • Support for up to 512 MB system memory • Support for single row or double row DIMMs
Chipset	The S815EBM1 board includes the Intel® 815E Chipset, consisting of: • Intel® 82815 Graphics and Memory Controller Hub (GMCH) • Intel® 82801BA I/O Controller Hub (ICH2) • 4 megabit Firmware Hub (FWH) (STM M50FW040)
I/O Control	SMSC LPC47M132 LPC bus I/O controller
Video	Intel 82815 integrated graphics support
Peripheral Interfaces	• Four Universal Serial Bus (USB) ports • One serial port and one serial port header • One parallel port • Two IDE interfaces with Ultra DMA, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports
Expansion Capabilities	Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2)
BIOS	• Intel® / AMI* BIOS (stored in an STM M50FW040 4 megabit FWH) • Support for Advanced Power Management (APM), Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Hardware Monitor Subsystem	• Voltage sense to detect out of range values • Two fan sense inputs used to monitor fan activity
SCSI LED Connector	Allows add-in SCSI host bus adapters to use the same LED as the on-board I/O controller
Chassis fan connector	Connector for an additional chassis fan
Chassis Intrusion Connector	Detects chassis intrusion
LAN Subsystem	Intel® 82562ET 10/100 megabit/sec Platform LAN Connect (PLC) device
Wake on LAN* Technology Connector	Support for system wake up using an add-in network interface card with remote wake up capability

For information about	Refer to
• The board's compliance level with APM, ACPI, Plug and Play, and SMBIOS	Table 2, page 6

2.1.2 Board Layout

Figure 1 shows the location of the major components on the S815EBM1 board.



Item	Description	Item	Description
A	Back panel connectors	M	Intel 82801BA I/O Controller Hub (ICH2)
B	Processor fan connector (fan 1)	N	SMSC LPC47M132 super I/O controller
C	Intel 82815E GMCH	O	Serial Port B Header
D	370-pin processor socket	P	SCSI hard drive activity LED connector
E	DIMM sockets	Q	Front panel switch/LED connector
F	Battery	R	Chassis intrusion connector
G	Speaker	S	Alternate front panel power LED connector
H	Main power connector	T	Chassis fan connector (fan 2)
I	Chassis fan (fan 3)	U	BIOS configuration jumper block
J	Floppy drive connector	V	Wake on LAN technology connector
K	Primary IDE connector	W	4 megabit Firmware Hub (FWH)
L	Secondary IDE connector	X	PCI expansion slots

Figure 1. Board Components

2.1.3 Block Diagrams

Figure 2 is a block diagram of the major functional areas of the S815EBM1 board.

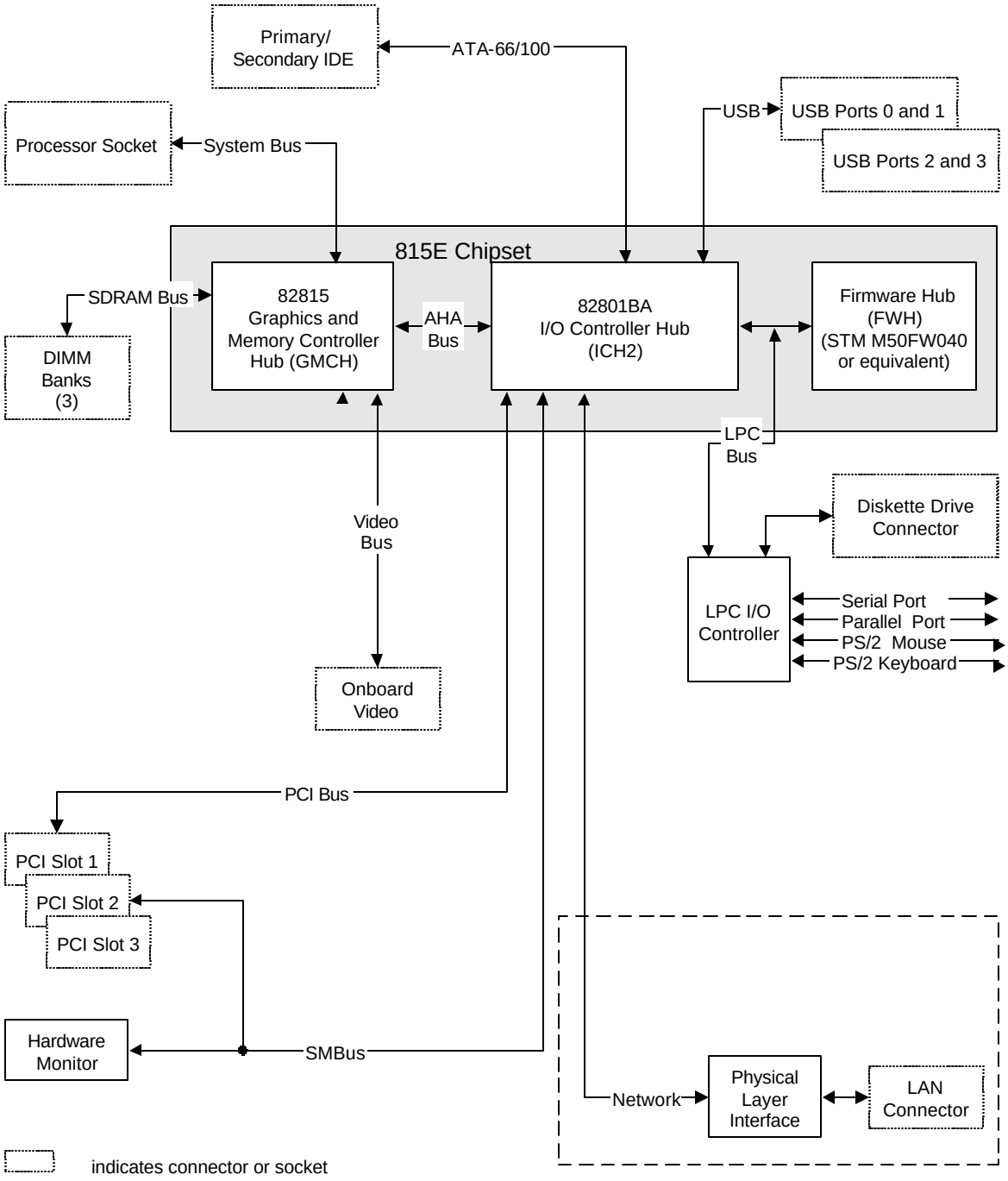


Figure 2. Block Diagram for the S815EBM1 Board

2.2 Online Support

For information about	Refer to:
• Intel's S815EBM1 board under "Product Info" or "Customer Support"	http://support.intel.com/support/motherboards/Server
• Processor data sheets	http://www.intel.com/design/litcentr
• ICH2 addressing	http://developer.intel.com/design/chipsets/datashts
• LAN software and drivers	http://support.intel.com/support/network/

2.3 Operating System Support

The S815EBM1 board supports drivers for all of the on-board hardware and subsystems under the following operating systems:

- RedHat* Linux 7.1
- Windows* 2000 Advanced Server

NOTE

Other drivers may be offered by other vendors.

2.4 Design Specifications

Table 2 lists the specifications applicable to the S815EBM1 board.

Table 2. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
ACPI	Advanced Configuration and Power Interface Specification	Version 2.0, July 27, 2000. • Compaq Computer Corporation • Intel Corporation • Microsoft Corporation • Phoenix Technologies Limited • Toshiba Corporation	http://www.teleport.com/~acpi/
AMI BIOS	American Megatrends BIOS Specification	AMIBIOS 99, 1999. • American Megatrends, Inc.	http://www.amij.com/amibios/bios.platforms.Server.html
APM	Advanced Power Management BIOS Interface Specification	Version 1.2, February 1996. • Intel Corporation • Microsoft Corporation	http://www.microsoft.com/hwdev/busbios/amp_12.htm
ATA/ ATAPI-5	Information Technology - AT Attachment with Packet Interface - 5 (ATA/ATAPI-5)	Revision 3, February 29, 2000 • Contact: T13 Chair, Seagate Technology	http://www.t13.org/
ATX	ATX Specification	Version 2.03, December 1998 • Intel Corporation	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
EPP	IEEE Std 1284.1-1997 (Enhanced Parallel Port)	Version 1.7, 1997 • Institute of Electrical and Electronic Engineers	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	Bootable CD-ROM Format Specification	Version 1.0, January 25, 1995 • Phoenix Technologies Limited • International Business Machines Corporation	http://www.phoenix.com/PlatSS/products/specs.html
LPC	Low Pin Count Interface Specification	Version 1.0, September 29, 1997 • Intel Corporation	http://www.intel.com/design/chipsets/industry/lpc.htm
MicroATX	microATX Motherboard Interface Specification	Version 1.0, December 1997 • Intel Corporation	http://www.formfactors.org/developer/specs/microatx/microatxspecs.htm
PCI	PCI Local Bus Specification	Version 2.2, December 18, 1998 • PCI Special Interest Group	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998 • PCI Special Interest Group	http://www.pcisig.com/

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
Plug and Play	Plug and Play BIOS Specification	Version 1.0a, May 5, 1994 • Compaq Computer Corporation • Phoenix Technologies Limited • Intel Corporation	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
SDRAM	PC SDRAM Unbuffered DIMM Specification	Revision 1.0, February 1998 • Intel Corporation	http://www.intel.com/technology/memory
	PC SDRAM Specification	Revision 1.7, November 1999 • Intel Corporation	http://www.intel.com/technology/memory
	PC Serial Presence Detect (SPD) Specification	Revision 1.2B, November 1999 • Intel Corporation	http://www.intel.com/technology/memory
UHCI	Universal Host Controller Interface Design Guide	Revision 1.1, March 1996 • Intel Corporation	http://www.usb.org/developers
USB	Universal Serial Bus Specification	Version 1.1, September 23, 1998 • Compaq Computer Corporation • Intel Corporation • Microsoft Corporation • NEC Corporation	http://www.usb.org/developers
WfM	Wired for Management Baseline	Version 2.0, December 18, 1998 • Intel Corporation	http://developer.intel.com/ial/WfM/wfmspecs.htm

2.5 Processor

CAUTION

Use only the processors listed below. The use of unsupported processors can damage the board, the processor, and the power supply. See the *Intel® Server S815EBM1 Specification Update* for the most current list of supported processors for the S815EBM1 board.

The S815EBM1 board supports a single Pentium® III or a Celeron™ processor. The system bus frequency is automatically selected. The S815EBM1 board supports the processors listed in Table 3.

Table 3. Supported Processors

Type	Designation	System Bus Frequency	L2 Cache Size
Intel Pentium III processor in an FC-PGA2 package	1.0 GHz [1], 1.26 GHz, 1.4 GHz	133 MHz	512 KB
	1.13 GHz, 1.26 GHz	133 MHz	256 KB
Intel Pentium III processor in an FC-PGA package	533EB, 600EB, 667, 733, 800B, 866, and 933 MHz; 1.0 GHz[1]	133 MHz	256 KB
	500E, 550E, 600E, 650, 700, 750, 800, and 850 MHz	100 MHz	256 KB
Celeron processor in an FC-PGA package	800 and 850 MHz	100 MHz	128 KB
	533A, 566, 600, 633, 667, 700, 733, and 766 MHz	66 MHz	128 KB

Note:

1. Support of the 1GHz Pentium III processor is dependent upon the package type. S815EBM1 Fan Heat Sink (FHS) supports only FCPGA2 packaging type. Customers can determine S815EBM1 support at this speed by product's specification.

All supported on-board memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

For information about	Refer to
• Product information on supported processors	Section 2.2, page 5

2.6 System Memory

CAUTION

Before installing or removing memory, make sure that AC power is disconnected by unplugging the power cord from the computer. Failure to do so could damage the memory and the board.

NOTE

To be fully compliant with all applicable Intel® SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency

The S815EBM1 board has three DIMM sockets and supports the following memory features:

- 3.3 V (only) 168-pin SDRAM DIMMs with gold-plated contacts
- Unbuffered single row or double row DIMMs
- Maximum total system memory: 512 MB; minimum total system memory: 64 MB
- 133 MHz SDRAM or 100 MHz SDRAM
- Serial Presence Detect (SPD) and non-SPD memory
- Non-ECC and ECC DIMMs (ECC DIMMs will operate in non-ECC mode only)
- Suspend to RAM

When installing memory, note the following:

- Non-SPD DIMMs will always revert to a 100 MHz with 3-3-3 timing SDRAM bus.
- Mixing Non-SPD DIMMs with SPD DIMMs will always revert to a 100 MHz with 3-3-3 timing SDRAM bus.
- The BIOS will not initialize installed memory above 512 MB.
- Mixed memory speed configurations (133 and 100 MHz) will default to 100 MHz.
- 133 MHz SDRAM operation requires a 133 MHz system bus frequency processor.
- The board should be populated with no more than four rows of 133 MHz SDRAM (two double-row or one double-row plus two single-row DIMMs).
- 100 MHz SDRAM may be populated with six rows of SDRAM (three double-row DIMMs).

NOTES

- At boot, the BIOS displays a message indicating that any installed memory above 512 MB has not been initialized.
- If more than four rows of 133 MHz SDRAM are populated, the BIOS will display a message indicating that it will initialize installed memory up to 512 MB at 100 MHz.

For information about	Refer to
• Obtaining the PC Serial Presence Detect (SPD) Specification	http://www.intel.com/technology/memory

Table 4 lists the supported DIMM configurations.

Table 4. Supported Memory Configurations

DIMM Capacity	Number of Rows	SDRAM Density	SDRAM Organization Front-side / Back-side	Number of SDRAM devices
32 MB	DR	16 megabit	2 M x 8/2 M x 8	16 [1]
32 MB	SR	64 megabit	4 M x 16/empty	4
48 MB	DR	64/16 megabit	4 M x 16/2 M x 8	12 [1, 2]
64 MB	DR	64 megabit	4 M x 16/4 M x 16	8
64 MB	SR	64 megabit	8 M x 8/empty	8
64 MB	SR	128 megabit	8 M x 16/empty	4
96 MB	DR	64 megabit	8 M x 8/4 M x 16	12 [1, 2)]
96 MB	DR	128/64 megabit	8 M x 16/4 M x 16	8 [1, 2)]
128 MB	DR	64 megabit	8 M x 8/8 M x 8	16 [1]
128 MB	DR	128 megabit	8 M x 16/8 M x 16	8 [1, 2]
128 MB	SR	128 megabit	16 M x 8/empty	8
128 MB	SR	256 megabit	16 M x 16/empty	4
192 MB	DR	128 megabit	16 M x 8/8 M x 16	12 [1, 2]
192 MB	DR	128/64 megabit	16 M x 8/8 M x 8	16 [1, 2]
256 MB	DR	128 megabit	16 M x 8/16 M x 8	16 [1, 2]
256 MB	DR	256 megabit	16 M x 16/16 M x 16	8 [1, 2]
256 MB	SR	256 megabit	32 M x 8/empty	8
512 MB	DR	256 megabit	32 M x 8/32 M x 8	16 [1, 2)]

Notes:

1. If the number of SDRAM devices is greater than nine, the DIMM will be double row.
2. Front side population/back side population indicated for SDRAM density and SDRAM organization.
3. In the second column, “DR” refers to double row memory modules (containing two rows of SDRAM) and “SR” refers to single row memory modules (containing one row of SDRAM).

2.7 Chipset

This section describes the Intel® 815E Chipset used by the S815EBM1 board.

2.7.1 Intel® 815E Chipset

The Intel 815E chipset consists of the following devices:

- 82815 Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801BA I/O Controller Hub (ICH2) with AHA bus
- Firmware Hub (FWH) (STM M50FW040)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the AHA bus. The ICH2 is a centralized controller for the board's I/O paths. The FWH provides the non-volatile storage for the BIOS.

The Intel 815E chipset provides the interfaces shown in Figure 3.

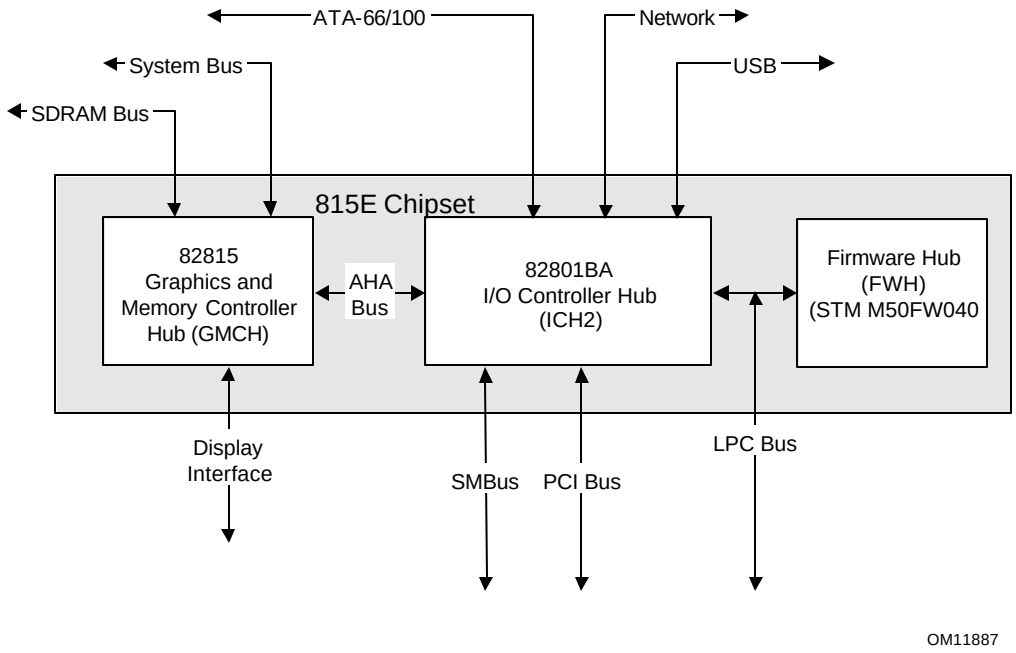


Figure 3. Intel 815E Chipset Block Diagram

For information about	Refer to
• The Intel 815E chipset	http://developer.intel.com/design/chipsets/815e
• The resources used by the chipset	Chapter 3, page 28
• The chipset's compliance with ACPI	http://www.teleport.com/~acpi/
• The chipset's compliance with APM	http://www.microsoft.com/hwdev/busbios/amp_12.htm

2.7.1.1 Intel® 82815 Graphics and Memory Controller Hub (GMCH)

The GMCH provides the following:

- An integrated synchronous DRAM memory controller with autodetection of SDRAM
- Support for ACPI Rev. 2.0 and APM Rev. 1.2 compliant power management

2.7.1.2 Intel® 82801BA I/O Controller Hub (ICH2)

The ICH2 provides the following:

- 33 MHz PCI bus interface
- Support for up to four PCI master devices
- A Low Pin Count (LPC) interface that supports an LPC-compatible I/O controller
- Support for two master / DMA devices
- An integrated IDE controller that supports Ultra DMA (33 MB/sec) and ATA-66/100 mode (66 MB/sec, 100 MB/sec)
- An integrated LAN Media Access Controller
- A Universal Serial Bus interface with two USB controllers providing four ports in a UHCI Implementation
- Power management logic for ACPI Rev. 1.0b compliance
- A System Management Bus
- A real-time clock with 256-byte battery-backed CMOS RAM

2.7.1.2.1 IDE Interfaces

The ICH2 IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): CPU controls data transfer.
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.

- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2 ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Table 55 on page 74.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The S815EBM1 board supports Laser Servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's boot menu to one of the following:

- ARMD-FDD (ATAPIremovable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
• The location of the IDE connectors	Table 32, page 42
• The signal names of the IDE connectors	Table 32, page 42
• BIOS Setup program's Boot menu	Table 62, page 80

2.7.1.2.2 USB

The ICH2 contains two separate USB controllers. The S815EBM1 board has four USB ports. One USB device can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. The S815EBM1 board fully supports the Universal Hub Controller Interface (UHCI).

The S815EBM1 board's four USB ports are implemented with stacked back panel connectors, routed through the ICH2.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use only shielded cables that meets the requirements for full-speed devices.

For information about	Refer to
• The signal names of the back panel USB connectors	Table 19, page 35
• The UHCI design guide	http://www.usb.org/developers
• The USB specification	http://www.usb.org/developers

2.7.1.2.3 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock provides a time-of-day clock and a multicentury calendar with alarm features. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE
If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS SRAM at power-on.

2.7.1.3 Firmware Hub (FWH)

The system BIOS is stored in the 4 megabit FWH.

2.8 I/O Controller

The S815EBM1 board supports the following I/O controller:

- The standard SMSC LPC47M132 I/O controller

Both I/O controllers provide the following features:

- Low pin count (LPC) interface
- 3.3 V operation
- One serial port and one serial port header
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive

- Intelligent power management, including a programmable wake up event interface
- PCI power management support
- Fan control
  - One fan control output
  - Two fan tachometer inputs

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
• The USB hubs on the S815EBM1 board	Section 2.7.1.2.2, page 13
• SMSC LPC47M132 I/O controller	http://www.smsc.com/

2.8.1 Serial Port

The S815EBM1 board has one serial port, which is located on the back panel, and one serial port header located next to the front panel header. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
• The location of the serial port connector	Figure 5, page 35
• The signal names of the serial port connector	Table 22, page 36

2.8.2 Parallel Port

The connector for the parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be set to the following modes:

- Output only (PC-AT*-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
• The location of the parallel port connector	Figure 5, page 35
• The signal names of the parallel port connector	Table 21, page 36
• Setting the parallel ports mode	Table 53, page 70

2.8.3 Floppy Drive Controller

The I/O controller supports one floppy drive that is compatible with the 82077 floppy drive controller and supports both PC-AT and PS/2 modes.

For information about	Refer to
• The location of the floppy drive connector	Section 2.1.2, page 3
• The signal names of the floppy drive connector	Table 31, page 40
• The supported floppy drive capacities and sizes	Table 56, page 75

2.8.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a thermistor, which limits the current to a specified amperage.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI* keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset (operating system dependent). This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the power-on self-test (POST).

For information about	Refer to
• The location of the keyboard and mouse connectors	Figure 5, page 35
• The signal names of the keyboard and mouse connectors	Table 18, page 35
• Overcurrent protection for back panel connectors	Table 17, page 35

2.9 Graphics Subsystems

This section describes the Intel 815E graphics subsystems used by the S815EBM1 board.

2.9.1 Intel 815E Graphics Subsystem

The 815E chipset allows the integrated graphics controller (contained within the 82815 GMCH) to be used on the S815EBM1 board.

2.9.1.1 Integrated Graphics Controller

The GMCH features the following:

- Integrated graphics controller
  - 3-D HyperPipelined architecture
  - Full 2-D hardware acceleration
  - Motion video acceleration
- 3-D graphics visual and texturing enhancement
- Display
  - Integrated 24-bit 230 MHz RAMDAC (random access memory digital-to-analog converter)
  - Display Data Channel Standard, Version 3.0, Level 2B protocols compliant
- Integrated graphics memory controller

Table 5 lists the refresh frequencies supported by the graphics subsystem.

Table 5. Supported Graphics Refresh Frequencies

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
320 x 200	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
320 x 240	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 480	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 576	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
400 x 300	256 colors	70	D

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
	64 K colors	70	D3
	16 M colors	70	D
512 x 384	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 400	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 480	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 75, 85	KD3O
	64 K colors	70, 72	KDO
640 x 480	16 M colors	60, 70, 72, 75, 85	KDO
800 x 600	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 70, 72, 75, 85	KD3O
	16 M colors	60, 70, 72, 75, 85	KDO
1024 x 768	256 colors	60, 70, 75, 85	KDO
	64 K colors	60, 70, 75	KD3O
	64 K colors	85	KD3
	16 M colors	60, 70, 75, 85	KD
1152 x 864	256 colors	60, 70, 72, 75	KDO
	256 colors	85	KD
	64 K colors	60, 70	KD3O
	64 K colors	72, 75, 85	KD3
	16 M colors	60	KDO
	16 M colors	75, 85	KD
1280 x 768	256 colors	60 (reduced blanking)	KDOF
	64 K colors	60 (reduced blanking)	KD3F
	16 M colors	60 (reduced blanking)	KDF
1280 x 1024	256 colors	60	KDO
	256 colors	70, 72, 75, 85	KD
	64 K colors	60, 70, 72, 75, 85	KD3
	16 M colors	60, 70, 75, 85	KD
1600 x 1200	256 colors	60, 70, 72, 75	KD

Notes:

K = Server

D = DirectDraw*

3 = Direct3D*and OpenGL*

O = Overlay

F = Digital Display Device only. A mode will be supported on both analog CRTs and digital display devices (KD3O applies to both types of displays), unless indicated otherwise.

For information about	Refer to
• Obtaining graphics software and utilities	Section 2.2, page 5

2.10 LAN Subsystem

The network interface controller subsystem consists of the ICH2, with integrated LAN Media Access Controller (MAC), and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master Interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET on-board LAN physical layer interface device
- PCI Power Management
  - Supports APM
  - Supports ACPI technology
  - Supports Wake up from suspend state (Wake on LAN technology)

For information about	Refer to
• Obtaining LAN software and drivers	Section 2.2, page 5

2.10.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN Connectivity
- Supports RJ-45 connector with status indicator LEDs
- Full driver compatibility
- Advanced Power Management support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

2.10.2 RJ-45 LAN Connector LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 6 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 6. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Megabit/sec data rate is selected.

	On	100 Megabit/sec date rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

2.11 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Hardware monitoring
- Chassis intrusion detect connector
- Fan control and monitoring

For information about	Refer to
• Obtaining the WfM specification	http://developer.intel.com/ial/WfM/wfmspecs.htm
• Fan control functions of the SMSC LPC47M132 I/O controller	Section 2.11.3, page 20

2.11.1 Hardware Monitor Component

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature (if supported in the processor)
- Power supply monitoring (+12 V, +5 V, +3.3 V, +2.5 V, 3.3 VSB, and V_{CCP}) to detect levels above or below acceptable values
- SMBus interface

2.11.2 Chassis Intrusion Detect Connector

The board supports a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion detect connector. The mechanical switch is closed for normal computer operation. Chassis intrusion detection can be supported with third party SMBus software.

For information about	Refer to
• The location of the optional chassis intrusion detect connector	Section 2.1.2, page 3

• The signal names of the optional chassis intrusion detect connector	Table 28, page 38

2.11.3 Fan Control and Monitoring

The SMSC LPC47M132 I/O controller provides fan tachometer input for the processor fan (fan 1) and the system fan (fan 2), and fan control output for the system fan (fan 2) and the chassis fan (fan 3). Monitoring and control can be implemented using third-party software.

For information about	Refer to
• The functions of the fan connectors	Section 2.12.2.2, page 25
• The location of the fan connectors	Section 2.1.2, page 3
• The signal names of the fan connectors	Section 3.7.2.2, page 37

2.12 Power Management

Power management is implemented at several levels, including:

- Software support:
  - Advanced Power Management (APM)
  - Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Wake on Ring
  - Resume on Ring
  - S5 wake on all PCI slots

2.12.1 Software Support

The software support for power management includes APM and ACPI. If the S815EBM1 board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

2.12.1.1 APM

APM makes it possible for the computer to enter an energy-saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program

- From the operating system, such as the standby menu item in Windows 2000 Advanced Server

In standby mode, the S815EBM1 board can reduce power consumption by spinning down hard drives and reducing power to, or turning off, VESA* DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default, but the operating system must support an APM driver for the power management features to work. For example, Windows 2000 Advanced Server supports the power management features upon detecting that APM is enabled in the BIOS.

For information about	Refer to
• Enabling or disabling power management in the BIOS Setup program	Section 5.5, page 77
• The S815EBM1 board's compliance level with APM	http://www.microsoft.com/hwdev/busbios/amp_12.htm

2.12.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the S815EBM1 board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support normally contained in the BIOS.
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives.
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state.
- A soft-off feature that enables the operating system to power-off the computer.
- Support for multiple wake up events (see Table 9 on page 24).
- Support for a front panel power and sleep mode switch. Table 7 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 7. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state

Off (ACPI G2/G5 – soft-off)	Less than seven seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than seven seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than seven seconds	Fail safe power-off (ACPI G2/G5 – soft-off)
Sleep (ACPI G1 – sleeping state)	Less than seven seconds	Wake up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than seven seconds	Power-off (ACPI G2/G5 – soft-off)

For information about	Refer to
• The S815EBM1 board's compliance level with ACPI	http://www.teleport.com/~acpi/

2.12.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 8 lists the ACPI power states along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 8. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power [1]
G0 – working state	S0 – working	C0 – working	D0 – working state	Full power > 30 W
G1 – sleeping state	S1 – CPU stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 30 W
G1 – sleeping state	S3 – suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake up logic.	Power < 5 W [2]
G2/S5	S5 – soft-off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake up logic.	Power < 5 W [2]
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

2.12.1.2.2 Wake Up Devices and Events

Table 9 lists the devices or specific events that can wake the computer from specific states.

Table 9. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S5
RTC alarm	S5 [1]
Wake on LAN technology connector	S5 [1]
PME#	S5 [1]

Notes:

1. For the Wake on LAN technology connector and PME#, S5 is disabled by default in the BIOS Setup program. Setting these options to Power On will enable a wake-up event from LAN in the S5 state.

NOTES

- The use of these wake up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.
- Wake up from PS/2 mouse is peripheral, operating system, and driver dependent; it is not a board-level feature.

2.12.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure S815EBM1 board devices that do not have other hardware standards for enumeration and configuration. PCI devices on the S815EBM1 board, for example, are not enumerated by ACPI.

2.12.2 Hardware Support

CAUTION

If the Wake on LAN and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing option.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors

- Wake on LAN technology connector
- Wake on Ring
- Resume on Ring
- Wake on S5 from all PCI slots

Wake on LAN technology requires power from the +5 V standby line. The sections discussing this feature describes the incremental standby power requirements.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

The use of Resume on Ring technology from an ACPI state requires an operating system that provides full ACPI support.

2.12.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the S815EBM1 board can turn off the system power through software control. To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power is restored, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the After Power Failure feature in the BIOS Setup program's Power menu.

For information about	Refer to
• The location of the power connector	Section 2.1.2, page 3
• The signal names of the power connector	Table 25, page 38
• The BIOS Setup program's Power menu	Section 5.5, page 77
• The ATX specification	Table 2, page 6

2.12.2.2 Fan Connectors

The S815EBM1 board has three fan connectors. The functions of these connectors are described in Table 10.

Table 10. Fan Connector Descriptions

Connector	Silkscreen Label	Reference Designator	Function
Processor fan	Fan 1	J1B1	Provides +12 V DC for a processor fan or active fan heatsink. A tachometer feedback connection is also provided.
System fan	Fan 2	J9H1	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided.
Chassis fan	Fan 3	J4G1	Provides +12 V DC for a system or chassis. The fan voltage can be switched on or off, depending on the power management state of the computer.

For information about	Refer to
• The location of the fan connectors	Section 2.1.2, page 3
• The signal names of the fan connectors	Section 3.7.2.2, page 37

2.12.2.3 Wake on LAN Technology

CAUTION

For Wake on LAN technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wakeup signal that powers up the computer. Depending on the LAN implementation, the S815EBM1 board supports Wake on LAN technology in the following ways:

- Through the Wake on LAN technology connector (APM only)
- Through the on-board LAN subsystem when enabled in Setup (ACPI only)

The Wake on LAN technology connector can be used with PCI bus network adapters that have a remote wake up connector, as shown in Figure 4. Network adapters that are PCI 2.2 compliant assert the wakeup signal through the PCI bus signal PME# (pin A19 on the PCI bus connectors).

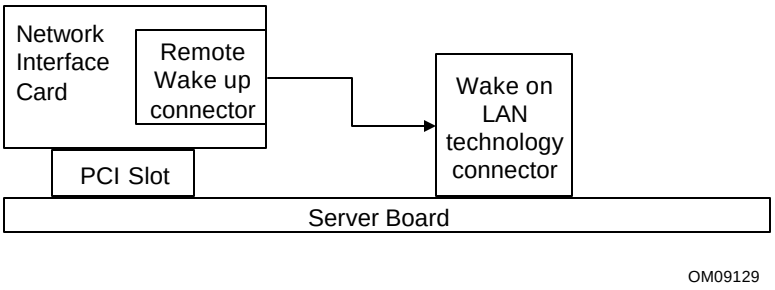


Figure 4. Using the Wake on LAN Technology Connector

For information about	Refer to
• The location of the Wake on LAN technology connector	Section 2.1.2, page 3
• The signal names of the Wake on LAN technology connector	Table 29, page 38

2.12.2.4 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from the APM sleep mode
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

2.12.2.5 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the server from the APM soft-off mode.
- Modem must support PME.
- Requires two calls to access the server:
  - The first call powers up the server.
  - The second call enables access (when the appropriate software is loaded).

For external modems, hardware on the server board monitors the ring indicate (RI) input of the serial ports.

3. Technical Reference

This chapter contains several standalone tables. Table 11 describes the system memory map, Table 12 shows the I/O map, Table 13 lists the DMA channels, Table 14 defines the PCI configuration space map, and Table 15 describes the interrupts.

3.1 Memory Map

Table 11. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 KB – 524288 KB	100000 – 1FFFFFFF	511 MB	Extended memory
960 KB – 1024 KB	F0000 – FFFFF	64 KB	Runtime BIOS
896 KB – 960 KB	E0000 – EFFFF	64 KB	Reserved
800 KB – 896 KB	C8000 – DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 KB – 800 KB	A0000 – C7FFF	160 KB	Video memory and BIOS
639 KB – 640 KB	9FC00 – 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 KB – 639 KB	80000 – 9FBFF	127 KB	Extended conventional memory
0 KB – 512 KB	00000 – 7FFFF	512 KB	Conventional memory

3.2 I/O Map

Table 12. I/O Map

Address (hex)	Size	Description
0000 – 000F	16 bytes	DMA controller
0020 – 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 – 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 – 0071	2 bytes	System CMOS/Real Time Clock
0072 – 0073	2 bytes	System CMOS
0080 – 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 – 00A1	2 bytes	PIC
00B2 – 00B3	2 bytes	APM control
00C0 – 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 – 0177	8 bytes	Secondary IDE channel
01F0 – 01F7	8 bytes	Primary IDE channel

Address (hex)	Size	Description
0228 – 022F [1]	8 bytes	LPT3
0278 – 027F [1]	8 bytes	LPT2
02E8 – 02EF [1]	8 bytes	COM4/video (8514A)
02F8 – 02FF [1]	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 – 037F	8 bytes	LPT1
03B0 – 03BB	12 bytes	Intel 82815 GMCH/AGP
03C0 – 03DF	32 bytes	Intel 82815 GMCH/AGP
03E8 – 03EF	8 bytes	COM3
03F0 – 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 – 03FF	8 bytes	COM1
04D0 – 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 – 0CFB [2]	4 bytes	PCI configuration address register
0CF9 [3]	1 byte	Reset control register
0CFC – 0CFF	4 bytes	PCI configuration data register
FFA0 – FFA7	8 bytes	Primary bus master IDE registers
FFA8 – FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH2 (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary		S815EBM1 board resource
64 contiguous bytes starting on a 64-byte divisible boundary		ICH2 LAN controller
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 USB controller #1
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 USB controller #2
16 contiguous bytes starting on a 16-byte divisible boundary		ICH2 (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801BA PCI bridge

Notes:

1. Default, but can be changed to another address range.
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH2 addresses aliassing.

For information about	Refer to
• ICH2 addressing	http://developer.intel.com/design/chipsets/datashts

3.3 DMA Channels

Table 13. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

3.4 PCI Configuration Space Map

Table 14. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82815 component
00	01	00	PCI to AGP bridge
00	02	00	Intel 82815 GMCH (graphics memory controller hub)
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801BA ICH2 PCI to LPC bridge
00	1F	01	IDE controller
00	1F	02	ICH2 USB controller #1
00	1F	03	SMBus controller
00	1F	04	ICH2 USB controller #2
01	08	00	LAN controller
01	09	00	PCI bus connector 1 (J7B1)
01	0A	00	PCI bus connector 2 (J8B2)
01	0B	00	PCI bus connector 3 (J9B2)

3.5 Interrupts

Table 15. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 [1]
4	COM1 [1]
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 [1]
8	Real-time clock
9	Reserved for ICH2 system management bus
10	User available
11	User available
12	On-board mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

Note:

1. Default, but can be changed to another IRQ.

3.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and on-board PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)

- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either on-board or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the S815EBM1 board and therefore share the same interrupt. Table 16 shows an example of how the PIRQ signals are routed on the S815EBM1 board.

For example, using Table 16 as a reference, assume that an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQH, which is already connected to the ICH2 USB controller #2. The add-in card in PCI bus connector 3 now shares interrupts with these on-board interrupt sources.

Table 16. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name				
	PIRQF	**PIRQG**	**PIRQH**	**PIRQB**	**Other**
GMCH/AGP				INTB	INTA to PIRQA
ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
ICH2 USB controller #2			INTC		
ICH2 audio/modem				INTB	
ICH2 LAN					INTA to PIRQE
PCI bus connector 1 (J7B1)	INTA	INTB	INTC	INTD	
PCI bus connector 2 (J8B2)	INTD	INTA	INTB	INTC	
PCI bus connector 3 (J9B2)	INTC	INTD	INTA	INTB	

NOTE

The ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3.7 Connectors

CAUTION

Only the back panel connectors of the S815EBM1 board have overcurrent protection. The S815EBM1 board's internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by an external device may result in a high output current that could damage the board, the interconnecting cable, and the external device itself.

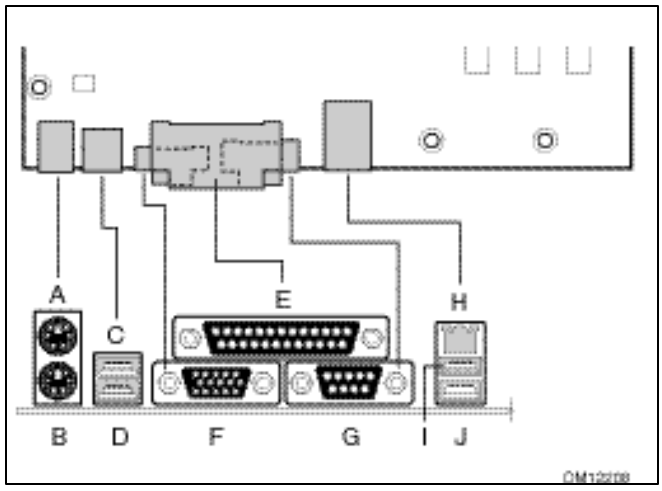
For information about	Refer to
• Overcurrent protection for the board's back panel connectors	Table 17, page 35

This section describes the board's connectors. The connectors can be divided into the following groups:

- Back panel I/O connectors (see page 34)
  - PS/2 keyboard and mouse
  - USB (four)
  - VGA
  - Parallel port
  - Serial port
  - LAN
- Internal I/O connectors (see page 37)
  - Fans
  - Power
  - Chassis intrusion
  - Wake on LAN technology
  - Add-in boards (three PCI bus connectors)
  - IDE (two)
  - Floppy drive
- External I/O connectors (see page 42)
  - SCSI LED
  - Serial port header
  - Front panel (power/sleep/message waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel LED)

3.7.1 Back Panel Connectors

Figure 5 shows the location of the back panel connectors on the S815EBM1 board. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color
A	PS/2 mouse port	Green
B	PS/2 keyboard port	Purple
C	USB port 1	Black
D	USB port 3	Black
E	VGA port	Dark blue
F	Parallel port	Burgundy
G	Serial port	Teal
H	LAN	Black
I	USB port 2	Black
J	USB port 0	Black

Figure 5. Back Panel Connectors

Table 17 lists the overcurrent protection for the S815EBM1 board. Overcurrent protection is provided to the board's back panel connectors through thermistors.

Table 17. Overcurrent Protection for Back Panel Connectors

Connectors	Maximum Current
PS/2 keyboard and mouse	1.5 A (total for both ports combined)
USB back panel	2.6 A (total for all four ports combined)
VGA	1.5 A

Table 18. PS/2 Mouse/Keyboard Connectors

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	+5 V
5	Clock
6	Not connected

Table 19. USB Connectors

Pin	Signal Name
1	+5 V
2	USB_BP0# [USB_BP1#, USB_BP2#, USB_BP3#]
3	USB_BP0 [USB_BP1, USB_BP2, USB_BP3]
4	Ground

Note:

Signal names in brackets ([ ]) are for USB ports 1, 2, and 3.

Table 20. VGA Port Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	Red	6	Ground	11	Not connected
2	Green	7	Ground	12	MONID1
3	Blue	8	Ground	13	HSYNC
4	Not connected	9	+5 V	14	VSYNC

5	Ground	10	Ground	15	MONID2

Table 21. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 - 25	Ground	Ground	Ground

Table 22. Serial Port Connector (and header)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 23. LAN Connector

Pin	Signal Name
1	TX+

2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

3.7.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Video, power, and hardware control (see page 37)
  - Fans
  - Power
  - Chassis intrusion
  - Wake on LAN technology
- Add-in boards and peripheral interfaces (see page 39)
  - PCI bus (three)
  - IDE (two)
  - Floppy drive

3.7.2.1 Expansion Slots

The board has three PCI Local Bus connectors (compliant with PCI Rev. 2.2 specification). The SMBus is routed to PCI bus connector 2. PCI add-in cards with SMBus support can access sensor data and other information residing on the server board.

NOTES

- This document refers to back-panel slot numbering with respect to processor location on the board. On the board's silkscreen, PCI slots are labeled as PCI 1, PCI 2, and PCI 3, starting with the slot closest to the processor.
- The ATX/microATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type, but refers to an actual connector location on a chassis. Figure 2 on page 4 illustrates the board's PCI connector numbering.

3.7.2.2 Video, Power, and Hardware Control Connectors

The following tables describe the location and pinout of the video, power, and hardware control connectors on the S815EBM1 board.

Table 24. Processor Fan Connector (J1B1)

Pin	Signal Name
1	Ground
2	+12 V
3	FAN1_TACH

Table 25. Power Connector (J4H1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD	18	Not connected
9	+5 V (standby)	19	+5 V
10	+12 V	20	+5 V

Table 26. Chassis Fan Connector (J4G1)

Pin	Signal Name
1	FAN3_PWM
2	+12 V
3	No connect

Table 27. System Fan Connector (J9H1)

Pin	Signal Name
1	FAN2_PWM
2	+12 V
3	FAN2_TACH

Table 28. Chassis Intrusion Connector (J9H3)

Pin	Signal Name

1	INTRUDER#
2	Ground

Table 29. Wake on LAN Technology Connector (J9G1)

Pin	Signal Name
1	+5 V (standby)
2	Ground
3	WOL

For information about	Refer to
• The power connector	Section 2.12.2.1, page 25
• The functions of the fan connectors	Section 2.12.2.2, page 25
• Wake on LAN technology	Section 2.12.2.3, page 26

3.7.2.3 Add-in Board and Peripheral Interface Connectors

The tables below show the locations and pinout of the add-in board and peripheral interface connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- SMBus signals are routed to PCI bus connector 2. This enables PCI bus add-in boards with SMBus support to access sensor data on the board. These SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41

Table 30. PCI Bus Connectors (J7B1, J8B2, and J9B2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#) [1]	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK) [1]	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	Not connected (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A9	Reserved	B9	Not connected (PRSNT1#) [1]	A40	Reserved [2]	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved [3]	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#) [1]	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

Notes:

1. These signals (in parentheses) are optional in the PCI specification and are not currently implemented.
2. On PCI bus connector 2 (J8B2), this pin is connected to the SMBus clock line.
3. On PCI bus connector 2 (J8B2), this pin is connected to the SMBus data line.

Table 31. Floppy Drive Connector (J6H2)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	Not connected
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	Not connected

17	Not connected	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	Not connected	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 32. IDE Connectors (J6H1, Primary and J6G2, Secondary)

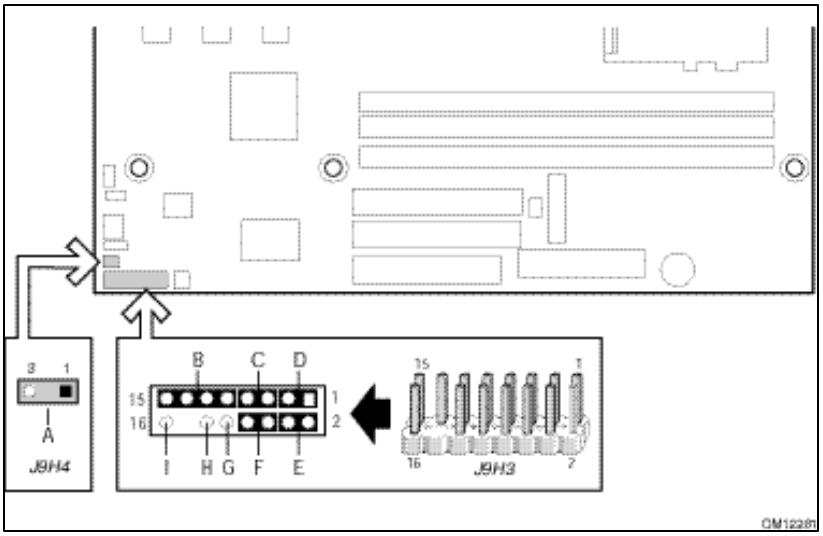
Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

Note:

Signal names in brackets ([ ]) are for the secondary IDE connector.

3.7.3 Front Panel Connectors

Figure 6 shows the locations of the front panel connectors on the S815EBM1 board. Please note that the Serial port B header (J8H1) is located next to the SCSI LED, although not shown in the picture below. Please see Figure 1 for exact location.



A. Chassis intrusion connector
B. Reserved
C. Reset switch
D. Hard drive activity LED
E. Power LED
F. On/Off Switch
G. No connect
H. Ground
I. +5 V

Figure 6. Front Panel Connectors

3.7.3.1 Auxiliary Front Panel Power LED Connector

This connector duplicates the signals on pins 2 and 4 of the front panel connector.

Table 33. Auxiliary Front Panel Power LED Connector (J9H2)

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

3.7.3.2 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows add-in SCSI host bus adapter to use the same LED as the IDE controller. This connector can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller. Table 34 lists the signal names of the SCSI hard drive activity LED connector.

Table 34. SCSI LED Connector (J8H2)

Pin	Signal Name
1	SCSI activity
2	Not connected

3.7.3.3 Front Panel Connector

This section describes the functions of the front panel connector. Table 35 lists the signal names of the front panel connector.

Table 35. Front Panel Connector (J9H3)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk activity LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	GND		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
9	+5 V	Out	Power	10	N/C		Not connected
11	N/C		Reserved	12	GND		Ground

13	GND		Ground	14	(pin removed)		Not connected
15	N/C		Reserved	16	+5 V	Out	Power

3.7.3.3.1 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the S815EBM1 board will reset and run the POST.

3.7.3.3.2 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the on-board IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

For information about	Refer to
• The SCSI hard drive activity LED connector	Section 3.7.3.2, page 43

3.7.3.3.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a single-colored or dual-colored LED. Table 36 shows the possible states for a single-colored LED. Table 37 shows the possible states for a dual-colored LED.

Table 36. States for a Single-Colored Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 37. States for a Dual-Colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE
To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

3.7.3.3.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the S815EBM1 board.) At least two seconds must pass before the power supply will recognize another on/off signal.

3.8 Jumper Blocks

CAUTION
Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 7 shows the location of the jumper block on the S815EBM1 board.

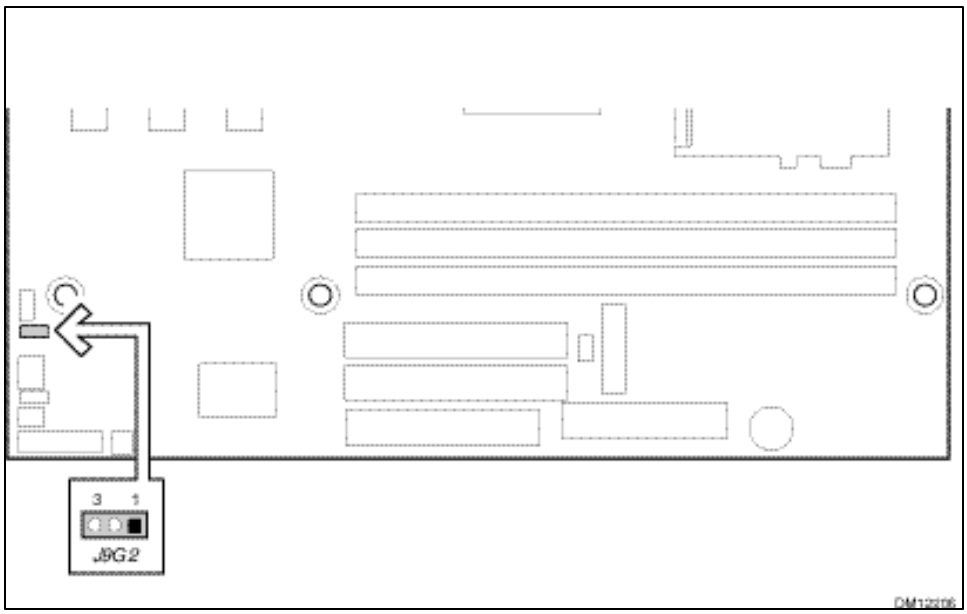


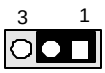
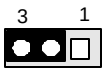
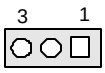
Figure 7. Location of the J9G2 BIOS Setup Configuration Jumper Block

3.8.1 BIOS Setup Configuration Jumper Block

This 3-pin jumper block determines the BIOS Setup program's mode. Table 38 describes the jumper settings for the three modes: normal, configure, and recovery.

When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

Table 38. BIOS Setup Configuration Jumper Settings (J9G2)

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
• How to access the BIOS Setup program	Section 5, page 63
• The maintenance menu of the BIOS Setup program	Section 5.1, page 64
• BIOS recovery	Section 4.6, page 59

3.9 Mechanical Considerations

3.9.1 Form Factor

The S815EBM1 board is designed to fit into a standard microATX-form-factor chassis. Figure 8 illustrates the mechanical form factor for the S815EBM1 board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 8.20 inches [243.84 millimeters by 208.28 millimeters]. The location of the I/O connectors and mounting holes are in compliance with the microATX specification (see Section 2.3).

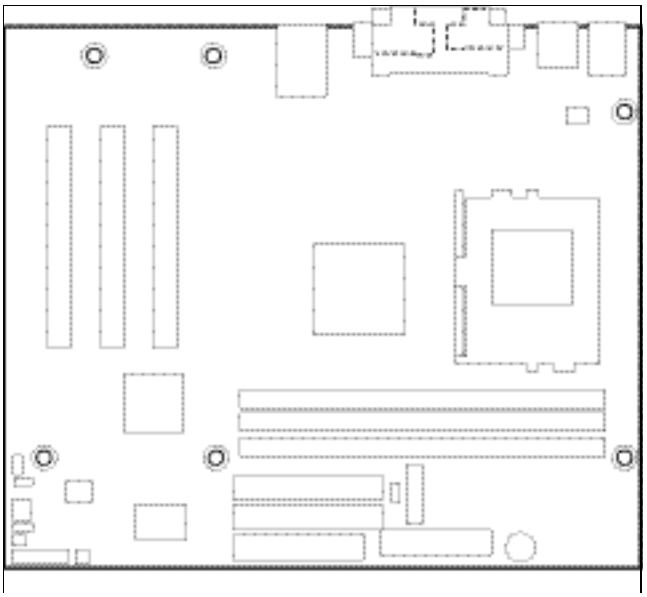


Figure 8. Location of Mounting Holes

3.9.2 I/O Shields

The back panel I/O shield for the S815EBM1 board must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass emissions (EMI) certification testing. Figure 9 shows the critical dimensions of the chassis-dependent I/O shield for use in a general purpose chassis. Dimensions are given in inches [millimeters], to a tolerance of ± 0.020 inches [0.508 millimeters]. If integrating the S815EBM1 board into a 1U chassis, please obtain an I/O shield from the chassis vendor.

This figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification.

For information about	Refer to
• The ATX specification	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
• The microATX specification	http://www.formfactors.org/developer/specs/microatx/microatxspecs.htm

NOTE

An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.

[Figure TBD]

Figure 9. I/O Shield Dimensions

3.10 Electrical Considerations

3.10.1 Add-in Board Considerations

The S815EBM1 board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards in a fully-loaded S815EBM1 board (all three expansion slots filled) must not exceed 8 A.

3.10.2 Standby Current Requirements

CAUTION

Power supplies used with the board must provide enough standby current to support the Instantly Available configuration. If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the board may lose register settings stored in memory and may not awaken properly.

To estimate the standby current required for a specific system configuration, the standby current requirements of all installed components must be combined. Follow these steps:

1. List the board's +5 V standby current requirement (767 mA).
2. List the PS/2 ports' standby current requirement (see note below).
3. List, from the PCI 2.2 slots (wake-enabled devices) row, the total number of wake-enabled devices installed and multiply by the standby current requirement.
4. List, from the PCI 2.2 slots (non-wake-enabled devices) row, the total number of wake-enabled devices installed and multiply by the standby current requirement.
5. List all additional wake-enabled devices' and non-wake-enabled devices' standby current requirements as applicable.
6. Add all the listed standby current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

Table 39. Standby Current Requirements

Description	Standby Current Requirements (mA) [1]
Total for the board	767
On-board LAN	95
Wake on LAN technology connector connected to wake-enabled PCI LAN card	525
PS/2 ports [2]	345
PCI 2.2 slots (wake-enabled devices) [2]	470
PCI 2.2 slots (non-wake-enabled devices) [2]	115
USB ports (Note 2)	507.5

Notes:

1. These values were measured in a power static state.
2. Dependent upon system configuration. See the note on the following page.

NOTE

PCI requirements are calculated by totaling the following:

- One wake-enabled device @ 375 mA
- Two non-wake-enabled devices @ 20 mA each
- PS/2 Ports requirements per the IBM PS/2 Port Specification (Sept 1991):
  - Keyboard @ 275 mA (Actual measurements are 220 mA-300 mA, depending on the type of keyboard and the operational state of the keyboard's LEDs.)
  - Mouse @ 70 mA

- USB requirements are limited to a combined total of 700 mA and are calculated by totaling the following:
  - One wake-enabled device @ 500 mA
  - Three USB non-wake-enabled devices @ 2.5 mA each

3.10.3 Fan Connector Current Capability

The S815EBM1 board is designed to supply a maximum of 225 mA per fan connector.

3.10.4 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported.

Measurements account only for current sourced by the S815EBM1 board while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
• The ATX form factor specification	http://www.formfactors.org/developer/specs/atx/atxspecs.htm

3.11 Thermal Considerations

CAUTIONS

- An ambient temperature that exceeds the board's maximum operating temperature by 10 ^{o}C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 3.13.
- The processor voltage regulator area can reach a temperature of up to 85 ^{o}C in an open chassis. System integrators should ensure that proper airflow is maintained in the

voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit.

Locations of the localized high temperature zones for the S815EBM1 board are listed below.

A Processor voltage regulator area

B Intel 82815 Graphics and Memory Controller Hub (GMCH)

C Processor

D Intel 82801BA ICH2

Table 40 provides maximum case temperatures for S815EBM1 board components that are sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the S815EBM1 board.

Table 40. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium III processor	For processor case temperature, see processor datasheets and processor specification updates
Intel Celeron processor	
Intel 82815 GMCH	116 °C (under bias)
Intel 82801BA ICH2	109 °C (under bias)

For information about	Refer to
• Processor datasheets and specification updates	http://www.intel.com/design/litcentr

3.12 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 35 ºC. S815EBM1 board's MTBF: 369,041 hours

3.13 Environmental

Table 41 lists the environmental specifications for the S815EBM1 board.

Table 41. S815EBM1 Board Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

3.14 Regulatory Compliance

This section describes the S815EBM1 board's compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

3.14.1 Safety Regulations

Table 42 lists the safety regulations the S815EBM1 board complies with when correctly installed in a compatible host system.

Table 42. Safety Regulations

Regulation	Title
UL 1950/CSA C22.2 No. 950, 3rd edition	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

3.14.2 EMC Regulations

Table 43 lists the EMC regulations the S815EBM1 board complies with when correctly installed in a compatible host system.

Table 43. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radiofrequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1994 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 2nd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

3.14.3 Product Certification Markings (Board Level)

The S815EBM1 Server board has the following product certification markings:

- UL joint US/Canada Recognized Component mark: Consists of lower case c followed by a stylized backward UR and followed by a small US. Includes adjacent UL file number for Intel Server board: E210882 (component side).
- FCC Declaration of Conformity logo mark for Class B equipment; to include Intel name and S815EBM1 model designation (solder side).
- CE mark: Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.
- Australian Communications Authority (ACA) C-Tick mark: consists of a stylized C overlaid with a check (tick) mark (component side), followed by Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.
- Korean EMC certification logo mark: consists of MIC lettering within a stylized elliptical outline.
- Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (solder side).
- PB part number: Intel bare circuit board part number (solder side) A44507-002. Also includes SKU number starting with AA followed by additional alphanumeric characters.

- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder.

4. BIOS Features Overview

The S815EBM1 board uses an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Plug and Play support.

The S815EBM1 board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as EA81520A.86B.

When the S815EBM1 board's jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
• The S815EBM1 board's compliance level with APM and Plug and Play	http://www.microsoft.com/hwdev/busbios/amp_12.htm

4.1 BIOS Flash Memory Organization

The FWH (an STM M50FW040) includes a 4 megabit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

4.2 Resource Configuration

4.2.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be on-board or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to system resources. The assignment of PCI interrupts to ISA IRQs is non-deterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 2.3.

4.2.2 IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 2.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTES

- ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest drive.
- Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

4.3 System Management BIOS (SMBIOS)

SMBIOS is a Server Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
• The S815EBM1 board's compliance level with the SMBIOS specification	http://developer.intel.com/ial/wfm/design/smbios

4.4 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards, mice, and hubs are recognized and may be used to configure the operating system. (Keyboards, mice, and hubs are not recognized during this period if legacy USB support was set to Disabled in the BIOS Setup program.)

To install an operating system that supports USB, verify that legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

Legacy USB support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode.

4.5 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on http://support.intel.com/:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Internet.
- Intel® Flash Memory Update utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

4.5.1 Language Support

The BIOS Setup program and help messages are available in five languages: US English, German, Italian, French, and Spanish. The default languages are US English and German, which are present unless another language is selected and updated via a .LNG file available from http://support.intel.com/.

4.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available at http://support.intel.com/.

4.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from Intel Customer Support at http://support.intel.com/.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
• The BIOS recovery mode jumper settings	Section 3.8.1, page 45
• The Boot menu in the BIOS Setup program	Section 5.6, page 80
• Contacting Intel customer support	http://support.intel.com/

4.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

4.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device with bootable media.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

For information about	Refer to
• The El Torito specification	http://www.phoenix.com/PlatSS/products/specs.html

4.7.2 Booting without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

4.8 Fast Booting Systems with Intel® Rapid BIOS Boot

There are three factors that affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS
- Selecting a compatible operating system

The BIOS is not configured by default to boot at the fastest possible speed. Empirical measurements have shown that some Intel® server boards, when optimized as described above, can complete POST (Power-On Self-Test) in six seconds or less and boot to an active Microsoft* Windows* ME operating system in 21 seconds.

4.8.1 Peripheral Selection and Configuration

The following techniques will help speed system boot:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds to minimize hard drive startup delays. The Western Digital Caviar* AA or BA series are examples of drives that meet this parameter.
- Select a CD-ROM drive with a fast initialization rate; variations can influence POST times.
- Eliminate unnecessary features such as video-company-logo displaying, screen repaints, or mode changes. These all add time in the boot process. The Plug and Play communication between the video BIOS and the monitor shows time variances.
- Try different monitors. Some monitors initialize more quickly, thereby enabling the system to boot more quickly.

4.8.2 Intel Rapid BIOS Boot

There are several BIOS settings, which if adjusted, can reduce the execution time of the POST:

- Set the hard disk drive as the first boot device. As a result, the POST will not seek a diskette drive (saving about one second from the POST time) or a CD-ROM drive (saving about two seconds).
- Make sure that Quiet Boot is disabled, to eliminate the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Make sure the Intel Rapid BIOS Boot option (in the Boot menu of the BIOS Setup Program) is enabled (this is typically the default setting). This feature bypasses memory count and floppy seek.
- Disable the LAN feature PXE (Preboot eXecutable Environment) if it will not be used. Doing so can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel Logo Screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen. If this should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds using the Hard Disk Pre-Delay feature in the IDE Configuration Submenu of the BIOS Setup Program.

For information about	Refer to
• IDE Configuration Submenu in the BIOS Setup Program	Table 54, page 73

4.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.

- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 44 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 44. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note:
If no password is set, any user can change all Setup options.

For information about	Refer to
• Setting user and supervisor passwords	Section 5.4, page 76

5. BIOS Setup Program

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

```
Maintenance  Main      Advanced   Security   Power     Boot      Exit
```

Table 45 lists the BIOS Setup program menu features.

Table 45. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and BIS credentials and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 3.8 on page 45 tells how to put the board in configuration mode. Table 46 lists the function keys available for the menu screens.

Table 46. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

5.1 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The menu shown in Table 47 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 3.8 on page 45 for configuration mode setting information.

Table 47. Maintenance Menu

Feature	Options	Description
Clear All Passwords	Yes (default) No	Clears the user and administrative passwords.
Clear BIS Credentials	Yes (default) No	Clears the Wired for Management Boot Integrity Service (BIS) credentials.
Extended Configuration	No options	Invokes the Extended Configuration submenu.
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.

5.1.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar, then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 48 is for setting video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 48. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	Default (default) User-Defined	User Defined allows setting memory control and video memory cache mode. If selected here, will also display in the Advanced Menu as: “Extended Menu: Used.”
Video Memory Cache Mode	USWC UC (default)	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining. Selects UnCacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining.
SDRAM Auto-Configuration	Auto (default) User Defined	Sets extended memory configuration options to Auto or User Defined.
CAS# Latency	3 2 Auto (default)	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay	3 2 Auto (default)	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	3 2 Auto (default)	Selects the length of time required before accessing a new row.

5.2 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 49 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 49. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Bus Frequency	No options	Displays the system bus frequency.
Internal Cache	Disabled WriteThru WriteBack (default) Reserved	Displays CPU internal cache and, if enabled, select WriteThru or WriteBack mechanism.
External Cache	Disabled WriteThru (default) WriteBack Reserved	Displays CPU external cache and, if enabled, select WriteThru or WriteBack mechanism.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 0 Memory Bank 1 Memory Bank 2	No options	Displays the amount and type of RAM in the memory banks.
Language	English (default) German	Selects the current default language used by the BIOS.
Processor Serial Number	Disabled (default) Enabled	Enables and disables the processor serial number. (Present only when a Pentium III processor is installed)
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week month/day/year	Specifies the current date.

5.3 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

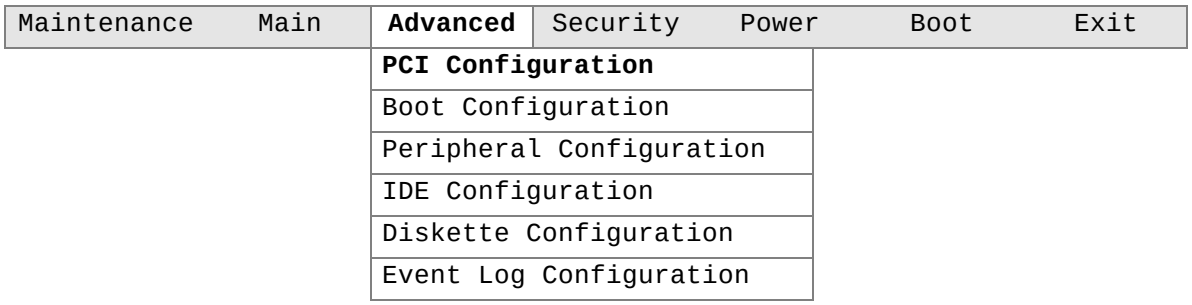
Table 50 describes the Advanced menu. This menu is used for setting advanced features that are available through the chipset.

Table 50. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If Used is displayed, User-Defined has been selected in Extended Configuration under the Maintenance Menu.
PCI Configuration	No options	Configures individual PCI slot's IRQ priority. When selected, displays the PCI Configuration submenu.
Boot Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Diskette Configuration submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.

5.3.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then PCI Configuration.



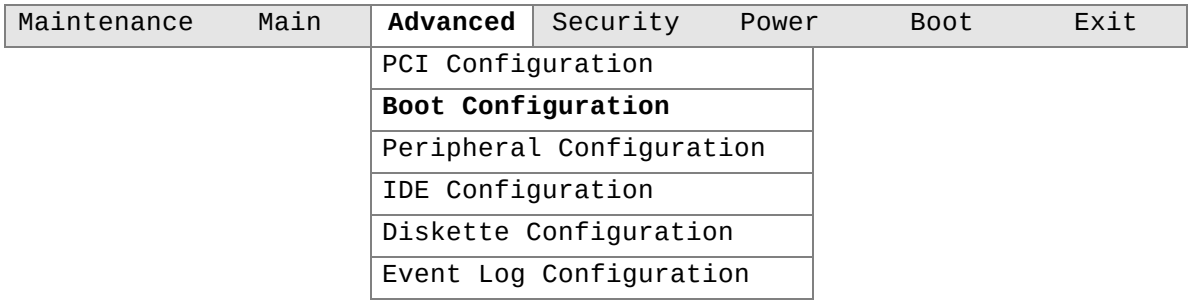
The submenu represented by Table 51 is for configuring the IRQ priority of PCI slots individually.

Table 51. PCI Configuration Submenu

Feature	Options	Description
PCI Slot 1 IRQ Priority	**Auto** (default) 3 9 10 11	Allows selection of IRQ priority and S5 wake.
PCI Slot 2 IRQ Priority	**Auto** (default) 3 9 10 11	Allows selection of IRQ priority and S5 wake.
PCI Slot 3 IRQ Priority	**Auto** (default) 3 9 10 11	Allows selection of IRQ priority and S5 wake.

5.3.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Boot Configuration.



The submenu represented by Table 52 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 52. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	No (default) Yes	No lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. Yes lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Reset Config Data	No (default) Yes	No does not clear the PCI/PnP configuration data stored in flash memory on the next boot. Yes clears the PCI/PnP configuration data stored in flash memory on the next boot.
Numlock	Off On (default)	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

5.3.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu represented in Table 53 is used for configuring computer peripherals.

Table 53. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	Disabled Enabled **Auto (default)**	Configures serial port. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Serial Port B	Disabled Enabled **Auto (default)**	Configures serial port. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.

Feature	Options	Description
Base I/O Address (This feature is present only when Serial Port A is set to *Enabled*)	**3F8 (default)** 2F8 3E8 2E8	Specifies the base I/O address for serial port A, if serial port A is Enabled.
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	IRQ 3 **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is Enabled.
Parallel Port	Disabled Enabled **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional** (default) • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT*-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O Address (This feature is present only when Parallel Port is set to *Enabled*)	• **378** (default) • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7** (default)	Specifies the interrupt for the parallel port.
LAN Device (This feature is present only when there is on-board LAN)	• Disabled • **Enabled** (default)	Enables or disables the LAN device.
Legacy USB Support	• Disabled • **Enabled** (default)	Enables or disables legacy USB support. (See Section 4.4 on page 57 for more information.)

5.3.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration

Event Log Configuration

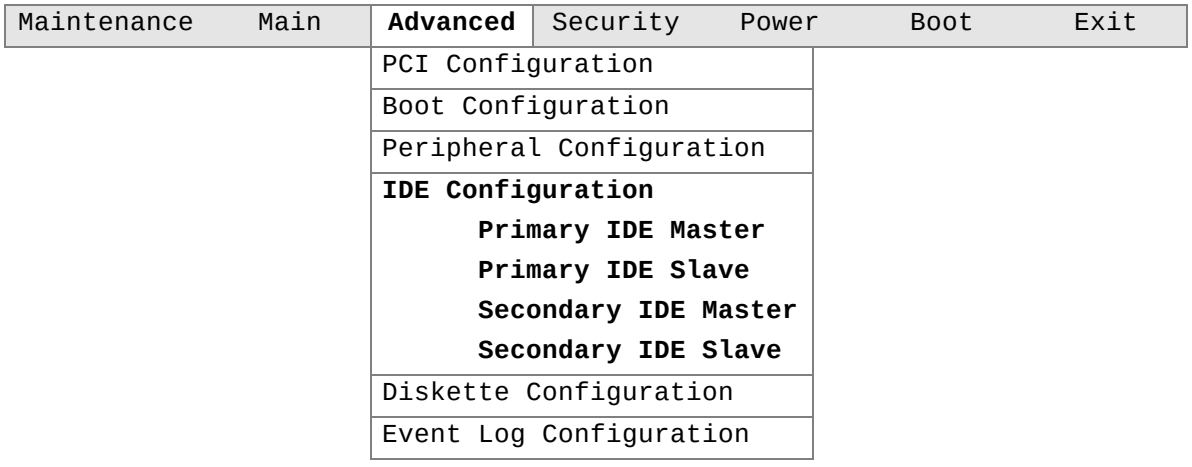
The menu represented in Table 54 is used to configure IDE device options.

Table 54. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both** (default)	Specifies the integrated IDE controller. Primary enables only the primary IDE controller. Secondary enables only the secondary IDE controller. Both enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled** (default) • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

5.3.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.



There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 55 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 55. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	None	Displays the type of drive installed.
Type	• None • User • **Auto** (default) • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. User allows capabilities to be changed. Auto fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	None	Displays the capacity of the drive.
LBA Mode Control	• Disabled • **Enabled** (default)	Enables or disables LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors** (default)	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode (Note)	• **Auto** (default) • 0 • 1 • 2 • 3 • 4	Specifies the PIO mode.
Ultra DMA	• **Disabled** (default) • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.
Cable Detected (Note)	None	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-66/100 devices).

Note:

These configuration options appear only if an IDE device is installed.

5.3.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar, then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu represented by Table 56 is used for configuring the diskette drive.

Table 56. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled** (default)	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½"** (default) • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Floppy B	• **Not Installed** (default) • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • 1.44/1.25 MB 3½" • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive B.
Diskette Write Protect	• **Disabled** (default) • Enabled	Disables or enables write-protect for the diskette drive.

5.3.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar, then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu represented by Table 57 is used to configure the event logging features.

Table 57. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View event log	[Enter]	Displays the event log.
Clear all event logs	• **No** (default) • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled** (default)	Enables logging of events.
Mark events as read	• Yes (default) • No	Marks all events as read.

5.4 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 58 is for setting passwords and security features.

Table 58. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if there is a supervisor password set.

If no password entered previously:		
Feature	**Options**	**Description**
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password [1]	• **Yes** (default) • No	Clears the user password.
User Access Level [2]	• Limited • No Access • View Only • **Full** (default)	Sets BIOS Setup Utility access rights for user level.
Unattended Start [1, 2, 3, 4]	• Enabled • **Disabled** (default)	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if both a user password and a supervisor password have been set.
3. If both Legacy USB Support (in the Peripheral Configuration submenu) and Unattended Start (in the Security menu) are enabled, USB aware operating systems can unlock a PS/2 style keyboard and mouse without requiring the user to enter a password.
4. When Unattended Start is enabled, a USB aware operating system may override user password protection if used in conjunction with a USB keyboard and mouse without requiring the user to enter a password.

5.5 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 59 is for setting the power management features.

Table 59. Power Menu

Feature	Options	Description
APM	No options	Sets the APM power management options.
ACPI	No options	Sets the ACPI power management options.
After Power Failure	• Stays Off • **Last State** (default) • Power On	Specifies the mode of operation if an AC power loss occurs. Stays Off keeps the power off until the power button is pressed. Last State restores the previous power state before power loss occurred. Power On restores power to the computer.

Feature	Options	Description
Wake on LAN (This feature is present only when there is no on-board LAN subsystem.)	• **Stay Off** (default) • Power-On	In APM soft-off mode only, determines how the system responds to a LAN wake up event.
Wake on PME	• **Stay Off** (default) • Power-On	In APM soft-off mode only, determines how the system responds to a PCI-PME wake up event.
Wake on Modem Ring	• **Stay Off** (default) • Power-On	In APM soft-off mode only, specifies how the computer responds to a Modem Ring wake up event on an installed modem.

5.5.1 APM Submenu

To access this menu, select Power on the menu bar, then APM.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				APM		
				ACPI		

The submenu represented in Table 60 is for setting APM power options.

Table 60. APM Submenu

Feature	Options	Description
Power Management	• Disabled • **Enabled** (default)	Enables or disables the APM feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes** (default) • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters APM standby mode.
Hard Drive	• Disabled • **Enabled** (default)	Enables power management for hard disks during APM standby mode.

5.5.2 ACPI Submenu

To access this menu, select Power on the menu bar, then ACPI.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				APM		
				ACPI		

The submenu represented in Table 61 is for setting ACPI power options.

Table 61. ACPI Submenu

Feature	Options	Description
Wake on LAN from S5	• **Stay Off** (default) • Power On	In ACPI soft-off mode only, determines how the system responds to a LAN wake up event when the system is in the ACPI soft-off mode.

5.6 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit

The menu represented in Table 62 is used to set the boot features and the boot sequence.

Table 62. Boot Menu

Feature	Options	Description
Quiet Boot	• **Disabled** (default) • Enabled	Disabled displays normal POST messages. Enabled displays OEM graphic instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled** (default)	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled** (default) • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
Boot Device Priority	No options	Specifies the boot sequence from the available types of boot devices.
Hard Disk Drives	No options	Specifies the boot sequence from the available hard disk drives.
Removeable Devices	No options	Specifies the boot sequence from the available removable devices.
ATAPI CDROM Drives	No options	Specifies the boot sequence from the available ATAPI CD-ROM drives.

5.6.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar, then Boot Devices Priority.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removeable Devices	
					ATAPI CDROM Drives	

The submenu represented in Table 63 is for setting boot devices priority.

Table 63. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device [1]	• Removable Dev. • Hard Drive • ATAPI CD-ROM • Intel® UNDI, PXE • Disabled	Specifies the boot sequence from the available types of boot devices. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. The default settings for the first through final boot devices are, respectively, listed below. The BIOS supports up to sixteen total boot devices in any combination of the boot device types below, with respect to these maximums per type. • Removable Dev. (maximum of four) • Hard Drive (maximum of twelve) • ATAPI CD-ROM (maximum of four) • Intel UNDI, PXE (maximum of five) [2] The boot devices appear in order by type. For example, assume that the default boot order is preserved and that seven boot devices of the following types are installed on the system: two removable devices, two hard drives, two ATAPI CD-ROMs, and an Intel UNDI (Universal Network Device Interface), PXE device. Both removable devices would appear as the first and second boot devices, the two hard drives would appear as the third and fourth, the two ATAPI CD-ROM drives would appear as the fifth and sixth, and the Intel UNDI, PXE device would appear as the seventh boot device.

Notes:

1. After the predefined boot device types (removable devices, hard drives, and ATAPI CD-ROM drives), the entries in this list will reflect as many boot entry vector (BEV) boot devices (for example, Intel UNDI, PXE devices) and SCSI CD-ROM drives as are installed, up to the five BEV boot devices supported by the BIOS.
2. While the predefined boot device types are listed individually in submenus by type, the BEV devices and SCSI
CD-ROM drives are all listed at this level.

5.6.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar, then Hard Disk Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removeable Devices	
					ATAPI CDROM Drives	

The submenu represented in Table 64 is for setting hard disk drive priority.

Table 64. Hard Disk Drives Submenu

Feature	Options	Description
1st Hard Disk Drive [1]	Dependent on installed hard drives	Specifies the boot sequence from the available hard disk drives. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <Enter> to set the selection as the intended boot device.

Note:

1. This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

5.6.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar, then Removable Devices.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CDROM Drives	

The submenu represented in Table 65 is for setting removable device priority.

Table 65. Removable Devices Submenu

Feature	Options	Description
1st Removeable Device [1]	Dependent on installed removable devices	Specifies the boot sequence from the available removable devices. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <Enter> to set the selection as the intended boot device.

Note:

1. This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

5.6.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar, then ATAPI CDROM Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removeable Devices	
					ATAPI CDROM Drives	

The submenu represented in Table 66 is for setting ATAPI CDROM drive priority.

Table 66. ATAPI CDROM Drives Submenu

Feature	Options	Description
1st ATAPI CDROM Drive [1]	Dependent on installed ATAPI CDROM drives	Specifies the boot sequence from the available ATAPI CDROM drives. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <Enter> to set the selection as the intended boot device.

Note:

1. This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CDROM drives, the maximum number of ATAPI CDROM drives supported by the BIOS.

5.7 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 67 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 67. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

6. Error Messages and Beep Codes

6.1 BIOS Error Messages

Table 68 lists the error messages and provides a brief description of each.

Table 68. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive – ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.

Error Message	Explanation
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in on-board memory. This error is followed by an address.
Parity Error	A parity error occurred in on-board memory at an unknown address.
NVRAM/CMOS/PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

6.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card, often called a POST card (PCI not ISA). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 69 defines the Uncompressed INIT Code Checkpoints, Table 70 describes the boot block recovery code checkpoints. Table 71 lists the runtime code uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 69. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. On-board KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 70. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	On-board Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, Zip*) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 71. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 0 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.

Code	Description of POST Operation
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 0 for details of different buses.)
39	Display different buses initialization error messages. (See Section 0 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 MB memory.
49	Amount of memory below 1 MB found and verified. Going to find out amount of memory above 1 MB memory.
4B	Amount of memory above 1 MB found and verified. Check for soft reset and going to clear memory below 1 MB for soft reset. (If power on, go to check point # 4Eh.)
4C	Memory below 1 MB cleared. (SOFT RESET) Going to clear memory above 1 MB.
4D	Memory above 1 MB cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h.)
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1 MB complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1 MB to follow.
52	Memory testing/initialization above 1 MB complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.

Code	Description of POST Operation
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 0 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.

Code	Description of POST Operation
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

6.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 72 describes the bus initialization checkpoints.

Table 72. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 73 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 73. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 74 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 74. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

6.4 Speaker

A 47 Ω inductive speaker is mounted on the S815EBM1 board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the on-board speaker	Figure 1, page 3

6.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 75). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 75. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure

4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g., POST module not found, etc.)

7. Errata Listing

7.1 Summary Errata Table

The following table indicates the errata that apply to the S815EBM1 server board. This table uses the following notations:

7.1.1 Codes Used in Summary Table

Doc: Intel intends to update the appropriate documentation in a future revision.

Fix: This erratum is intended to be fixed in a future stepping of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

NO.	Plans	ERRATA
1	Fixed	Use of PCI video adapters in S815EBM1 server system requires BIOS upgrade.

7.2 Errata

1. Use of PCI video adapters in S815EBM1 server system requires BIOS upgrade.

PROBLEM: The S815EBM1 BIOS was not designed to allow PCI video adapters to be installed in the server board.

IMPLICATION: Intel has found that PCI video adapters will not be recognized by BIOS and the system will not boot if a PCI video adapter is installed in any of the PCI slots.

WORKAROUND: None.

STATUS: Fixed. This issue has been resolved in BIOS Production Release 4. Please upgrade to BIOS release 4 if using add-in PCI video adapters.

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Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the S815EBM1 board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Megabit	1,048,576 bits
Megabit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate other names and brands that may be claimed as the property of others.

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