VT82C691

Apollo Pro

**66 / 100 MHz
Single-Chip Socket-8 / Slot-1 North Bridge
for Desktop and Mobile PC Systems
with AGP and PCI
plus Advanced ECC Memory Controller
supporting DDR SDRAM-II,
SDRAM, EDO, and FPG**

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VIA TECHNOLOGIES, INC.

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Offices:

USA Office:
1045 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 218-5452
Fax: (886-2) 218-5453

Online Services:

Home Page: http://www.via.com.tw (Taiwan) –or- http://www.viatech.com (USA)
FTP Server: ftp.via.com.tw (Taiwan)
BBS: 886-2-2185208

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- **AGP / PCI / ISA Mobile and Deep Green PC Ready**

    − Supports 3.3V and sub-3.3V interface to CPU
    − Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
    − PC-98 compatible using VIA VT82C586B (208-pin PQFP) south bridge chip with ACPI Power Management for cost-efficient desktop applications
    − Modular power management and clock control for mobile system applications
    − Combine with VIA VT82C596 (Intel PIIX4 pin compatible 324-pin BGA) "Mobile South" south bridge chip for state-of-the-art mobile applications

- **High Integration**

    − Single chip implementation for 64-bit Socket-8 / Slot-1-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
    − **Apollo Pro** Chipset: **VT82C691** system controller and **VT82C586B** PCI to ISA bridge
    − Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip

- **High Performance CPU Interface**

    − Supports Socket-8 (Intel Pentium Pro™) and Slot-1 (Intel Pentium II™) processors
    − 66 / 100 MHz CPU external bus speed
    − Built-in deskew DLL (Delay Lock Loop) circuitry for optimal skew control within and between clocking regions
    − Five outstanding transactions (four In-Order Queue (IOQ) plus one input latch)
    − Supports WC (Write Combining) cycles
    − Dynamic deferred transaction support
    − Sleep mode support
    − System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**

    - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

PCI	AGP	CPU	Mode
33 MHz	66 MHz	100 MHz	3x synchronous
33 MHz	66 MHz	66 MHz	2x synchronous

    - AGP v1.0 compliant
    - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
    - Supports 133MHz 2X mode for AD and SBA signalling
    - Pipelined split-transaction long-burst transfers up to 533 MB/sec
    - Eight level read request queue
    - Four level posted-write request queue
    - Thirty-two level (quadwords) read data FIFO (128 bytes)
    - Sixteen level (quadwords) write data FIFO (64 bytes)
    - Intelligent request reordering for maximum AGP bus utilization
    - Supports Flush/Fence commands
    - Graphics Address Relocation Table (GART)

        - One level TLB structure
        - Sixteen entry fully associative page table
        - LRU replacement scheme
        - Independent GART lookup control for host / AGP / PCI master accesses

    - Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

- **Concurrent PCI Bus Controller**

    - PCI buses are synchronous / pseudo-synchronous to host CPU bus
    - 33 MHz operation on the primary PCI bus
    - 66 MHz PCI operation on the AGP bus
    - PCI-to-PCI bridge configuration on the 66MHz PCI bus
    - Supports up to five PCI masters
    - Peer concurrency
    - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
    - Zero wait state PCI master and slave burst transfer rate
    - PCI to system memory data streaming up to 132Mbyte/sec
    - PCI master snoop ahead and snoop filtering
    - Five levels (double-words) of CPU to PCI posted write buffers
    - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
    - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
    - Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
    - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
    - Delay transaction from PCI master accessing DRAM
    - Read caching for PCI master reading DRAM
    - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
    - Symmetric arbitration between Host/PCI bus for optimized system performance
    - Complete steerable PCI interrupts
    - PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**

  - DRAM interface synchronous with host CPU (66/100 MHz) or AGP (66MHz) for most flexible configuration
  - Concurrent CPU, AGP, and PCI access
  - FP, EDO, SDRAM, and SDRAM-II
  - Supports JEDEC BDDR (Bidirectional Double Data Rate) SDRAM-II standard
    (edge DQ for read and central DQ for write)
  - Virtual Channel SDRAM support
  - Enhanced Synchronous DRAM (ESDRAM) support
  - Different DRAM types may be used in mixed combinations
  - Different DRAM timing for each bank
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in mobile systems
  - Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
  - 8 banks up to 1GB DRAMs
  - Flexible row and column addresses
  - 64-bit data width only
  - 3.3V DRAM interface with 5V-tolerant inputs
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA signals for improved drive
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection)
    or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
  - Independent SDRAM control for each bank
  - Seamless DRAM command scheduling for maximum DRAM bus utilization
    (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four quadwords of CPU to DRAM read prefetch buffers
  - Concurrent DRAM writeback
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - 5-2-2-2-2-2-2-2 back-to-back accesses for EDO DRAM
  - 6-1-1-1-2-1-1-1 back-to-back accesses for SDRAM
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh with staggered RAS timing
  - Programmable refresh rate and refresh on populated banks only
  - CAS before RAS or self refresh

- **Mobile System Support**

  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - Dynamic clock gating for internal functional blocks for power reduction during normal operation
  - Low-leakage I/O pads

- **Built-in NAND-tree pin scan test capability**

- **3.3V, 0.35um, high speed / low power CMOS process**

- **35 x 35 mm, 492 pin BGA Package**

OVERVIEW

The *Apollo Pro* is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / PCI / ISA desktop and notebook personal computer systems from 66 MHz to 100 MHz based on 64-bit Socket-8 (Intel Pentium Pro) and Slot-1 (Intel Pentium-II) super-scalar processors.
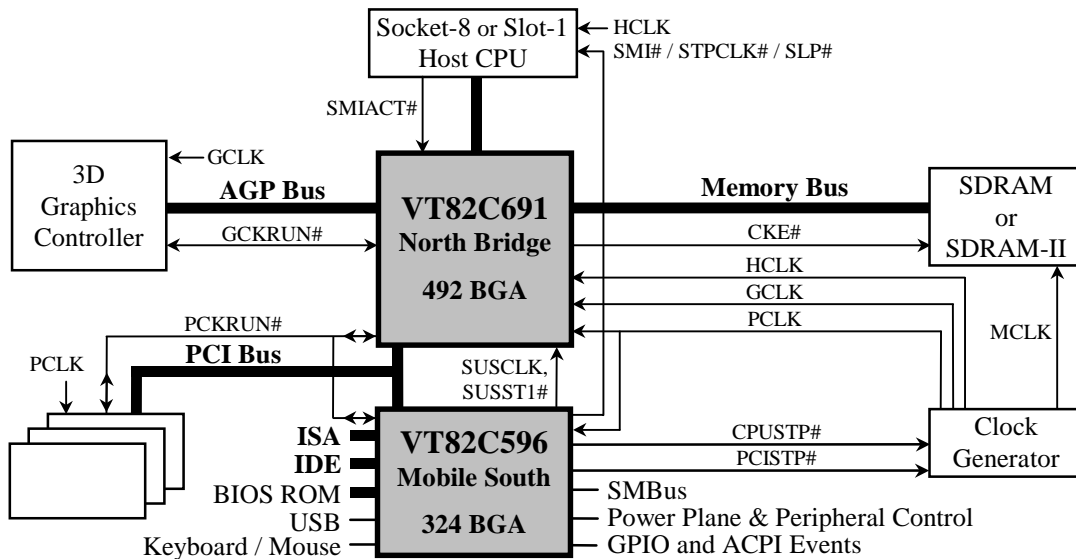

Figure 1. Apollo Pro System Block Diagram Using the VT82C596 Mobile South Bridge

The Apollo-Pro chip set consists of the VT82C691 system controller (492 pin BGA) and the VT82C596 PCI to ISA bridge (324 pin BGA). The system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation. Four cache lines (16 quadwords) of CPU to DRAM write buffers with concurrent write-back capability are included on chip to speed up cache read and write miss cycles.

The VT82C691 supports eight banks of DRAMs up to 1GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM), Virtual Channel SDRAM, Enhanced Synchronous DRAM (ESDRAM), and JEDEC standard BDDR (Bidirectionally strobed Double Data Rate) SDRAM-II in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM Controller can run at either the host CPU bus frequency (66 /100 MHz) or at the AGP bus frequency (66 MHz) with built-in deskew DLL timing control. Coupled with DDR, the VT82C691 allows implementation of the most flexible, reliable, and high-performance DRAM interface with data transfers at 66 / 100 / 133 / 200 MHz.

The VT82C691 also supports full AGP v1.0 capability for maximum bus utilization including 2x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT82C691 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are

supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 324-pin Ball Grid Array VT82C596 PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C596 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter and gather capability and extension to UltraDMA-33 / ATA-33 for 33MB/sec transfer rate, integrated USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated notebook implementations, the VT82C691 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT82C596 "Mobile South" chip, a complete notebook PC main board can be implemented with no external TTLs.

The Apollo Pro chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / ISA computer systems.