# LC11
# DECwriter system manual

DEC-11-HLCB-D

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# CHAPTER 1
# INTRODUCTION

## 1.1 INTRODUCTION

The LC11 DECwriter System is a high-speed teletypewriter system designed to interface with the PDP-11 family of processors to provide both input (keyboard) and output (printer) functions for the system. The system can receive characters from the keyboard or can print at speeds up to 30 characters per second in standard ASCII formats. The LC11 System consists of two distinct components: an LA30 DECwriter and a DEC PDP-11 interface unit, which is referred to as the LC11 Controller.

| | |
|---|---|
| LA30 DECwriter | A dot matrix impact printer and keyboard for use as a full-scale hard copy I/O terminal teletypewriter.<br><br>Keyboard is either 97 or 128 characters. Print set is 64 ASCII characters, 80 characters per line, 10 characters per inch. |
| LC11 Controller | An interface between the DECwriter and the PDP-11 Unibus. Controls data transfers between the DECwriter and other devices in a PDP-11 System. Also monitors printer status, indicates when the keyboard buffer is full, and enables the interrupt logic.<br><br>Also referred to as "control unit," "interface," and "DECwriter control." |

## 1.2 SCOPE

This manual provides the user with the information necessary to operate the LC11 DECwriter System and provides the theory of operation and logic diagrams necessary to understand and maintain the LC11 Controller.

This manual and the appropriate LA30 DECwriter manual must be used together for a complete understanding of the entire LC11 System. The prime subject of this manual is the LC11 Controller. In addition to providing complete coverage of the controller, this manual includes sections covering overall system operation and programming.

The prime subject of the *LA30 DECwriter Manual* (DEC-00-LA30-DA) is the teletypewriter itself. The manual presents a detailed discussion of the print mechanism and electronics including installation, operation, principles of operation, maintenance, troubleshooting, and engineering drawings.

Table 1-1 lists related PDP-11 System documents that are applicable to the LC11 DECwriter System.

## 1.3 SPECIFICATIONS

Operating and physical specifications for the LC11 Controller are given in Table 1-2. Specifications for the LA30 DECwriter are given in Table 1-3.

**Table 1-1**
**Applicable Documents**

| Title | Number | Coverage |
|---|---|---|
| *Unibus Interface Manual,* Second Edition | DEC-11-HIAB-D | Provides detailed theory, flow, and logic descriptions of the Unibus and external device logic. |
| *PDP-11/20 System** (7-volume series) | DEC-11-HR1B-D through DEC-11-HR7B-D | Provides detailed theory of operation, flow, logic diagrams, operation, installation, and maintenance for components of the PDP-11 System including processor, memory, console, and power supply. |
| *PDP-11 Processor Handbook* | DEC, 1972 | A two-part general handbook. The first part discusses system architecture, addressing modes, the instruction set, and programming techniques. The second part is devoted to a discussion of software. |
| *PDP-11 Peripherals and Interfacing Handbook* | DEC, 1972 | A two-part handbook. The first part is devoted to a discussion of the various peripherals used with PDP-11 Systems. The second part provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces. |
| *Paper-Tape Software Programming Handbook* | DEC-11-GGPB-D | Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package. |

*Applicable PDP-11/05, 11/15, and 11/45 manuals provide system coverage on other PDP-11 Systems.

**Table 1-2**
**LC11 Controller Specifications**

| | | | |
|---|---|---|---|
| Registers | Keyboard Status Register (KBS)<br>Keyboard Buffer Register (KBB)<br>Printer Status Register (PRS)<br>Printer Buffer Register (PRB) | | |
| Register Addresses | KBS<br>KBB<br>PRS<br>PRB | 777560<br>777562<br>777564<br>777566 | (when used as console) |
| Data Type | 7-bit parallel character in ASCII code | | |

(continued on next page)

**Table 1-2 (Cont)**
**LC11 Controller Specifications**

| | |
|---|---|
| Interrupts | Priority = BR4 (keyboard slightly higher level than printer)<br>Vectors = location 60 for keyboard (when used as console)<br>location 64 for printer (when used as console)<br>Flags = DONE (keyboard has loaded buffer)<br>READY (printer ready to receive data) |
| Bus Cycles | DATI or DATOB |
| Status Indications | DONE, READY, MAINT, and IE bits for keyboard and printer |
| Size | The LC11 Controller is a single quad module (M7910) that occupies 1/4 of a DD11-A or one of two controller slots in a KA11, KC11, or other PDP-11 processor system unit. |
| Power | 0.25A @ +5V (derived from H720 Power Supply in mounting box where controller is installed) |
| Cable | 25 ft<br>18 twisted pairs |

**Table 1-3**
**LA30 DECwriter Specifications**

| | |
|---|---|
| Printing Speed | 30 characters/sec, asynchronous<br>300-ms carriage return<br>30 line feeds/sec |
| Print Characters | 64 upper case ASCII subset<br>(lower case codes print in upper case) |
| Print Format | 5x7 dot matrix typeface<br>80 characters/line<br>10 characters/in.<br>6 lines/in. |
| Paper | 9-7/8 in. wide<br>tractor-driven continuous form original plus one carbon<br>(can be adjusted for up to 6 copies) |
| Ribbon | nylon, 1/2 in. by 120 ft |
| Keyboard | 97 characters (normal)<br>128 characters (optional)<br>USASCII 1968 characters |
| Dimensions | 20-1/2 in. wide<br>31 in. high<br>24 in. deep |
| Weight | 110 lb |
| DC Power | self-contained |

(continued on next page)

Table 1-3 (Cont)
LA30 DECwriter Specifications

| | |
|---|---|
| Power Input | voltage and frequency dependent on model:<br>LA30 PA 115V/60 Hz<br>LA30 PB 230V/60 Hz<br>LA30 PC 115V/50 Hz<br>LA30 PD 230V/50 Hz |
| Power Dissipation | 300W, maximum |
| Temperature | 50°F to 130°F |
| Humidity | 5% to 90% (non-condensing) |

## 1.4 MAINTENANCE

The basic maintenance philosophy of the LC11 DECwriter System is to present the user with the information necessary to understand normal operation of the system. The user can use this information when analyzing trouble symptoms to determine necessary corrective action. It is beyond the scope of this manual to present detailed troubleshooting information.

General PDP-11 maintenance information is presented in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D, as well as in the *KA11 Processor Manual,* DEC-11-HR2B-D, and the *KC11 Processor Manual,* DEC-11-HKCA-D. Detailed maintenance and troubleshooting information for the DECwriter itself is included in the *LA30 DECwriter Manual,* DEC-00-LA30-DA.

## 1.5 ENGINEERING DRAWINGS

A complete set of reduced engineering drawings and module circuit schematics is provided in a companion volume to this manual which is entitled, *LC11 DECwriter System, Engineering Drawings.* The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1971. Specific symbols and conventions are also included in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D.

## 1.6 TERMINOLOGY

The *PDP-11 Conventions Manual,* DEC-11-HR6B-D, contains a list of terminology and abbreviations used with the PDP-11 family of systems. A glossary of PDP-11 terms, as well as general computer and programming terms, is also included.

# CHAPTER 2
# GENERAL DESCRIPTION

## 2.1 INTRODUCTION

The LA30 DECwriter serves as an input (keyboard) and output (page-printer) device for PDP-11 Systems. The LC11 Controller is an interface that handles parallel data transfers between the DECwriter and the PDP-11 Unibus. The controller consists of a single integrated circuit module mounted on 1/4 of a system unit (such as the DD11-A Peripheral Mounting Panel) or in a small controller slot in a PDP-11 processor. Thus, four DECwriter control interfaces can be mounted in the space of a single system unit.

## 2.2 DECwriter

The LA30 DECwriter is a dot matrix impact printer and keyboard designed for use as a full-scale hard copy I/O terminal teletypewriter. The DECwriter operates at a speed of up to 30 characters per second and prints on a continuous form paper. There are four models available (refer to Table 2-1). The prime difference among models is the input power requirement.

**Table 2-1**
**DECwriter Models**

| Model No. | Voltage | Frequency |
|---|---|---|
| LA30-PA | 115 Vac | 60 Hz |
| LA30-PB | 230 Vac | 60 Hz |
| LA30-PC | 115 Vac | 50 Hz |
| LA30-PD | 230 Vac | 50 Hz |

The DECwriter keyboard is capable of producing either a 128- or 97-character ASCII subset. The letter keys and the additional printing and non-printing (control) keys are laid out similar to a Teletype® keyboard. The keyboard inputs character codes into the interface but does not type directly on the paper unless an echo program is used.

The DECwriter printing head is capable of printing 64 different characters under control of the interface. The printing head is advanced by a stepping motor that is controlled by solid-state logic. Seven spring-loaded wires in the print head are activated by solenoids to impact a standard nylon ribbon in order to form the required character. No special thermal or electrostatic paper is needed and standard 80-column, fanfold paper is used. The DECwriter is normally set for single or two-sheet copy but up to six-part paper can be used by factory adjustment of the print head.

Signals transferred between the DECwriter and the LC11 Controller consist of 7-bit character codes and four control signals. All information, regardless of direction of transfer, is transmitted in parallel. No start or stop codes

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are required. The 7-bit standard ASCII code is used for all printing and non-printing characters. Standard codes for these characters are given in Appendix A.

The DECwriter is a free-standing, pedestal-mounted unit. All operating controls and indicators, with the exception of the power circuit breaker and the printer head motor circuit breaker, are mounted on the front of the DECwriter.

## 2.3 LC11 CONTROLLER

The LC11 Controller handles data one character at a time for parallel transfer to or from the Unibus. The transfer can be handled either by a program interrupt or by testing the control bit (reading the status register) to determine if the keyboard buffer has an available character (DONE bit set) or if the printer buffer is ready for a character (READY bit set). When the processor addresses the bus, the LC11 Controller decodes the incoming address to determine if the DECwriter is the selected external device and, if selected, whether it is to perform an input or output operation. For the following discussion, refer to the simplified block diagram shown in Figure 2-1.

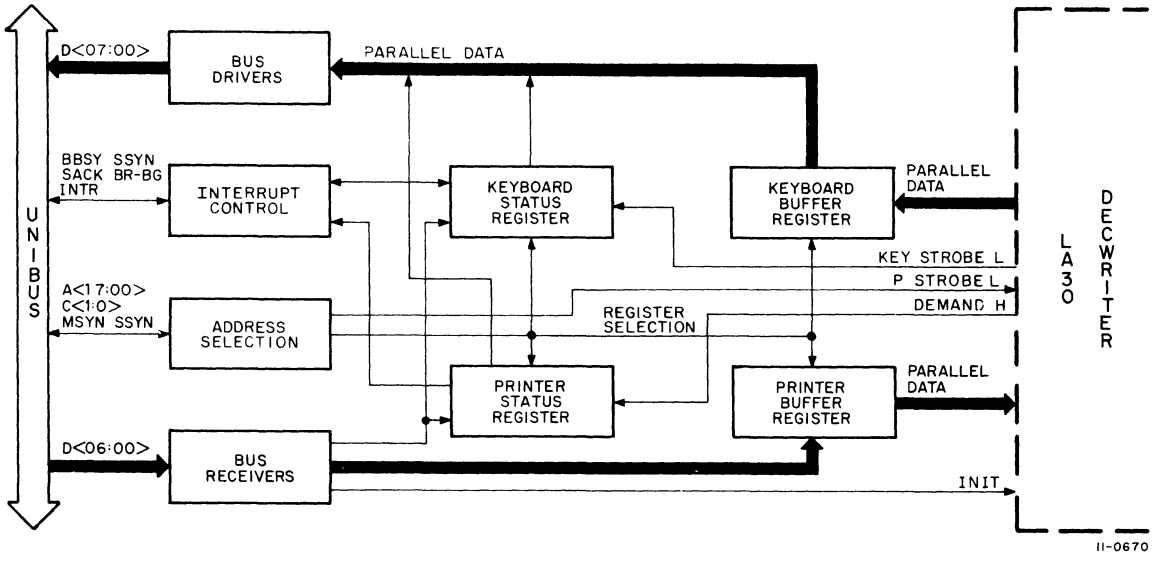



Figure 2-1 LC11 Controller – Simplified Block Diagram

The address selection logic decodes the incoming address and responds to one of four possible sequential addresses. The register that is selected and the type of bus data transfer operation being performed determine whether a keyboard or printer operation is to be used. If, for example, the DECwriter has been selected to accept information for printout, the program waits for a READY flag, which indicates the printer is available and is requesting a character from the controller. At this point, the controller strobes a character from the bus into the printer buffer, which is a series of gates used to transfer the character to the LA30 printer. The printer READY flag is also used to activate the interrupt control logic, provided the logic is enabled (IE true). The purpose of this logic is to cause a program interrupt to a specific vector address which the processor immediately recognizes as coming from the LC11 reader (vector address 60) or printer (vector address 64).

When receiving data from the DECwriter, the operation is essentially the reverse. When the keyboard has assembled a character, it generates a KEY STROBE signal to activate the interface and the 7-bit character is parallel loaded into the keyboard buffer. When the buffer is loaded, the interface sets a DONE flag, indicating to the program that a character is ready for transfer to the Unibus. The DONE flag activates the interrupt control logic (if enabled), thereby causing a vectored interrupt.

The keyboard and printer status registers can be addressed and read by the program to determine the status of the READY flag, DONE flag, MAINT bit, and the two interrupt enable (IE) bits.

Although the information transferred between the DECwriter and LC11 Controller is a 7-bit ASCII character, the controller can add an eighth bit to the keyboard character prior to loading the character onto the bus. This additional bit is controlled by jumpers on the LC11. If the jumper is installed at J1, the state of bit 07 (MAINT bit) in the keyboard data buffer is dependent on the state of the MAINT flip-flop. If the jumper is installed at J2, bit 07 is always 0. A jumper may be installed at either J1 or J2, but never at both. The jumpers and MAINT bit are described more fully in Paragraph 5.4.

# CHAPTER 3
# OPERATION

## 3.1 INTRODUCTION

This chapter provides the information necessary for normal operation of the LC11 DECwriter System and is divided into three major parts: controls and indicators, keyboard, and paper installation. Additional operating procedures, such as ribbon replacement, calibration, and mechanical adjustments, are covered in the *LA30 DECwriter Manual,* DEC-00-LA30-DA.

## 3.2 CONTROLS AND INDICATORS

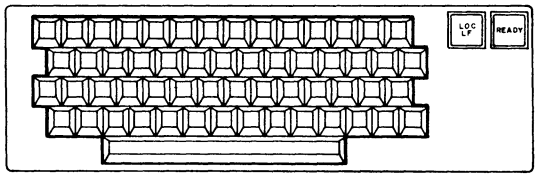
The controls and indicators used to operate the LC11 DECwriter System (with the exception of the keyboard) are shown in Figure 3-1 and listed in Table 3-1. The table lists each control, its location, type, and function.

**Table 3-1**
**Controls and Indicators**

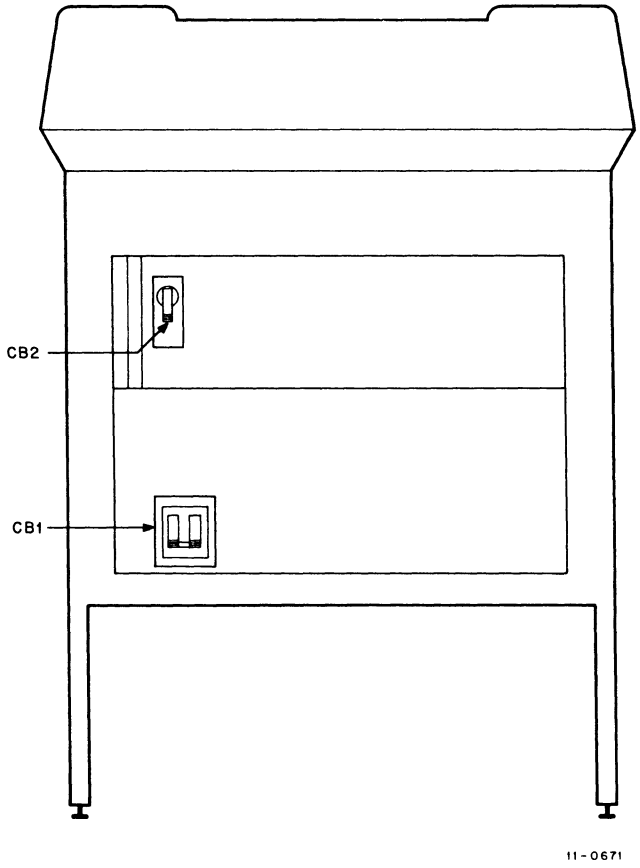
| Control or Indicator | Location | Type | Function |
|---|---|---|---|
| READY indicator | front panel | single light (white) | When lit, indicates that power has been applied to the system and the DECwriter is ready for use in either an input (keyboard) or output (printer) mode. |
| LOC LF switch | front panel | pushbutton switch with indicator | When depressed, advances paper as long as switch is held down. Keyboard and printer operation disabled during line feed. This is an off-line operation and has no effect on the controller. |
| CB2 | rear panel | circuit breaker 2-position toggle switch | When set to on (up) position, applies power to printer stepping motor electronics. |
| CB1 | rear panel | circuit breaker double-pole, single throw | When set to on (up) position, applies primary power to the DECwriter. |

## 3.3 KEYBOARD

The following discussion covers only certain operational notes regarding the keyboard. It is beyond the scope of this manual to provide a detailed description of the keyboard. A complete description is given in the *LA30 DECwriter Manual,* DEC-00-LA30-DA.




a. front panel




b. rear panel

Figure 3-1 DECwriter Controls and Indicators

The keyboard does not type directly into the printer; it simply sends the appropriate ASCII code to the LC11 Controller for transmission to the bus. Therefore, in order to have the keyboard type directly on the paper, it is necessary to use an echo keyboard program. An example of this program is given in Paragraph 4.6. Basically, the controller receives the code from the keyboard and then transmits the same code to the DECwriter printer for printing.

The keyboard can be set to produce either 97 or 128 characters, even though the printer is capable of printing only 64 different characters. The additional keyboard characters can be handled by the LC11 Controller for

transfer to another device, such as a 96-character line printer. Because many of the additional keyboard characters are actually control commands, an output printing device may have fewer characters than the associated keyboard.

## 3.4 LOADING PAPER

The proper procedure for loading paper into the LA30 DECwriter is detailed below and shown in Figure 3-2.

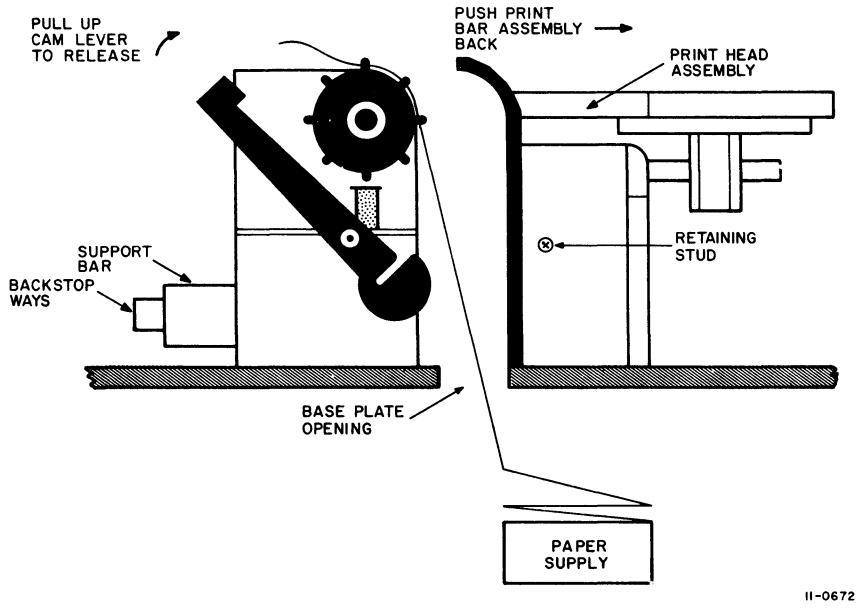



Figure 3-2 Loading Paper into LA30 DECwriter

| Step | Procedure |
|---|---|
| 1 | Set main power circuit breaker CB1 to the off (down) position. |
| 2 | Open DECwriter cover by pressing up on both sides of front panel. |
| | **CAUTION**<br>**Release both ball studs from their spring retainers at approximately the same time to avoid skewing and/or damage to the top cover.** |
| 3 | Raise cam lever located on left-hand side of print bar assembly until it disengages. Slide the bar assembly back. |
| 4 | Feed paper from its box on the floor under the DECwriter up through the opening in the bottom of the base plate casting. Pull fresh supply into machine; discard any unused portions of the previous supply. |
| 5 | Make certain paper is feeding straight and then engage paper with the sprocket feed wheels. |
| 6 | Advance paper by rolling knobs. Make certain paper rolls smoothly. |
| 7 | Feed end of paper over lid and close lid, making certain that both ball studs latch to the base assembly. |
| 8 | Place circuit breaker CB1 to the on (up) position. |

# CHAPTER 4
# PROGRAMMING INFORMATION

## 4.1 SCOPE

This chapter presents general programming information for software control of the LC11 DECwriter Controller. Although a few typical program examples are included, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming, refer to the *Paper-Tape Software Programming Handbook,* DEC-11-GGPB-D.

This chapter is divided into four major portions:

*a.* device registers
*b.* interrupts
*c.* timing considerations
*d.* programming examples

## 4.2 DEVICE REGISTERS

All software control of the LC11 DECwriter Controller is performed through four device registers. These registers have been assigned memory addresses, and can be read or loaded (with the exceptions noted) using any PDP-11 instruction that refers to their address.

The four device registers and associated addresses are listed in Table 4-1. Note that these addresses can be changed by altering the jumpers on the address selection logic. However, any DEC programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed.

**Table 4-1**
**Standard Device Register Assignments**

| Register | Mnemonic | Address* |
|---|---|---|
| Keyboard Status Register | KBS | 777560 |
| Keyboard Buffer Register | KBB | 777562 |
| Printer Status Register | PRS | 777564 |
| Printer Buffer Register | PRB | 777566 |

*When used as a console keyboard/printer.

Figures 4-1 through 4-4 show the bit assignments within the four device registers. The "unused" and "load only" bits are always read as zeros. Loading "unused" or "read only" bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the

| Bit | Designation | Meaning and Operation |
|---|---|---|
| 07 (cont) | READY (cont) | Note that the printer sets READY approximately 2 μs after it receives a carriage return (CR) command. This permits *non-printing* characters, such as line feed, to be received during a carriage return time. If a *printing* character is received during carriage return time, READY is cleared and is then set after CR and printing are complete.<br><br>When set, READY causes an interrupt, provided IE (bit 06) is set. Read only bit. |
| 06 | IE | Interrupt enable bit. When this bit is set, it enables READY (bit 07) to start an interrupt sequence. Read/write bit; cleared by INIT. |
| 05–03 | Unused | Not Applicable |
| 02 | MAINT | When set, this bit forces bits 00–07 of the keyboard data buffer to read as all 0s. It also causes loading of the printer buffer to set the keyboard DONE flag. If jumper J1 is connected, it causes KBB bit 07 to be read as a 1. Read/write bit; cleared by INIT. |
| 01–00 | Unused | Not Applicable |

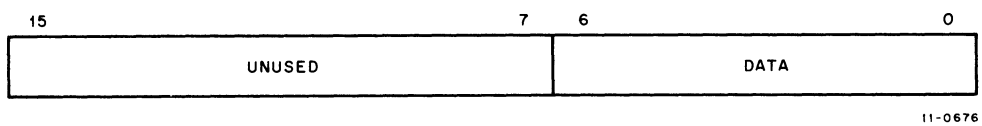



Figure 4-4 Printer Data Buffer Register – Bit Assignments

| Bit | Designation | Meaning and Operation |
|---|---|---|
| 15–07 | Unused | Note that bit 07 is not offered as a parity option with the LA30. |
| 06–00 | Data Buffer | 7-bit ASCII character buffer. Transfers data from the Unibus to the LA30 printer.<br><br>**NOTE**<br>**Any instruction (word or byte) that modifies the printer data buffer clears the READY bit and initiates the print cycle.**<br><br>Load only. |

## 4.3 INTERRUPTS

The LC11 Controller uses interrupts to gain control of the bus in order to perform data transfers. When the processor grants the request and other Unibus conditions are met, the LC11 gains control of the bus (becomes bus master) and interrupts the processor so that the program can branch to a handling routine that requests data from, or sends data to, the LC11.

When the keyboard DONE flag and associated IE bit are set, it activates the interrupt control logic so that it can notify the processor that a character has been assembled. When the printer READY flag and associated IE bit are

set, it activates the interrupt control logic so that it can notify the processor that another character can be loaded into the printer buffer.

The keyboard initiates an interrupt whenever DONE=1 and IE=1 become true. The vector address is 60 when used as a console keyboard. The printer initiates an interrupt whenever READY=1 and IE=1 become true. The vector address in this case is 64 if used as a console printer. The standard priority interrupt level is set at the BR4 level for both the keyboard and the reader. The keyboard has a slightly higher priority.

Although the vector addresses and priority levels are standard, they can be changed by the user, if desired. However, all DEC programs reference the standard addresses and priority and, therefore, must also be changed if the standard assignments are changed.

**NOTE**

**Although the bus request level can be 4, 5, 6, or 7, both the printer and the keyboard must be at the same level. For example, if the standard BR level is changed to 6, both keyboard and printer are at level 6.**

## 4.4 TIMING CONSIDERATIONS

The LC11 Controller provides parallel operation on the bus and operates in a demand response mode; therefore, there are no special timing requirements that must be considered.

The basic operating times of the keyboard and printer are as follows:

| | |
|---|---|
| Keyboard | maximum key-in rate = 30 characters/sec<br>time between buffer loads = 33.3 ms |
| Printer | printing rate = 30 characters/sec<br>carriage return time = 300 ms<br>line feed time = 33.3 ms<br>time between buffer loads = 33.3 ms (during printing) |

## 4.5 PROGRAMMING NOTE

If any difficulty is experienced when reading the keyboard buffer register (KBB), inspect the jumper at J1 or J2 on the M7910 module. There must be a jumper at either J1 or J2, but not both. If there is no jumper, the bus may hang with BUS D07 asserted. If both jumpers are present, the keyboard buffer reads as all 0s even if the MAINT bit is not set.

## 4.6 PROGRAMMING EXAMPLES

The following examples represent typical programs for reading a character from the keyboard and for echoing the keyboard:

*a.* Reading a Character (from Keyboard)

```
LOOP:   TSTB TKS        ;LOOK FOR DONE
        BPL LOOP        ;WAIT IF DONE=0
READ:   MOV TKB,R0      ;READ CHARACTER

        *HALT
```

*JMP LOOP or some other appropriate instruction may be used instead of HALT.

*b.* Echoing Keyboard

```
ECHO:   TSTB TKS        ;CHARACTER AVAILABLE?
        BPL ECHO        ;WAIT IF DONE=Ø
WAIT:   TSTB TPS        ;IS PRINTER READY?
        BPL WAIT        ;WAIT IF READY=Ø
        MOV TKB,TPB     ;PRINT CHARACTER
        BR ECHO         ;REPEAT FOR NEXT CHARACTER
```

# CHAPTER 5
# THEORY OF OPERATION

## 5.1 INTRODUCTION

This chapter provides a detailed description of the LC11 DECwriter Controller. The controller may be divided into four major functional areas: selection logic, interrupt logic, keyboard logic, and printer logic. Each of these areas is covered separately in subsequent paragraphs. The purpose of each of these functional areas is as follows:

| | |
|---|---|
| Selection Logic | Determines if the DECwriter has been selected for use, which register is to be used, and what type of transfer (DATI or DATO) is to be performed. |
| Interrupt Logic | Permits the controller to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by user. Consists of the interrupt control logic and the IE (interrupt enable) bits in the keyboard and printer status registers. |
| Keyboard Logic | Consists of a data buffer that receives one character from the keyboard for parallel transmission to the bus and a status register that indicates to the program when the character has been loaded. Also provides the interrupt enable bit so that the character can be transferred by means of an interrupt. |
| Printer Logic | Consists of gating logic and a status register. The gating logic transfers the data to the printer. The status register indicates when the printer is ready and also provides an interrupt enable bit so that the data can be transferred by means of an interrupt. |

## 5.2 SELECTION LOGIC

The address selection logic decodes the address information from the bus and provides four select lines and three (two are used) gating signals that determine which register has been selected and whether it is to perform an input or output function. The logic jumpers are arranged so that the module responds only to standard device register addresses 777560, 777562, 777564, and 777566 (jumpers in bit positions 3 and 7). Although these addresses have been selected by DEC as the standard assignments for the LC11 DECwriter Controller, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the LC11 standard address assignments must be modified if other than the standard assignments are used.

The first five octal digits of the address (77756) indicate that the LC11 has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. Actually, the operation is always a byte operation even if a word operation is selected because bits 8 through 15 in all four registers are unused. The two mode control lines, C00 and C01, determine whether the selected register is to perform an input or output operation.

Address lines A02 and A01 are decoded to produce one of four select line signals, which select the register to be used (refer to Table 5-1). The mode control lines produce IN and OUT LOW gating signals (Table 5-1) that

determine whether the bus cycle is a DATI or DATO. Note that an IN gating signal is not supplied for select line 6 (printer buffer register) because the printer buffer cannot be read from the bus; it is a load only register. Note also, that an OUT LOW gating signal is not provided for select line 2 because the keyboard buffer is a read only buffer and cannot be loaded from the bus.

**Table 5-1**
**Gating and Select Line Signals**

| Select Line | Gating Signal | Function Selected | Register | Bus Cycle |
|---|---|---|---|---|
| 0 | IN | Keyboard status to bus | KBS | DATI |
| 2 | IN | Keyboard buffer to bus | KBB | DATI |
| 4 | IN | Printer status to bus | PRS | DATI |
| 0 | OUT LOW | Bus to keyboard status | KBS | DATO or DATOB |
| 4 | OUT LOW | Bus to printer status | PRS | DATO or DATOB |
| 6 | OUT LOW | Bus to printer buffer | PRB | DATO or DATOB |

### 5.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 5-1. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the LC11 Controller is used, an OUT transfer is a transfer of data out of the master (the processor) and into the device. Likewise, an IN transfer is the operation of the controller furnishing data to the processor.

The address selection logic input signals consist of 18 address lines, A ⟨17:00⟩; 2 bus control lines, C ⟨1:0⟩; and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 5-2. Note that all input gates are standard bus receivers.

*a.* Line A00 is used for byte control.

*b.* Lines A01 and A02 are decoded to select one of the four addressable device registers.

*c.* Decoding of lines A ⟨12:03⟩ is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.

**NOTE**
**Connection of jumpers on the M7910 quad module is identical to the method used on earlier versions of the LC11 Controller which employed an M105 Address Selector Module.**

*d.* Address lines A ⟨17:13⟩ must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

**NOTE**
**Pin EA1 (EXT. GND) must be grounded by the user to ensure proper operation of the address selection logic.**

### 5.2.2 Outputs

The address selection logic output signals permit selection of four 16-bit registers (actually, only the low-order byte of each register is used) and provide three signals used for gating information to and out of the master device. All of the output signals are listed in Table 5-1. Note, however, that only two gating signals are listed (IN and OUT). Actually, there are two OUT signals: OUT LOW and OUT HIGH. The address selection logic is shown on drawing LC-3. Table 5-2 and 5-3 indicate the input signals that select the control output line states.

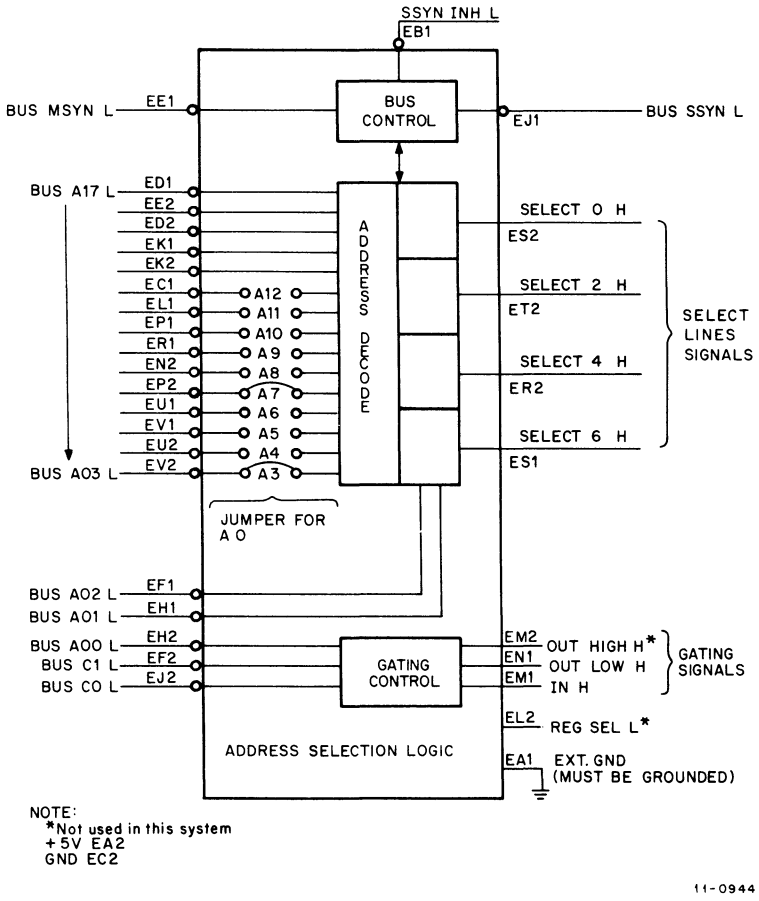



Figure 5-1 Address Selection Logic – Simplified Diagram

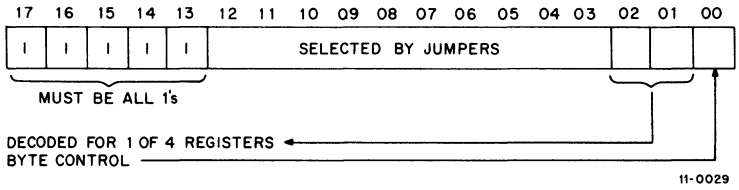



Figure 5-2 Controller Select Address Format

### 5.2.3 Slave Sync (SSYN)

When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the address selection logic.

Table 5-2
Select Lines

| Input Lines A ⟨02:01⟩ | Select Lines True (+3V) |
|---|---|
| 00 | 0 |
| 01 | 2 |
| 10 | 4 |
| 11 | 6 |

NOTES: 1. Lines A ⟨17:13⟩ must be all 1s (0V on Unibus).
2. Lines A ⟨12:03⟩ are selected by jumpers.

Table 5-3
Gating Control Signals

| Mode Control C ⟨1:0⟩ | Byte Control A00 | Gating Control Signals True (+3V) | Bus Sequence |
|---|---|---|---|
| 00 | 0 | IN | DATI |
| 00 | 1 | IN | DATI |
| 01 | 0 | IN | DATIP |
| 01 | 1 | IN | DATIP |
| 10 | 0 | OUT LOW<br>OUT HIGH | DATO |
| 10 | 1 | OUT LOW<br>OUT HIGH | DATO |
| 11 | 0 | OUT LOW | DATOB |
| 11 | 1 | OUT HIGH | DATOB |

NOTE: Gating control signals may become true although select lines are not.

## 5.3 INTERRUPT CONTROL LOGIC

The interrupt control logic (drawing LC-3) permits the LC11 Controller to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 060 for the keyboard and 064 for the printer (jumpers in bit positions 4 and 5). Although this is the recommended vector address when used as a console keyboard/printer, the user may change the jumpers to correspond to any address desired, but MainDEC programs and other software referencing the standard vector address assignments must be changed to reflect the new assignments. Changing the jumpers affects only the first part of the address (06). The last digit is controlled internally by the interrupt control logic and is always either 0 or 4.

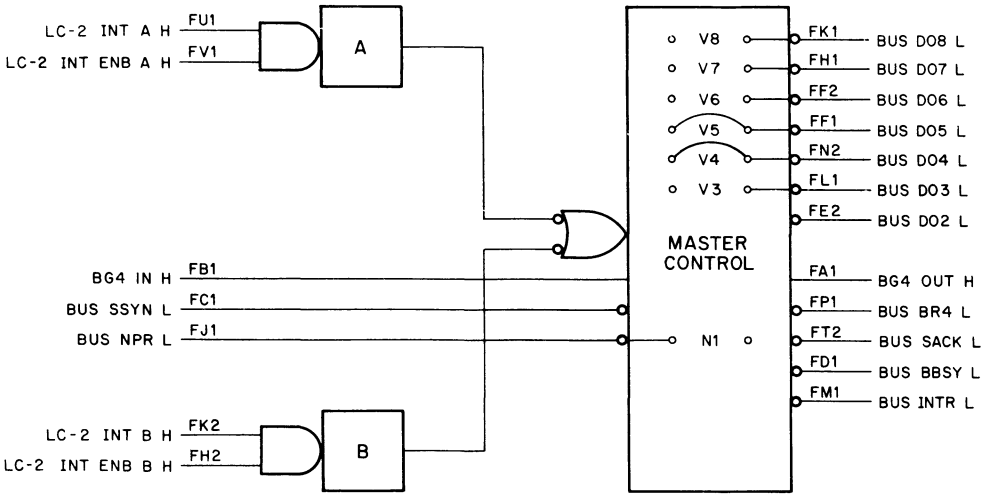
**NOTE**
**Connection of jumpers on the M7910 quad module is the reverse of the method used on M782 and M7820 Interrupt Control Modules and the same as the M7821 module. On this quad module, a jumper represents a 1, no jumper represents a 0.**

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control. The A input is connected to the keyboard control logic and provides a vector address of 60; the B input is connected to the printer control logic and provides a vector address of 64.

Before the A input interrupt logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. The logic that produces these two signals is shown on drawing LC-2. When the KBD INT ENB (interrupt enable) bit is loaded by the program, a 1 is loaded onto bus data line BUS D06, which is the D input to the KBD INT ENB flip-flop. The C input to the flip-flop is high when both SELECT 0 and OUT LOW are high, indicating that the keyboard status register has been selected for loading. The output of the flip-flop is INT ENB A H which is applied to the interrupt control logic as an enabling signal.

The second signal that must be present to generate an interrupt is INT A H. When the LA30 DECwriter produces a KEY STROBE signal, indicating a character is ready for transfer (DONE), it sets the KBD DONE flip-flop which produces the INT A H pulse that causes the Master Control to initiate an interrupt. If the LA30 does not issue KEY STROBE but the LC11 MAINT bit is set, the output of the MAINT flip-flop enables a gate that allows P STROBE L (loading the printer buffer) to set KBD DONE to produce INT A H.

The A input section of the interrupt logic (see Figure 5-3) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the LC11 Controller is BR4 but this may be changed on the priority plug, if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the LC11 Controller has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false), the master control section asserts BBSY.




NOTES:
1. Bus request made on level 4.
2. Interrupt vector is 60 for input A; 64 for input B.
3. Jumpers are: jumper V bits for a 1; jumper N1 to sample NPR line.

11-0943

Figure 5-3 Interrupt Control Logic – Simplified Block Diagram

The B input interrupt logic operates in a similar manner to that of the A input logic. In this case, the two input signals that must be high are: INT B and INT ENB B. The logic for these two signals is shown on drawing LC-2.

When a 1 is loaded into bit 06 of the printer status register, it sets the PRINTER INT ENB flip-flop to produce INT ENB B which is applied to the interrupt control logic as an enabling signal.

The second signal that must be present is INT B H. When the LA30 DECwriter is ready to receive data, it issues a P DEMAND H signal which sets the PRINTER RDY flip-flop to inform the program that the printer is ready to receive data. The output of the flip-flop is INT B H which causes the Master Control logic to initiate an interrupt.

The B input interrupt logic functions in an identical manner to the A input logic except that it generates a different vector address. Although both the reader and the printer are at a BR4 level, the reader has a slightly higher priority.

Note that the same bus data line (BUS D06) is used as an input for both the KBD INT ENB and PTR INT ENB flip-flops. Therefore, any time a 1 is loaded into bit position 06, the D lines of both flip-flops are true. However, the flip-flop that becomes set is dependent on the C line input which consists of the SELECT line and GATING signals used to reference either the keyboard or the printer status register.

Once the LC11 Controller has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown in Figure 5-3. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1.

The six selectable (jumpered) lines determine the two most significant octal digits of the vector address. The least significant octal digit is controlled by bit 02 so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs on Channel A, bus line D02 is *not* asserted, and the interrupt causes a vector at location 060. When an interrupt occurs at the B input logic, bus line D02 is asserted, and the interrupt causes a vector at location 064. Note that the first two digits (06) can be changed by jumpers but the last digit is always either 0 or 4.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT and INT ENB must be satisfied. These levels must be true until the interrupt service routine clears INT or INT ENB. Once bus control has been attained, it is released when the processor responds with BUS SSYN after it has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests from that input (A or B) even if INT and INT ENB remain asserted. In order to make another bus request, INT or INT ENB must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the master control is used to generate interrupts. Note that the interrupt control logic used in the LC11 Controller is not capable of issuing NPR requests. To improve NPR latency, the NPR line is sampled and prevents completion of an interrupt sequence until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the controller module.

**CAUTION**

**Only certain PDP-11 processors can work with the special circuit described above. The jumper (N1) on the module, when cut, prevents the special circuit from working.**

## 5.4 KEYBOARD LOGIC

During keyboard operation of the DECwriter, the keyboard buffer register in the controller receives each character as it is produced. The character is stored in the buffer until placed on the Unibus for transfer to memory or some other bus device, or until another KEY STROBE L signal again loads the buffer. Note that there is no overrun indication and the previous character is lost if not read before the next key is depressed. The keyboard buffer and associated logic is shown on drawing LC-2.

Whenever a key on the DECwriter keyboard is depressed, the DECwriter logic produces a 7-bit ASCII code that represents the symbol shown on the key. This 7-bit code is applied in parallel to the data input lines of the seven flip-flops comprising the keyboard buffer register. Although each bit of the buffer functions as an individual flip-flop, six are physically on a single 74174 IC chip. In the subsequent discussions, each bit is referred to as a single flip-flop; however, on the logic diagram (LC-2) they are shown as a 74174 IC. Therefore, a simplified logic diagram of the IC chip is shown in Figure 5-4.

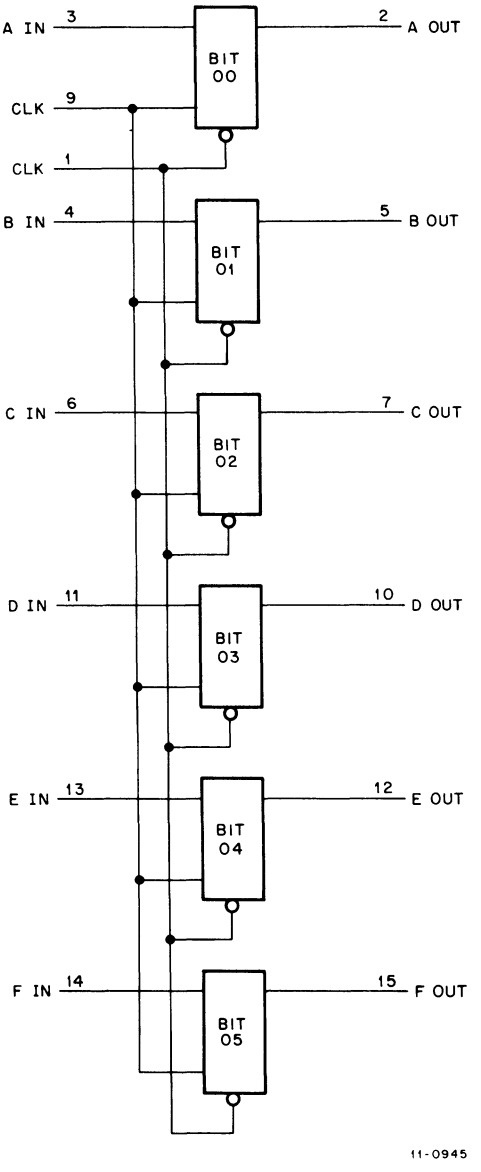



Figure 5-4 IC 74174 – Simplified Logic Diagram

After the data has had time to settle, the DECwriter issues a KEY STROBE L signal, which is used as a clock input for the seven flip-flops. Thus, when the KEY STROBE L is issued by the DECwriter, the LC11 strobes the information on the data lines into the buffer. At this point, the status of each flip-flop (set or cleared) corresponds to the information that was placed on the corresponding data line by the DECwriter.

The output of each flip-flop is tied to one input of an associated 2-input NAND gate. The other input for all seven gates is connected to a NAND gate that is true only when both SELECT 2 and IN are true, which indicates the buffer has been selected for reading. When these conditions are true, the buffer output is coupled to bus data lines BUS D00 through BUS D06.

As explained in Paragraph 5.3, the KEY STROBE L signal also sets a flip-flop that produces the INT A H signal that initiates an interrupt request so that the contents of the buffer can be transferred to the bus as a result of an interrupt sequence, as well as just waiting for the KBD DONE flag mode. This INT A H signal is also applied to one leg of a 2-input AND gate to provide the DONE indication (bit 07) when reading the keyboard status register. The other input to the AND gate is qualified when the keyboard status register is addressed for reading (SELECT 0 H and IN H are both true).

An eighth data bit can also be gated onto the bus (BUS D07) if desired. However, this bit does not come directly from the DECwriter keyboard but is provided by a jumper on the controller module. If a jumper is added at J1, the state of this bit is dependent on the condition of the MAINT flip-flop. If MAINT is cleared, bit 07 is a 1; if MAINT is set, bit 07 is a 0. If a jumper is added at J2, bit 07 is always read as 0.

**CAUTION**

**A jumper must be added to either J1 or J2 but never to both. If neither jumper is present, the bus may hang with BUS D07 asserted. If both jumpers are present, the keyboard buffer reads as all 0s, regardless of the state of the MAINT flip-flop. In effect, regardless of the input character from the keyboard, the controller can read only 0s.**

Note that there is no bit 00 for the keyboard. The keyboard data bits are numbered 1 through 7 (KB1 through KB7 on the drawing) and correspond to bus data lines D00 through D06 respectively. Thus, for example, keyboard bit 3 is read on bus data line D02.

## 5.5 PRINTER LOGIC

During printer operation of the DECwriter, a character from memory or some other bus storage device is transferred to the DECwriter for printing. When a print operation is desired, the program must wait for a READY flag to be set, indicating that the DECwriter is ready to receive a character for printing. This flag is set by the printer logic and cannot be controlled by the LC11 Controller. When the READY flag is received (P DEMAND H) it causes an interrupt to be generated, and the controller loads a character from the bus into the printer buffer register (PRB). This character and a print command signal are strobed into the DECwriter. The DECwriter immediately drops the READY flag to indicate that it is busy and cannot accept another print command at this time, and then prints out the character. After the character is printed, the READY flag is again set and the process repeated for the next character from the bus. The printer buffer register and associated logic is shown on drawing LC-2.

Whenever the DECwriter is ready for printing, it sets the READY flag which is applied to the LC11 Controller as the P DEMAND H signal. This signal passes through a gate and inverter and is applied as a clock input to the PTR RDY flip-flop, thereby setting it. The output of this flip-flop is gated onto bus line D07. Therefore, the P DEMAND H signal sets the READY bit (bit 07) in the printer status register.

The output of the PTR RDY flip-flop is also applied to the interrupt control logic as INT B H. Thus, an interrupt sequence is started by READY, provided bit 06 (IE) in the printer status register is set. Bit 06 causes the INT ENB H signal to be generated. Interrupts are described in Paragraph 5.3.

When the interrupt request is granted, the controller loads a character into the DECwriter, issues a print command, and clears the READY bit in the status register. This sequence is described in the following paragraphs.

During the interrupt, the program addresses the printer buffer register and places a 7-bit ASCII code, representing one character, on Unibus data lines D00 through D06. The levels on the bus lines are inverted and applied to printer input lines P01 through P07, respectively. Note that there is no printer P00 line. Therefore, bus line D00 feeds printer line P01, bus line D01 feeds P02, etc.

As soon as the program addresses the printer buffer register, the SELECT 6 H and OUT LOW H signals become true and qualify a gate to produce P STROBE L. The P STROBE L signal is the print command sent to the DECwriter (referred to as PRINT STROBE in the printer logic). When the printer receives the print command, it starts printing the data from the buffer and drops the READY flag, causing P DEMAND H to go low. If the program addresses the printer status register while P DEMAND H is still low, the READY status bit is clear because P DEMAND H being low prevents the PTR RDY flip-flop from setting. Thus, when the printer buffer register is addressed, a print command is issued, data is gated from the bus into the DECwriter, and the READY flag drops.

## 5.6 INTERFACE SIGNALS

The operational state of the DECwriter is determined by two signals (KEY STROBE L and P DEMAND H) applied from the DECwriter to the LC11 Controller logic. The KEY STROBE L signal, when active (low), indicates that the DECwriter keyboard has assembled a character for the keyboard buffer; the P DEMAND H indicates that the printer is able to accept a character for printing. Either one, but not both, of these signals may be true at any given time, even though PRINTER READY and KEYBOARD DONE are both true.

Nine input lines originate in the controller logic and terminate in the DECwriter. Seven of these are PRINTER DATA (P01 through P07), the eighth is the STROBE line, and the ninth is the P INiT signal. When the P STROBE L line goes true, data on the seven PRINTER DATA lines is parallel-transferred into the printer, causing P DEMAND H to go low until the printer logic has shifted the printable character into its associated memory.

Nine output lines originate in the DECwriter and terminate in the controller logic. Seven of these are KEYBOARD DATA lines (KB1 through KB7), the eighth is the KEY STROBE line, and the ninth is the P DEMAND H signal. When the KEY STROBE L line goes true, data on the seven KEYBOARD DATA lines is parallel-transferred into a controller flip-flop register. This register stores the character until it is loaded onto the Unibus for transfer to some other bus device, such as memory, or until another keyboard character is depressed.

All interface signals are shown in Figure 5-5 and listed in Table 5-4 along with their related function. The signal names used on the table are the functional names; the name in parenthesis indicates the nomenclature used on the print set. Table 5-5 lists these same interface signals, but includes wiring information. A complete list of ASCII codes (as used in the LA30 DECwriter) is given in Appendix A.

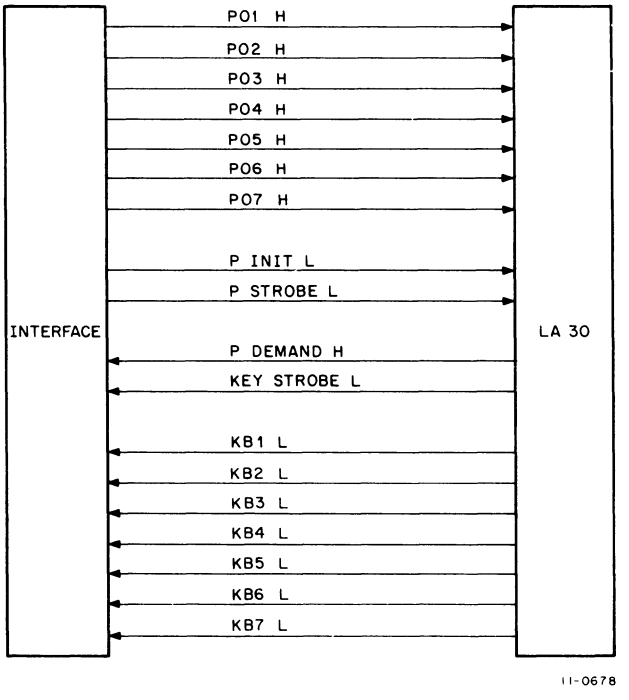



Figure 5-5 Interface Signals

**Table 5-4**
**Controller/DECwriter Interface Signals**

| Signal | Source | Function |
|---|---|---|
| READY<br>(P DEMAND H) | DECwriter | Indicates to the user's system that the DECwriter printer is available for use; synchronizes data transmission between the DECwriter and LC11 Controller.<br><br>The P DEMAND H signal requests a character from the controller and this signal remains true until the PRINT STROBE signal is received. The READY indication (P DEMAND H) is disabled while the character is being stored in memory and during the print operation. When printing is complete, READY again becomes true unless KEY STROBE is true. |
| PRINT STROBE<br>(P STROBE L) | Controller | P STROBE L indicates that the printer can accept the information on the PRINTER DATA lines. Each time the P STROBE L signal occurs, the DECwriter printer samples the data lines and READY goes false while the data character is being stored. |
| PRINTER DATA<br>(P01 – P07) | Controller | PRINTER DATA is coded information transmitted from the controller to the printer on seven data lines. Each character of the ASCII character set is transmitted as 7-bit PRINTER DATA. |
| KEYBOARD STROBE<br>(KEY STROBE L) | DECwriter | KEY STROBE indicates when the keyboard has generated a character for transfer to the controller. Each time the KEY STROBE signal occurs, the controller samples the KEYBOARD DATA lines, and stores the character in a buffer for transfer to the Unibus. |
| KEYBOARD DATA<br>(KB1 – KB7) | DECwriter | KEYBOARD DATA is coded information transmitted in parallel from the DECwriter keyboard to the controller on seven data lines. Each character of the ASCII character set is transmitted as a 7-bit KEYBOARD DATA character.<br><br>The controller may add an eighth bit to this data prior to loading on the bus. |

Table 5-5
Controller Input/Output Signals

| Signal Name | Direction | LC11 Pin | LA30 Pin | Signal Function |
|---|---|---|---|---|
| KEY STROBE L | From LA30 | Z | M1 | Indicates character is ready in keyboard buffer |
| KEYBOARD DATA | From LA30 | | | These seven data bits represent the ASCII code for the character being transmitted from the keyboard. |
| KB1 | | N | S1 | |
| KB2 | | L | D2 | |
| KB3 | | V | H2 | |
| KB4 | | R | M2 | |
| KB5 | | F | P2 | |
| KB6 | | J | S2 | |
| KB7 | | T | T2 | |
| PRINTER READY (P DEMAND H) | From LA30 | X | B1 | Indicates printer is ready to accept a character from the interface. |
| PRINT STROBE (P STROBE L) | To LA30 | VV | E2 | Print command that causes printer to accept data and print it out. |
| PRINTER DATA | To LA30 | | | These seven data bits represent a character from the controller that is being transferred to the DECwriter for printing. |
| P01 | | JJ | D1 | |
| P02 | | LL | E1 | |
| P03 | | BB | H1 | |
| P04 | | FF | J1 | |
| P05 | | TT | K2 | |
| P06 | | RR | L1 | |
| P07 | | DD | P1 | |
| INIT L | To LA30 | NN | V2 | Initializes printer. |

# APPENDIX A
# CHARACTER CODES

| $b_7$ | $b_6$ | $b_5$ | | | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $b_4$ | $b_3$ | $b_2$ | $b_1$ | COLUMN / ROW | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | NUL | DLE | SP | 0 | @ | P | ` | p |
| 0 | 0 | 0 | 1 | 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| 0 | 0 | 1 | 0 | 2 | STX | DC2 | " | 2 | B | R | b | r |
| 0 | 0 | 1 | 1 | 3 | ETX | DC3 | # | 3 | C | S | c | s |
| 0 | 1 | 0 | 0 | 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| 0 | 1 | 0 | 1 | 5 | ENQ | NAK | % | 5 | E | U | e | u |
| 0 | 1 | 1 | 0 | 6 | ACK | SYN | & | 6 | F | V | f | v |
| 0 | 1 | 1 | 1 | 7 | BEL | ETB | ' | 7 | G | W | g | w |
| 1 | 0 | 0 | 0 | 8 | BS | CAN | ( | 8 | H | X | h | x |
| 1 | 0 | 0 | 1 | 9 | HT | EM | ) | 9 | I | Y | i | y |
| 1 | 0 | 1 | 0 | 10 | LF | SUB | * | : | J | Z | j | z |
| 1 | 0 | 1 | 1 | 11 | VT | ESC | + | ; | K | [ | k | { |
| 1 | 1 | 0 | 0 | 12 | FF | FS | , | < | L | \ | l | ¦ |
| 1 | 1 | 0 | 1 | 13 | CR | GS | – | = | M | ] | m | } |
| 1 | 1 | 1 | 0 | 14 | SO | RS | . | > | N | ^ | n | ~ |
| 1 | 1 | 1 | 1 | 15 | SI | US | / | ? | O | _ | o | DEL |

128 – CHARACTER SET (KEYBOARD)

97 – CHARACTER SET (KEYBOARD)

64 – CHARACTER SET (PRINTER)

11-0677

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