1531

Thurlby

LA-160

logic analyser

SERVICE MANUAL

For Service Manuals Contact
MAURITRON TECHNICAL SERVICES
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INDEX

INTRODUCTION

This manual is intended to assist skilled personnel in the maintenance and repair of the LA-160 logic analyser.

Knowledge of digital and analogue electronic theory and practice, and access to normal test instruments is assumed.

The analyser should only be dismantled if absolutely necessary. Repair work inexpertly carried out will void the guarantee.

N.B. This manual does not contain any operating instructions for the analyser. For operating information refer to the 'Operating Manual'.

DISMANTLING THE ANALYSER

To dismantle the analyser, first remove all connecting leads including the AC line cord. Remove the four bolts which pass through the foot mouldings. Lift up the top cover using a firm but even pressure. Remove the two side mouldings. The analyser can now be lifted upwards out of the bottom cover.

When re-assembling the instrument ensure that the case mouldings are re-fitted in their original orientation. Take care to avoid damage to the edges of the front panel membrane when fitting it into the slots of the top and bottom covers.

GENERAL MECHANICAL DESCRIPTION

The LA-160 is constructed around two printed circuit boards mounted one above the other and separated by an aluminium plate.

The lower PCB carries the power supply, the data acquisition circuitry, the oscilloscope interface, the RS232 interface and other input/output circuitry.

The upper PCB carries the microprocesor components and the LED displays. Connection is made to the lower PCB via an unpluggable ribbon cable connector and two soldered wires which carry the power rails. The membrane type keyboard is also connected via an unpluggable flexible tail.

CIRCUIT DESCRIPTIONS

a) The Microprocessor PCB

A 6502 microprocessor (IC3) communicates with a 6522 versatile interface adaptor (IC2), two 8K x 8 Eproms (IC6 and IC11), and a 2K x 8 static RAM (IC5) via an 8 bit data bus.

The address bus is used in conjunction with the address decoder IC4 which provides 8 chip select lines. IC2 provides two 8 bit input/output ports. The 8 bit latch (IC7) and 6 bit latch (IC11) together provide 14 dedicated output lines, whilst IC8 provides 4 dedicated input lines, (IC9 is not fitted).

Transistor Q19 operates as a 4MHz crystal controlled oscillator which is divided by IC10 to provide a 1MHz clock signal for the microprocessor.

Transistor Q20 is used to disable the astable, formed by the schmitt trigger inverter 1/6 IC1, whilst the interrupt request line is regularly pulsed. If interrupt request pulses cease, as happens at switch-on or in the event of a program corruption, the astable pulses the microprocessor reset line in order to correctly restart the program.

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The eight digit common cathode LED display is fully multiplexed. The digit lines are driven by inverting NPN saturating transistors controlled by the 8 bit latch IC7. The segment lines are driven by NPN emitter followers controlled from port A of IC2 with the segment current being defined by resistors in series with the collector of each transistor. (Resistor pack RP1).

The keyboard is arranged as an 8 x 4 matrix of which only 31 positions are used. The four keyboard scan lines are connected to port B of IC2 whilst the eight drive lines are commoned with the eight display digit drive lines.

The 2K x 8 CMOS RAM IC6 has battery back-up supplied via Q2. The IC6 chip select line is gated by Q1 to ensure that it is de-selected before the 5 volt rail falls below the voltage needed to maintain correct operation of the other circuits.

The interface between the Microprocessor PCB and Acquisition PCB is performed via 16 lines. These are the four lines from the two serial ports of IC2, four lines from port B of IC2, four lines to the input latch IC8, and four lines from the output latch IC12.

b) The Power Supply

TheLA-160 power supply provides three separate voltage rails. These are +5V (1.3A), -5V5 (10mA) and 5V floating (100mA). The +5V supply powers all the main circuitry, the -5V5 supply is used as the negative supply for the RS232 interface, while the 5V floating supply is used for powering external options such as data pods.

The +5V supply is series regulated by an NPN pass transistor (Q5) mounted on the back panel to disipate heat. This is controlled by transistors Q6 and Q7 and zener diode Z2. The thermister TH1 provides termperature stability. The preset potentiometer VR5 is used to set the supply to exactly 5V.

The -5V5 supply is unregulated and will vary with AC line input volts.

The 5V floating supply is regulated by the three terminal regulator IC50. R44 causes the more negative side to be connected to OV unless an LC-02 data pod is fitted in which case the LC-02 links the more positive side to OV, turning it into a -5V supply.

c) The Data Acquisition Section

The basic operation of the Data Aquisition Section of the analyser is most easily understood by reference to the simplified block diagram of Fig 1. This diagram shows the main functional blocks of the data acquisition section but omitts the controlling shift registers and some other components.

The data aquisition section interfaces to the microprocessor PCB via a 16 way connector (connector E). Most of the control of the acquisition section is achieved via two lines which operate six serially linked 8 bit shift registers. The 48 parallel outputs from these set up all the main functions of the analyser such as selecting clock polarity, setting the trigger word, selecting arm delay etc. Sixteen bit parallel data is fed back to the microprocessor via another serial link. Ten further lines provide various other interface functions.

The logic analyser operates by sampling the logic levels at its 16 data inputs and 7 control inputs in synchromism with a clock signal known as the "sample clock". The sample clock may be generated within the analyser (internal clock) or generated externally and supplied via the clock input on Pod C (external clock).

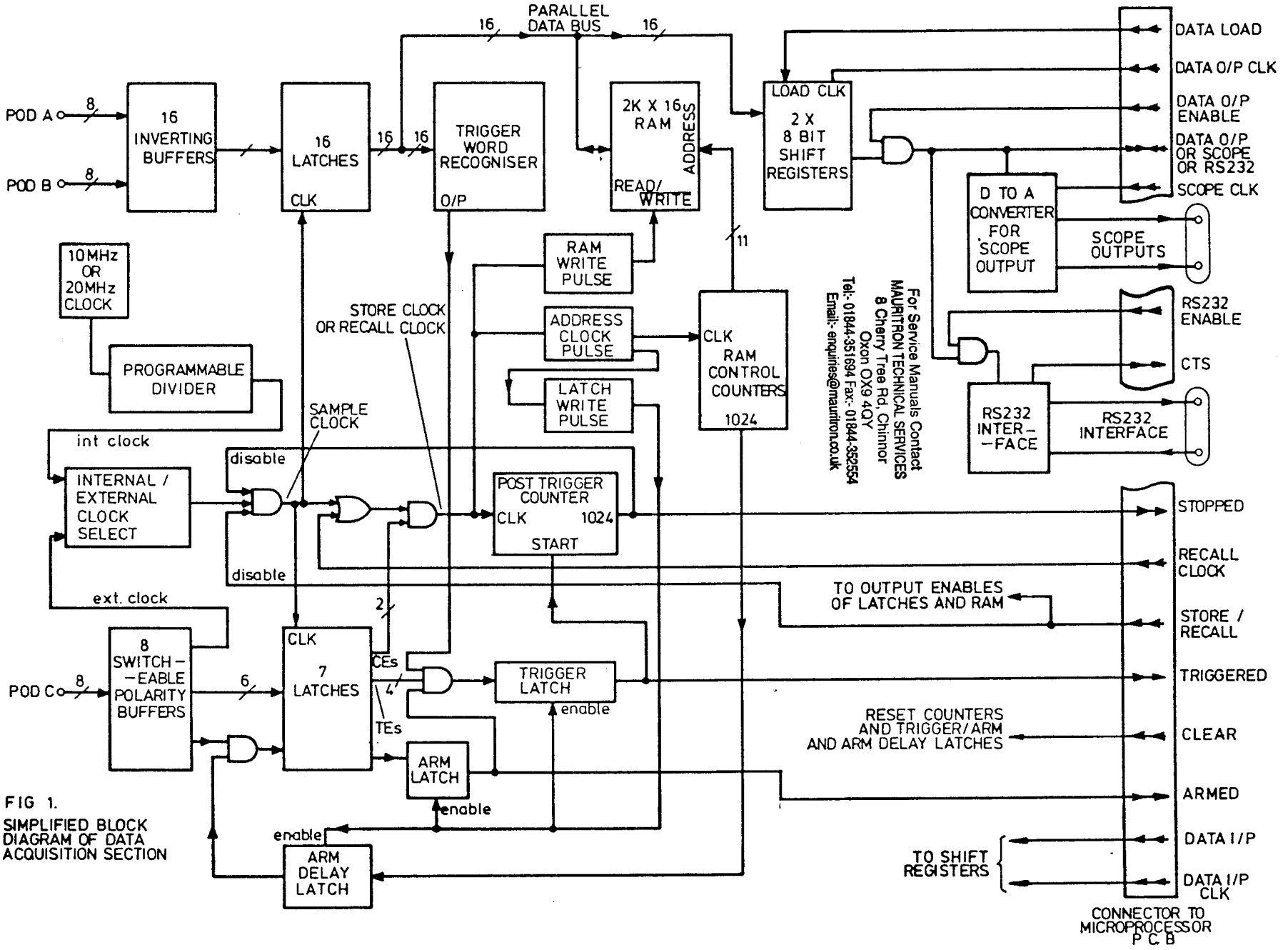


FIG 1.
SIMPLIFIED BLOCK DIAGRAM OF DATA ACQUISITION SECTION

In "Monitor" mode, the states of the latches which sample the 16 data lines are fed to the microprocessor 600 times per second via the data output shift registers. The microprocessor updates the display with this information thus providing a real-time monitor of the data inputs.

In "Single" mode, the states of the latches which sample the 16 data lines are written into a memory so that they may be stored. When the "Single" key is depressed the analyser starts to write data into the memory in synchronism with a signal called the "store clock". The store clock is generated by an AND function of the sample clock and the two clock enable inputs from Pod C. Thus data is only stored if both clock enable inputs are true.

The writing of data into the memory is continuous with new data overwriting old data each time the memory becomes full, until the acquisition is terminated by a trigger event or by the 'stop' key being depressed.

The writing of data into the memory (RAM) is controlled by the store clock which generates two pulses. The first is the Address Clock Pulse which increments an 11 bit counter which controls the RAM address. The second is the RAM Write Pulse which causes the data to be written into the RAM at the newly incremented address.

A further pulse known as the Latch Write Pulse is also generated. This enables the Trigger, Arm and Arm Delay Latches, and is delayed relative to the sample clock in order that the Trigger Word Recogniser output has time to be validated as true. The Trigger Word Recogniser compares the states of the 16 data inputs with the Trigger Word set by the user. If the Trigger Word Recogniser output, the latched Trigger Arm and the 4 Trigger enables are all true together the Trigger Latch is set and the analyser is then 'Triggered'.

The Triggered condition starts the post trigger counters which count 1024 occurrences of the store clock before stopping the acquisition. The analyser is now quiescent with the sample clock and store clock disabled and with the memory containing the 1024 data words before the Trigger event and the 1024 words after the Trigger Event.

The microprocessor defines the present RAM address as position +1023. It can now takeover control in order to read the data out of the RAM. It does this by generating a clock signal known as the Recall Clock which replaces the store clock. The microprocessor clocks the RAM forward until the required word to be read is reached. For instance, to get to cursor position 000 it clocks the RAM forward by 1024. The data at that cursor position is then read out by enabling the two 8 bit shift registers connected to the RAM data bus, and clocking out the 16 bit word as a serial data stream to the VIA on the µP PCB.

Alternatively if the acquisition is stopped by depressing the 'stop' key, the sample clock and store clock are disabled immediately by the store/recall line going to Recall. The microprocessor then defines the present RAM address as position 000.

When the microprocessor pulls the 'store/recall' control line to recall, the 23 input latches have their outputs disabled and the RAM has its outputs enabled.

Prior to a new data acquisition the microprocessor activates the "clear" control line which resets all the counters and resets the Trigger Latch, Arm Latch, and Arm Delay Latch.

Function of Interface Lines (Connector E)

Data 1/P (Pin 10):- Input.48 bit data stream which sets up the controlling shift registers.

Data 1/P CLK (Pin 7):- Input. Clock signal for the above.

Store/Recall (Pin 14):- Input high for store, low for recall. When high - enables the sample clock, enables the data and control input latches, enbales the RAM Write Pulse generator. When low - enables the RAM data outputs.

Recall Clock (Pin 8):- Input. Used to clock the RAM address counters.

Clear (Pin 12):- Input, active high. Used to clear the Post Trigger counter, the RAM address counters, the Trigger Latch, the Arm Latch and the Arm Delay Latch.

Triggered (Pin 4):- Output, active low. Informs the microprocessor that the Trigger Latch is set.

Armed (Pin 1):- Output, active low. Informs the microprocessor that the Armed Latch is set.

Stopped (Pin 2):- Output, active high. Informs the microprocessor that Post Trigger counters have reached 1024 and the acquisition has therefore stopped.

Data O/P or Scope or RS232 (Pin 16):- Input/Output. Multifunction bi-directional serial data line.

Data O/P enable (Pin 5):- Input. Enables serial data to be clocked from the shift register to the microprocessor via pin 16.

Data O/P Clock (Pin 15):- Input. Clock signal for the above.

Data Load (Pin 3):- Input, active low. Causes the data output shift register to be loaded from the 16 bit parallel data bus.

Scope Clk (Pin 9):- Input. Clocks the oscilloscope output D to A convertor to produce the staircase waveform needed for the oscilloscope display.

RS232 Enable (Pin 6):- Input. Enables serial data to be sent from the microprocessor to the RS 232 output amplifier via Pin 16.

CTS (Pin 13):- Output. Informs the microprocessor that an external RS232 device is ready to receive data (clear to send).

The Data Input Shift Registers

The 6 eight bit shift registers IC13, 18, 19, 22, 29, 33 are serially linked and are operated via the two interface lines "Data 1/P" and "Data 1/P CLK". Their 48 outputs are used as follows:- 32 control the trigger word, 7 control the polarity of the trigger enable inputs trigger arm inputs and clock enable inputs, 1 controls the external clock polarity, 5 control the internal clock frequency, 1 selects internal or external clock, 1 selects trigger arm delay and 1 selects trigger hold-off. A 48 bit data stream is clocked through the shift registers whenever a change in any of these set-up parameters is required.

The Internal Clock

A crystal controlled oscillator operating at 10MHz (LA-160A) or 20MHz (LA-160B) is formed around Q1. The signal is inverted and fed to a set 3 decade and 3 binary dividers. 2 four way selector gates enable 16 division ratios between 1 and 8,000 to be obtained.

The External Clock and Sample Clock

The External Clock input from Pod C is passed directly to a high speed gate IC32B. IC32A and IC32B combined with IC31A provide selection of external or internal clock and of external clock polarity. The output of IC31A forms the Sample Clock signal which can be disabled by a low level at the output of IC35A.

Sampling the Data and Control Inputs

The 16 Data inputs are passed through inverting buffers IC1,2,3 to the octal latches IC4,5. The 7 control inputs are passed through polarity selectors IC30,31 to the octal latch IC34. All three octal latches sample the input lines in synchronism with the sample clock.

When the store/recall line is high (store mode), the outputs of all these latches are enabled causing the sampled data inputs to appear on the 16bit parallel data bus, and the sampled control inputs to appear on the control gating circuitry IC37A, IC32C etc. When the store/recall line is low (Recall Mode) the outputs are disabled (this results in all the outputs of IC34 being pulled high by the gates to which they are connected).

The Trigger Arm Circuitry

When "Arm Delay" is set to "Off", the Arm input from Pod C is passed through IC31 to the octal latch (IC34). When "Arm Delay" is set to "On", the Arm input is gated off until the Arm Delay Latch is set by the '1024 counts' output of the RAM Address Counters. The latched state of the Arm Input is ANDed with the Latch Write Pulse to operate the Arm Latch (½IC38). The Arm Latch drives the "Armed" line true (active low).

The Arm Latch and Arm Delay Latch are both reset by a high level on the "clear" line.

The Post Trigger Counters

The Post Trigger Counters IC45,46,47 are enabled by the Triggered line going true, and are clocked by the Store Clock. When the count reaches 1024 the Stopped line is pulled true. This disables the the Sample Clock and hence the Sample Clock signal.

The Trigger Word Recognition Circuitry

The latched states of the 16 data inputs are passed through the polarity selectors IC14,15,16,17 and then through the gates IC20,21,23,24 to be Wire-ORed onto the Trigger Word Recognition output line (active low).

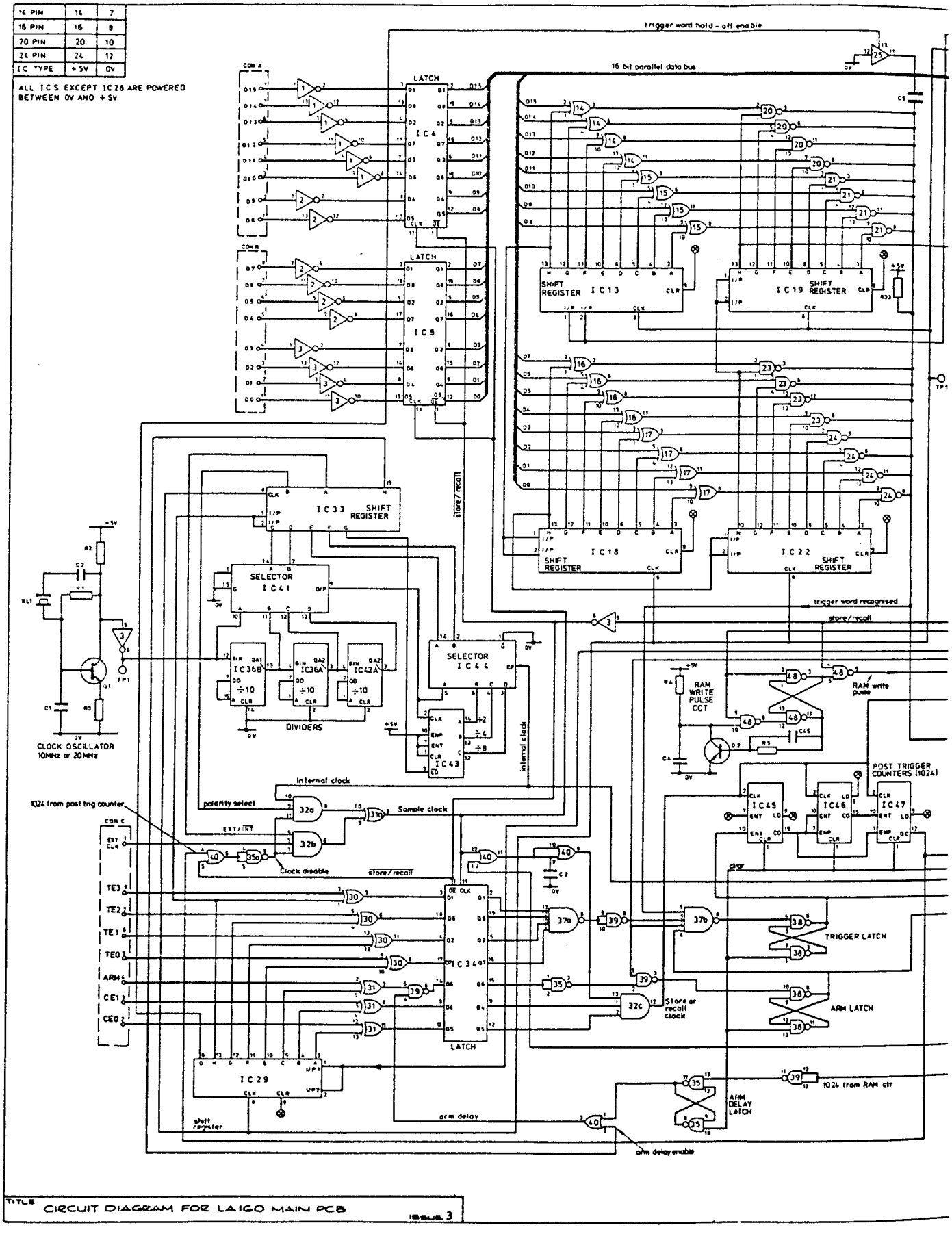
If Trigger Hold-off is selected, capacitor C5 is activated in order to delay recognition of a trigger word until it has been present for more than one sample clock cycle.

The Trigger Latch Circuitry

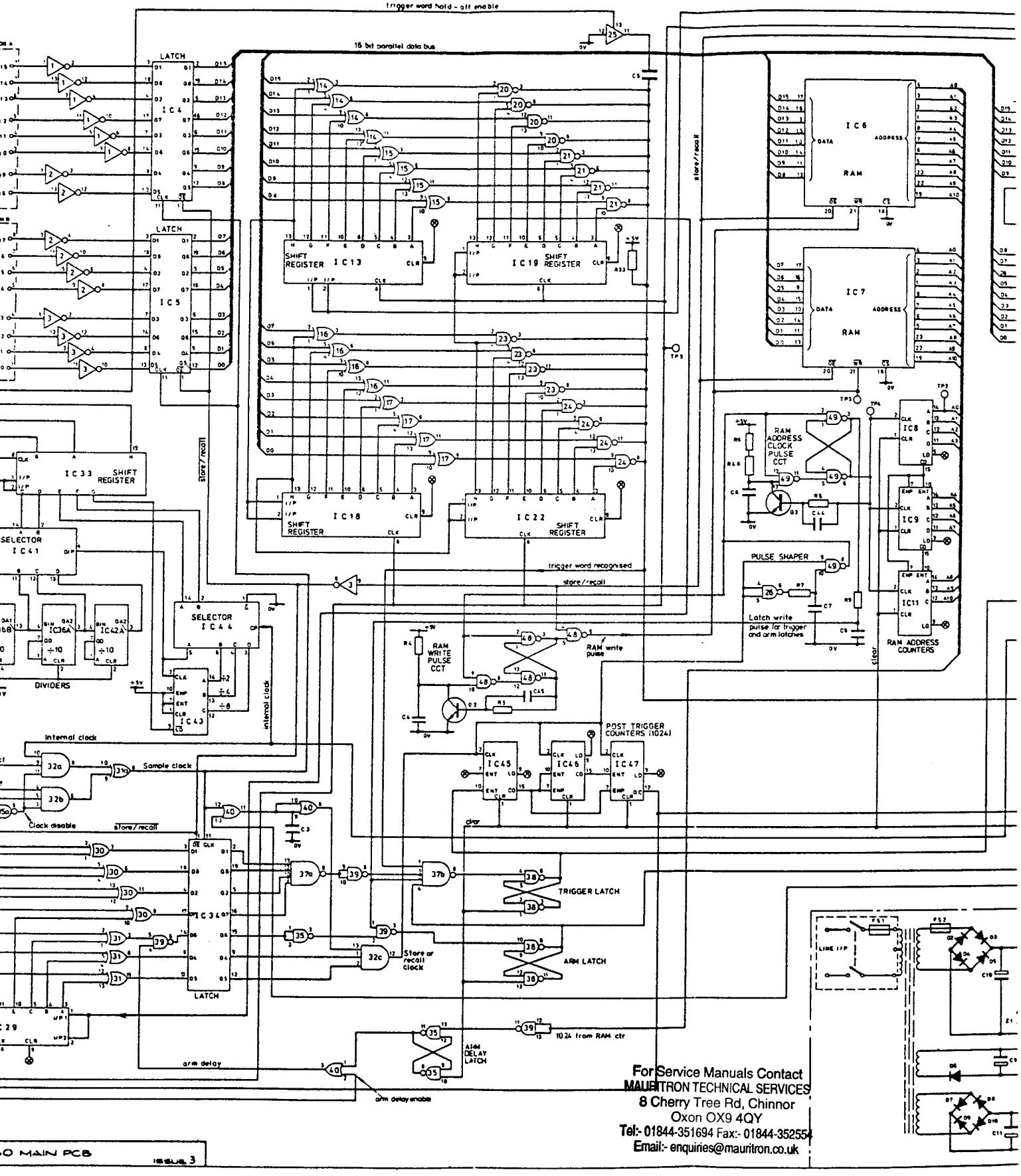
The latched state of the 4 Trigger Enable Inputs are ANDed together in IC37A. The resulting output is ANDed with 3 other signals (the Armed signal, the Trigger Word Recognition Signal and the Latch Write Pulse) to drive the Trigger Latch (½IC38)

14 PIN	14	7
16 PIN	16	8
20 PIN	20	10
24 PIN	24	12
I C TYPE	+5V	0V

ALL I C'S EXCEPT IC28 ARE POWERED BETWEEN 0V AND +5V



TITLE CIRCUIT DIAGRAM FOR LA1GO MAIN PCB ISSUE 3



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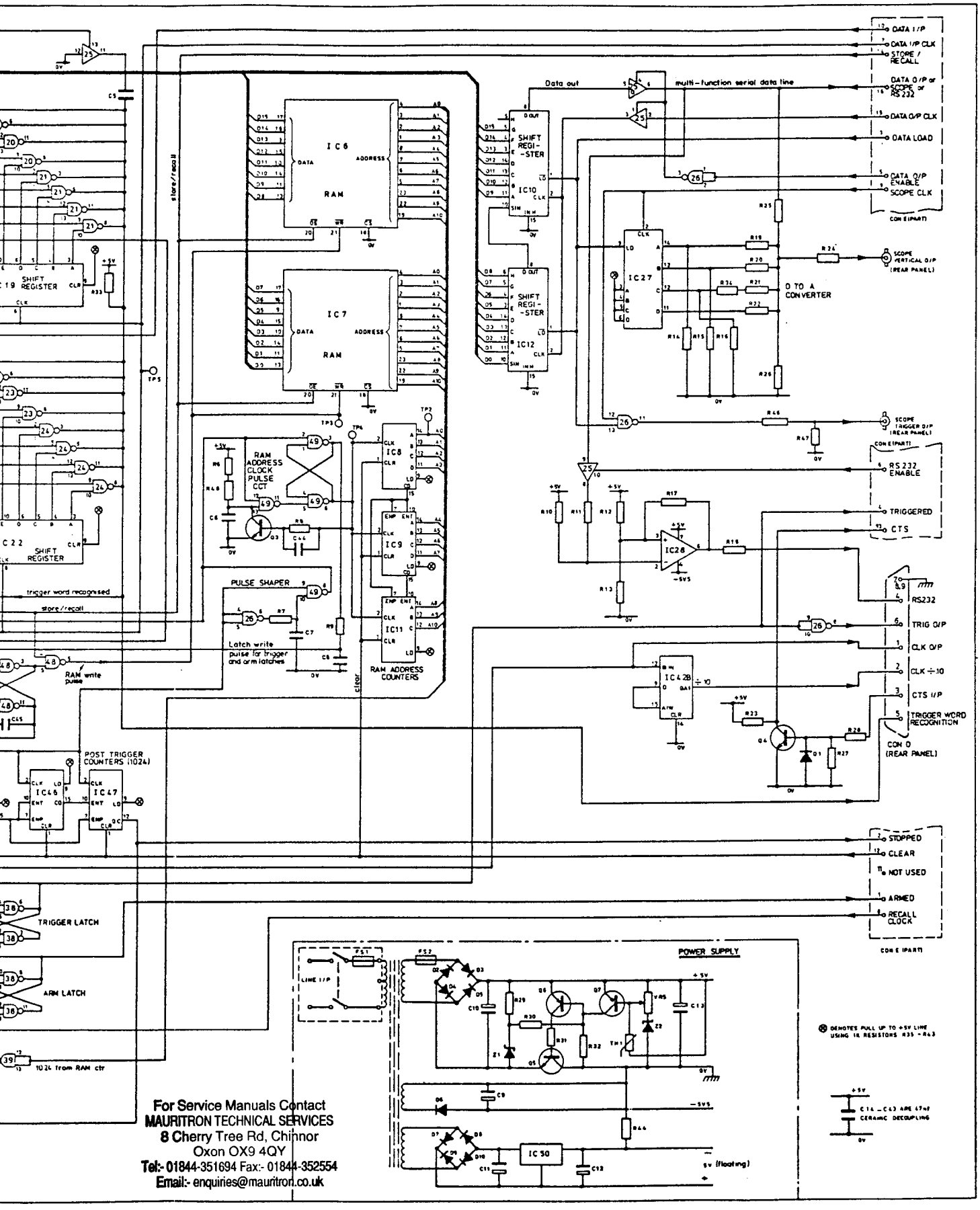

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which drives the Triggered line true (active low). The Trigger Latch is reset by a high level on the "clear" line.

Storing data in the RAM

When the microprocessor has set the "store/recall" line to store and the "clear" line false, the analyser is enabled to store data into RAM in synchronism with the store clock. If no store clock is present (because of the absence of the sample clock or because either clock qualifier is false) no data will be stored.

The positive going edge of the store clock is converted to a narrow negative going pulse by the Pulse Shaper circuit around R7 and C7. This narrow pulse is fed to two precision pulse width generators.

The first is the RAM Address Clock Pulse Circuit formed around IC49 and Q3. This generates a negative going pulse of defined width that clocks the RAM Address Counters on its trailing edge (an inverted version of this pulse is delayed by a CR network to form the write pulse for the Trigger latch and Arm latch).

The second is the RAM Write Pulse Circuit formed around IC48 and Q2. This also generates a negative going pulse but of longer width so that the data is clocked into the RAM at a defined period after the RAM address has been incremented. The RAM write pulse is gated off when the "store/recall" line is taken into recall.

Transferring Data to The Microprocessor

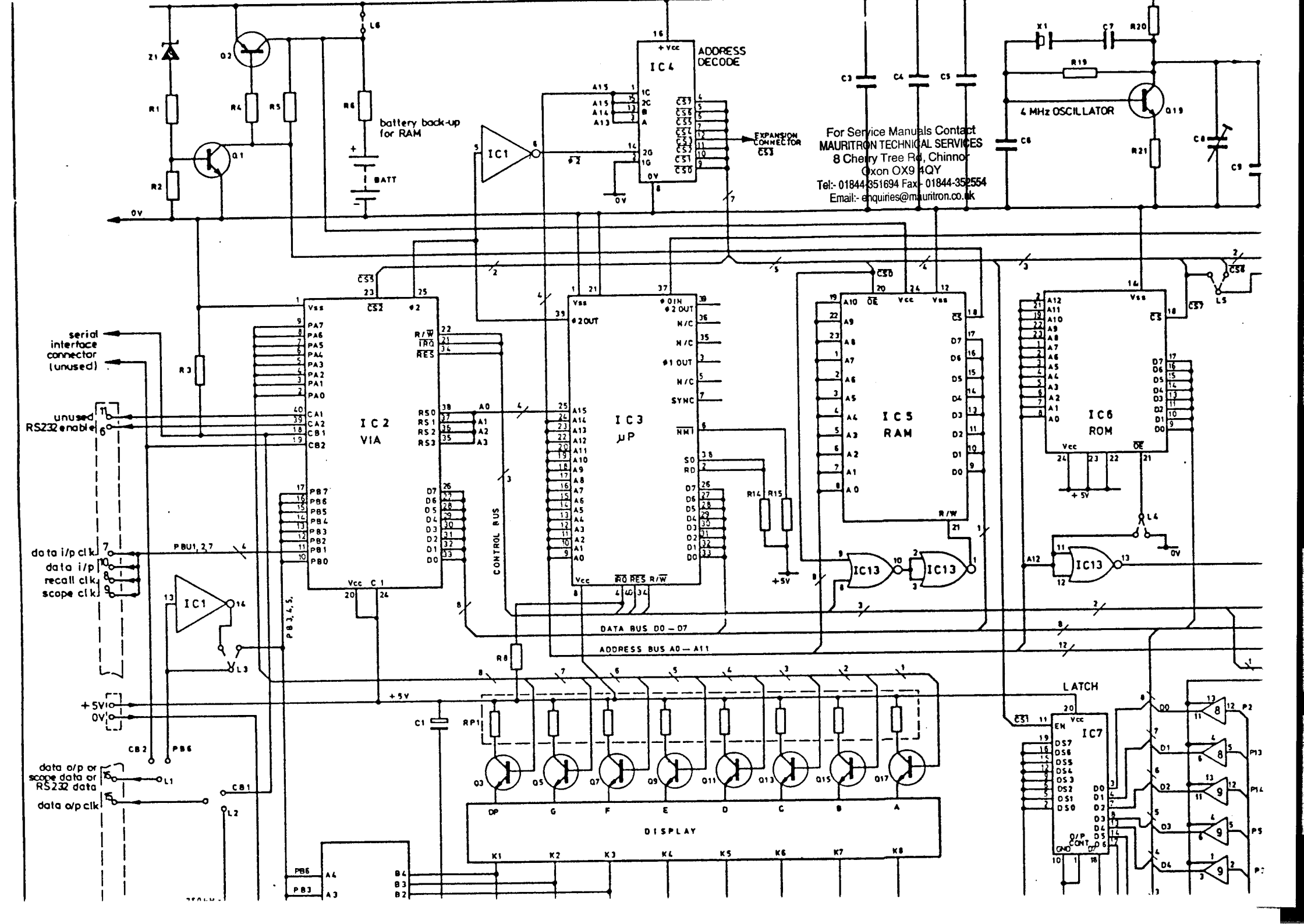
The data appearing on the 16bit parallel data bus is transferred to the microprocessor via 2 eight-bit shift registers IC10,12. Data is loaded into the shift registers by pulling the "data load" line true. With the 'data o/p enable' line true, the data is clocked out to the microprocessor via IC25A in synchronism with the "data o/p CLK" signal on the multifunction serial data line.

The Oscilloscope Display Outputs

Unless the data is being transferred from the 16 bit parallel bus to the microprocessor, or data sent from the microprocessor to the RS232 interface, the multifunction serial data line is used to carry data for the oscilloscope vertical output. This data is attenuated and superimposed onto an 8 or 16 level staircase waveform generated by IC27. IC27 is clocked by the 'scope clk' signal and reset by the 'data load' signal. These two signals are gated together and attenuated to provide the oscilloscope trigger signal.

The RS232 Output

The multifunction serial data line is also used to send data to the RS232 output amplifier IC28. This is enabled by the 'RS232 enable' line going true. IC28 drives the RS232 output line with a bipolar signal of typically ±4V. Transistor Q4 senses the state of the CTS (clear to send) input line and feeds the information to the microprocessor.


ADDRESS DECODE
IC4
battery back-up for RAM
BATT
IC1
EXPANSION CONNECTOR
4 MHz OSCILLATOR
Q19
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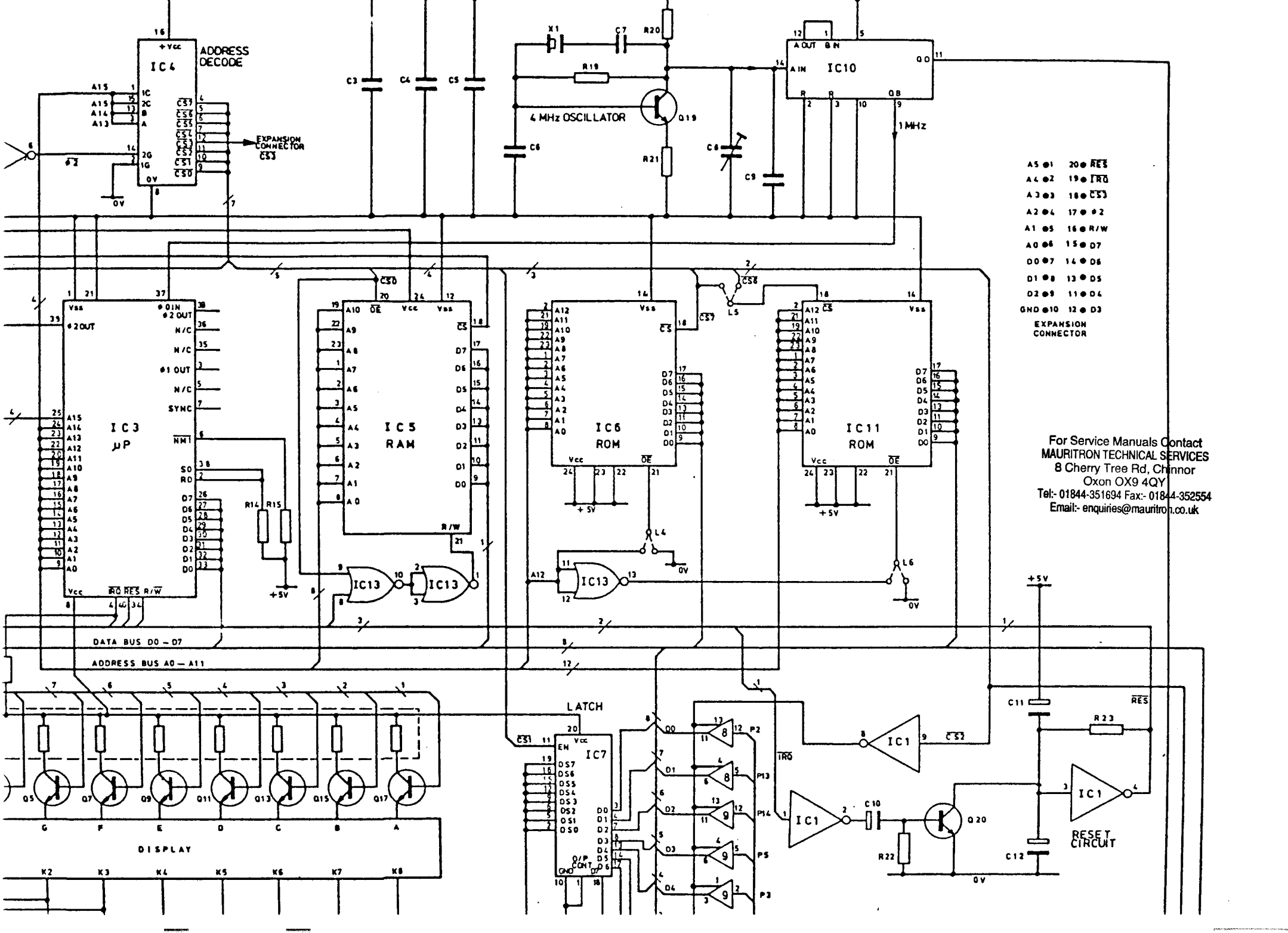
serial interface connector (unused)
unused
RS232 enable
data i/p clk
data i/p
recall clk
scope clk
+5V
0V
data o/p or scope data or RS232 data
data o/p clk
IC2
VIA
IC3
µP
IC5
RAM
IC6
ROM
CONTROL BUS
DATA BUS D0 — D7
ADDRESS BUS A0 — A11
IC13
LATCH
IC7
DISPLAY



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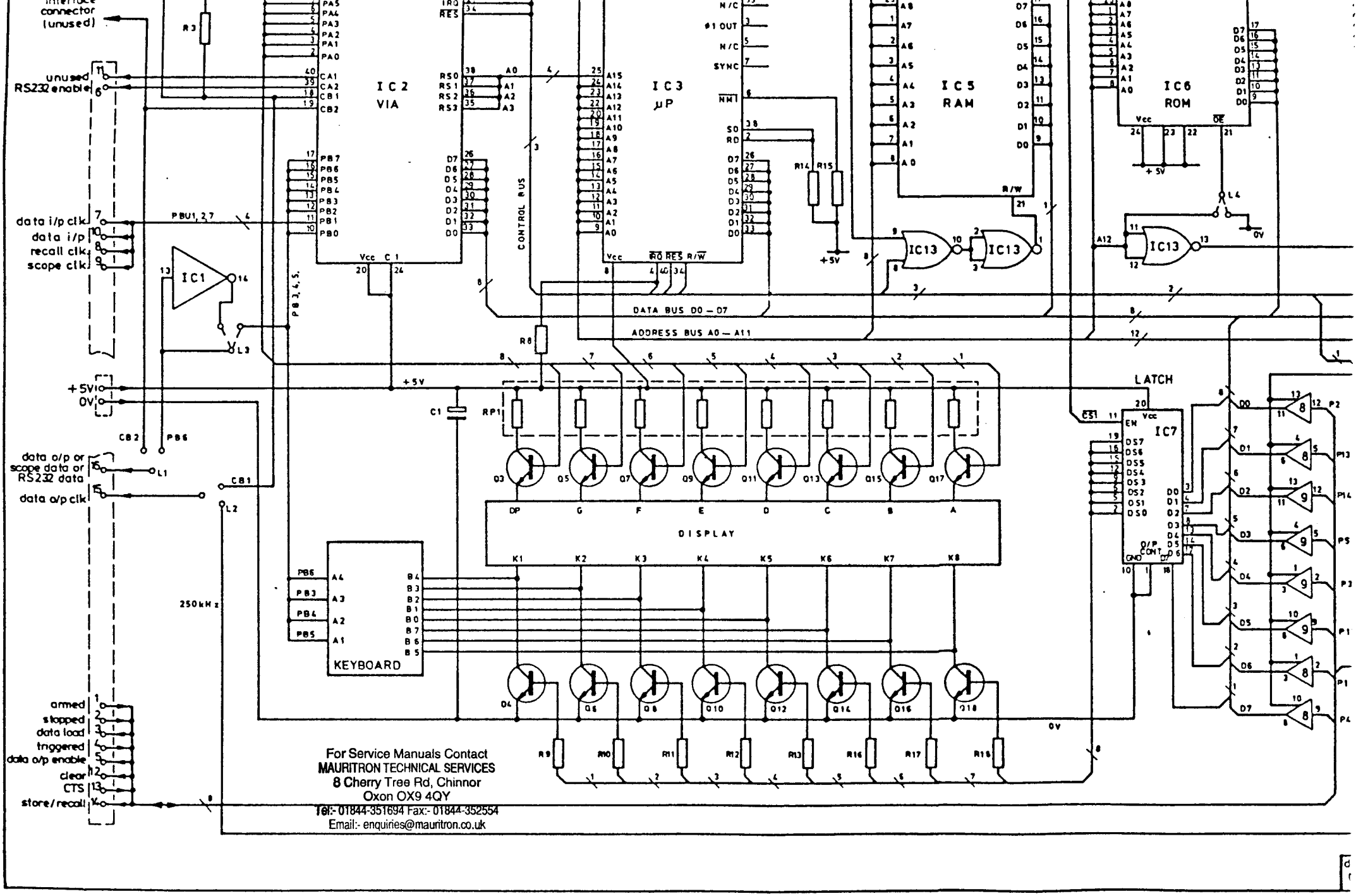
IC2 VIA
IC3 µP
IC5 RAM
IC6 ROM
IC7 LATCH
IC1
IC13
KEYBOARD
DISPLAY
CONTROL BUS
DATA BUS D0 – D7
ADDRESS BUS A0 – A11
unused
RS232 enable
data i/p clk
data i/p
recall clk
scope clk
data o/p or scope data or RS232 data
data o/p clk
armed
stopped
data load
triggered
data o/p enable
clear
CTS
store/recall
250kHz
+5V
0V
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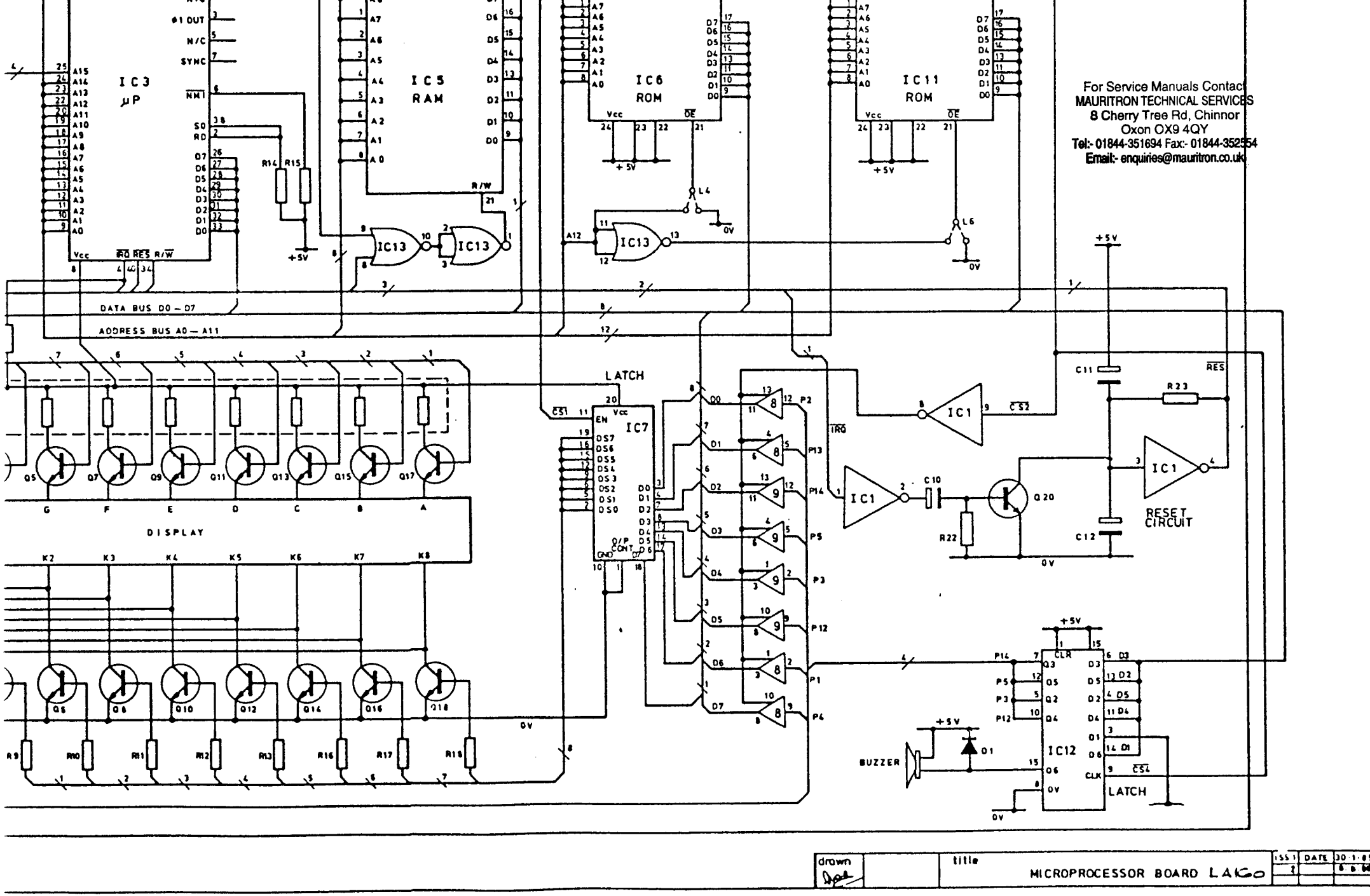
IC3
µP
IC5
RAM
IC6
ROM
IC11
ROM
IC13
IC13
IC13
IC7
IC1
IC1
IC1
IC12
DATA BUS D0 — D7
ADDRESS BUS A0 — A11
LATCH
DISPLAY
RESET
CIRCUIT
BUZZER
+5V
0V
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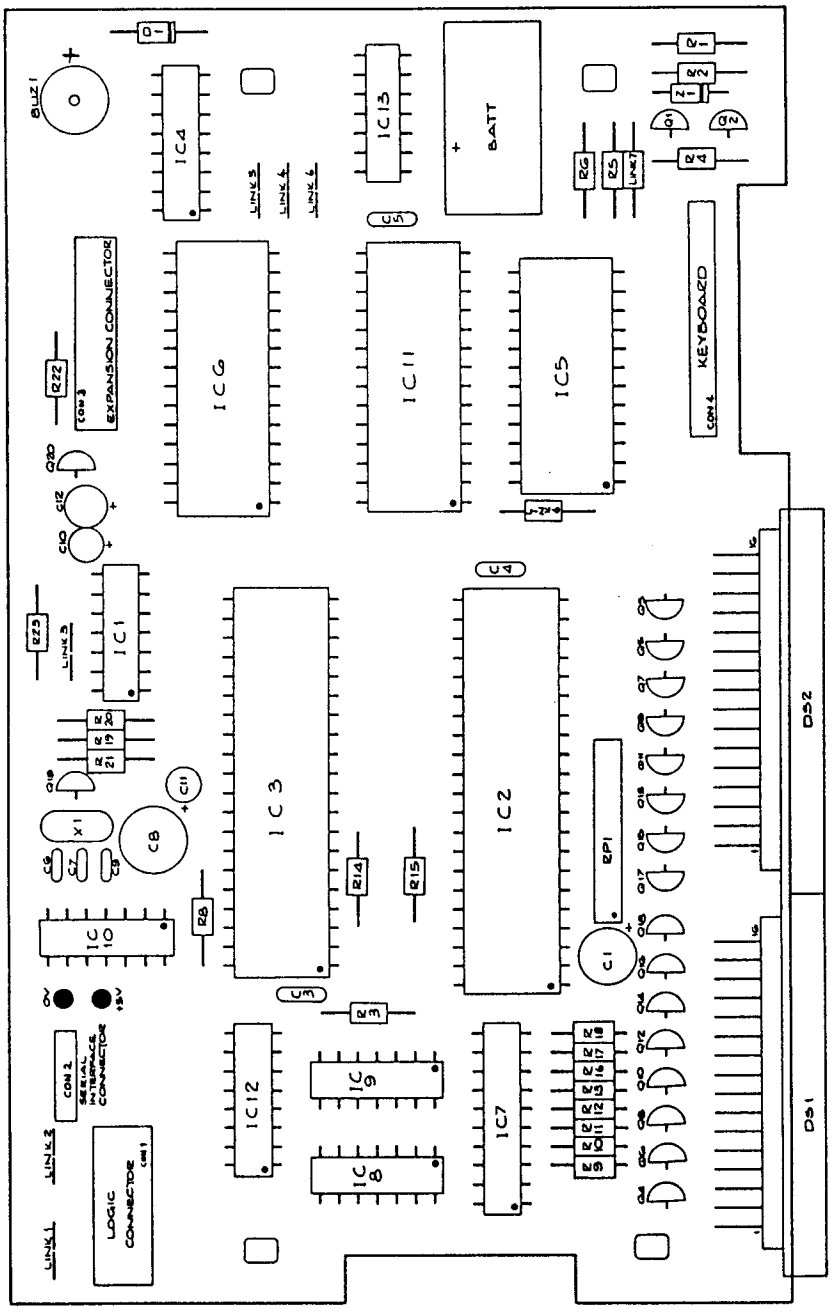

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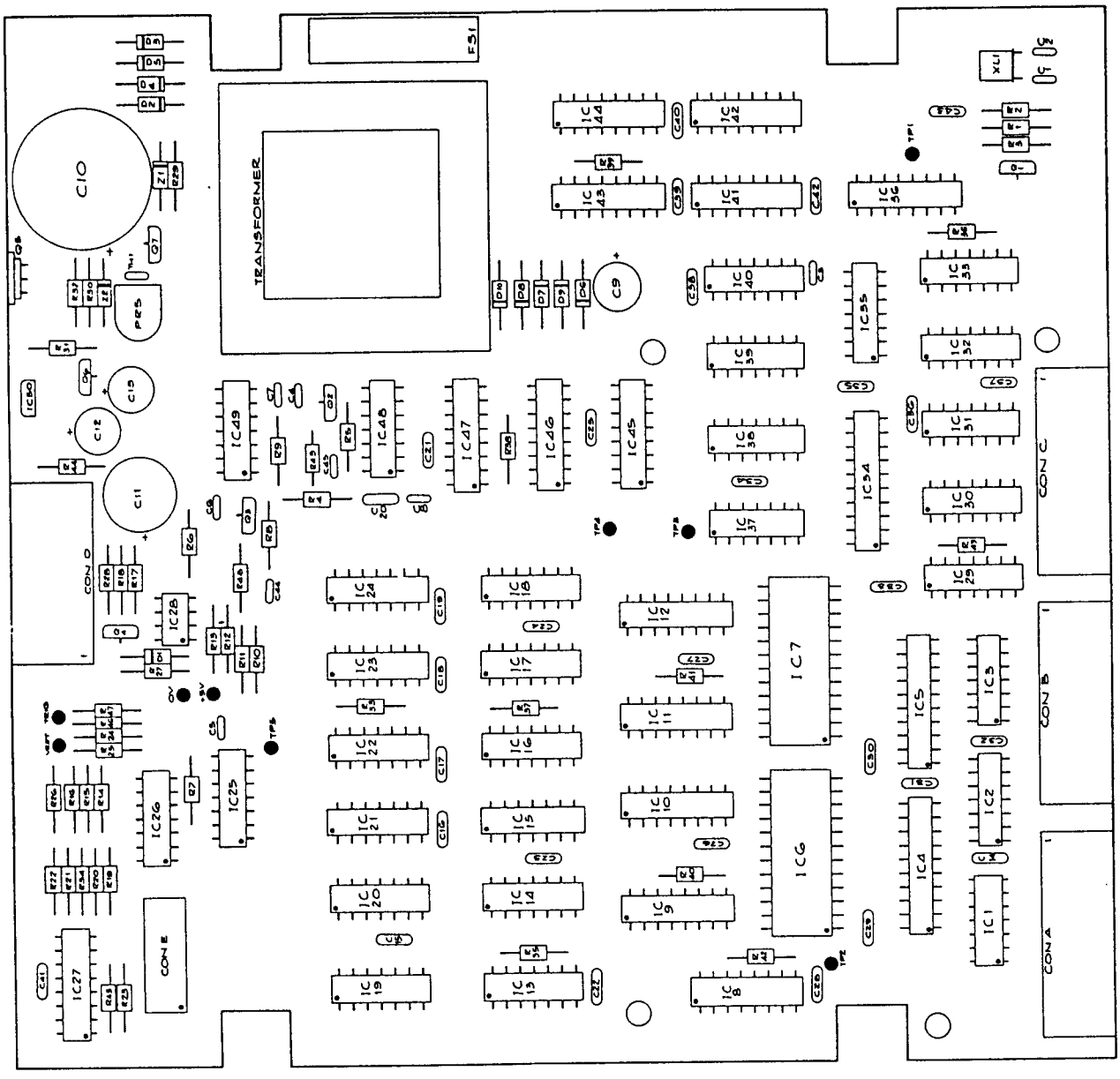

COMPONENT LAYOUT FOR
LM80 AMPLIFIER BOARD

ELECTRICAL PARTS LIST FOR MICROPROCESSOR PCB

(All resistors are ¼ watt 5% carbon film unless otherwise stated)

IC1 - 74LS14
IC2 - 6522
IC3 - 6502
IC4 - 74LS155
IC5 - 6116
IC6 - 2764(System ROM)
IC7 - 74LS374
IC8 - 74LS126
IC9 - Not Fitted
IC10 - 74LS93
IC11 - 2764(Option)
IC12 - 74LS174
IC13 - 74LS02

R1 - 220R
R2 - 220R
R3 - 4K7
R4 - 47K
R5 - 22K
R6 - 2K2
R7 - Not Fitted
R8 - 4K7
R9toR18 - 470R
R19 - 47K
R20 - 4K7
R21 - 22R
R22 - 1K8
R23 - 1K8
RN1 - 8x82R Network

C1 - 100µF/10V
C2 - Not Fitted
C3 - 47nF
C4 - 47nF
C5 - 47nF
C6 - 47nF
C7 - 47nF
C8 - Not Fitted
C9 - 47pF
C10 - 10µF/16V
C11 - 47µF/16V
C12 - Not Fitted

Q1 - ZTX239
Q2 - ZTX214
Q3toQ18 - ZTX450
Q19 - ZTX313
Q20 - ZTX239

D1 IN4148
Z1 4V3 Zener

DS1 MMN 59440
DS2 MMN 59440
BATT 2.4V, 100MAh
X1 4.000 MHz Crystal

Electrical Parts List for Main PCB

Reference	LA-160A	LA-160B (if different)	Reference	LA-160A	LA-160B (if different)
IC1	74LS14		R7	100R	
IC2	74LS14		R8	1K	
IC3	74LS14		R9	100R	
IC4	74LS374	74F374	R10	10K	
IC5	74LS374	74F374	R11	1K	
IC6	2016-100(90)	2018-45	R12	10K	
IC7	2016-100(90)	2018-45	R13	3K9	
IC8	74LS161		R14	2K7	
IC9	74LS161		R15	2K7	
IC10	74LS165		R16	4K7	
IC11	74LS161	74F161	R17	10M	
IC12	74LS165		R18	330R	
IC13	74LS164		R19	24K 1% 50ppm	
IC14	74LS86	74F86	R20	12K 1% 50ppm	
IC15	74LS86	74F86	R21	2K4 1% 50ppm	
IC16	74LS164		R22	2K4 1% 50ppm	
IC17	74LS86	74F86	R23	10K	
IC18	74LS86	74F86	R24	220R	
IC19	74LS164		R25	56K	
IC20	74LS03	74S38	R26	910R	
IC21	74LS03	74S38	R27	4K7	
IC22	74LS164		R28	4K7	
IC23	74LS03	74S38	R29	470R	
IC24	74LS03	74S38	R30	33K	
IC25	74LS126		R31	100R	
IC26	74LS00		R32	4K7	
IC27	74LS161		R33	470R	100R
IC28	LF351		R34	2K4 1% 50ppm	
IC29	74LS164		R35-R45	1K	
IC30	74LS86		R46	10K	
IC31	74F86		R47	220R	
IC32	74F11		R48	470R	680R
IC33	74LS164		R49	470R	680R
IC34	74LS374	74F374	PR3	500R	
IC35	74LS00	74F00			
IC36	74LS390				
IC37	74LS20	74F20	C1	47pf	
IC38	74LS00	74F00	C2	47pf	
IC39	74LS00	74F00	C3	100pf	33pf
IC40	74LS32	74F32	C4	100pf	47pf
IC41	74LS153		C5	150pf	680pf
IC42	74LS390		C6	100pf	47pf
IC43	74LS161		C7	68pf	NOT FITTED
IC44	74LS153		C8	100pf	47pf
IC45	74LS161		C9	220µF	
IC46	74LS161		C10	10,000µF	
IC47	74LS161	74F161	C11	470µF	
IC48	74LS00	74F00	C12	470µF	
IC49	74LS00	74F00	C13	470µF	
IC50	79L05		C14-C43	47nf	
R1	47K		X1	10MHz	20MHz
R2	4K7	6K8	FS2	2A Fast Blow	
R3	22R				
R4	100R		Z1	6V2 Zener	
R5	1K		Z2	3V9 Zener	
R6	100R				

Reference	LA-160A	LA-160B (if different)	Reference	LA-160A	LA-160B (if different)
Q1	ZTX 313				
Q2	ZTX 313				
Q3	ZTX 313				
Q4	ZTX 239				
Q5	TIP31A				
Q6	ZTX214				
Q7	ZTX214				
D1	1N4148				
D2-D10	1N4003				

Addendum

Early models of the LA-160 differ as follows:-

R24 is 1KΩ
R46 is not mounted on the PCB
R47,R48 and R49 are replaced by preset potentiometers.