User's Guide

HP Debug User Interface

for H8/3003/32/42 Series

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Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

Instruction manual symbol: The product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

Alternating current.

Direct current.

On (Supply).

Off (Supply).

Frame (or chassis) terminal. A connection to the frame (chassis) of the equipment which normally include all exposed metal structures.

Warning

This Warning sign denotes a hazard. It calls your attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution

This Caution sign denotes a hazard. It calls your attention to a procedure, practice, condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

Note denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

In This Book

The HP B3750A Debug User Interface, which is used with the HP 64784A Emulator, is a high-level language debugger for the Hitachi H8/3003/32/42 Series.

This book describes processor-specific functions and usage of the HP B3750A Debug User Interface.

For common functions and usage of the HP Debug User Interface, refer to the *HP Debug User Interface User's Guide*.

For installation of the HP Debug User Interface, refer to the *HP Debug User Interface Installation Guide*.

For installation of the HP 64784A Emulator, refer to the *HP 64787 H8/3003 Emulator Terminal Interface User's Guide*.

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Connecting the Target System

Connecting the Target System

This chapter shows you how to connect the emulator to your target system.

Overview

To connect the HP 64784A Emulator and the target system, the following two methods are provided.

- Connecting with the **QFP adapter**.
- Connecting with the **PGA adapter** and the **QFP cable**.

In both methods, the **QFP socket/adapter** (attached to the QFP adapter and QFP cable products) is also used.

Caution

To prevent the emulator and the target system from being damaged, be sure to follow the cautions below when handling them.

- **To prevent damage by static discharge, use the emulator in a place resistant to static electricity.**
- **Be sure to turn off the emulator and the target system before connecting them.**
- **Be sure that orientation of each connector is right.**
- **Check that the ground line of the emulator and that of the target system are properly connected.**
- **When turning the system on, switch on the target system first and then the emulator.**
- **When turning the system off, switch off the emulator first then the target system.**

The **QFP adapter** is a board assembly to adapt ribbon cables of the emulator to the QFP socket/adapter on the target system. The QFP adapter can be used only for target systems operated with 5V power supply. The emulator can emulate the following processors with the QFP adapter.

Table 1-1. Supported Processors of Each QFP Adapter

Processor	Package (Pitch)	QFP Adapter
H8/3002	QFP/TQFP-100 (.5 mm)	**HP 64784D**
H8/3003	QFP-112 (.65 mm)	**HP 64784C**
H8/3040/41/42	QFP/TQFP-100 (.5 mm)	**HP 64784D**

The **PGA adapter** is a board assembly to adapt ribbon cables of the emulator to the QFP cable. The PGA adapter can be used for all emulation processors. There are two types of the PGA adapters. One is **HP 64784E** for target systems with 5V power supply. Another is **HP 64797B** for target systems with low voltage power supply.

The **QFP cable** is a cable assembly to connect the PGA adapter to the QFP socket/adapter on the target system. Use one of the following QFP cables.

Table 1-2. Supported Processors of Each QFP Cable

Processor	Package (Pitch)	QFP Cable
H8/3001	TQFP-80 (.5 mm)	**HP 64784J**
H8/3002	QFP/TQFP-100 (.5 mm)	**HP 64784G**
H8/3003	QFP-112 (.65 mm)	**HP 64784F**
H8/3004/05	QFP-80 (.65 mm)	**HP 64784K**
H8/3030/31/32	QFP-80 (.65 mm)	**HP 64784H**
H8/3040/41/42	QFP/TQFP-100 (.5 mm)	**HP 64784G**

The **QFP socket/adapter** is a part to adapt the QFP adapter or the QFP cable to the target system. You must solder this part to your target system. The QFP socket/adapter can be used as a "socket" to mount a real processor. The following QFP socket/adapters are provided.

Table 1-3. QFP Socket/Adapters

Processor	Package (Pitch)	QFP Socket/Adapter
H8/3001	TQFP-80 (.5 mm)	**HP 64784-61614**
H8/3002	QFP/TQFP-100 (.5 mm)	**HP 64784-61612**
H8/3003	QFP-112 (.65 mm)	**HP 64784-61611**
H8/3004/05	QFP-80 (.65 mm)	**HP 64784-61613**
H8/3030/31/32	QFP-80 (.65 mm)	**HP 64784-61613**
H8/3040/41/42	QFP/TQFP-100 (.5 mm)	**HP 64784-61612**

Connecting with the QFP Adapter

To connect the target system with the QFP adapter,

1. Verify both the emulator and the target system are turned off.
2. Solder the QFP socket/adapter to the target system.
3. Attach ribbon cables of the emulator to the QFP adapter.
4. Align pin #1 of the QFP adapter and the QFP socket/adapter, then fix them with four screws.
5. Turn on the target system and then the emulator.

Caution

Do not apply excessive force to the QFP adapter. It may cause damage to the QFP socket/adapter and the target system.

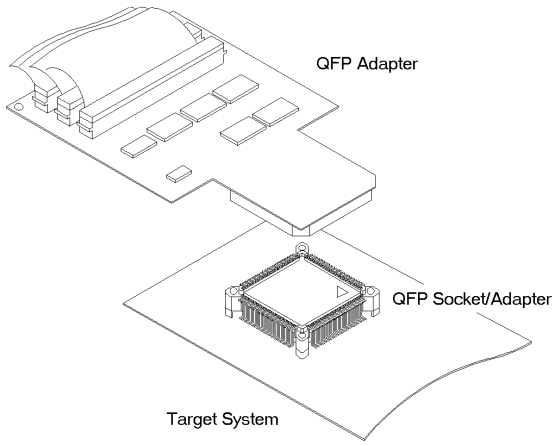

Figure 1-1. Connecting with QFP Adapter

Connecting with the PGA Adapter and the QFP Cable

To connect the target system with the PGA adapter and the QFP cable,

1 Verify both the emulator and the target system are turned off.

2 Solder the QFP socket/adapter to the target system.

3 Attach ribbon cables of the emulator to the PGA adapter.

4 Attach the QFP cable to the PGA adapter.

- When emulating the H8/3001/04/05 operated in mode 3 or 4, attach the **pin exchange board HP 64784-66509** between the QFP cable and the PGA adapter.

5 Align pin #1 of the QFP cable and the QFP socket/adapter, then fix them with four screws.

6 Turn on the target system and then the emulator.

Caution

When emulating the H8/3001/04/05 operated in mode 3 or 4, you must attach the **pin exchange board HP 64784-66509** between the QFP cable and the PGA adapter.

Without this board, it may cause damage to the emulator and the target system.

And, never attach the pin exchange board when emulating other processors or other operation modes. It may also cause damage to them.

Caution

Do not apply excessive force to the QFP cable. It may cause damage to the QFP cable, the QFP socket/adapter and the target system.

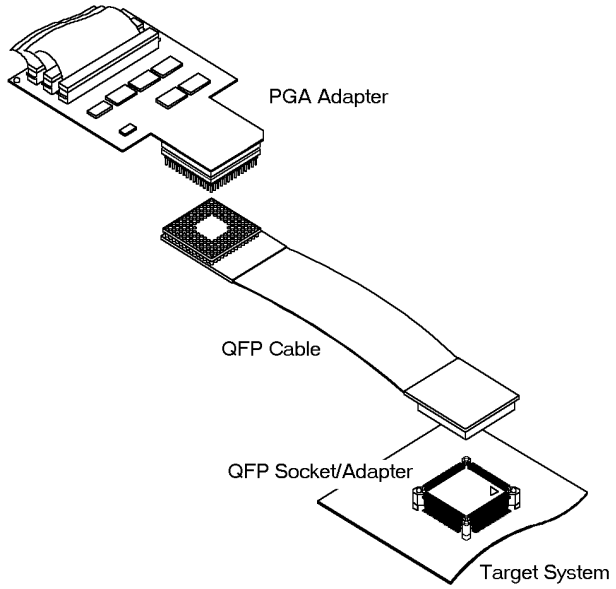

Figure 1-2. Connecting with PGA Adapter and QFP Cable

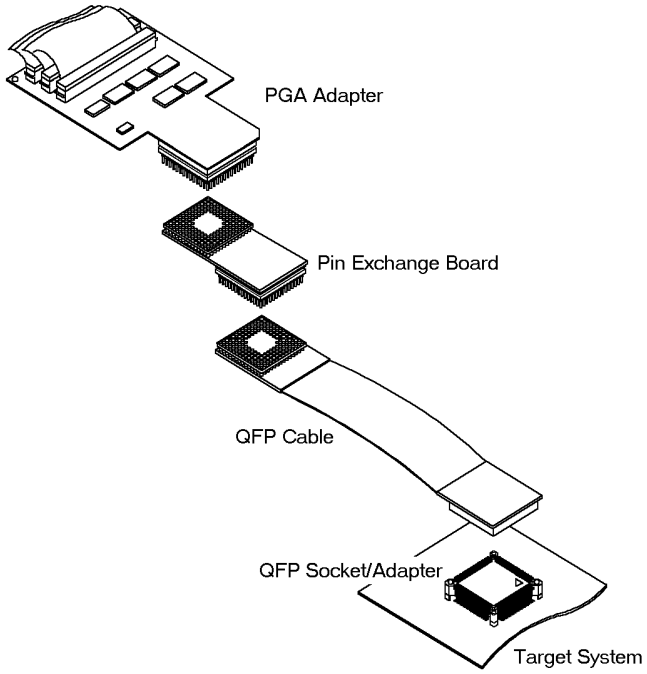

Figure 1-3. Using Pin Exchange Board

Note

2

Configuring the Emulator

Configuring the Emulator

This chapter shows you how to set the following items to configure the emulator.

- Hardware Options
- Memory Map

Hardware Options

The emulator can be configured to suit developments of various target systems and user programs by setting the hardware options.
The HP 64784A Emulator has the following hardware options.

- **Clock Source**
- **Restrict to Real Time**
- **Respond to Target System BREQ**
- **Respond to Target System NMI**
- **Respond to Target System Reset**
- **Drive Background Cycles to Target**
- **Drive Reset to Target System**
- **Break on Write to ROM**
- **Language Tool Type**
- **Processor Type**
- **Processor Operation Mode**
- **Stack Pointer Reset Value**

Setting the Hardware Options

To set the hardware options,

1. Choose **Settings→Configuration→Hardware...** (Alt, S, C, H) from the control menu of the Debug window.
2. Set the hardware options using the Emulator Configuration dialog box.
3. Click the OK button.

Note In the Emulator Configuration dialog box, the option button checked means **Yes**, the option button not checked means **No**.

Note Setting the hardware options will drive the emulator into a reset state.

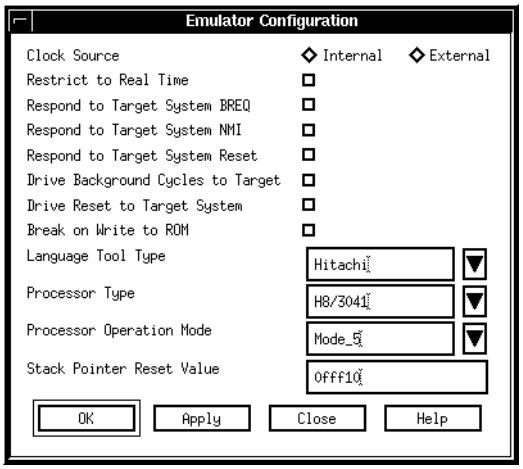

Figure 2-1. Emulator Configuration Dialog Box

Clock Source

This option allows you to select whether the processor's clock is sourced by the emulator's internal clock or by the target system.

Internal The processor's clock is sourced by the internal clock.

Select this setting when the emulator is not connected to the target system.

The internal clock speed is **16 MHz**. When using the low voltage PGA adapter **HP 64797B**, the speed is **8 MHz**.

When emulating the H8/3003 clock-halving version, the clock speed is fixed to **8 MHz** (system clock).

External The processor's clock is sourced by the target system.

Select this setting when the emulator is connected to the target system.

Usable clock speed is **500 kHz to 16 MHz**. When using the low voltage PGA adapter **HP 64797B**, the speed is **500 kHz to 10 MHz**.

When emulating the H8/3003 clock-halving version, the speed is **1 MHz to 24 MHz** (system clock: 500 kHz to 12 MHz) without the **HP 64797B**, or **1 MHz to 20 MHz (system clock: 500 kHz to 10 MHz) with the HP 64797B**.

Restrict to Real Time

The emulator has to break to the monitor to access processor registers and target memory. While running the user program, this break is done implicitly and called "temporary break".

With temporary breaks, the user program cannot be executed in real time. This may cause unexpected result if your target system circuitry is dependent on constant execution time of the program code.

This option allows you to select whether the emulator is restricted to real-time runs.

Yes The emulator is restricted to real-time runs.

While running the user program, all commands that cause a temporary break are refused. The user program is guaranteed to be executed in real time.

Commands to display/modify registers and target memory are not allowed when the emulator is running the user program. However, you can still execute the run control commands such as reset, break, run, step.

No The emulator is not restricted to real-time runs.

All commands, regardless of whether or not they require a break to the monitor, are accepted by the emulator.

Respond to Target System BREQ

This option allows you to select whether the emulator responds to the $\overline{\text{BREQ}}$ signal from the target system.

Yes The emulator responds to the $\overline{\text{BREQ}}$ signal from the target system.

While running the user program or the monitor, the emulator releases the bus if the $\overline{\text{BREQ}}$ signal is asserted.

No The emulator always ignores the $\overline{\text{BREQ}}$ signal from the target system.

If the $\overline{\text{BREQ}}$ pin is configured to other functions such as an I/O port, this option has no effect on those functions.

Note The target system cannot perform direct memory access to the emulation memory.

Note The emulator cannot break to the monitor during a bus-released state.

Respond to Target System NMI

This option allows you to select whether the emulator responds to the NMI signal from the target system.

Yes The emulator responds to the NMI signal from the target system.

While running the user program, the emulator starts an NMI exception process if the NMI signal is asserted. While running the monitor, the emulator suspends an NMI request; the request will be serviced upon return to the user program.

No The emulator always ignores the NMI signal from the target system.

Note

Regardless of this option setting, while running the monitor, the emulator responds to no interrupts including NMI.

The emulator suspends interrupt requests while running the monitor; the requests will be serviced upon return to the user program.

Respond to Target System Reset

This option allows you to select whether the emulator responds to the $\overline{\text{RES}}$ and STBY signals from the target system.

Yes The emulator responds to the $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ signals from the target system.

While running the user program, the emulator enters a reset state if the $\overline{\text{RES}}$ or $\overline{\text{STBY}}$ signal is asserted. While running the monitor, the $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ signals are ignored.

No The emulator always ignores the $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ signals.

Note The emulator does not support hardware standby mode.
The $\overline{\text{STBY}}$ signal from the target system is connected to the reset signal in the emulator. So, if the $\overline{\text{STBY}}$ input is asserted, the emulator enters a reset state instead of hardware standby mode.

Note Regardless of this option setting, while running the monitor, the $\overline{\text{RES}}$ and STBY signals are ignored.

Note The emulator cannot break to the monitor during a reset state by the target system.

Drive Background Cycles to Target

This option allows you to select whether the emulator drives memory cycles in the monitor (background cycles) to the target system.

Yes The emulator drives the background cycles to the target system.

While running the monitor, the emulator drives the address bus, CS0, AS and RD signals to the target system, and can respond to the WAIT signal from the target system. The CS7 to CS1, HWR and LWR signals go high. The data bus goes high-impedance.

No The emulator does not drive the background cycles to the target system.

While running the monitor, the emulator drives only the address bus and CS0 signal. The CS7 to CS1, AS, RD, HWR and LWR signals go high. The data bus goes high-impedance. The WAIT signal from the target system is ignored.

However, memory cycles to access target memory are still driven to the target system.

If the address bus, data bus, CS7 to CS0, AS, RD, HWR and LWR pins are configured to other functions such as an I/O port, this option has no effect on those functions.

Drive Reset to Target System

This option allows you to select whether the emulator drives the $\overline{\text{RESO}}$ signal to the target system during a reset state caused by the watchdog timer (WDT).

Yes The emulator drives the $\overline{\text{RESO}}$ signal to the target system.

The $\overline{\text{RESO}}$ signal goes low during a reset state by the watchdog timer.

No The emulator does not drive the $\overline{\text{RESO}}$ signal to the target system.

Note

The emulator ignores the reset output enable bit (RSTOE) of the reset control/status register (RSTCSR), and uses this option setting instead.

Break on Write to ROM

This option allows you to select whether the emulator breaks to the monitor when the user program writes to a memory area mapped as ROM.

Yes The emulator breaks to the monitor when the user program writes to a memory area mapped as ROM.

No The emulator does not break to the monitor upon a write to ROM.

Language Tool Type

This option allows you to specify language tools which is used to create the user program.

Hitachi The user program created with the Hitachi language tools can be debugged.

IAR The user program created with the IAR language tools can be debugged.

Note

When using the IAR language tools, the following commands cannot be used.

- Display a back trace.
- Return to a caller routine.

Processor Type

This option allows you to select the emulation processor.

H8/3001	The emulator emulates the H8/3001.
H8/3002	The emulator emulates the H8/3002.
H8/3003T	The emulator emulates the H8/3003 (1:1 clock version).
H8/3003	The emulator emulates the H8/3003 (clock-halving version).
H8/3004	The emulator emulates the H8/3004.
H8/3005	The emulator emulates the H8/3005.
H8/3030	The emulator emulates the H8/3030.
H8/3031	The emulator emulates the H8/3031.
H8/3032	The emulator emulates the H8/3032.
H8/3040	The emulator emulates the H8/3040.
H8/3041	The emulator emulates the H8/3041.
H8/3042	The emulator emulates the H8/3042.

Note

When emulating the H8/3005, the memory area 0FEF10H to 0FF00FH (mode 1) and 0FFEF10H to 0FFF00FH (mode 3) cannot be used as the on-chip RAM.

If you want to use this area, map this area as emulation RAM. However, this area works as 8-bit external address space accessed in three clock cycles.

Processor Operation Mode

This option allows you to select the processor operation mode.

Mode_1 The emulator operates in mode 1.

Mode_2 The emulator operates in mode 2.

Mode_3 The emulator operates in mode 3.

Mode_4 The emulator operates in mode 4.

Mode_5 The emulator operates in mode 5.

Mode_6 The emulator operates in mode 6.

Mode_7 The emulator operates in mode 7.

Note The emulator ignores the MD2 to MD0 inputs, and uses this option setting instead.

Stack Pointer Reset Value

This option allows you to specify the value that the stack pointer (SP, ER7) is set to when the monitor is entered after emulation reset.

The stack pointer must be set to a 32-bit even address but not to the on-chip peripheral module register area. Normally, specify the default value of the user program.

Note If the stack pointer is set to an odd value or points to the on-chip peripheral module register area, the emulator cannot perform run control functions such as run and step.

Memory Map

The HP 64784A Emulator memory mapper allows you to define up to 16 different map terms. The minimum size of each map term is 512 bytes. You can specify one of the following memory types to each map term.

eram Emulation RAM.

This area operates as read/write emulation memory.

erom Emulation ROM.

This area operates as read only emulation memory. When the user program writes to this area, the data is not written. And, you can configure the emulator to break to the monitor at an attempted write to this area.

tram Target RAM.

This area operates as read/write target memory.

trom Target ROM.

This area operates as read only target memory. You can configure the emulator to break to the monitor when the user program writes to this area.

grd Guarded memory.

This area operates as an access-prohibited area. When the user program attempts to access to this area, the emulator breaks to the monitor. Access with emulator commands are also prohibited.

The memory type of other area (area of no map terms defined) can be defaulted to **tram**, **trom** or **grd**.

Note The target system cannot perform direct memory access to the emulation memory.

Setting the Memory Map

To set the memory map,

1. Choose **Settings→Configuration→Memory Map...** (Alt, S, C, M) from the control menu of the Debug window.

2. Set the memory map using the Memory Map dialog box.

   - **Setting a map term**

     1. Specify an area to the Address Range text box.

        Format: <*start address*>..<*end address*>

     2. Select a memory type in the Attribute option box.
     3. Click the Apply button.

   - **Deleting a map term**

     1. Select a map term in the Map Term list box.
     2. Click the Delete button.

   - **Deleting all map terms**

     1. Click the Del.All button.

   - **Setting a memory type of other area**

     1. Select a memory type in the Other option box.

3. Click the Close button.

Note Setting the memory map will drive the emulator into a reset state.

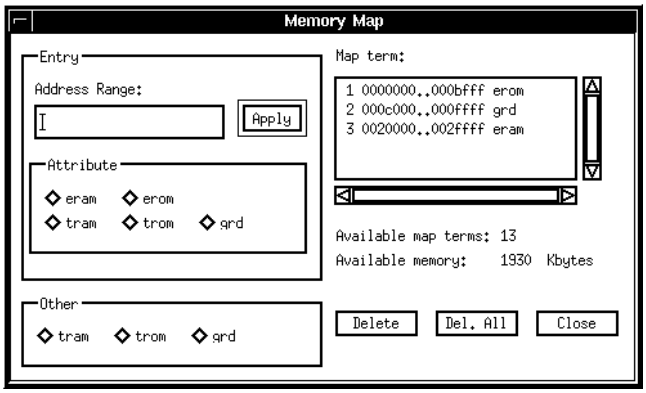

Figure 2-2. Memory Map Dialog Box

On-Chip ROM

When using the on-chip ROM, map the on-chip ROM area as emulation ROM.

On-Chip RAM

The on-chip RAM is mapped automatically as emulation RAM regardless of the memory map settings. You don't have to map this area. However, this mapping is not displayed as a map term.

If you define a map term of this area, the map term is handled as that for external address space overlapped with the on-chip RAM.

Note

When emulating the H8/3005, the memory area 0FEF10H to 0FF00FH (mode 1) and 0FFEF10H to 0FFF00FH (mode 3) cannot be used as the on-chip RAM.

If you want to use this area, map this area as emulation RAM. However, this area works as 8-bit external address space accessed in three clock cycles.

Note The external address space overlapped with the on-chip RAM can be accessed by the user program, but cannot be accessed by emulator commands.

Note Do not map the on-chip RAM area as guarded memory. Access with emulator commands will be prohibited.

On-Chip Peripheral Module Registers

The on-chip peripheral module registers work as the on-chip peripheral module registers regardless of the memory map settings. You don't have to map this area.

Note Do not map the on-chip peripheral module register area as guarded memory. Access with emulator commands will be prohibited.

Configuration Commands

You can also configure the emulator by configuration files or command files. The HP B3750A Debug User Interface has the following configuration commands. Case is not significant in both commands and parameters.

Note

The hardware option commands and the memory map commands must be placed between its own start and end commands.

Table 2-1. Configuration Commands

Command	Parameter 1	Parameter 2	Operation
config	start		Start of Hardware Option Commands
config	clk	internal | external	Clock Source
config	rrt	enable | disable	Restrict to Real Time
config	ba	enable | disable	Respond to Target System BREQ
config	nmi	enable | disable	Respond to Target System NMI
config	trst	enable | disable	Respond to Target System Reset
config	dbc	enable | disable	Drive Background Cycles to Target
config	drst	enable | disable	Drive Reset to Target System
config	rombreak	enable | disable	Break on Write to ROM
config	language	Hitachi | IAR	Language Tool Type
config	chip	<*processor type*>	Processor Type
config	mode	<*mode number*>	Processor Operation Mode
config	rsp	<*sp value*>	Stack Pointer Reset Value
config	end		End of Hardware Option Commands
map	start		Start of Memory Map Commands
map	<*map range*>	<*memory type*>	Setting Map Term
map	other	<*memory type*>	Setting Memory Type of Other Area
map	end		End of Memory Map Commands

enable | disable Specify **`enable`** when **Yes**, **`disable`** when **No**.

<*processor type*> Specify one of the following emulation processors.

- **H8/3001**
- **H8/3002**
- **H8/3003T** (1:1 clock version)
- **H8/3003** (clock-halving version)
- **H8/3004**
- **H8/3005**
- **H8/3030**
- **H8/3031**
- **H8/3032**
- **H8/3040**
- **H8/3041**
- **H8/3042**

<*mode number*> Specify a number from **1** to **7** for the processor operation mode.

<*sp value*> Specify a 32-bit even address except the on chip peripheral module register area. Normally, specify the default value of the user program.

<*map range*> Specify an area to be mapped.

Format: <*start address*>..<*end address*>

<*memory type*> Specify one of the following memory types.

- **eram**
- **erom**
- **tram**
- **trom**
- **grd**

For a memory type of other area, **eram** and **erom** cannot be specified.

```
# Configuration File
# Hardware Options
config start
config ba enable
config chip H8/3041
config clk internal
config dbc disable
config drst enable
config mode 5
config nmi enable
config rrt disable
config rsp 0fff10
config trst enable
config rombreak enable
config language IAR
config end

# Memory Map
map start
map 0000000..000bfff erom
map 000c000..000ffff grd
map 0020000..002ffff eram
map other tram
map end
```

Figure 2-3. Configuration File Example

Note

3

Language Tools

Language Tools

This chapter describes language tools which can be used with the HP B3750A Debug User Interface.

Hitachi Language Tools

The HP B3750A Debug User Interface can debug user programs created with the following Hitachi language tools.

Table 3-1. Hitachi Language Tools

Tool	Command	Description
C Compiler	**ch38**	H8S, H8/300 Series C Compiler
Assembler	**asm38**	H8S, H8/300 Series Cross Assembler
Linker	**lnk**	H Series Linkage Editor

For version numbers of language tools supported by the HP B3750A Debug User Interface, contact your nearest HP support office.

Command Options

This section describes important command options when using the Hitachi language tools.

C Compiler

-debug Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

-optimize=<*level*>

Specifies an optimization level. When **1** is specified, it performs optimizations. When **0** is specified, it performs no optimizations.

The following functions do not work correctly with optimized modules.

- Display a back trace.
- Return to a caller routine.
- Display and modify a variable located on a stack area.

If you need above functions, specify an optimization level **`0`**.

Assembler

`-debug` Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

Linker

`-debug` Generates debug information.
You must always specify this option. Programs without debug information cannot be debugged.

IAR Language Tools

The HP B3750A Debug User Interface can debug user programs created with the following IAR language tools.

Table 3-2. IAR Language Tools

Tool	Command	Description
C Compiler	**icch8**	IAR H8 C-Compiler
Assembler	**ah8**	IAR H8 Assembler
Linker	**xlink**	IAR Universal Linker
Converter	**iar2ieee**	UBROF to IEEE-695 Converter

The converter is not required when using the linker which can generate the IEEE-695 format.

For version numbers of language tools supported by the HP B3750A Debug User Interface, contact your nearest HP support office.

Note

When using the IAR language tools, the following commands cannot be used.

- Display a back trace.
- Return to a caller routine.

Command Options

This section describes important command options when using the IAR language tools.

C Compiler

-r Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

-s <*level*> Specifies a speed optimization level in **0** to **9**.
Modules which are optimized at level **7** or higher cannot be debugged.

-z <*level*>	Specifies a speed optimization level in **0** to **9**. Modules which are optimized at level **7** or higher cannot be debugged.

Assembler

-r	Generates debug information. You must always specify this option. Modules without debug information cannot be debugged.

Linker

-F <*format*>	Specifies an output file format. When **debug** is specified, it generates the UBROF format. When **ieee695** is specified, it generates the IEEE-695 format. When the linker cannot generate the IEEE-695 format, you must convert the output file from the UBROF format to the IEEE-695 format by the converter.

Converter

No command options are required.

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Emulation Status

Emulation Status

This chapter describes the emulation status messages which are displayed in the Debug window.

An emulation status message is displayed in the Debug window.
The HP B3750A Debug User Interface has the following emulation status messages.

- **Emulation reset**

  The emulator is resetting the processor.

- **Running in monitor**

  The emulator is executing the monitor.

- **Running user program**

  The emulator is executing the user program.

- **Awaiting target reset**

  The emulator is awaiting a reset signal from the target system.

  When a "run from reset" command is executed, the emulator enters this state. During this state, the emulator cannot break to the monitor.

- **Target reset**

  The target system is resetting the processor.

  When the emulator accepts the $\overline{\text{RES}}$ or $\overline{\text{STBY}}$ signal from the target system while running the user program, the emulator enters this state. During this state, the emulator cannot break to the monitor.

Note

The emulator does not support hardware standby mode.
The $\overline{\text{STBY}}$ signal from the target system is connected to the reset signal in the emulator. So, if the $\overline{\text{STBY}}$ input is asserted, the emulator enters a reset state instead of hardware standby mode.

- **Bus grant**

  A bus-released state.

  When the emulator accepts the $\overline{\text{BREQ}}$ signal from the target system, the emulator enters this state. During this state, the emulator cannot break to the monitor.

- **Sleep**

  Sleep mode.

  Sleep mode is cleared when the emulator breaks to the monitor. When entering the monitor from sleep mode, the program counter (PC) points to the next instruction from the SLEEP instruction.

- **Standby**

  Software standby mode.

  Software standby mode is cleared when the emulator breaks to the monitor. When entering the monitor from software standby mode, the program counter (PC) points to the next instruction from the SLEEP instruction.

- **Slow clock**

  The processor's clock is abnormally slow or stopped.

  When setting a hardware option to use the processor's clock sourced by the target system, turning off the target system or a broken-down clock on the target system may cause this state.

- **No bus cycles**

  A state with no bus cycles.

  The $\overline{\text{WAIT}}$ signal from the target system may cause this state.

- **Unknown state**

  An abnormal state.

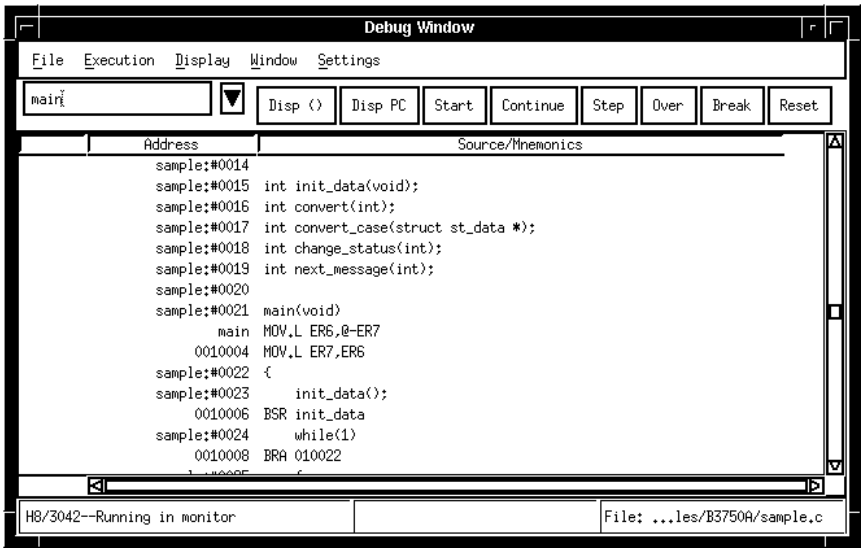

Figure 4-1. Debug Window

Note

5

Trace

Trace

This chapter describes trace functions specific to the HP B3750A Debug User Interface.

Trace Clock Speed

When using the analyzer boards **HP 64703/04A**, you can set the trace clock speed.

For the HP B3750A Debug User Interface, setting the trace clock speed is not required. Do not change it from the default value "**Slow**".

The analyzer boards **HP 64794A/C/D** have no trace clock speed setting.

Data and Status Conditions

This section describes the data and status conditions in the following dialog boxes of the HP B3750A Debug User Interface.

- Trace Trigger Store Condition dialog box.
- Trace Pattern dialog box of sequential trace.

Data Condition

The data bus to the emulation analyzer is 16-bit width. Bus width of memory area and access size influence whether upper or lower byte data is valid.

- When accessing in word to a 16-bit data bus area, both upper and lower byte data are valid.
- When accessing in byte or accessing to an 8-bit data bus area, only upper byte data is valid at an even address. Only lower byte data is valid at an odd address.
- A longword access is divided into two word accesses.

Use "**x**" for invalid byte data to set the data condition as examples shown in the following table.

Table 5-1. Data Condition Settings

Area	Bus Width	Access Size	Address	Upper Byte	Lower byte	Example
On-Chip ROM On-Chip RAM	16-Bit	Byte	Even	Valid	-	**0a5xx**
			Odd	-	Valid	**0xx5a**
		Word	Even	Valid	Valid	**0a55a**
External Memory On-Chip Peripheral	8-Bit	Byte	Even	Valid	-	**0a5xx**
			Odd	-	Valid	**0xx5a**
		Word	Even (1st)	Valid	-	**0a5xx**
			Odd (2nd)	-	Valid	**0xx5a**
	16-Bit	byte	Even	Valid	-	**0a5xx**
			Odd	-	Valid	**0xx5a**
		Word	Even	Valid	Valid	**0a55a**

Status Condition

You can specify the following items as the status condition.

fetch Instruction fetch cycle.

data Data access cycle.

read Read cycle.

write Write cycle.

mem Access cycle to the on-chip ROM/RAM and external memory area.

io Access cycle to the on-chip peripheral module register area.

byte Byte access cycle.

word Word access cycle.
A longword access is divided into two word accesses. A longword access and a word access cannot be distinguished from each other.

cpu CPU cycle.

dma DMA controller (DMAC) cycle.

intack Interrupt acknowledge cycle.
When entering sleep or software standby mode, an interrupt acknowledge cycle happens. However, this cycle does not happen at interrupts to clear those modes.
When the emulator breaks to the monitor, an interrupt acknowledge cycle may also happens.

refresh Refresh cycle.

wrrom Write cycle to an area mapped as ROM.

grd Access cycle to an area mapped as guarded memory.

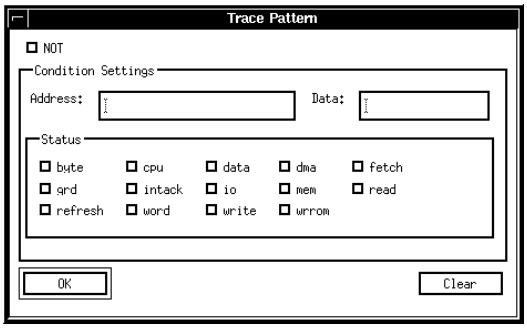

Figure 5-1. Trace Pattern Dialog Box

6

Windows

Windows

This chapter describes windows specific to the HP B3750A Debug User Interface.

Register Window

In the Register window of the HP B3750A Debug User Interface, the internal registers of the CPU can be displayed and modified.

- Program Counter (PC)
- Condition-Code Register (CCR)
- General Registers (ER0 to ER7)
- Stack Pointer (SP)
- Mode Control Register (MDCR)

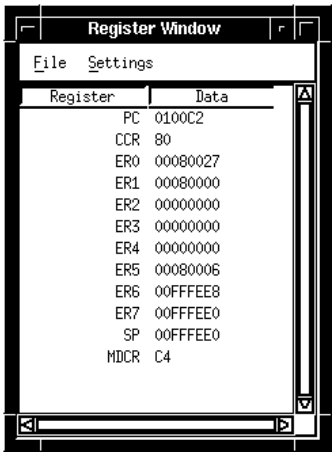

Figure 6-1. Register Window

Peripheral Window

In the Peripheral window of the HP B3750A Debug User Interface, all registers of the following on-chip peripheral modules can be displayed and modified.

- System Control Registers
- Interrupt Controller
- Bus Controller
- Refresh Controller
- DMA Controller (DMAC)
- I/O Ports
- 16-Bit Integrated Timer Unit (ITU)
- Programmable Timing Pattern Controller (TPC)
- Watchdog Timer (WDT)
- Serial Communication Interface (SCI)
- A/D Converter
- D/A Converter

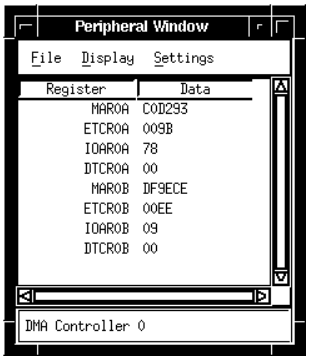

Figure 6-2. Peripheral Window

7

Restrictions and Limitations

Restrictions and Limitations

This chapter describes restrictions and limitations.

The HP B3750A Debug User Interface and the HP 64784A Emulator have the following restrictions and limitations.

IAR Language Tools

When using the IAR language tools, the following commands cannot be used.

- Display a back trace.
- Return to a caller routine.

- **Direct Memory Access**

  The target system cannot perform direct memory access to the emulation memory.

- **On-Chip RAM of the H8/3005**

  When emulating the H8/3005, the memory area 0FEF10H to 0FF00FH (mode 1) and 0FFEF10H to 0FFF00FH (mode 3) cannot be used as the on-chip RAM.

  If you want to use this area, map this area as emulation RAM. However, this area works as 8-bit external address space accessed in three clock cycles.

- **Reset and Standby**

  While running the monitor, the $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ signals from the target system are ignored.

- **Interrupts**

  While running the monitor, the emulator responds to no interrupts.

  The emulator suspends interrupt requests in the monitor; the requests will be serviced upon return to the user program.

- **Reset Output**

  The emulator ignores the reset output enable bit (RSTOE) of the reset control/status register (RSTCSR).

  Use the hardware option **Drive Reset to Target System** to select whether the emulator drives the $\overline{\text{RESO}}$ signal to the target system or not.

- **Watchdog Timer**

  When entering the monitor, the watchdog timer (WDT) stops counting regardless of its mode, watchdog or interval. And, it resumes counting upon return to the user program.

- **Sleep and Software Standby Modes**

  Sleep and software standby modes are cleared when the emulator breaks to the monitor.

  When entering the monitor, the program counter (PC) points to the next of the SLEEP instruction.

- **Hardware Standby Mode**

  The emulator does not support hardware standby mode.

  The $\overline{\text{STBY}}$ signal from the target system is connected to the reset signal in the emulator. So, if the $\overline{\text{STBY}}$ input is asserted, the emulator enters a reset state instead of hardware standby mode.

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