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NetROM™

Hardware Interface Reference

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Trademarks

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Preface

Introduction

NetROM is a powerful communications and ROM-emulation tool for use in embedded-systems design. Although NetROM's most important function is communication between the development host and the target system, NetROM allows design engineers to substitute NetROM for the target's ROM during software design. This simplifies and shortens a project's software development. For example, you can use NetROM's RAM instead of the time-consuming process of burning and reburning PROMs during design development and testing. When you are satisfied that the design is functional, disconnect NetROM and create a permanent ROM to replace the temporary NetROM circuit.

For NetROM to work most effectively as a design tool, engineers should consider several design elements to reduce or eliminate potential circuit problems.

This document describes some aspects of the design process in which designers can avoid design pitfalls. Most circuits in the field, perhaps 99%, function satisfactorily without any of the problems discussed here. However, we have found these design recommendations will optimize the performance of many circuits, not just the problem ones.

Conventions

This manual uses the following conventions:

- Target device refers to the printed circuit board to which the NetROM is temporarily attached.
- ROM is used to indicate ROMs, PROMs, and Flash ROMs, except in instances when differentiating between them is important.
- Book titles, emphasized words, command names, and keywords are in *italics.*
- Command parameters (both alpha and numeric) are in **boldface.**
- Computer programs are in `constant-spaced font.`
- Environment variable names are in "quotation marks."
- Items that are completely optional are enclosed in [square braces].
- Items that are mutually exclusive are separated by a vertical bar |.
- Mutually exclusive items, one of which is mandatory, are enclosed in {braces}.

Warnings, cautions, notes

Warning

Warning messages appear before procedures and alert you to the danger of personal injury which may result unless certain precautions are observed.

Caution

Caution messages appear before procedures and indicate that damage may be done to the emulator or to your target system unless certain steps are observed.

Note

Notes indicate important information for the proper operation and installation of your emulator.

Support services

Applied Microsystems provides a full range of support services. The NetROM is covered by a 90-day warranty that includes full applications phone support. Additional support agreements are available to extend the initial warranty and to provide additional services.

If you have trouble installing or using the product, consult your manuals to verify that you are following the correct procedures.

If the problem persists, call Customer Support. Customers outside the United States should contact their sales representative or local Applied Microsystems office. When you contact Customer Support, have your serial number available.

Telephone

800-ASK-4AMC (800-275-4262)

(206) 882-2000 (in Washington State or from Canada)

Internet address

If you have access to the Internet, you can contact Applied Microsystems Customer Support using the following address:

support@amc.com

You can also browse the Applied Microsystems World Wide Web page using the following URL:

http://www.amc.com

FAX

(206) 883-3049

Chapter 1

Optimizing TTL Bus Design

This chapter discusses potential problems occurring in TTL bus design and recommends ways to optimize bus design.

Keep the ROM TTL bus on the PC board

Ideally, the bus should stay on the target's PC board and not go through a connector. If the target device contains more than one board, good design practice suggests that the bus stay on one board not go from board to board. Connectors and their connecting cables tend to add stray capacitance and inductance, which effects the performance of the bus.

Keep bus length short

The longer the bus the more inductance and capacitance. Independent empirical studies show that about 10 inches is the longest a bus should be without considering the analog effects on bus performance.

Minimize tees (stubs) and keep tee length short

A tee is formed on a PC board when the designer places a junction in the etch to carry a signal to two locations, rather than to a single destination. Typically, the etch or wires should go from point to point (serial fashion) without any intersections. Ideally, there are no tees on the bus. In practice, however, small stubs of one-quarter inch or less are acceptable. Longer stubs of one inch or more often create unnecessary problems.

Basically, stubs are undesirable because they cause reflections going back into the driver. A receiver can reflect energy back to the driver through both paths. With no stub, there is only one source of reflections back to the driver.

Reflections are undesirable because they effect the wavefront. A perfect waveform goes from a logical 1 to a logical 0 state, or vice versa, in the 3-to-6 nanosecond range. A tee adversely affects the sharp edges of the wavefront because of the reflections.

Figure 1-1 shows the effects a stub can have on a buffer. The signals going into (A) the buffer and out from the buffer show sharp delineated wavefronts when there is no stub, with the output waveform looking very similar to the input. When you add a tee in the circuit, not only does the wavefront input to the buffer (B) become very ragged, but reflections can cause the output to switch falsely (C), thus sending an errant low-going signal down the line.

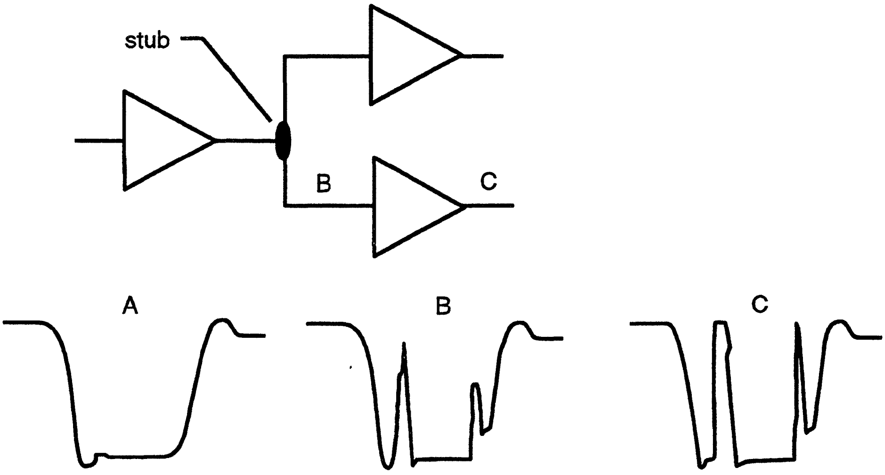

Figure 1-1 Effect of a tee (stub) on a buffer

If you must use tees, use as few as possible, and for each tee, keep the length as short as possible.

Daisy chain bus elements

Connect bus nodes (circuit devices such as buffers, drivers, receivers or any other ICs) in serial daisy-chain fashion. That is, directly connect the output of one node to the input of the next node in a chain. Although this technique may take extra board-layout design time initially, the extra effort will keep unwanted reflections and circuit noise to a minimum. If there are many nodes to be connected to a bus, you may want to reduce the number of etches by adding tees; however, as discussed above, adding tees can increase the noise level and unreliability of a circuit, and is not recommended.

Chapter 2
Optimizing PC Board Design

General design considerations

The following sections discuss factors to consider when designing boards of any size.

Multilayer PC board construction

Using multilayer construction for PC boards is one way to tighten the circuit parameters and reduce potential analog problems on the board. Multilayer design is important especially on boards that have long buses. It can also benefit boards with short buses. In multilayer design, there is a VCC plane, a ground plane, and one or more signal planes. The embedded power planes offer distributed capacitance and controlled impedance for the signal etches.

Using NetROM's interface connector

NetROM has four 40-conductor ribbon cables that can connect to four target connectors. The cables are for Pod 0 through Pod 3. The four ribbon cables connect to NetROM through two dual 40-pin connectors. Cables for Pods 0 and 1 connect to the left connector on NetROM's front panel, and Pods 2 and 3 connect to the right connector. Pod 0 and Pod 2 connect to the top rows and Pods 1 and 3 to the bottom rows. Each Pod connector includes two flat ribbon cables. See Chapter 4 for more information about pod connections.

The four ribbon cables can be connected externally in either of two ways:

- By using plugs that would plug into a target's existing memory DIP or PLCC sockets; or

- ❑ By using either a dual 40-pin or a single 40-pin connector that could be plugged into a special mating connector that is designed into the target board.

Existing memory DIP or PLCC sockets

The memory-socket connection is the easiest to connect. Typically, when a target is designed, PLCC or DIP sockets are used for memory devices and ROMs are plugged into the sockets. Applied Microsystems supplies cables with plugs for these sockets.

A drawback to this approach is that the sockets were not designed for external cables, and the pin connections could become unstable and the long cables can fall out of the sockets or make intermittent connections. Another drawback is potentially inserting the plugs backwards into the sockets, which can damage NetROM, the target, or both.

Dual 40-pin or a single 40-pin connector

We recommend, if possible, that one 40-pin connector be designed on the board for each pod to be used, with a maximum of four connectors per NetROM box.

You can also use dual 40-pin connectors with a maximum of two connectors per NetROM box. In this way, the NetROM cable plugs into a mating connector, allowing a reliable connection. When design is complete and NetROM disconnected, the connectors remain on the board, making it easy to reconnect NetROM in the future. Production units can have this connector removed to save the connector cost.

If you wish to design matching connectors into your target's PC board, use the following connectors:

3M 40- pin connectors

Right-angle	Part Number 3432-1XXX
Straight	Part Number -N3432-2XXX

Fujitsu dual 40-pin connectors

Right-angle	Part Number FCN-235P080-G/MA
Straight	Part Number FCN-234P080-G/MA

This gives the cabling system a robust mechanical advantage so if the cable is accidentally tapped or the target is moved, there will not be an intermittent problem caused by a marginal PLCC or DIP socket connection.

Design considerations for boards with long TTL buses

Design considerations for long TTL buses are different than those for short buses. Here are two examples:

- The longer etch adds extra capacitance. Think of the etch as a capacitor that causes the signal to have slower rise and fall times. On a short bus, the rise and fall times have sharper edges with less undershoot or overshoot.
- Additional sockets add capacitance because there are more sockets on long buses. Also the IC socket pins connecting to the trace increase capacitance. Moreover, a driver or receiver in the IC itself has some capacitance effects. Because the etch leaves the controlled impedance of the PC board and goes up to a socket or some mechanical device, controlled impedance is lost, which may cause problems.

For long buses there are ways to clean up the signals and mitigate any adverse effects. When long-bus board designs are optimized, not only will the board function better and more efficiently, but such a design will facilitate NetROM's working with the board. The following paragraphs contain additional recommendations.

Divide buses into branches and add buffers

Instead of having 10 to 12 nodes (drivers or receivers) or more, divide the bus into two sections, each with five to six nodes (or more). Branch the bus close to its origin, and put a buffer on each of the shorter buses. Figure 2-1 shows how one trace or one line on a long bus can be divided into two smaller lines, each driven by its own buffer.

About 10 to 12 nodes is the practical limit for most buses. Most buses - control, address, and data types - can have buffers added to clean up the signals.

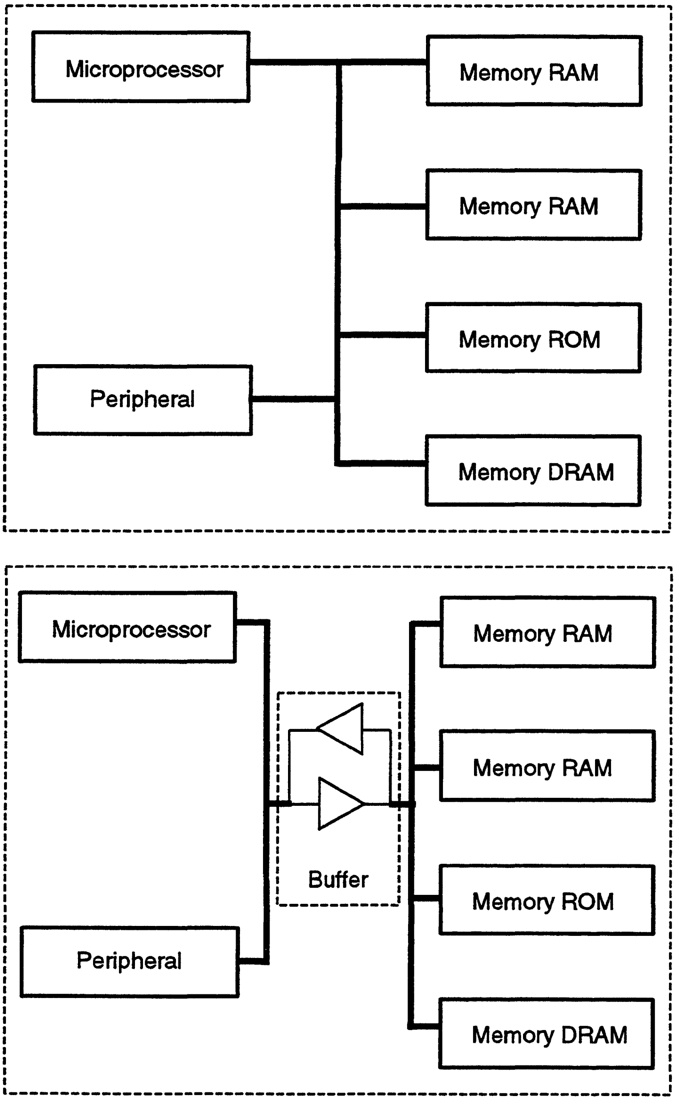

Figure 2-1 Dividing a long bus and adding buffers

However, a buffer will add some propagation delay, thus slowing the circuit. The beneficial effect is a buffer will reduce capacitance and reflections inherent with longer buses, and, therefore, increase circuit speed. So the added propagation delay through the buffers is mitigated by the fact that there is less capacitance.

Note

Empirical evidences shows that circuitry on two shorter buses runs better than circuitry run on one longer bus with no buffers.

You will want to add buffers in cases where there are many loads. Just adding a 12-inch cable segment will degrade the signal. An example of a suitable buffer is the one that NetROM uses as an input buffer, which is an IDT (Integrated Device Technology) 74FCT162244TPV.

Terminate at both ends of the bus

For long bi-directional data buses, we recommend terminating the bus at both ends, rather than just at one end. Use either parallel or Thevenin termination.

Thevenin termination on both ends provides resistors, which are tied to VCC and ground that will absorb any noise or adverse reflections on the wavefront. If, for example, one of the mid-bus drivers is active, the signal will travel to both ends of the bus. Thevenin termination also balances the impedance of drivers and receivers, thereby reducing adverse reflections and noise from the bus. Figure 2-2 shows a long bus with dual Thevenin termination.

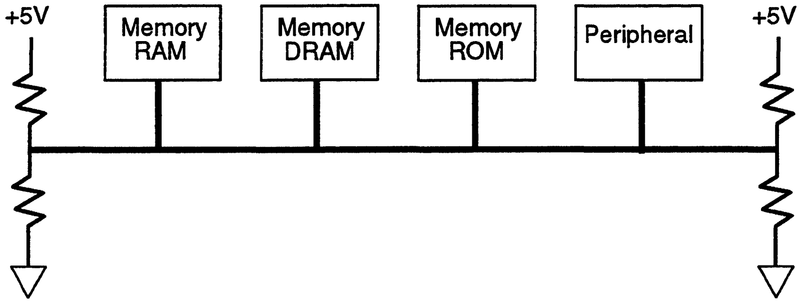

Figure 2-2 A long bus with dual Thevenin termination

Connect NetROM at the end of the bus

Because the NetROM cables can be plugged either into existing ROM sockets or into connectors added to the target's PC board, it is beneficial during the design phase to place the intended sockets or connectors at one end of the TTL bus. In any event, try to avoid connecting NetROM to any tee or stub in the middle of a bus.

Chapter 3
NetROM's Cable Termination

A NetROM cable termination circuit consists of these three elements:

- Thevenin termination
- Clamping diode
- Receiver

Figure 3-1 illustrates the termination circuit inside NetROM. The figure is for one line of a bus. Because there are four pod connections and 29 bus lines (18 address, 8 data, and 3 control) per pod, there are 116 separate termination circuits within NetROM, one circuit for each line.

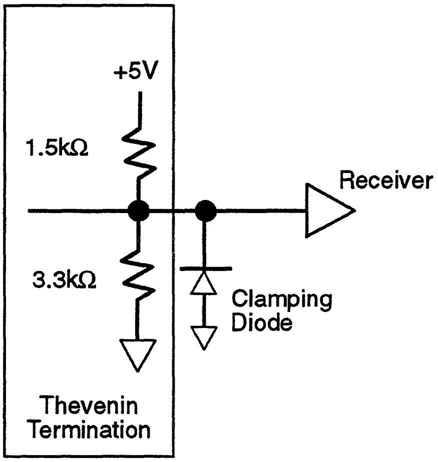

Figure 3-1 NetROM's internal termination circuit

Thevenin termination

NetROM has a Thevenin termination circuit on each line of a bus. This consists of a nominal 1.5 kohm pull-up resistor placed between the signal line and NetROM's VCC (+5.0 Volts) and a nominal 3.3 kohm pull-down resistor between the signal line and ground.

Clamping diodes

Each termination circuit has a clamping diode, a TI SN74S1056SC, connected between the signal line and ground, which clamps the line at -0.4 Volt. The clamping diode keeps undershoot to a maximum of -0.4 Volts (below ground). The clamping diode effects the circuit in this way: When a signal comes into NetROM through the connecting cables, as the waveform on the falling edge goes low, without the diode the waveform may tend to go below ground one or two volts depending upon the amount of undershoot on the line and then come up above ground as a bounce before settling back down. The clamping diode clamps the signal at -0.4 Volt, which lessens the subsequent overshoot or ring. In addition, the diode also gives some amount of static protection.

Input receivers

NetROM also uses a special receiver in each circuit, which is an IDT (Integrated Device Technology) 74FCT162244TPV. The receiver connects in series between the signal line and the emulation RAM in NetROM. The receiver has typically 200 millivolts of hysteresis.

Chapter 4
Using Mass Terminated Connectors

If you are designing your target from conception, you may want to add one, two, three, or four dedicated NetROM interface connectors to your target board for flat ribbon cables. This type of connection provides more reliability than possible by plugging connectors directly into memory PLCC or DIP sockets on your board. Refer to "Using NetROM's interface connector" on page 2-1.

Interface connectors

Each 40-conductor ribbon cable has independent control, address, and data buses that can be used for ROM emulation. Table 1 shows the four connectors that plug into a target board and the pin assignments for the signals.

Table 4-1 Pin assignments for target POD connections

POD 0		POD 1		POD 2		POD 3	
Pin	**Assignment**	**Pin**	**Assignment**	**Pin**	**Assignment**	**PIn**	**Assignment**
1	No Connection	1	No Connection	1	No Connection	1	No Connection
2	P0_OE*	2	P1_OE*	2	P2_OE*	2	P3_OE*
3	P0_CE*	3	P1_CE*	3	P2_CE*	3	P3_CE*
4	VCC	4	VCC	4	VCC	4	VCC
5	P0_WE	5	P1_WE	5	P2_WE	5	P3_WE
6	Ground	6	Ground	6	Ground	6	Ground
7	POD_0_A16	7	POD_1_A16	7	POD_2_A16	7	POD_3_A16
8	POD_0_A17	8	POD_1_A17	8	POD_2_A17	8	POD_3_A17
9	POD_0_A15	9	POD_1_A15	9	POD_2_A15	9	POD_3_A15

Table 4-1 Pin assignments for target POD connections

POD 0		POD 1		POD 2		POD 3	
Pin	**Assignment**	**Pin**	**Assignment**	**Pin**	**Assignment**	**Pln**	**Assignment**
10	POD_0_A14	10	POD_1_A14	10	POD_2_A14	10	POD_3_A14
11	POD_0_A12	11	POD_1_A12	11	POD_2_A12	11	POD_3_A12
12	POD_0_A13	12	POD_1_A13	12	POD_2_A13	12	POD_3_A13
13	POD_0_A7	13	POD_1_A7	13	POD_2_A7	13	POD_3_A7
14	POD_0_A8	14	POD_1_A8	14	POD_2_A8	14	POD_3_A8
15	POD_0_A6	15	POD_1_A6	15	POD_2_A6	15	POD_3_A6
16	POD_0_A9	16	POD_1_A9	16	POD_2_A9	16	POD_3_A9
17	POD_0_A5	17	POD_1_A5	17	POD_2_A5	17	POD_3_A5
18	POD_0_A11	18	POD_1_A11	18	POD_2_A11	18	POD_3_A11
19	POD_0_A4	19	POD_1_A4	19	POD_2_A4	19	POD_3_A4
20	POD_0_A3	20	POD_1_A3	20	POD_2_A3	20	POD_3_A3
21	POD_0_A10	21	POD_1_A10	21	POD_2_A10	21	POD_3_A10
22	POD_0_A2	22	POD_1_A2	22	POD_2_A2	22	POD_3_A2
23	POD_0_A1	23	POD_1_A1	23	POD_2_A1	23	POD_3_A1
24	POD_0_A0	24	POD_1_A0	24	POD_2_A0	24	POD_3_A0
25	Ground	25	Ground	25	Ground	25	Ground
26	Ground	26	Ground	26	Ground	26	Ground
27	Ground	27	Ground	27	Ground	27	Ground
28	No Connection	28	No Connection	28	No Connection	28	No Connection
29	Ground	29	Ground	29	Ground	29	Ground
30	Ground	30	Ground	30	Ground	30	Ground
31	Ground	31	Ground	31	Ground	31	Ground
32	POD_0_D7	32	POD_1_D7	32	POD_2_D7	32	POD_3_D7
33	POD_0_D6	33	POD_1_D6	33	POD_2_D6	33	POD_3_D6
34	POD_0_D0	34	POD_1_D0	34	POD_2_D0	34	POD_3_D0
35	POD_0_D5	35	POD_1_D5	35	POD_2_D5	35	POD_3_D5

Table 4-1 Pin assignments for target POD connections

POD 0		POD 1		POD 2		POD 3	
Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
36	POD_0_D1	36	POD_1_D1	36	POD_2_D1	36	POD_3_D1
37	POD_0_D4	37	POD_1_D4	37	POD_2_D4	37	POD_3_D4
38	POD_0_D2	38	POD_1_D2	38	POD_2_D2	38	POD_3_D2
39	POD_0_D3	39	POD_1_D3	39	POD_2_D3	39	POD_3_D3
40	Ground	40	Ground	40	Ground	40	Ground

Notes

VCC is the target's +5.0 Volt supply, not NetROM's.

P0_OE*, P1_OE*, P2_OE* and P3_OE* are output enable control lines.

P0_CE*, P1_CE*, P2_CE* and P3_CE* are chip enable control lines.

P0_WE*, P1_WE*, P2_WE* and P3_WE* are write enable control lines.
* indicates a low-true state.

POD_0_A##, POD_1_A##, POD_2_A## and POD_3_A## are address bus lines.

POD_0_D##, POD_1_D##, POD_2_D## and POD_3_D## are data bus lines.

The following is a description of the lines and their signals:

Control lines

The output enable (OE*), chip enable (CE*), and write enable (WE*) lines are driven just like the output enable, chip enable, and write enable of a PROM device. Each line is low-true.

Address lines

A0 to A17 are the address inputs to NetROM's RAM. If your target is not driving all address lines (0 through 17), we recommend you terminate high or leave the unused lines disconnected. For example, if your target only uses address lines A0 through A15, then leave A16 and A17 unconnected or terminate using a 1 kohm to 10 kohm pull-up resistor to VCC (+5.0 Volts).

Note

The NetROM software, when configuring itself, assumes that unused address lines are terminated high or are unconnected. Do not tie unused lines to ground!

Data lines

D0 to D7 are bi-directional data lines. Some type of termination on the target board, such as 1.3 kohm/3.3 kohm Thevenin termination should be added to each data line on long-bus designs.

Grounds

Pins 5, 24, 25, 26, 28, 29, 30 and 39 are grounds to be connected to the target's ground plane.

Target VCC

NetROM uses the target's VCC (+5 Volt supply) to power the POD LEDs on the NetROM front panel. You should connect the target's +5 Volt supply to this line. This is the only case where NetROM uses the target's VCC. Current drain is in the milliamp range. NetROM receives its power from its own power supply.

Plugging cables into target connectors

Before applying power, take care to plug the cables correctly into the target interface connectors.

Caution

Plugging a cable in backwards can cause the target power supply to reverse drive the NetROM power supply. This would connect NetROM's plus and minus supplies to the target's minus and plus supplies creating a direct short circuit. The target or NetROM or both could be damaged.

On some sockets, ground and power pins are in opposite corners of the socket, so switching the cable switches the ground and power pins. Unfortunately, we cannot design against installing the cables backwards.

Pin 1 is clearly marked on both sockets and cables. Pin 1 on the cables has a red identifier marking; pin 1 on DIP sockets is marked with a “1” or an arrow; and PLCC sockets have a little key. This key on the PLCC socket makes it difficult to put the PLCC plug in backwards.

Cable status LEDs

There are four status LEDs on the NetROM front panel; one LED for each cable. When you plug the cable correctly into the target, the corresponding NetROM green LED lights. If the cable is plugged in backwards, the LED will not light.

Chapter 5

Using the Command Status Connector

In addition to the ROM emulation connectors (described in Chapter 4), NetROM has a special 20-pin command status connector on its front panel. The use of this connector is optional. When this connector is attached to a target via a 20-pin cable and a connector designed into the target, the command status feature permits the target to send status signals and control signals to NetROM, providing an external write line that when driven low allows the target to write to the emulation ROM (RAM) within NetROM. The part number of the mating command status connector is 3M 3421. Table 5-1 shows the pin assignments for the NetROM connector.

Table 5-1 Pin assignments for command status connector

Pin	ID	Assignment	Pin	ID	Assignment
1	R	TAR_CTL0*	11		
2	1	TAR_CTL1*	12		TAR_STS1*
4	3	TAR_CTL3*	14		TAR_STS3*
5	4	TAR_CTL4*	15		TAR_STS4*
6	5	TAR_CTL5*	16		TAR_STS5*
7	6	TAR_CTL6*	17		TAR_STS6*
8	7	TAR_CTL7*	18		TAR_STS7*
9		No Connection	19		Ground
10		Ground	20	W	TAR_WR*

Notes

Pin 1 (R) is usually used for reset.

TAR_CTL is a Target Control Line.

TAR_STS is a Target Status Line.
TAR_WR is a Target Write Line.
* indicates a low-true state.

There are eight target control signal lines TAR_CTL0* through TAR_CTL7*. NetROM's open collector driver drives these lines. Each line must be terminated through a nominal 1.5-kohm resistor to VCC (+5.0 Volts) for proper operation.

There are also eight target status signal lines, TAR_STS0* through TAR_STS7*. NetROM reads the TTL signals on these lines off the cable.

The external write line, TAR_WR*, when driven low, allows data to be written to NetROM's RAM. There are two ground lines, pins 10 and 19, which are to be connected to the target's ground plane. Pin 9 is not used.

You can connect these lines to different parts of your circuit as needed. For example, TAR_CTL0*, Target Control 0, generally goes to your reset logic. When you are programming and logged into NetROM, you can send out a command to make this line go assertive (low-true) and non-assertive (false-high) resetting your target for you. That may be easier than coming over to the target and pressing a button somewhere or turning the target's power off and on, etc. Using the reset line is simply a convenience.

Another connector use is to take TAR_CTL1*, Target Control 1, and run it over to the non-maskable interrupt (NMI) line of your processor, if you have one. That allows you to cause an interrupt or exception to the process that is going on in the target.

Note

These lines are *options* to aid in your software development phase.

NetROM also reads status lines. The eight status lines, TAR_STS0* through TAR_STS7*, constitute a bus on which the target can send status data to NetROM.

When used together, the status lines, which carry signals from the target to NetROM, and the control lines, which carry signals from NetROM to the target, can communicate bi-directionally between the two devices.

Pin 20 is the target write line, TAR_WR*. There are cases when you want the target to modify (write) the NetROM's memory. There are two ways to do that. If NetROM is connected to a connector or memory device that allows writing, such as a Flash ROM or RAM, then NetROM can pick up the write signal from the existing socket, and through the existing cables using the ROM emulation Connectors. Refer to Chapter 4.

However, in the case of a ROM on your target, there is no write line; i.e., you cannot write to a read-only memory. So you need some way to get a write attribute over to NetROM. Using pin 20, the target write line, is one way to do this. Some applications require the target to write to NetROM and others do not. Use of this line depends on your application.

NetROM software is powerful enough so you can specify a high-true or low-true state on any one of these signal lines (except TAR_WR*) and make whatever assertive-state modifications that you want. The NetROM *User's Guide* explains how to make these changes.

Chapter 6
Writing to NetROM Memory

Typically, a target writes to NetROM to perform some input-output function not designed into the target. For example, a very small target board that connects to an appliance most likely would not have a console or a monitor or a keyboard.

One way to emulate a console is to use a read-address console. The read-address console does not require the target to write to NetROM. Another way to emulate a console is to have the target write to NetROM through the pod connectors or the command status connectors:

Pod connectors.
If the target's memory device is a Flash ROM, RAM or PROM, then the write pin (WE or W) of that device can be used. This is the method most often used with NetROM if the read-address console is not used. If the target's memory device is a ROM, then there is no write line. In that case, if the NetROM cables are connected through 40-pin installed connectors on the target board, the write line in these cables can be used.

Command status connectors.
If the target's memory device is a ROM, there is no write-enable pin at the ROM socket; however, you can use the external write line of the command status connector (refer to Chapter 5). This write-enable feature can be used in one of two ways:

- A 20-pin connector can be added to the target board and connected to the NetROM command status connector via a cable.
- For temporary use, a single wire can be attached to the target write line, pin 20 of the command status connector, and the other end of the wire, with an alligator clip, can be attached to the write-enable connection (wherever it is) on the target.

The following rules apply to all NetROM write cycles, either directly through the pod, or via the external write line:

- NetROM write cycle is similar to a static-ram write cycle.
- There is no algorithm required for writes, such as with Flash devices that use algorithms such as AAAA or 5555.
- The output enable (OE) pin on the pod connector must not be asserted while the target is driving data for the write cycle. NetROM has been designed to emulate PROMs. In a PROM device, if you assert output enable to tell the PROM that you want to read data, and if you also assert the read/write line in a write mode, you are telling the PROM that you want to write to it. NetROM will look at those signals and emulate a PROM. In that case, output enable will take precedence and there will be a read cycle instead of a write cycle. So when you are writing to NetROM, you must have the output enable control signal false (high) during the write cycle.

When writing to NetROM, certain timing considerations must be met. Figure 6-1 shows write-timing diagrams for two controlled-write cycles. The upper half of the figure is a read/write control cycle and the lower half is a chip-enable control cycle.

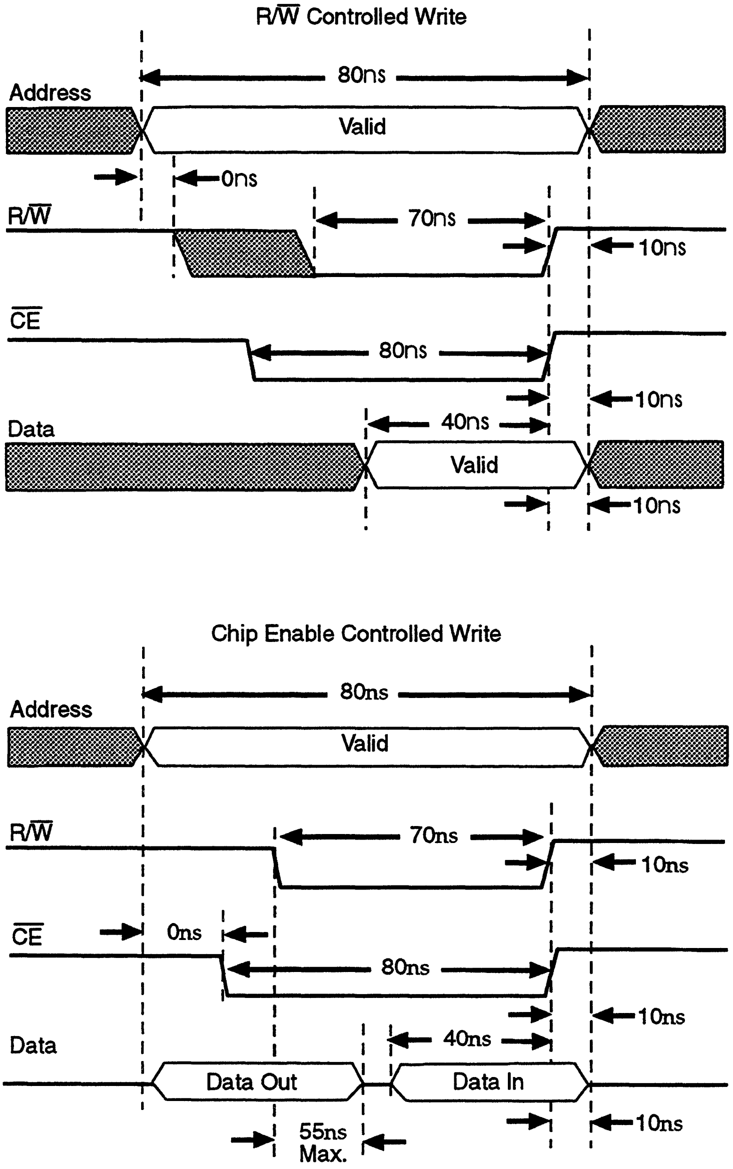

Figure 6-1 NetROM write-timing diagram

Chapter 7
Circuit Design Recommendations

Summary of recommendations

The following list summarizes the circuit design recommendations made in this document:

- Keep the ROM TTL bus length short. Maximum length should be 10 inches before using termination techniques. (Chapter 1)
- Do not use tees (stubs) if you can avoid them. If you must use them, keep the tee length to under a quarter-inch. Keep the number of tees to a minimum. (Chapter 1)
- Use a single driver and a single receiver on a bus whenever possible; otherwise, keep the number to a minimum to reduce noise and reflections. (Chapter 1)
- Connect the output of one node (driver or receiver) directly to the input of another node. (Chapter 1)
- Design dedicated connectors on the target board to ensure more reliable connections than using adapters to plug the NetROM cables into PLCC or DIP memory sockets. For target PC boards, use a Fujitsu connector Part Number FCN-235P080-G/MA (for a right-angle connector) and Part Number FCN-234P080-G/MA (for a straight connector). The NetROM cable will plug into any of these connectors on your PC board. (Chapter 2)
- Use buffers to clean up noisy signals. If there are more than eight to ten nodes on a bus, add buffers to the bus. An example would be the buffer that NetROM uses as an input buffer, which is an IDT (Integrated Device Technology) 74FCT162244TPV. (Chapter 2)
- Use multilayer PC boards to reduce analog problems and provide more uniform impedance on the bus. Multilayer construction is especially useful on long-bus boards.

- ❑ Divide long buses into branches and add buffers to reduce noise, reflections and other analog problems. (Chapter 2)
- ❑ Terminate at both ends of a long bus to reduce reflections and increase performance. (Chapter 2)
- ❑ Connect NetROM at one end of the bus and not in its middle to reduce reflections. (Chapter 2)
- ❑ Use the command status connector to provide control functions to a target. Also use the command status write line when writing to NetROM if there is no write enable in the target's circuitry. (Chapter 5, Chapter 6)

Suggested reading

- ❑ *1993 IDT High-Speed CMOS Logic Design Guide*, Integrated Device Technology, Santa Clara, California, 1993
- ❑ Pace, Charles. "Terminate Bus Lines to Avoid Overshoot and Ringing." *Electronic Design News*, September 17, 1987
- ❑ Quinnell, Richard. "High-Speed Bus Interfaces." *Electronic Design News*, September 30, 1993
- ❑ Sterner, Rudy. "Guide to Designing with High-Speed CMOS ICs." *Electronic Design*, September 12, 1991

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