CIRCUIT DESCRIPTION

MS4620-A4
SOURCE/LO1 MODULE

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I. ABSTRACT

A4 generates the primary source signal and the first local oscillator signal for the instrument. The module contains voltage controlled oscillators, their phase lock circuitry, and circuitry for the various frequency bands and associated switched filter sections. The source output level is controllable via an ALC loop, whereas the LO1 output level is fixed. In addition to the source and LO1 RF outputs, the module also generates Common Offset & Heterodyne VCO signals to be used by the optional second source.

II. REVISION HISTORY

Rev 0	08/14/97	Initial draft
Rev 0.1	02/27/98	New method for level dip & additional AMON lines Table updates per pilot board changes
Rev 0.2	10/05/98	Update harmonic specifications

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III. SPECIFICATIONS

A. PCB INPUTS

1. **Microprocessor Board Control**
   16 data lines + 5 address lines + 5 boards select lines from the A1 Microprocessor Board via the motherboard (P1:17A - P1:30C)
2. **10 MHz Reference**
   coax from the A5 Receiver Module via MCX cable (J2)
3. **ALC Detector**
   coax from the A5 Receiver Module via MCX cable (J4)
4. **Group Delay Modulation**
   coax form the options board via MCX cable (J5)

B. PCB OUTPUTS

1. **Source RF Output**
   semirigid coax to the A5 Receiver Module via SMA cable (J7)
2. **First Local Oscillator RF Output**
   semirigid coax to the A5 Receiver Module via SMA cable (J6)
3. **Common Offset Output**
   coax to the A3 Optional Source Module via MCX cable (J1)
4. **Heterodyne Oscillator Output**
   coax to the A3 Optional Source Module via MCX cable (J3)
5. **Status Line**
   1 signal line to the A1 Microprocessor Board via the motherboard (P1:12C)
6. **Analog Monitor Line**
   1 signal line to the A5 Receiver Module via the motherboard (P1:12A)

C. ELECTRICAL (TYPICAL)

1. **RF Output**

   a) **Frequency Range**

(1)	Source Output	10 MHz to 3 GHz
(2)	LO Output	10 MHz to 3 GHz
(3)	Heterodyne Output	800-1600 MHz
(4)	Common Offset Output	800-1600 MHz

   b) **Power Level**

(1)	Source Output	> 20 dBm
(2)	LO Output	3 dBm +/- 3 dB
(3)	Heterodyne Output	3 dBm +/- 3 dB
(4)	Common Offset Output	3 dBm +/- 3 dB

2. **Source ALC**
   - a) **Voltage Input** -0.5 mV to -700 mV
   - b) **Flatness (leveled)** +/- 1 dB max.
   - c) **Resolution** 0.01 dB
   - d) **Power Sweep Range** -11 dBm to +20 dBm
3. **RF Output Signal Purity**
   - a) **Source Spurious @ +15 dBm Leveled Output Power**
     - (1) Non-harmonic spurs > 30 dBc
     - (2) Harm Generator OFF
       - (a) 1/2 Sub-harmonics > 37 dBc
       - (b) 3/2 Sub-harmonics > 33 dBc
       - (c) All other harmonics > 30 dBc
     - (3) Harm Generator ON
       - (a) 2^{nd} & 3^{rd} Harmonic < 45 dBc
   - b) **LO1 Spurious Signals** > 30 dBc
   - c) **LO Integrated Power, 50 MHz-3 GHz**
     - (1) 25 ± 4 MHz from carrier < -80 dBm
   - d) **Phase Noise, 10 KHz from Carrier**
     - (1) 10-400 MHz 77 dBc/Hz
     - (2) 400-800 MHz 86 dBc/Hz
     - (3) 800-1600 MHz 80 dBc/Hz
     - (4) 1600-3000 MHz 74 dBc/Hz
4. **Frequency Resolution** 1 Hz
5. **Group Delay Modulation Input**
   - a) **Modulation Sensitivity** TBD MHz/Volt

IV. FUNCTIONAL DESCRIPTION

A. DIGITAL INTERFACE

All modules in the instrument share the same bus connections to the microprocessor via the motherboard. The common data and address bus consists of 16 data bits, 5 address lines, and 5 board select lines. Within the Source/LO1 module, a programmable logic device (U43) decodes the incoming address and board select lines to direct data between the bus and internal module latches. Transceivers (U45 & U47) are used to buffer the common 16-bit data bus from a data bus internal to the module. When a latch located on the module is addressed, the transceivers will be enabled to allow the transfer of data to/from the internal data bus.

B. MAIN OSCILLATOR LOOPS

The Source and LO1 RF outputs are both generated by voltage controlled oscillators (VCOs) that nominally span 800-1600MHz. Y6 and Y5 are the VCOs for the Source and LO1, respectively. The outputs of the VCOs are processed to ultimately produce the final outputs of the module. Hence, these

oscillators are dubbed the "Source Main" and "LO1 Main" VCOs. The outputs of the main oscillators are sampled and fed back in order to be phase-locked to the system reference 10 MHz. The implementation of the phase locking circuitry for the Source and LO1 VCOs are essentially.

When phase locking the main oscillator, the VCO is mixed with an offset oscillator to produce a lower frequency signal (typically in the 6-9 MHz range). The product from the mixer is input to a phase detector and is compared against a signal produced by a direct digital synthesis (DDS) IC. The phase detector (U74 for the source and U10 for LO1) output is fed into a loop filter, which supplies the tuning voltage for the VCO.

The Analog Devices AD9850 DDS (U58 for the source and U14 for LO1) has 32 bits for frequency programming. As a result, finer than 1 Hz resolution is achievable. The resolution of the DDS is transferred to the main VCO output signal. Programming requirements of the DDS are discussed later in the document (Section V.E).

C. OFFSET OSCILLATOR LOOPS

The offset oscillators used by the source and the LO1 are also 800-1600 MHz VCOs. The VCOs (Y4 for the source and Y1 for the LO1) are phase-locked to the system 10 MHz reference (f_{ref}) using a PLL IC. The PLL IC used in the module is the National LMX2325 Serial Input PLL Frequency Synthesizer. The PLL IC integrates two programmable dividers, a prescaler and a phase/frequency detector. The circuitry used to lock up the Source Offset oscillator is reproduced for the LO1 Offset VCO. The PLL IC used for the Source Offset loop is U56, while the LO1 Offset PLL IC is U21.

For a given frequency, the outputs of the two dividers are programmed to 625 KHz. Programming of the PLL IC is described in Section V.D below. The phase detector compares the divided-down signals and issues a current pulse from the internal charge pump if a correction is needed. Current pulses from the PLL IC are integrated by the loop filter and used to develop the tuning voltage for the Offset VCO.

Note that the tuning sensitivity at the PLL IC output is very high. The tuning sensitivity at the VCO input is approximately 50 MHz/V, and the loop amplifier has a gain of 4. The effective sensitivity at the PLL output is in the order of 100 MHz/V. Any noise injected at this point, has noticeable affects on the output noise characteristics.

D. DDS REFERENCE CLOCK

In order to generate precise DDS frequencies, an accurate reference clock must be provided to the DDS IC's. 32-bit wide phase accumulators enable the DDS to achieve minimum resolutions of:

$$\Delta F_{min} = \frac{F_{CLK}}{2^{32}}$$

By phase locking the DDS reference clock VCXO (Y3) to 26.8435456 MHz, the resulting minimum resolution is 0.00625 Hz.

To obtain the precisely needed VCXO frequency, a third DDS is used to lock the oscillator to the system 10 MHz. The third DDS IC uses the VCXO as its clock, and is programmed to output 100 KHz. The system reference is divided down to 100 KHz and is compared against the DDS output. Only when the clock is exactly 26.8435456 MHz, will the programmed DDS produce a phase locked 100 KHz. The phase detector (U31) feeds back to the VCXO tuning line.

E. BOUNDING CIRCUITRY

The mixing of the main and offset signals produces both an additive as well as the desired subtractive product. Therefore, there is the potential that the main oscillator loops will try to lock on to the wrong signal. To prevent locking up on the wrong side, additional LMX2325 PLL ICs are wrapped around the

main loop phase detector as bounding circuits. The proper polarity in the loop requires that the main oscillator always be lower in frequency than the offset oscillator.

The upper bound PLL is programmed using the offset VCO frequency. When the main VCO goes higher in frequency than the offset VCO, a correction pulse is generated that is fed into the main oscillator loop. This magnitude of the correction pulse is large enough to push the main VCO to the right side.

In addition to being prevented from swinging too high, the main VCO must also be bounded on the low end. For decreasing main VCO frequencies, the difference frequency increases. However, the mixer possesses a limited bandwidth. When the bandwidth is exceeded, the output response drops off and the difference frequency will appear to decrease. As a result, it will seem as though the main VCO is too high in frequency, instead of too low. The loop will be unable to lock itself up. The lower bound PLL issues a correction pulse to push the main VCO higher in frequency when the bound is exceeded.

Both the source and the LO1 main VCO loops incorporate bounding circuits. For the source, U71 is the lower bound PLL and U72 is the upper bound PLL. For the LO1, U2 serves as the lower bound PLL and U3 is the upper bound PLL. When the main VCO is within an acceptable range, there is no contribution from the bounding circuits. The PLL ICs used for the bounding circuits are the same components used in the offset VCO loops.

F. SPEED-UP CIRCUITRY

In addition to phase-lock and bounding circuitry, there is also circuitry to help speed the locking of the loop. The settling time of the main loop and its phase detector is very slow. U83 acts as an additional frequency lock detector and emits pulses to help get the source main VCO locked on frequency quicker. U1 performs the same duty for the LO1 main VCO. Once the desired frequency is reached, the speed-up circuits discontinue and the normal phase lock circuitry locks up the loop the rest of the way. In this way, the loop locking occurs more rapidly, but the stability of the loop is not compromised.

However, for this speedup to work, the polarity of the loop must be correct. If on the wrong side, then the speedup circuitry only acts to push the VCO farther off frequency, even faster. Thus a hierarchy of control must be established. The bounding correction circuits must be strong enough to counter the contribution of the speedup circuits, but should not be so strong that the loop ends up banging back and forth between its two extremes.

G. FREQUENCY BANDS & SWITCHED FILTERS

Although the main oscillator produces an output of 800-1600 MHz only, the module output frequency spans 10-3000 MHz. There are four distinct bands of operation to achieve the desired frequency range. If the desired output frequency is between 10-400 MHz, the circuit is in the Heterodyne Mode. The VCO output is mixed down with the Heterodyne oscillator (typically 1200 MHz). Passing the VCO output through a Divide-by-2 circuit produces frequencies between 400-800 MHz (Divider band). For 800-1600 MHz (Thru Band), the VCO signal passes directly. Finally, to achieve 1600-3000 MHz (x2 Band), a doubler is used.

To improved harmonics and spurious performance of the output signals, they are passed through various switched filter sections. A given frequency mode (Heterodyne, Divider, Thru, or x2) may have one or more switched filter band sections. The switching for the frequency generation modes is combined with the control for the switched filter section. Table 4 shows the control bits for the source and LO1. The selection of frequency and switched filter band is decoded by U43.

H. HETERODYNE OSCILLATOR

The Heterodyne oscillator is used to mix with the main VCO outputs of the source and LO1 to generate frequencies less than 400 MHz. This VCO (Y2) is the same type as that used for the main and offset loops. The VCO has an 800-1600 MHz range, but will typically be tuned to 1200 MHz. The main VCO is tuned higher than the fixed heterodyne oscillator. As a result, positive steps in system frequency will translate to positive steps in the main VCO. Lock times of the loops were optimized in a manner that positive frequency steps locked up quicker than negative frequency steps.

To avoid mixing spurs, the heterodyne VCO may be tune away from the nominal 1200 MHz. The VCO is allowed to step down as far as 900 MHz. The circuitry for the phase locking of this heterodyne oscillator is similar to the offset VCO locking and utilizes the integrated PLL ICs. The heterodyne VCO signal is also output from the module. It is supplied to the A3 Optional Source Module for use in its heterodyne mode.

I. ALC CIRCUITRY

The source side differs from the LO1 side primarily in its ability to have controllable output power. The feedback from a level detector located on the Receiver Module controls the level of the source output. The level of the signal can be controlled over at least a 20dB range. In the ALC circuitry, the Power Level DAC (U75) is set to a calibrated value for a desired power level. The ALC loop then controls a modulator (U97). The level of the source is adjusted until the detector output matches the reference voltage.

Once installed into a system, calibration of the Source ALC loop may be performed. In general, Source is tuned to a fixed frequency, while the port output level is adjusted to 0dBm. The Power Level DAC is stepped as the port output is monitored with a power meter. The power level at the port is dependent not only on the source output power itself, but also upon the losses through various components in the RF deck. The results are then used to curvefit an equation that relates DAC values to port power. For a 3 GHz system, the measurements are performed at 1 GHz. If the system is a 6 GHz unit, the measurements are performed both at 1 GHz and 4 GHz.

It was found that the overall shape of the power curve did not change much with frequency, only the offsets. Therefore the same curvefit equations could be used with a correction for the different offsets at various frequencies. The offsets for different frequency steps are stored in a table and intermediary frequencies are interpolated. The curvefit equation calculated using 1 GHz data is applied for system freqs < 3 GHz, and the 4 GHz curvefit equation is used in doubler band (i.e. freqs > 3 GHz). To generate the offset table, the power DAC is set to "0dBm port power" using the appropriate curvefit equation and then the resulting error is measured.

Additionally, a shaper cal DAC calibration is performed when the system is a 6 GHz unit. The shaper DAC (U76) circuit helps compensate for the non-linear characteristics of the doubler.

At band switch points, the source takes longer to settle. During the settling period, there is a lack of RF signal to the ALC diode and thus the ALC circuitry will rail the output power higher. Therefore, the ALC is "level-dipped" at band switch point to prevent large power spikes from hitting the DUT during these transition periods. The level dip is performed by switching in a fixed voltage into the loop to fool the circuitry into believing that source power is present. Level dips are triggered by a single bit, Latch A3_BS4, Bit D0.

J. OPERATION MODES

1. COMMON OFFSET MODE

Traditionally, the source and LO1 output signals are generated independently. An alternative mode of operation is possible where the LO1 Offset VCO also locks up the source loop. U57 is switched so that

the LO1 Offset is fed into the Source Main mixer U60. Also, the Source Offset VCO (Y4) bias will be disabled. The DDS outputs on the two sections then make up the frequency difference between the two outputs. Sharing a common offset VCO allows the two RF signals to better track each other. The resulting IF has improved phase noise, because much of the offset VCO noise is ratioed out.

In addition to cleaner IF signals, the Common Offset Mode allows faster sweeping of the instrument. To make accurate measurements, the IF must be settled before the DSP processing is triggered. When operating in Common Offset Mode, the IF settles faster. Even though the offset VCO (and therefore the main VCOs) may still be slewing in phase, the IF itself may already be settled because the Source and LO1 are tracking. The two main VCO are able to track the offset VCO settling because of their higher bandwidths. Therefore, measurements can be made sooner in the Common Offset Mode, and overall system speed is thus faster.

However, the Common Offset Mode is only permitted when the Source and LO1 frequencies are relatively close. The range of the DDS limits the frequency difference of the two main VCO. Additionally, the Source and LO1 must be operating in the same frequency band. High-IF frequency measurements, such as Wide-Band Noise Figure must operate in the independent offset mode. However, Common Offset Mode is beneficial for typical S-parameter measurements where speed is an important parameter.

In Common Offset Mode, the Source Offset loop lock indicator will show an "unlocked" state. However, since it is undesirable to have the Status line pulled LOW, the offset lock indicator is disabled from line.

2. HARMONIC GENERATOR MODE

In most measurements, the presence of harmonics on the source RF is undesirable. However, in order to improve accuracy of the harmonic measurement application, a reference signal is needed at the receiver frequency. The 2nd and 3rd harmonics of the source are used, and therefore must be of significant enough level to be measured accurately. A harmonic generator diode (CR32) can be switched into the circuit to increase the harmonics to levels typically above 30 dBc. Without the harmonic generator, the harmonics would often be lower than 45 dBc.

3. GROUP DELAY MODE

This mode has yet to be implemented. However, for future implementation of this option, a switched input path has already been incorporated. A group delay modulation signal can be routed into the main source loop via J5. The signal is summed in at the loop filter and can be used to modulate the frequency of the source output.

K. DATA READING

The Analog Monitor output routes one of ten monitored test points out to the A5 Receiver Module. These test voltages are used for diagnostics, calibration and self-test. The test voltages measured on the Analog Monitor output line are typically 1/11th of their actual amplitude. The signal is passed through a voltage divider in order to avoid overloading the switch. Diagnostic voltages related to ALC are first multiplexed with switch U120, and then its output line is fed into the primary Analog Monitor switch U35.

The module also possesses a readback latch that can be polled to discover the status of the module. Each phase-lock loop on the board has a dedicated bit to monitor its "lock" condition. Also, a bit is used to indicate whether the ALC loop is leveled or unleveled. Additionally, there is a loopback bit that can be addressed to verify proper communication with the module. Refer to Table 7, page 13 for a definition of the readback latch bits.

For quick feedback on the lock condition of the module, the Status output line can be monitored. If any of the loops are unlocked or if the power is unleveled, the status line will be pulled LOW. The frequency lock indicator is also diode-OR'ed onto the status line. Because of the slower response times of the phase lock loop indicator circuits, a small frequency step may not register an unlocked state. However, the frequency lock indicators are much quicker and will act to pull the status LOW. To ensure that the Status line goes LOW for every frequency step, the LLOAD line is also put onto the Status line.

V. MICROPROCESSOR INTERFACE

A. DATA LOADING

Refer to Table 1, Page 12 for a description of the various latches on this module. The reference number, title and address bits of the latches are listed. The required data bits for frequency programming are defined in Table 2, Page 12.

B. FREQUENCY BAND AND FILTER CONTROL LINES

The U43 PLD not only serves as the module's address decodes, but it also generates the appropriate driver lines for the different bands and switched filter sections. The control lines for the various band switching and mode controls are defined in Table 3, Page 12.

C. ANALOG MONITOR PROGRAMMING

Table 6, page 13 lists the appropriate data bits required to select a particular test voltage. Since the analog monitor line output to the common system bus, care needs to be taken to prevent contention on the line. Therefore, the Analog Monitor Latch data bits should all be initialized LOW at powerup.

D. PLL IC PROGRAMMING

A three-wire interface is used to serially input data into the National LMX2325 PLL IC. The *DATA* line carries the actual programming bits, which are input to the internal shift registers on the rising edge of the *CLK* (clock) input. The stored data is transferred into latches for the programmable dividers when the *LE* (load enable) pin is HIGH, which is triggered by the LLOAD pulse. The last bit of a programming word will always be a control bit, which designates which of the programmable dividers is being addressed. If the control bit is HIGH, then the data is sent to the 15-bit shift register for the reference divider. If the control bit is LOW, then the data is sent to the 18-bit programmable internal shift register.

The 15-bits of data sent for the reference divider actually consists of 14-bits for the reference (R) divide ratio and 1 bit to indicate the prescaler mode. If the first bit (*SW*: prescaler select bit) is LOW, then the prescaler operates in the 64/65 mode. A HIGH setting for *SW* places the prescaler in the 32/33 mode. For the Scorpion source module, a 32/33 prescaler mode is desired. The remaining 14-bits are used to program the reference divider between 3 and 16383 (most significant bit first).

The reference divide ratio, R, can be calculated:

$$R = \frac{f_{REF}}{f_{PD}}$$

where f_{PD} is the phase detector frequency and f_{REF} is the reference signal frequency,

The programmable divider is specified by 18-bits of data. Two counters are programmed: an 11-bit programmable N-counter and a 7-bit swallow A-counter. The most significant 11-bits program the N-counter to a value between 16 and 2047. The remaining 7-bits program the A-counter between 0 and 127.

The VCO input divide ratio, *K*, is obtained by programming the *N*-counter and *A*-counter.

$$K = (P * N) + A$$

where P is either 32 or 64 depending on the prescaler mode selected. For the Scorpion Source/LO1 Module, a value of 32 is used.

The values of N and A are then calculated given a desired K.

$$N = \text{int}\left(K / P\right)$$

$$A = K - \left(P * N\right)$$

All of the PLL IC's on the module are programmed simultaneously. Each PLL IC receives its DATA line input from a designated bit on Latch A0_BS4. This single latch is addressed repeatedly to generate the required serial stream of data. Table 2, Page 12 identifies each PLL IC and its dedicated data bit.

E. DDS PROGRAMMING

The DDS chip used in the module is the Analog Devices AD9850 DDS/DAC Synthesizer. The DDS IC requires an input reference clock and then the output frequency can be controlled via a 32-bit tuning word. The actual output frequency of a DDS function is determined by the following equation:

$$F_{DDS} = \left(\frac{F_{CLK}}{2^{32}}\right) * P$$

where *P* is the value programmed to the phase accumulator.

Solving for *P* yields:

$$P = 2^{32} * \left(\frac{F_{DDS}}{F_{CLK}}\right) = 160 * F_{DDS}$$

Thus, to realize frequency steps of 1 Hz, *P* increases in steps of 160.

The output phase of the DDS signal can be controlled by an additional five bits. To program the DDS chip, five iterative loads of an 8-bit word are required. The first byte contains the phase modulation bits, power-down enable bit, and two bits to indicate the loading format (parallel vs. serial). The next four bytes contain the 32-bit frequency tuning word, with the MSB byte loaded first. Each phase increment register is double buffered so that increment used by the phase accumulator is unaffected by a new phase increment value until a LLOAD pulse is received.

On power-up, the DDS chips need to be reset. There are certain data codes that are unallowable, and may put the DDS IC in an invalid test state. Since there is no way to ensure what is loaded into the registers upon power up, care must be taken to ensure that valid information is presented to the registers. A master reset bit [Latch A4_BS4, Bit D4] controls the signal to a hard-wired reset of the DDS IC's. When the master reset bit is set high, the DDS all internal registers are cleared, but the input registers are not. So, to ensure valid data for the DDS to operate on, the programming information for the frequency is loaded into the registers prior to issuing the first LLOAD pulse.

F. MODES CONTROL

1. Common Offset Mode

As indicated in Table 3, Page 12, the Common Offset Mode is toggled with a single bit [Latch A4_BS4, Bit D7]. A setting of HIGH will enable the mode.

2. Harmonic Mode

As shown in Table 3, Page 12, the Harmonic Mode is toggled with a single bit [Latch A3_BS4, Bit D5]. A LOW setting will enable the harmonic generator.

3. Group Delay Mode

In Table 3, Page 12, it can be seen that Group Delay Mode is toggled with a single bit [Latch A3_BS4, Bit D7]. A LOW setting will enable the modulation drive input switch.

VI. PERFORMANCE VERIFICATION

Refer to Scorpion Component Test Plan document for Primary Source/LO & Option Source

VII. TABLES

A. Table 1: Latch Addresses

No.	LATCH TITLE	A4	A3	A2	A1	A0	LBS4
A0_BS4	PLL Control	0	0	0	0	0	0
A1_BS4	Ref Clock DDS Control	0	0	0	0	1	0
A2_BS4	Source Status Read	0	0	0	1	0	0
A3_BS4	Mode Control	0	0	0	1	1	0
A4_BS4	Analog Monitor	0	0	1	0	0	0
A13_BS4	Src1/LO1 DDS Control	0	1	1	0	1	0
A14_BS4	Src1/LO1 SF Band & Shaper	0	1	1	1	0	0
A15_BS4	Src1 Power Level DAC	0	1	1	1	1	0

B. Table 2: Programming Data

FUNCTION	# BITS	LATCH NO	DATA
Src1 Offset PLL IC Data Bit	1	A0_BS4	D0
Src1 Lower Bound PLL IC Data Bit	1	A0_BS4	D1
Src1 Upper Bound PLL IC Data Bit	1	A0_BS4	D2
LO1 Offset PLL IC Data Bit	1	A0_BS4	D3
LO1 Lower Bound PLL IC Data Bit	1	A0_BS4	D4
LO1 Upper Bound PLL IC Data Bit	1	A0_BS4	D5
Heterodyne PLL IC Data Bit	1	A0_BS4	D6
Source1 Reference Clock DDS Program	8	A1_BS4	D0-D7
Source1 DDS Program Data	8	A13_BS4	D8-D15
LO1 DDS Program Data	8	A13_BS4	D7-D0
Source1 Shaper DAC Control	8	A14_BS4	D8-D15
LO1 Switched Filter Band Control	3	A14_BS4	D5-D3
Source1 Switched Filter Band Control	3	A14_BS4	D2-D0
Source1 Power Level DAC Program	16	A15_BS4	D15-D0

C. Table 3: Mode Control Lines

FUNCTION	1	0	LATCH NO	DATA
Source1 Level Dip	disable	enable	A3_BS4	D0
Source1 Fixed Gain Mode	disable	enable	A3_BS4	D1
Source1 ALC Level Loop Cntrl	open	closed	A3_BS4	D2
Source1 Level Status Indicator	enable	disable	A3_BS4	D3
Source1 Speedup Circuits	enable	disable	A3_BS4	D4
Source1 Harmonic Mode	disable	enable	A3_BS4	D5
LO1 Speedup Circuits	enable	disable	A3_BS4	D6
Group Delay Mode	disable	enable	A3_BS4	D7
Source1/LO1 DDS Reset	reset	normal	A4_BS4	D4
Heterodyne Oscillator Circuits	disable	enable	A4_BS4	D5
Source1 Common Offset Mode	enable	disable	A4_BS4	D7

D. Table 4: Primary Source Switched Filter Control Lines (A14_BS4)

FREQUENCY BAND	D2	D1	D0
10 - 400 MHz	0	0	0
400-565 MHz	0	0	1
565-800 MHz	0	1	0
800-1131 MHz	0	1	1
1131-1600 MHz	1	0	0
1600-1960 MHz	1	0	1
1960-2600 MHz	1	1	0
2600-3000 MHz	1	1	1

E. Table 5: LO1 Switched Filter Control Lines (A14_BS4)

FREQUENCY BAND	D5	D4	D3
10 - 400 MHz	0	0	0
400-565 MHz	0	0	1
565-800 MHz	0	1	0
800-1600 MHz	0	1	1
1600-1960 MHz	1	0	1
1960-2600 MHz	1	1	0
2600-3000 MHz	1	1	1

F. Table 6: Analog Monitor Control Lines (A4_BS4)

MONITOR VOLTAGE	D6	D3	D2	D1	D0
Source Offset VCO Tuning	0	1	0	0	0
Source Main VCO Tuning	0	1	0	0	1
LO1 Offset VCO Tuning	0	1	0	1	0
LO1 Main VCO Tuning	0	1	0	1	1
Assembly ID	0	1	1	0	0
Heterodyne VCO Tuning	0	1	1	0	1
ALC Level Amplifier	0	1	1	1	0
ALC Log Amplifier	0	1	1	1	1
Power Level DAC	1	1	1	1	0
ALC Modulator Drive	1	1	1	1	1

G. Table 7: Read back Latch Bits (A2_BS4)

FUNCTION	DATA
Source1 Offset Loop Lock	D0
Source1 Main Loop Lock	D1
LO1 Offset Loop Lock	D2
LO1 Main Loop Lock	D3
Heterodyne Loop Lock	D4
DDS Reference Clock Lock	D5
Source1 ALC Leveled	D6
Source1/LO1 Module Loopback	D7