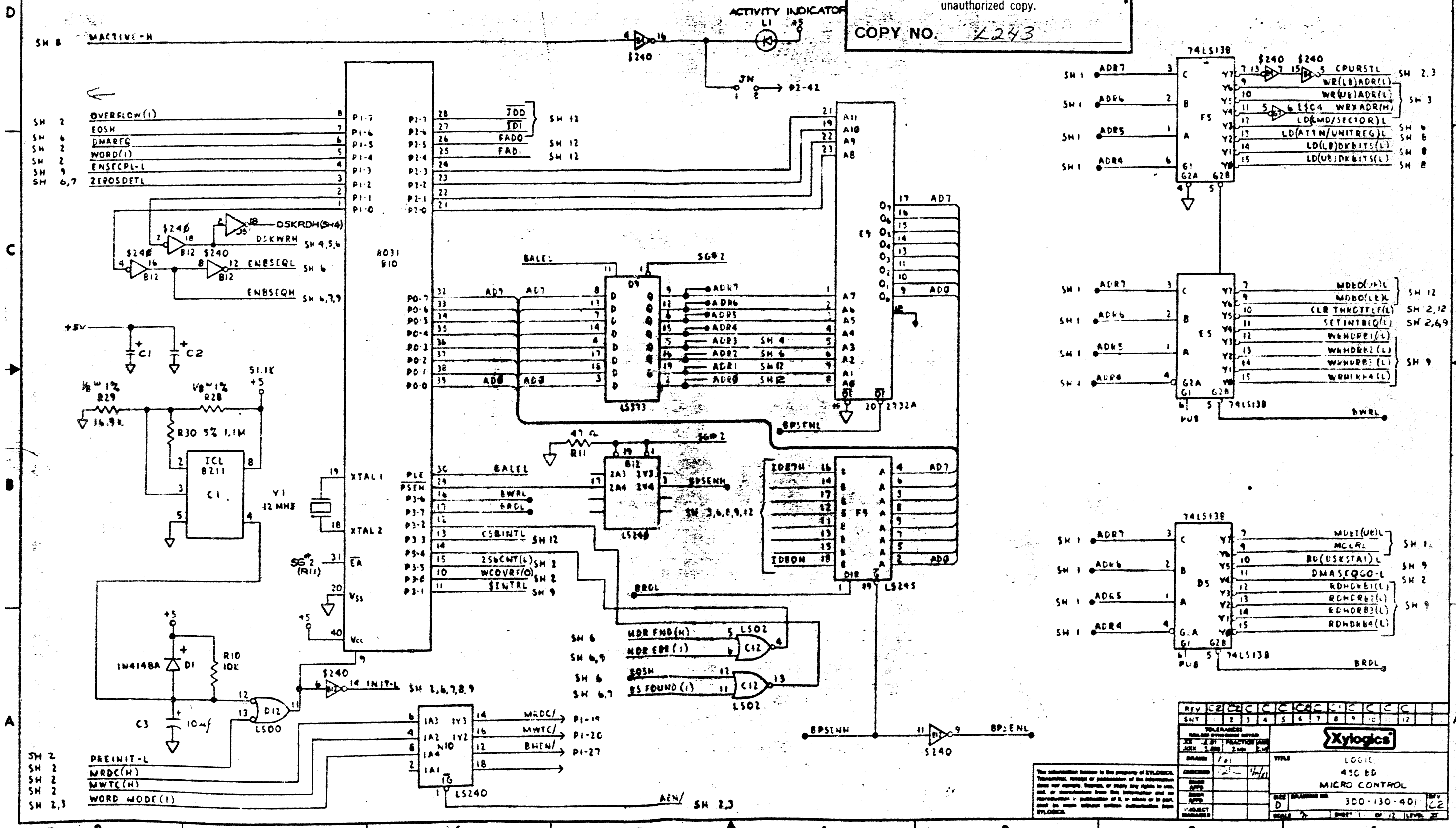


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ZONE	REV	DESCRIPTION	DATE	APPROVED
A	1189		11 SEP 68	DAVE
B	1182		24 SEP 68	DAVE
C	1169		26 JUN 68	DAVE
CI	1174		3 JUL 68	DAVE
CE	1186		12 FEB 69	DAVE



REV	1	2	3	4	5	6	7	8	9	10	11	12
CHKD												
APPD												
TEST												
INSTR												
MANAGER												

**XYLOGICS**

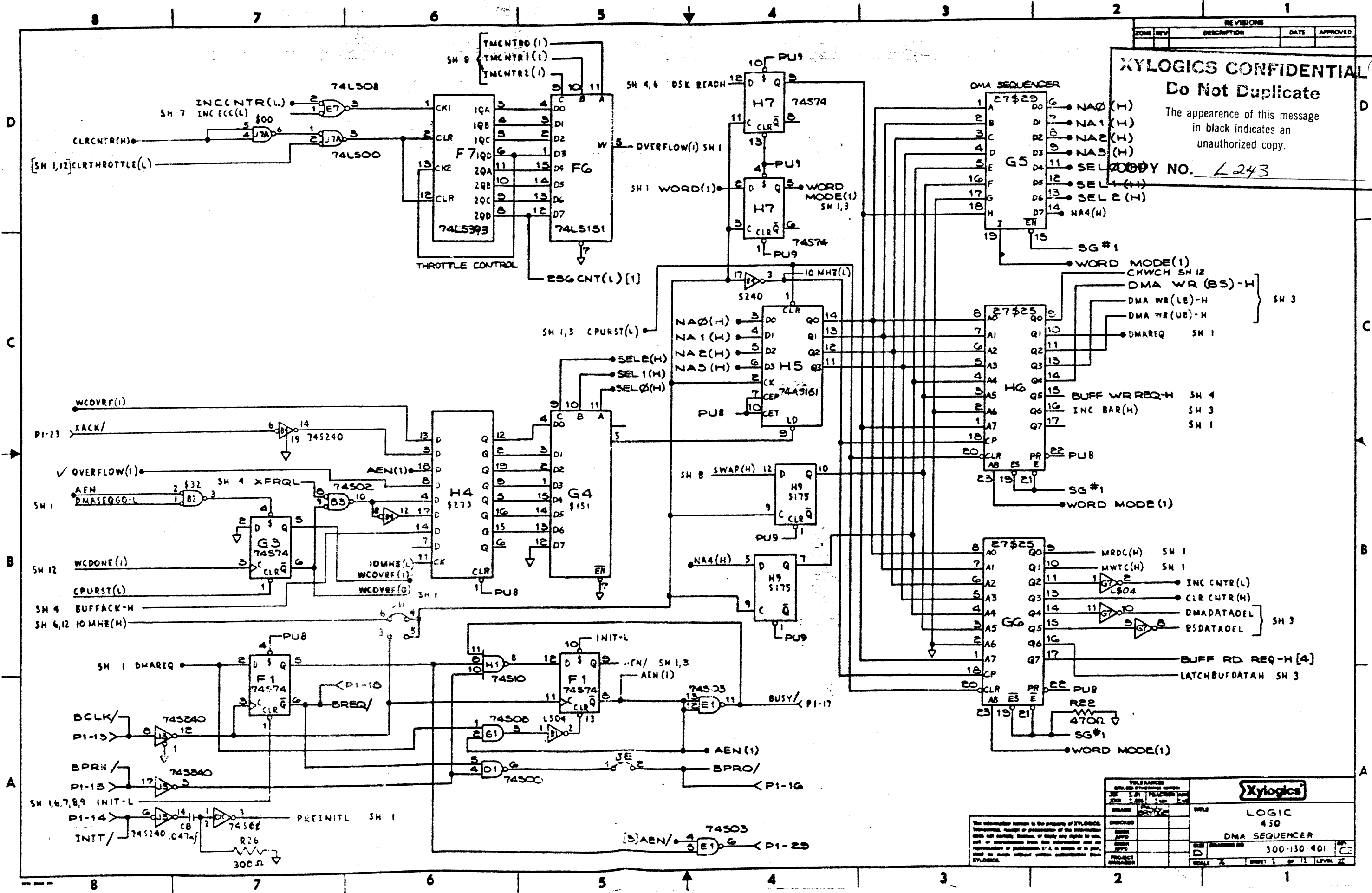
LOGIC  
45C 6D  
MICRO CONTROL

300-130-401

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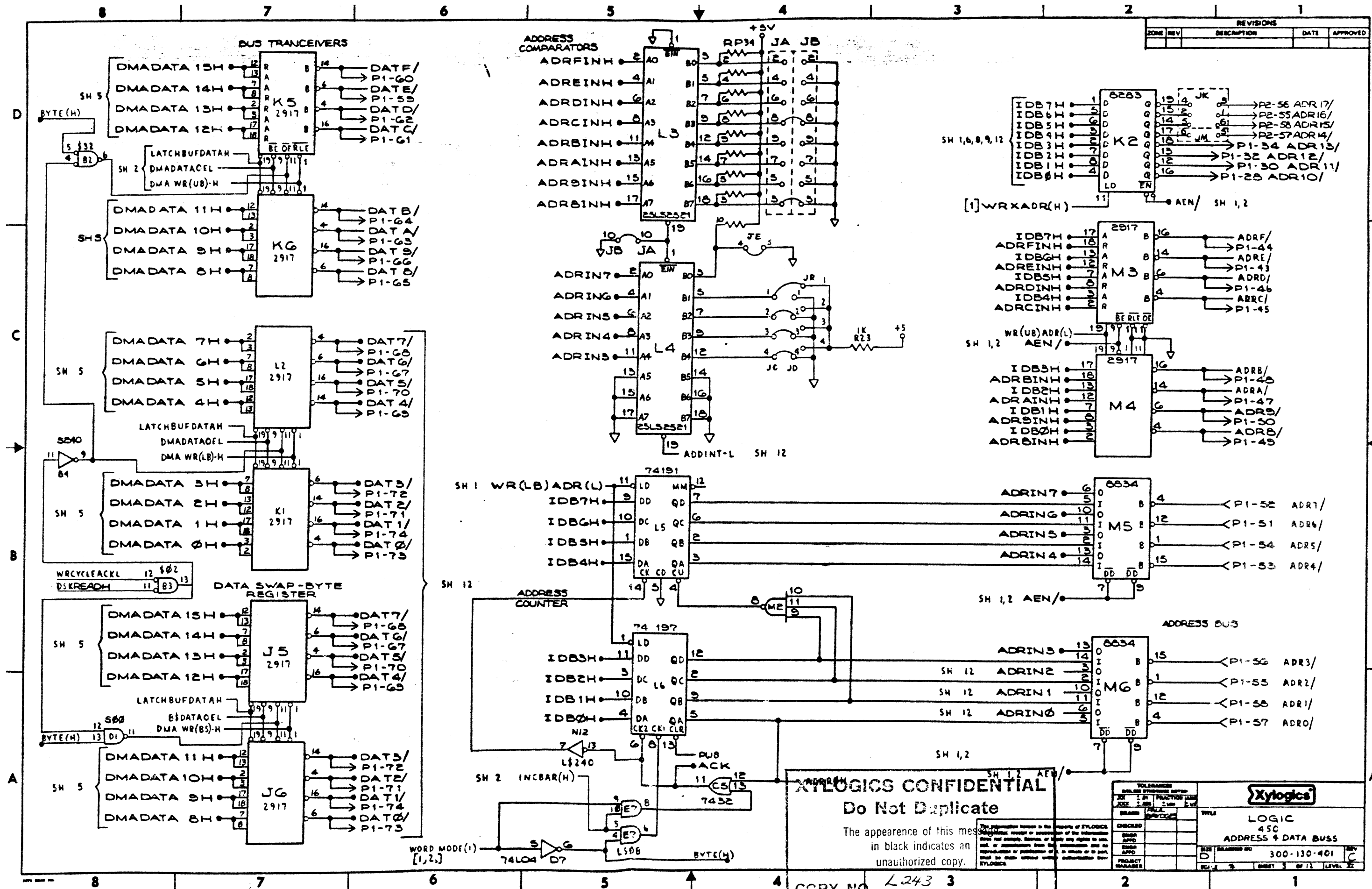
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TOLERANCES UNLESS OTHERWISE SPECIFIED		WFL	LOGIC	450	DMA SEQUENCER
RES	FIL				
±1%	±1%				
±5%	±5%				
±10%	±10%				
±20%	±20%				
±50%	±50%				
±100%	±100%				

REVISIONS				
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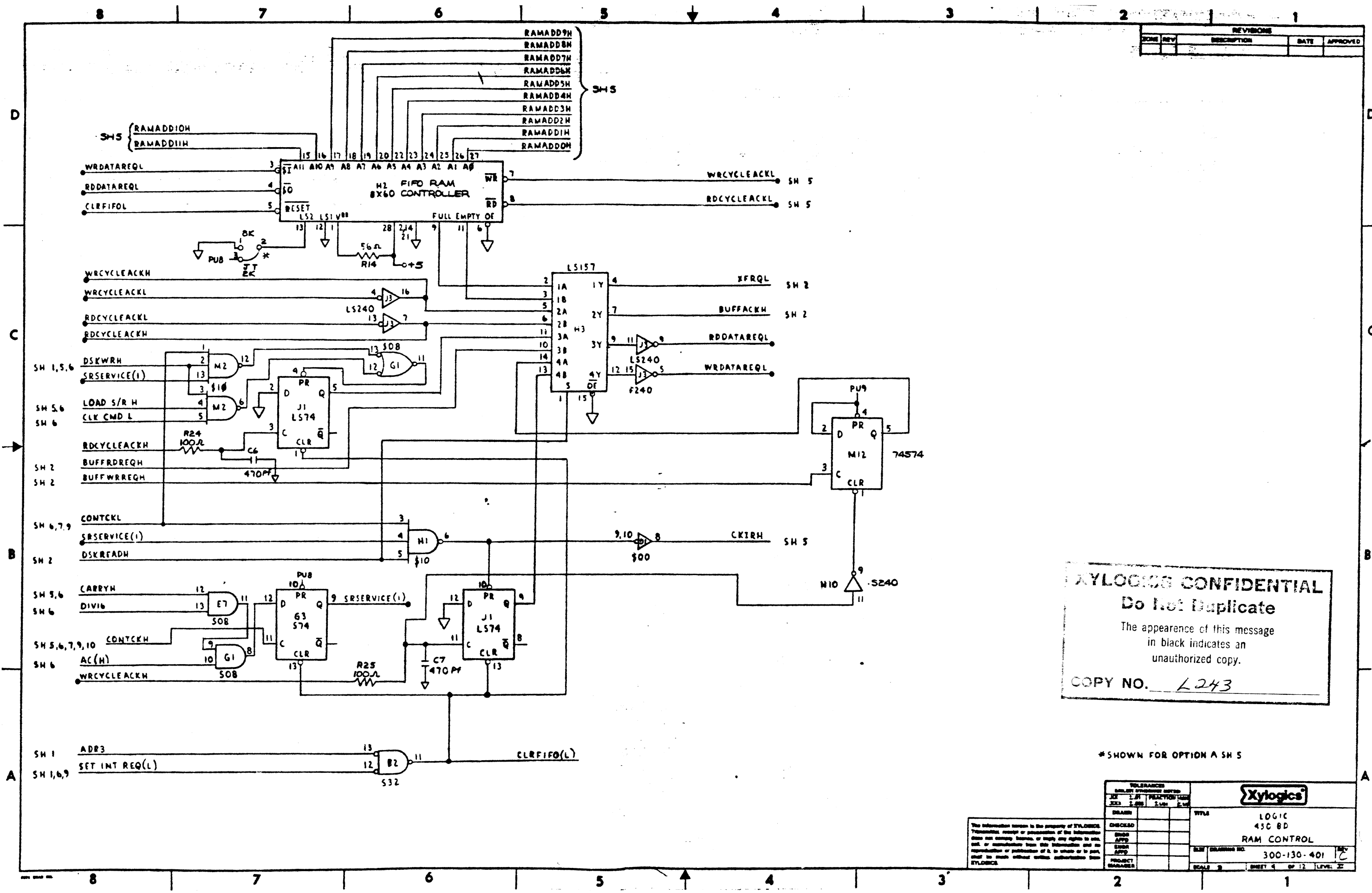
VOLUNTARILY DECLASSIFIED BY: 10/13/00		DATE: 10/13/00	
CLASSIFIED			
EXEMPT			
EXEMPT			
PROJECT			
MANAGER			

WFLC  
LOGIC  
450  
ADDRESS & DATA BUSS

300-130-401  
300-130-401  
300-130-401

COPY NO L243 3

REVISIONS				
DATE	REV	DESCRIPTION	DATE	APPROVED

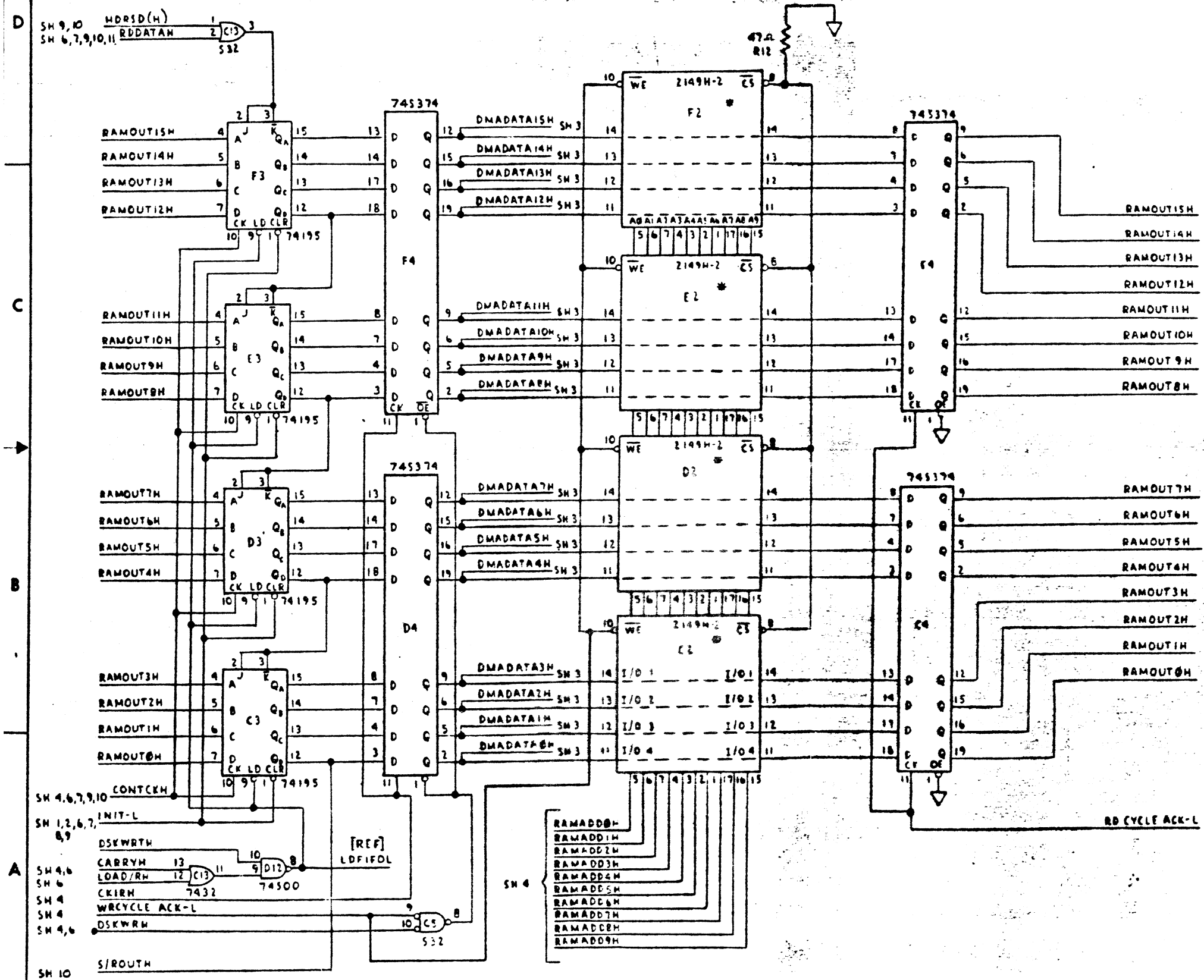


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\* SHOWN FOR OPTION A SH 5

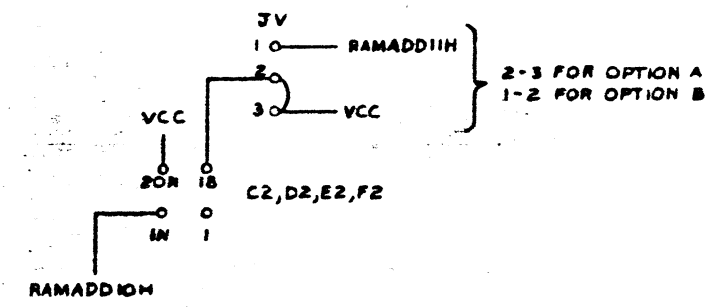
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PROJECT MANAGER DATE DRAWN CHECKED DESIGNED	PROJECT NO. SHEET NO. OF 12 LEVEL 2C		

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



**OPTION A**  
 FOR 1K X 16 BUFFER LOGICS ARE AS SHOWN  
 [LOCATIONS C2, D2, E2 AND F2 WILL CONTAIN  
 2149H-3 PARTS WHICH ARE 18 PIN IC'S]

**OPTION B**  
 FOR 4K X 16 BUFFER LOCATIONS C2, D2, E2 AND  
 F2 WILL CONTAIN EITHER 1M51420-55 OR  
 MBB160-55 PARTS WHICH ARE 20 PIN IC'S



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SH 9,10 HDRSD(H)  
 SH 6,7,9,10,11 RDDATAH

SH 4,6,7,9,10 CONTCKH  
 SH 1,2,6,7,8,9 INIT-L  
 SH 4,6 DSKWRH  
 SH 6 CARRYH  
 SH 4 LOAD/RH  
 SH 4 CKIRH  
 SH 4 WR CYCLE ACK-L  
 SH 4,6 DSKWRH  
 SH 10 S/ROUTH

RAMADD0H  
 RAMADD1H  
 RAMADD2H  
 RAMADD3H  
 RAMADD4H  
 RAMADD5H  
 RAMADD6H  
 RAMADD7H  
 RAMADD8H  
 RAMADD9H

SH 4

DESIGNER				DATE			
NO.	REV.	DESCRIPTION	DATE	NO.	REV.	DESCRIPTION	DATE

WYLE LOGIC  
 45C 60  
 RAM BUFFER

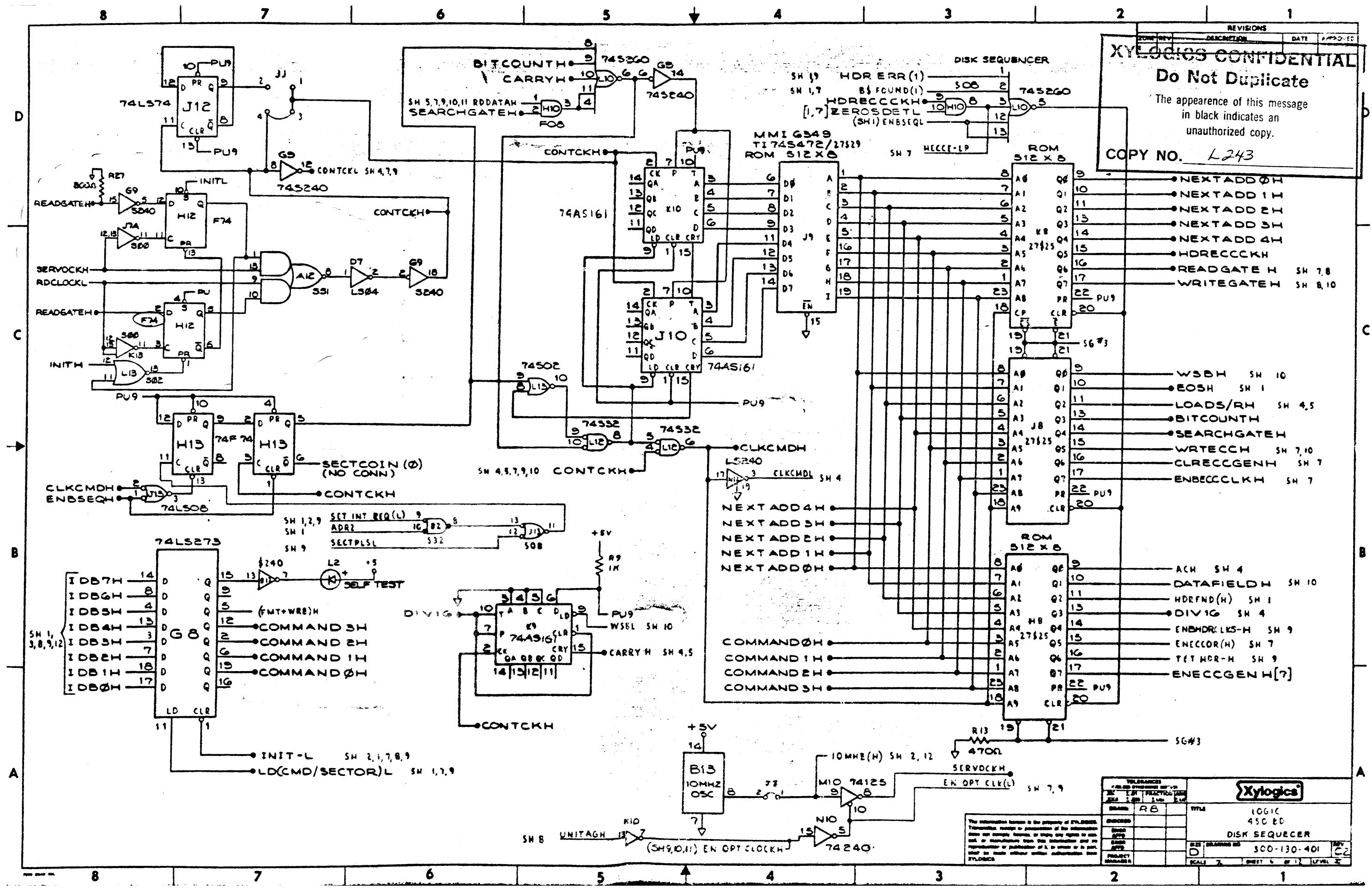
300-130-40

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TOLERANCES			
RES	IND	PACTIC	VAL
RES	IND	PACTIC	VAL
RES	IND	PACTIC	VAL
RES	IND	PACTIC	VAL
RES	IND	PACTIC	VAL

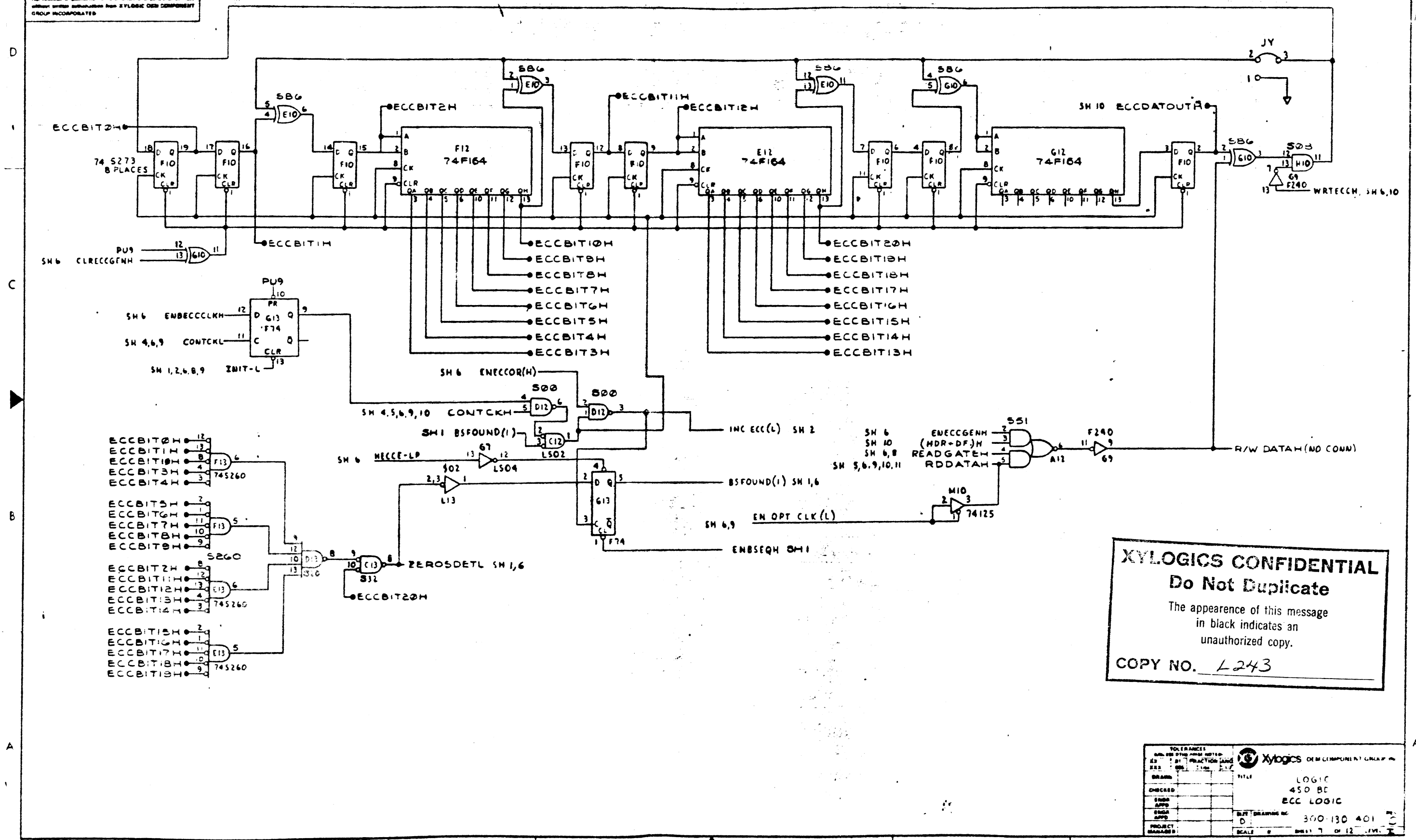
  

Xylogics		TITLE: LOGIC 450 ED	
DISIGNED: RB		PROJECT MANAGER: 300-130-401	
DRAWN: RB		SCALE: 1:1	
CHECKED: RB		SHEET 6 OF 11 LEVEL 2	
DATE: 10/1/78		BY: C2	



REVISIONS			
ZONE	REV	DESCRIPTION	DATE

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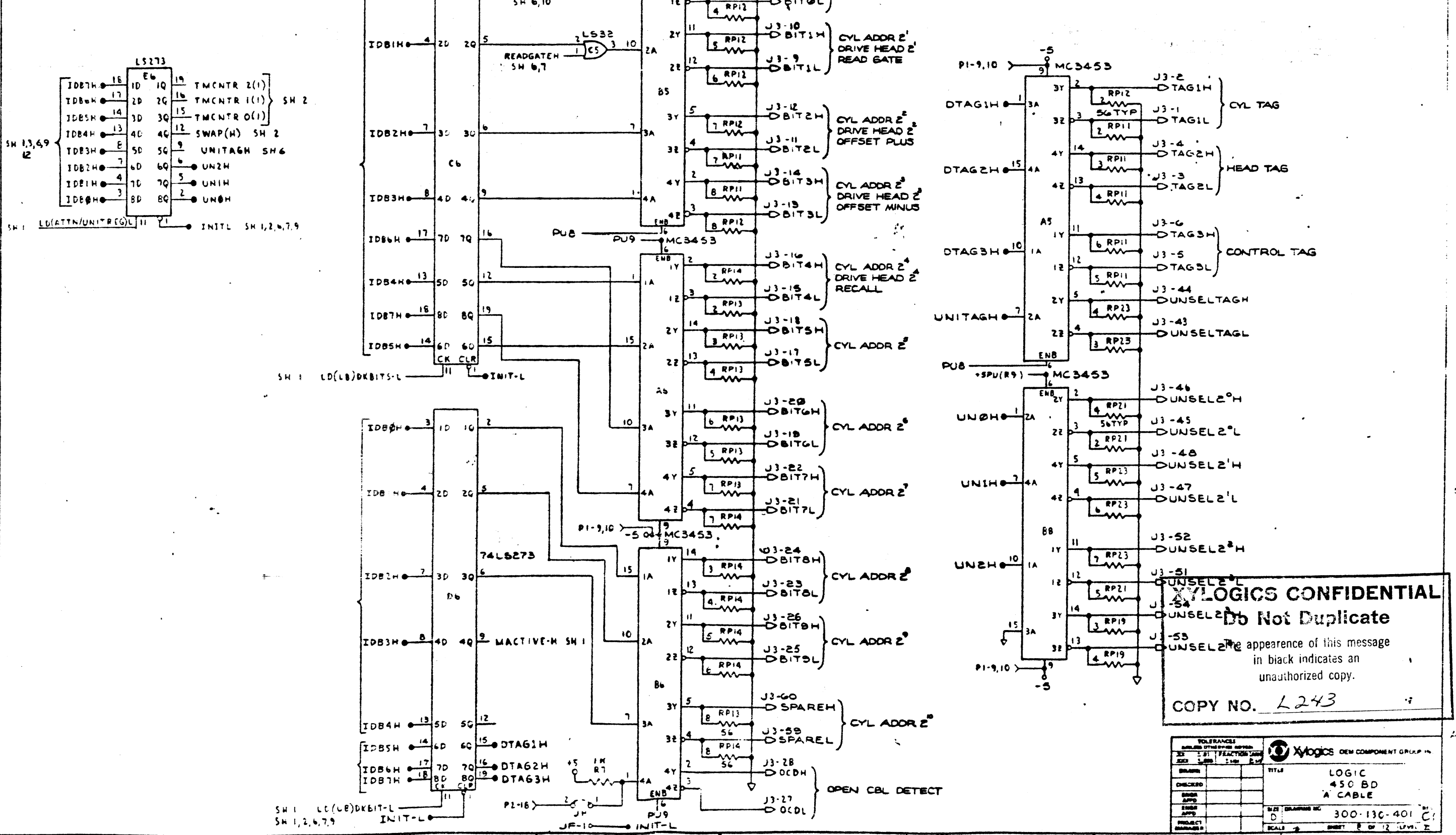
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TOLERANCE	DATE	BY	CHKD	APPD	PROJ	SCALE

**XYLOGICS ODS COMPONENT GROUP INC.**  
 TITLE: LOGIC  
 450 BC  
 ECC LOGIC  
 SHEET NO. 300-130-401  
 SCALE: 1" = 1" SHEET 7 OF 12

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ZONE	REV	DESCRIPTION	DATE



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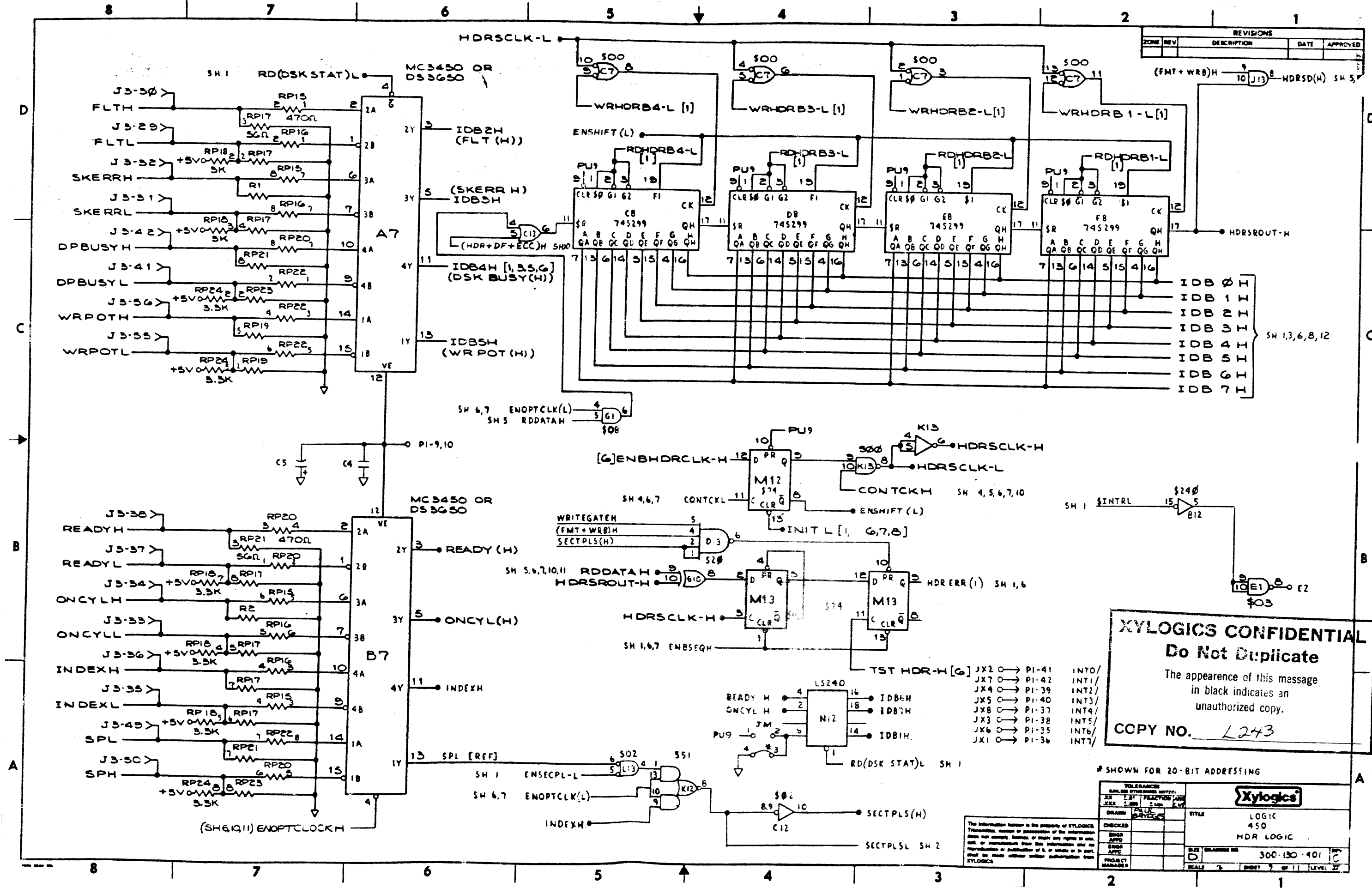
TOLERANCES		UNLESS OTHERWISE SPECIFIED	
RES	1% 5% 10%	RES	1% 5% 10%
RES	1% 5% 10%	RES	1% 5% 10%
RES	1% 5% 10%	RES	1% 5% 10%
RES	1% 5% 10%	RES	1% 5% 10%
RES	1% 5% 10%	RES	1% 5% 10%

DESIGNED BY		TITLE	LOGIC
CHECKED BY			450 BD
			A CABLE

XYLOGICS ODS GROUP COMPONENT GROUP INC.  
 300-130-401  
 SCALE: 1:1 SHEET 2 OF 12



REVISIONS				
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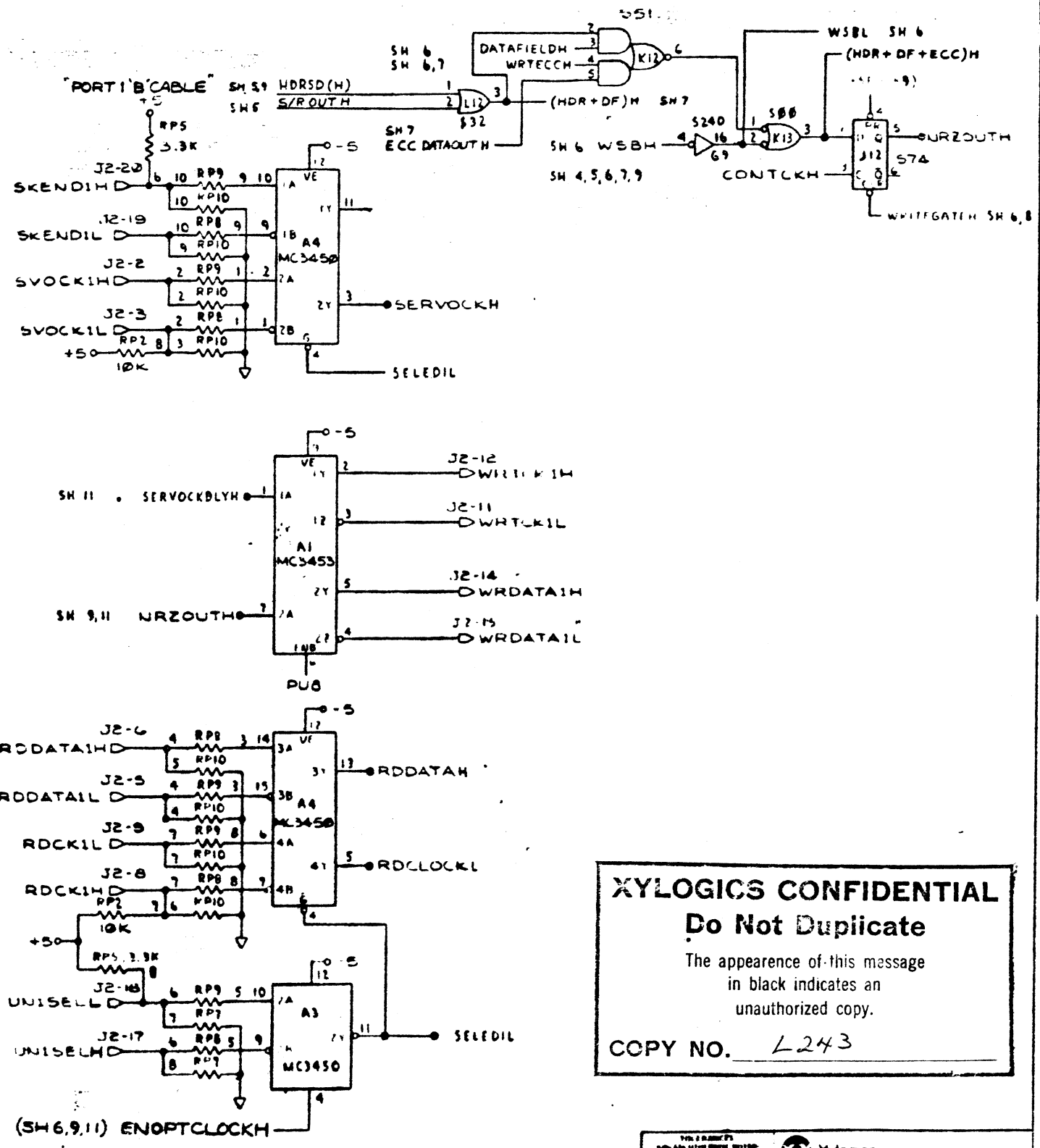
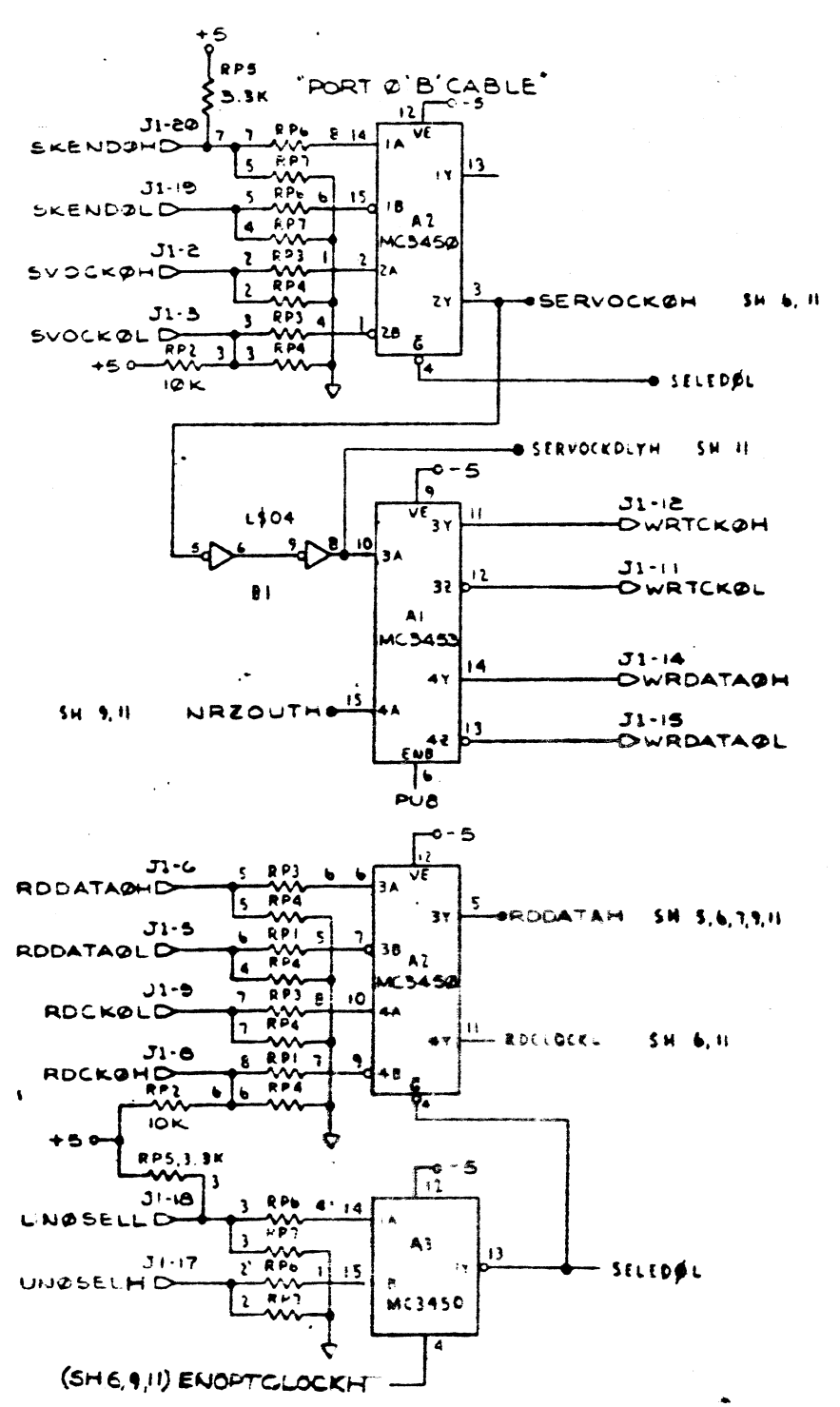
TOLERANCE		UNLESS OTHERWISE NOTED	
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT
DR	FR	FRAC	UNIT

TITLE	LOGIC 450 HDR LOGIC
SIZE	300-130-401
SCALE	1/8" = 1"
DATE	7/11/77
LEVEL	2

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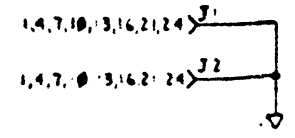
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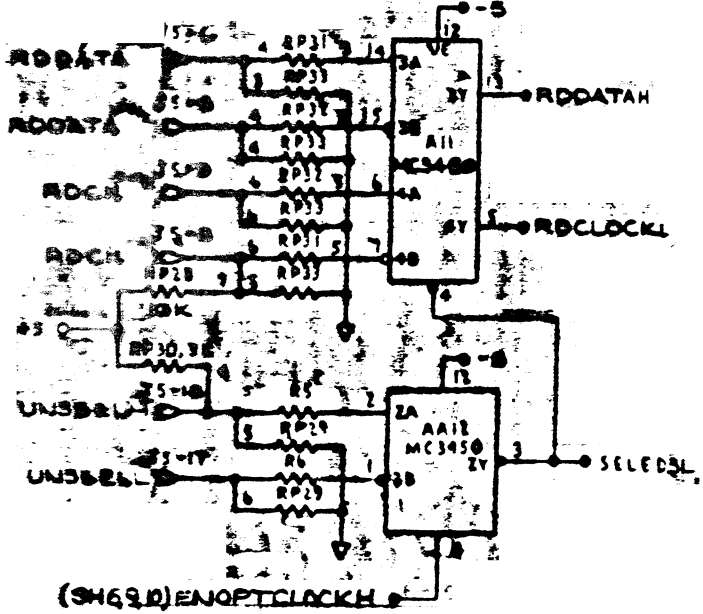
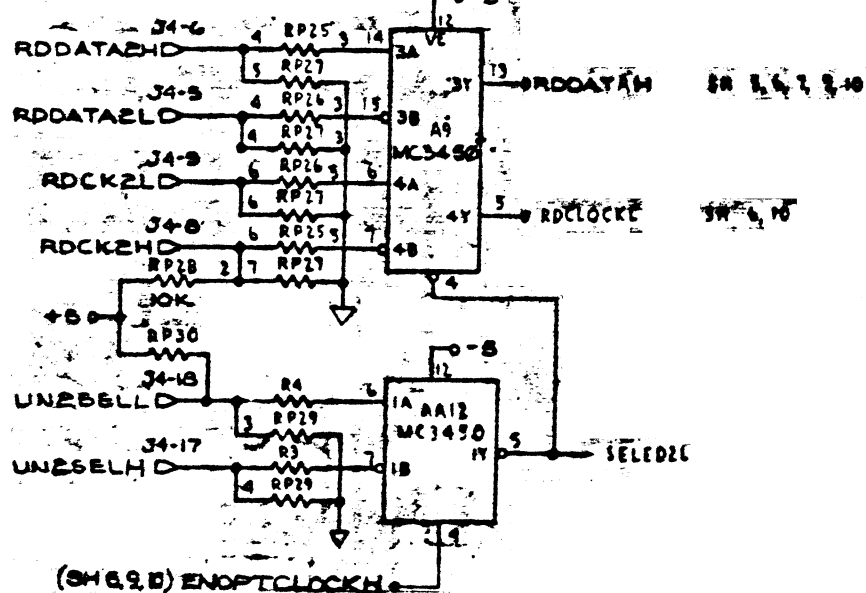
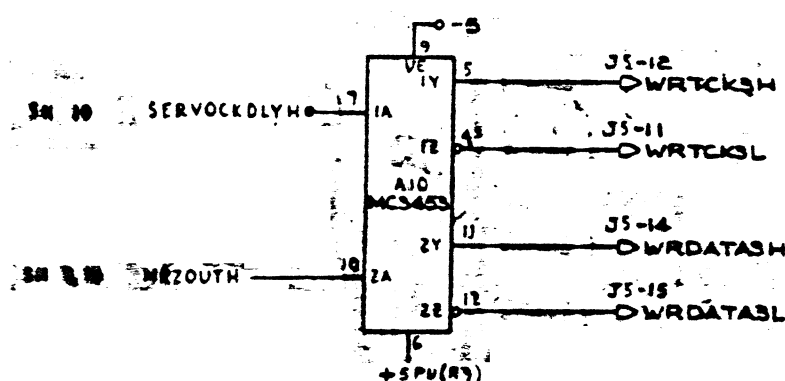
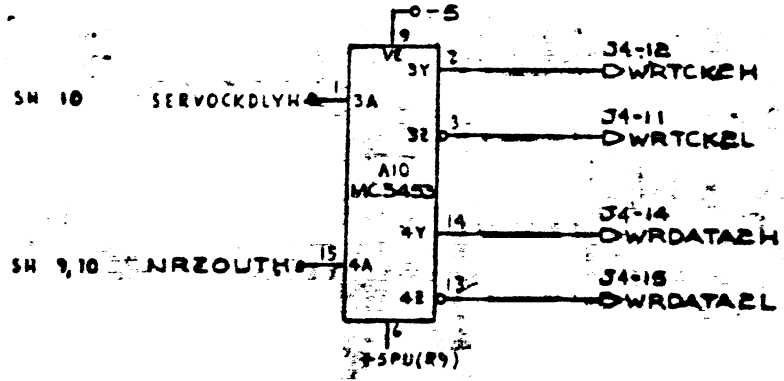
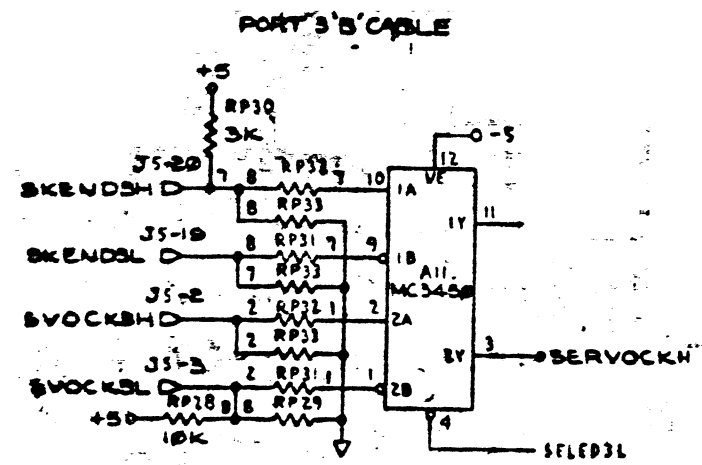
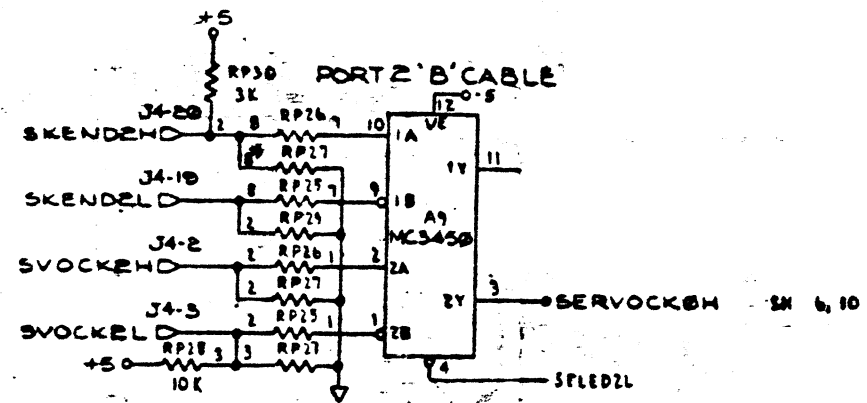
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XYLOGICS DESIGN COMPONENT LINEAR INC.  
 LOGIC  
 450 BD2  
 B PORT 0 + 1  
 300-130-40  
 10 12

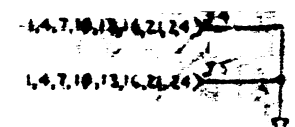


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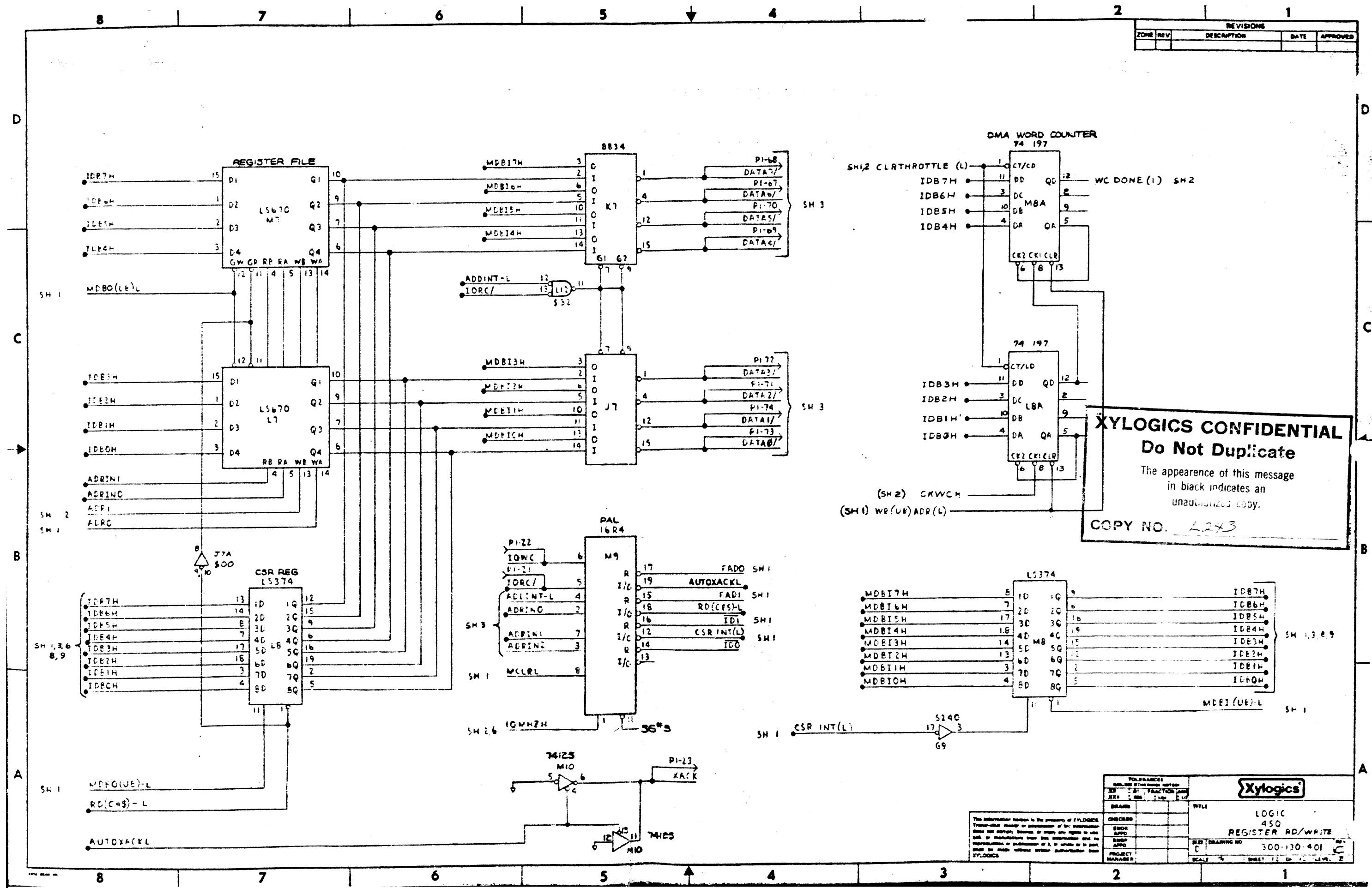
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DESIGNED	DATE	BY	APPROVED	DATE	BY

**XYLOGICS SEMI-CONDUCTOR GROUP INC.**  
 LOGIC  
 450 BDI  
 8 PORT 2,3  
 300-130-401  
 SHEET 11 OF 12 LEVEL II

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TOLERANCES		UNLESS OTHERWISE SPECIFIED	
RES	FRACTION	RES	FRACTION

DESIGNED BY		DATE	
CHECKED BY			
ENGINEER			
PROJECT MANAGER			

WTL	LOGIC
	450
	REGISTER RD/WRITE
DWG NO.	300-130-401
SCALE	1:1
SHEET	12 OF 12