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NoteTaker2 System Manual

BY Douglas G. Fairbairn and Bruce Horn

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ABSTRACT

This manual describes the NoteTaker2 computing system. The NoteTaker2 is a portable computer of considerable power useful for a wide range of computational and simulation-oriented functions.

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road / Palo Alto / California
94304

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PREFACE

NoteTaker2 is a very powerful portable computer intended for a wide variety of applications. Its intended users are "children of all ages": five-year-olds and high school students, as well as writers, researchers, artists, managers, and engineers. NoteTaker2 offers the capability of a general-purpose minicomputer, and allows it to be used without even plugging it into an AC power outlet.

This manual describes the hardware components of the system in three levels of detail. The introduction summarizes the main features of the NoteTaker2 hardware. Section 2 gives an overview of the architecture. Section 3 offers the detail required to program the system and to interface other devices to it.

NoteTaker2 has its roots in the long-time desire of the Learning Research Group at the Xerox Palo Alto Research Center (Xerox PARC) to have a portable system on which to experiment with its ideas concerning personal computers. The architecture of the machine was defined by Douglas Fairbairn of the LSI Systems Area at PARC in conjunction with LRG. The design of the system was handled largely by the Special Programs Group in the Electronics Division of Xerox. This group is headed by Douglas Stewart. The principal electronics designers were James Leung, and Ron Freeman(SPG) and Ben Sato of the Advanced Systems Department. Dick Resnick of SPG offered crucial help by writing the system maintenance and checkout diagnostics as well as programming the keyboard controller. The mechanical design and documentation were done or coordinated by Bob Nishimura (SPG). The successful and timely completion of the project is due largely to the way this group worked together and carried out their respective tasks with skill and thoroughness. Larry Tesler, Dan Ingalls, and Ted Kaehler of LRG played key roles in helping to define the needed hardware functions and they plus Bruce Horn offered invaluable aid in the debugging of the system. The project was managed by Doug Fairbairn. Special thanks is due Bert Sutherland, manager of the Systems Science Lab (PARC) and Lynn Conway, manager of the LSI Systems Area, who so actively supported the project.

1.0 Introduction

The decisions about the form and capabilities of NoteTaker2 were based on a wide range of often conflicting desires. The system had to offer a computing capability in the class of the Alto computer and it had to be packaged in a form which allowed it to be carried home, on airplanes, or wherever its owner desired to take it. There was a very strong feeling that the user should not have to "pack it up" to take it somewhere. That is it should go from being used to being carried in only a few seconds, and it should not be necessary to carry it in some additional case which would have to be stored somewhere when the unit was being used.

The capabilities offered by NoteTaker2 had to be sufficient such that the user did not always have to plug in external interfaces to make the machine useful. We therefore included all of the basic peripherals we felt were necessary. Because no current technology offered a secondary storage medium suitable for swapping operations, it was decided to include the maximum amount of random-access memory the package would allow. The minifloppy disk was included as a non-volatile storage device because the proximity of suitably fast and reliable communications facilities could not be guaranteed. The 7" CRT was chosen because it offers the largest number of viewable dots of any display device which met the size and power limitations of the package.

The hardware components which make up a NoteTaker2 system are as follows:

- 256K bytes of main memory with single-bit error correction and double-bit detection. This is expandable to 512K bytes using 32K memory chips and 1M byte using 64K chips.
- Two 16-bit general purpose processors (Intel 8086 CPU) and 12K bytes of local memory consisting of either RAM or ROM in 4K byte increments.
- One of the general purpose processors is connected to the following I/O devices using the 8086 bus.
    - An EIA interface for general purpose communications needs.
    - An 10-bit analog-to-digital converter with an 8 input analog multiplexer and sample/hold on the input.

- A two channel, 12-bit digital-to-analog converter with preamp output.
- A double-density, double-sided, minifloppy disk capable of storing about 340K bytes of data.
- A 7" diagonal CRT displaying 640 dots horizontally and 480 dots in the vertical direction. This provides a resolution of 118 dots/inch. The I/O processor handles the setup of the display controller but a display refresh controller with the display logic handles the transfer of data from the memory to the display.
- A standard keyboard, identical to the Alto I keyboard layout. The keyboard is interfaced to the I/O processor over a serial data link. The keyboard has within it a single-chip microprocessor for controlling power on the keyboard, keeping track of the mouse and serializing the data which is transferred to the I/O processor.
- A mouse. The mouse is actually interfaced to the single-chip microprocessor in the keyboard and its state is transmitted along with the keyboard state.
- A transparent overlay tablet for pointing on the screen

- A small 3" speaker for audio output.
- A power system capable of supplying 100 watts. The peak demand of the system is about 80 watts. The power supply can get its primary power from the AC line (120 or 240 VAC) or from a battery pack (28.8 VDC) which is an option on NoteTaker2. The battery pack can be carried as a separate piece or easily attached to the rear of the case for easy transport. It is expected that the system can be operated on the batteries for about 2 hours at a time. A recharging system is built into the power supply.
- There are several I/O connections on the rear panel which the user may find useful:
  - A latched output port is available on the back of each processor card. This port offers 24 lines which can be defined in different combinations of input, output, and clock bits.
  - A connector to plug in an external CRT is availale on the rear of the disk/display card. The external CRT may be driven at a higher line rate than the 525 rate used by the internal monitor. The display controller is programmable and could be set to run at about 875 lines if required.
  - Three of the inputs to the analog multiplexer (multiplexed into the analog-to-digital converter) are available on the rear of the communications card.
  - The EIA interface connector is available on the communications card.

- The architecture of the system is such that up to 16 processors can be operated in parallel. Although these extra processors may not fit within the package, the system will offer a useful test-bed for experimenting with multi-processor architectures.

- The package is about 19" wide, 14" deep, and 7" high. The total weight without batteries is about 40 lbs. With batteries the system weighs about 40 lbs.

2.0 System Architecture

A block diagram of the NoteTaker2 system is shown in Fig. 1. The computer offers a multiprocessor architecture based around a single system bus. Each of the processors and the main memory are connected to the system bus. The processors do not communicate directly with each other but rather do so by passing messages in main memory. The system bus is synchronous with the main memory. Each of the processors runs asynchronously from the other and from the system bus. The basic NoteTaker2 configuration allows for 16 processors. The processors do not have to be of the same type. In the current configuration, there are two Intel 8086 processors for general purpose computation and one display refresh processor.

2.1 System bus

The system bus links the processors with memory and includes 16 information lines and 21 control lines. The information lines carry both data and addresses. Control functions on the bus include a bus clock for synchronizing transfers, a parallel hardware priority system for controlling access, and capability for any processor to interrupt, reset, or boot any other processor.

These last three functions are implemented by writing the target processor's address and the desired function code into a reserved global I/O location. The memory system then takes care of generating the appropriate reset, boot, or interrupt signals.

Bus arbitration is handled in a distributed fashion. When a processor wants control of the bus it sets an internal access request signal which is synchronized by the next *BusSync* signal to produce a *BusReqn* signal. There are 8 parallel bus request lines on the backplane, each of which is assigned to a processor. Each of the processors monitors the request lines of higher priority than itself. A processor assumes control of the bus when it is requesting control and no other processors of a higher priority are doing so also.

There is a bus lock capability implemented on the system bus to allow any of the processors to inhibit access of the shared memory by another processor during a critical section. A processor can set an internal bit which indicates that the bus is to be locked the next time that processor gets control. When a processor gains bus control and asserts *BusLock*, all other processors capable of doing *write operations* to the memory are forced to disable their bus request signals and leave them disabled until the locking processor resets the *BusLock* signal. Note that a processor such as the display refresh processor is allowed continued access to the memory because it can in no way modify the memory's contents.

Table I summarizes the signals on the bus. There are a total of 52 devoted to system wide functions. Of these, 16 are information, 21 are control, and 13 are power. The bus is implemented on a backplane of 100 pin connectors, leaving 50 pins available for I/O device interfacing.

2.2 Main memory

The main memory is organized as 64K 32-bit words with an additional 7 bits with each word for double-bit error detection and single-bit correction. Although all data is accessed 32 bits at a time, the memory can be byte addressed. The information path on the system bus

is 16 bits wide and transfers bytes, words or double words in a synchronous fashion between the processors and the memory. Both addresses and data are transferred on the information path.

A normal read operation takes 560 ns. plus about 80 ns of bus arbitration overhead. This assumes no conflicting requests from higher priority devices. A write operation takes 880 ns for the memory to complete but the processor is allowed to proceed after 320 ns of the cycle. In block transfer mode, the memory can transfer data at the rate of 1 doubleword every 320ns. The peak bandwidth available on the bus is thus 100 Mbs. The hardware will allow any device to make up to 128 consecutive double-word transfers although because of refresh requirements on the dynamic memories, the real limitation is about 46 double-words.

The main memory is constructed of special 32Kx1 hybrid dynamic RAMs. These chips are two standard 16K RAMs on a single package. Memory capacity can grow to 512K bytes with 32Kx1 chips and can expand to 1 M byte with 64K chips. The address space of the Intel 8086 processors is 20 bits or 1M byte.

This subsystem also has the ability to trap attempted accesses to memory locations $FFFC0_H$ to $FFFDF_H$. An access to any of these locations will cause an interrupt and vector the processor to the appropriate routine. This interrupt can be disabled in software as can the others described below.

2.3 Processors

The basic processor subsystem consists of an 8086 processor with up to 12K bytes of local memory. This memory is made up of either RAM or ROM. These two types of memory can be traded off in 4K byte increments. The standard NoteTaker 2 configuration will have two such processor boards. One of the processors will be largely dedicated to Smalltalk emulation while the second will be the primary I/O controller.

Each processor has 8 hardware interrupts. They are listed below in priority order.

1. Main memory parity error
2. 60 Hz.
3. System interrupt
4. Illegal address trap
5. Undefined
6. Undefined
7. Undefined
8. Undefined

Each processor is interfaced to the system bus in a standard way. The logic for a typical interface is shown in Fig. 2. The address of each processor is defined with dip-switch.

In the standard configuration one of the processors is interfaced to a number of low-speed I/O devices. This I/O processor handles much of the overhead associated with setting up and completing I/O transfers. The communication between the I/O section and the other processors is handled through main memory and the system interrupts.

The I/O processor communicates with the controllers for the display, keyboard, and floppy disk. It acts as a controller for the tablet, a 10-bit A/D converter with 8 analog inputs, a dual output 12-bit D/A converter, and an EIA line interface.

2.4 The I/O System Components

2.4.1 Display Refresh Processor

The display refresh processor is a semi-independent processor within the I/O system. It gets its initialization from the I/O processor but handles transfer of data between the memory and display independently. There is no hardware cursor in the display controller and the 8086 must reset the bit map starting address at the beginning of each frame. The display bit map must be contiguous in main memory and the two fields of the frame are *not* interlaced in memory as they are on the Alto.

2.4.2 Keyboard Processor

The keyboard has the same layout as the Alto I keyboard. Within the keyboard is a single-chip microprocessor (Intel 8748) which receives requests for data from the I/O processor and sends back the state of the keys and the mouse. All communications take place over a serial path between the keyboard and the I/O processor. The keyboard processor is continuously monitoring the state of the mouse direction signals and keeping track of the change in mouse coordinates from the last time the I/O processor polled the keyboard. The power to the keyboard keys is normally off. When the I/O processor sends a request to the keyboard, the keyboard processor turns on the power to the keys, samples the state of each of the keys, and transmits one bit to the I/O processor for each key in the array. Also reported at this time is the state of the mouse switches and the relative coordinates since the last poll.

2.4.3 Disk Controller

The minifloppy disk controller is a Western Digital 1791 capable of handling double density floppies or minifloppies. There is additional logic which allows up to 3 drives to be controlled. The extra drives can be attached to the connector on the rear panel. Each drive may be single or double sided.

2.4.4 Transparent Tablet

The tablet is a transparent device which fits over the front of NoteTaker2 screen. It allows the CRT to be touch sensitive for use in a variety of user interface experiments. The I/O processor can sample the coordinates where the panel is touched by reading two of the inputs of the A/D converter.

2.4.4 A/D Converter

The A/D converter can sample the state of the tablet as mentioned above. It can also monitor the state of the battery voltage, and the +5 volt and +12 volt supplies for NoteTaker2. The last three outputs are brought to a rear connector for the user. The converter can sample at a rate up to 12 Khz and can be programmed to sample at slower rates.

2.4.4 D/A Converter

The D/A converter is a single 12-bit converter with two sample and hold circuits on the output. The input to the converter is fed by a 16 word FIFO which is loaded by the

processor. The rate at which the samples are clocked out of the FIFO and into the converter is set by software and can be a maximum of 16 Khz..

2.4.4 EIA Interface

The EIA interface implements standard RS-232 type protocols operating at speeds of 150, 300, 600, 1200, 2400, 4800, and 9600 baud.

NoteTaker2: Detailed Specifications

3.0 System Bus and Protocols

The following operations are possible on the system bus

1. Memory

   >byte read and write
   >word read and write
   >double word read and write - double word operations may be repeated 16 times on each access, thus transferring 32 16-bit words.

2. Input/Output

   >byte read and write
   >word read and write

The system bus is multiplexed to allow transfer of information and control over the minimum number of wires. The basic 16 information bit lines are used for both data, addresss, and control information. These lines are used as follows:

BT0:	BT1:
Info00 - Read/Write	Addr08
Info01 - Word/Byte	Addr09
Info02 - IO/Memory	Addr10
Info03 - unused	Addr11
Info04 - unused	Addr12
Info05 - unused	Addr13
Info06 - unused	Addr14
Info07 - unused	Addr15
Info08-Info15 - Addr00-07	Addr16-Addr23

During a write operation (Info00 low during BT0) the data will be placed on Info00-Info15 during BT2. If it is a byte operation the processor must put the byte on the appropriate half of the bus.

During a read operation, the processor tristates all its data and control lines and awaits a DataReady signal from the memory or I/O device to signal it that data is on the bus and the processor may latch it and proceed.

3.0.1 Address Space

NoteTaker2 supports a memory address space of 24 bits or 16 Mbytes. The address is transferred between processors and memory over a 16 bit information path. The 24-bit address is multiplexed as described in section 3.0.2.

The I/O address space in NoteTaker2 is divided into 2 parts: local and global. Local I/O (LIO) occupies addresses 0_H to $7FFF_H$. Global I/O occupies the remaining half of the 64K total I/O address space: 8000_H to $FFFF_H$. The global I/O accesses will use the same multiplexed information bus and the high-order 8 bits will be 0.

3.0.2 System Timing

Figures xx through xx show the detailed timing for the system bus for all types of memory and I/O operations. The basic cycle time of the bus is 83.3 ns. (12 mhz.).

3.1 Memory Storage modules

3.2 Memory Control Module

3.3 Processor Module

3.4. Disk/Display Module

3.5 Communications Module

Table 1 - NoteTaker2 System Bus Signals

Signal	Description	Originates in processor (P) or Memory(M)
Information Bus		
MData00(MSB) - MData15(LSB)	Data and Addresses	P/M
Control Bus		
PageMode'	Current processor wants to access memory in page mode	P
GoMem'	Memory is ready - processor may proceed with request	M
BusLock'	Restrict access of any other processor	P
BusClkDly'	Delayed version of basic bus clock	M
ProcBoot'	Boot the addressed processor	M
ProcInt'	Interrupt the addressed processor	M
BusReq0-7	Bus request lines for each processor	P
MemComp	Indicates memory is finished with current request	M
ParErr	The main memory has detected as error	M
DataReady	The data requested from memory is available	M
ProcReset'	Stop the addressed processor	M
CorrOn'	Enable error correction circuitry	P
BusClk	Basic System Clock for synchronizing transfers	M
Reset	Power on reset	P
Power		
+5 volts	8.5 amps	
+12 volts	4.0 Amps	
-20 volts	400 ma.	
+28.8 volts	Battery Output: 4 amp-hours	
+15 volts	<50 ma. - derived from +30 volts	
-15 volts	<50 ma. - derived from -20 volts	
+30 volts	Raw output of power supply inverter - unregulated	
+42 volts	Charging voltage for batteries	