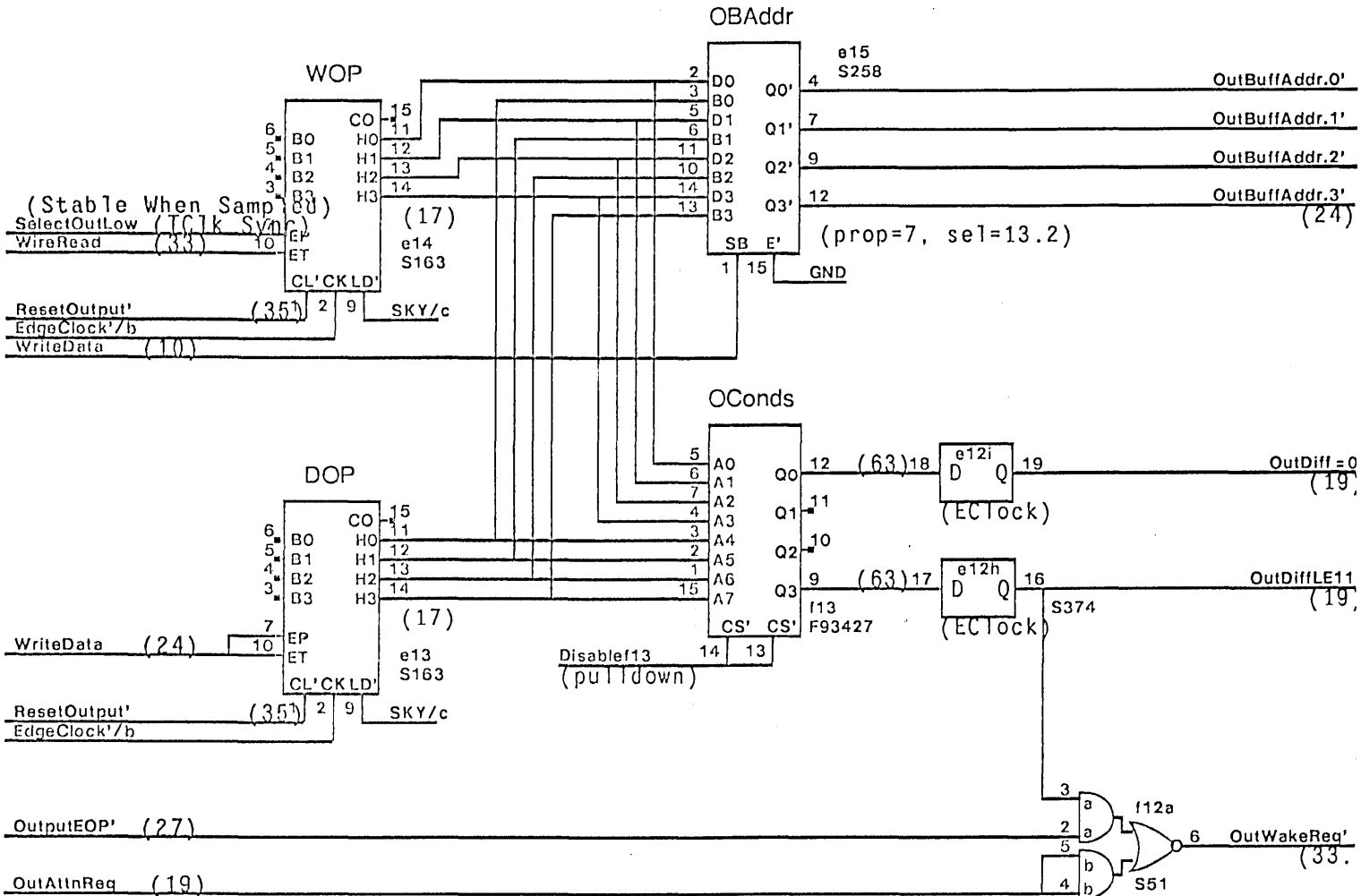
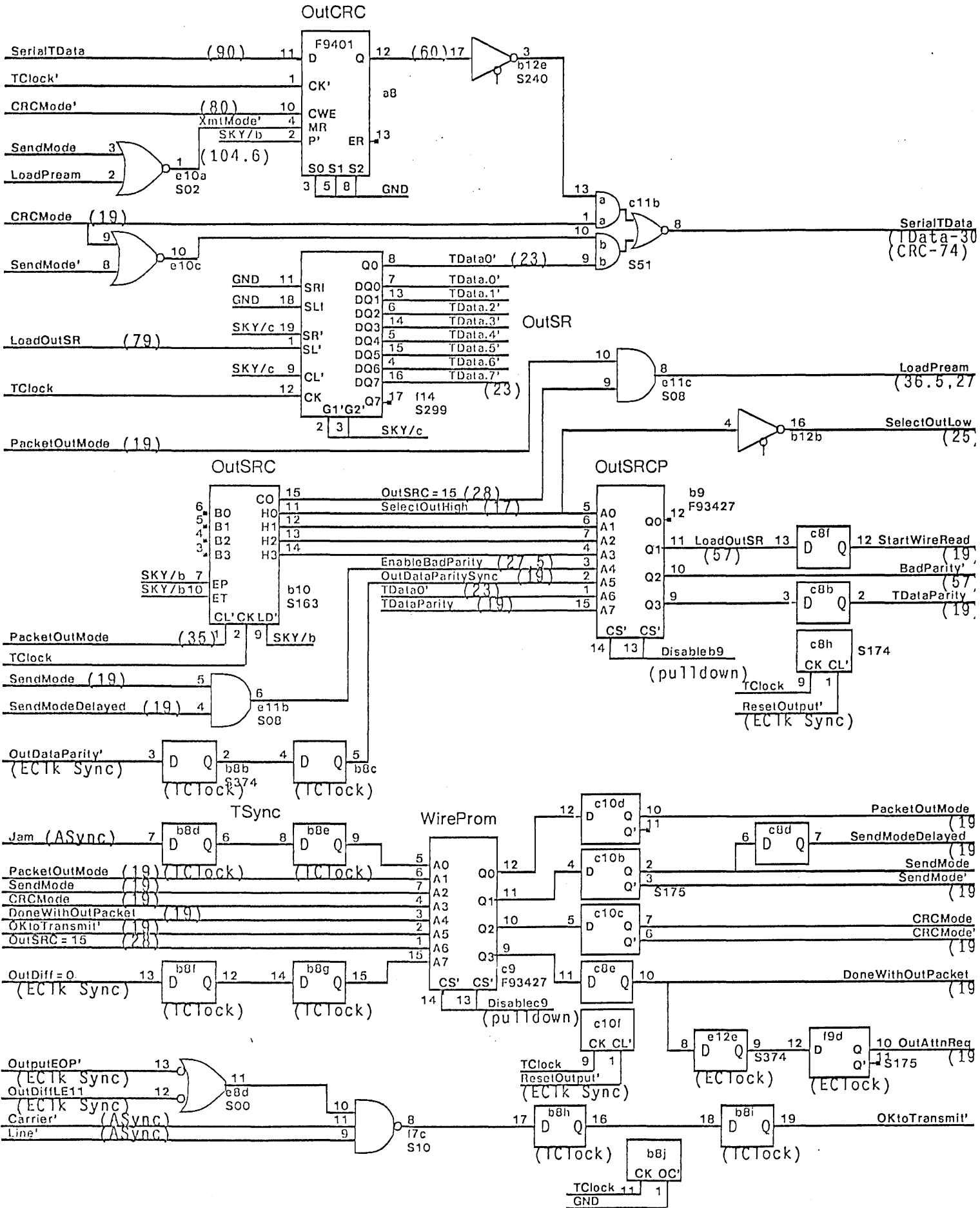
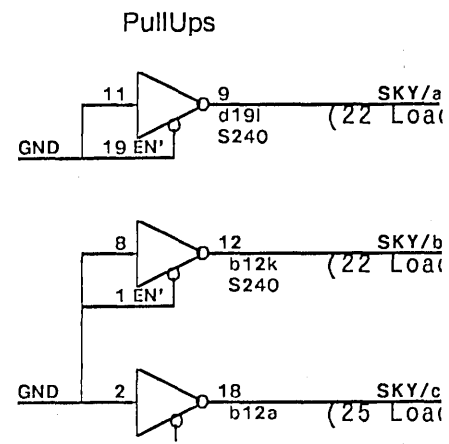
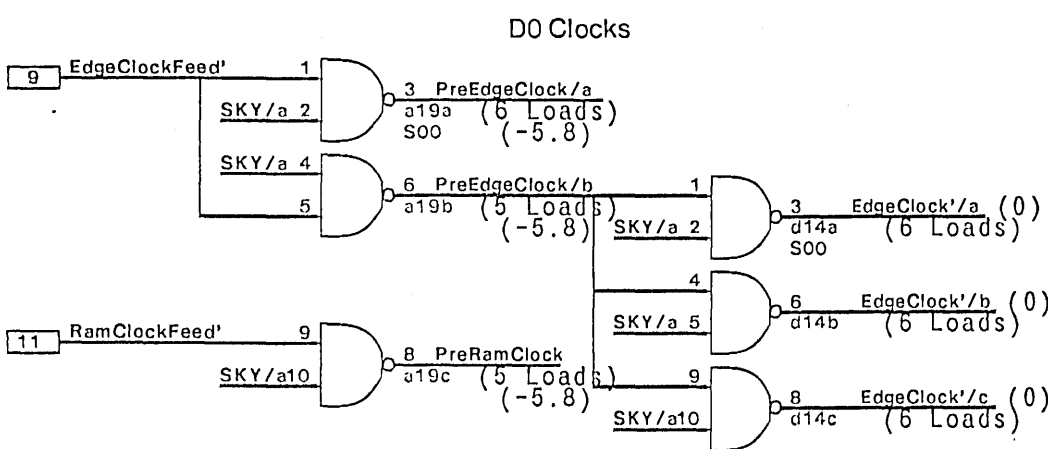
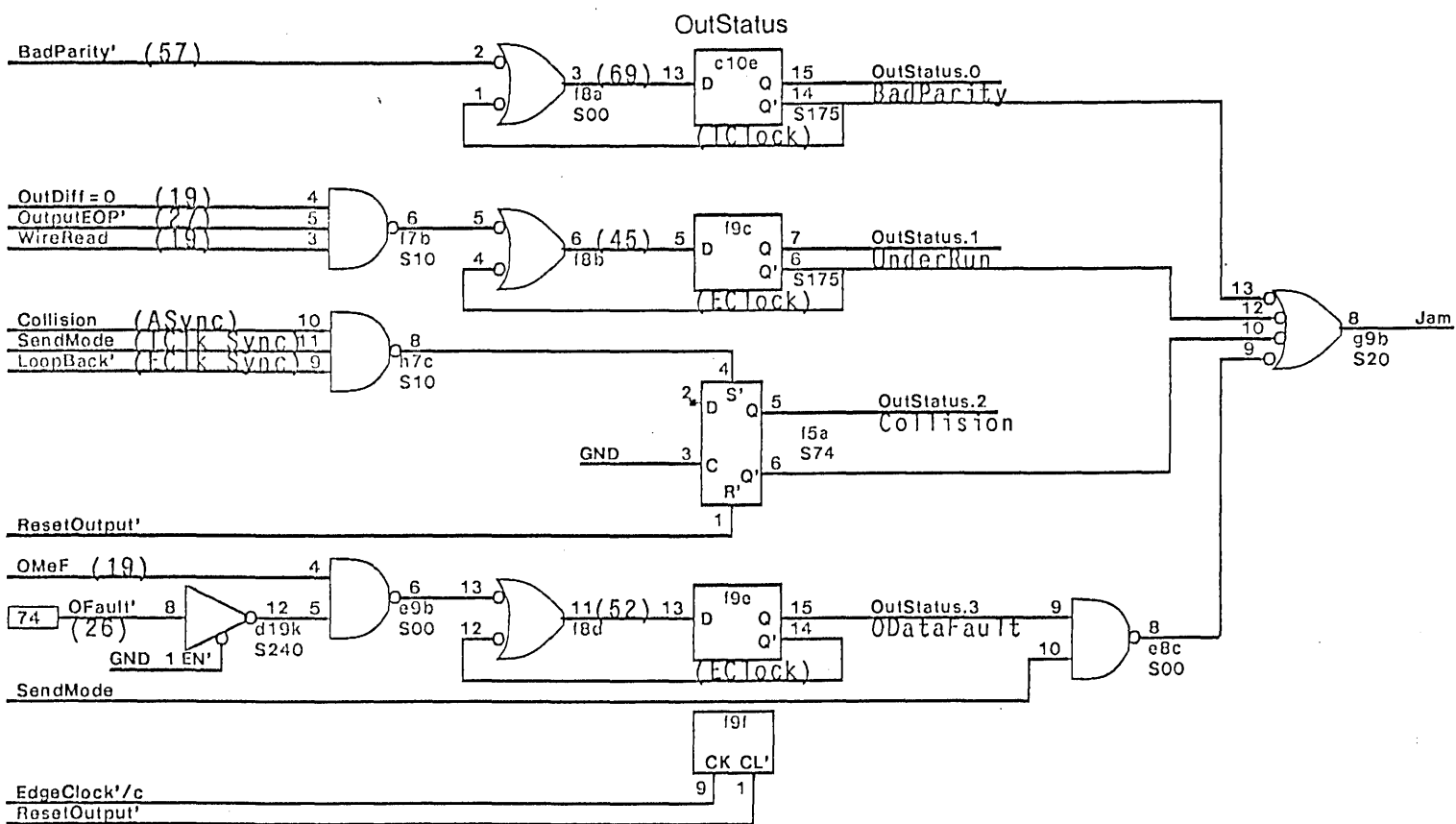
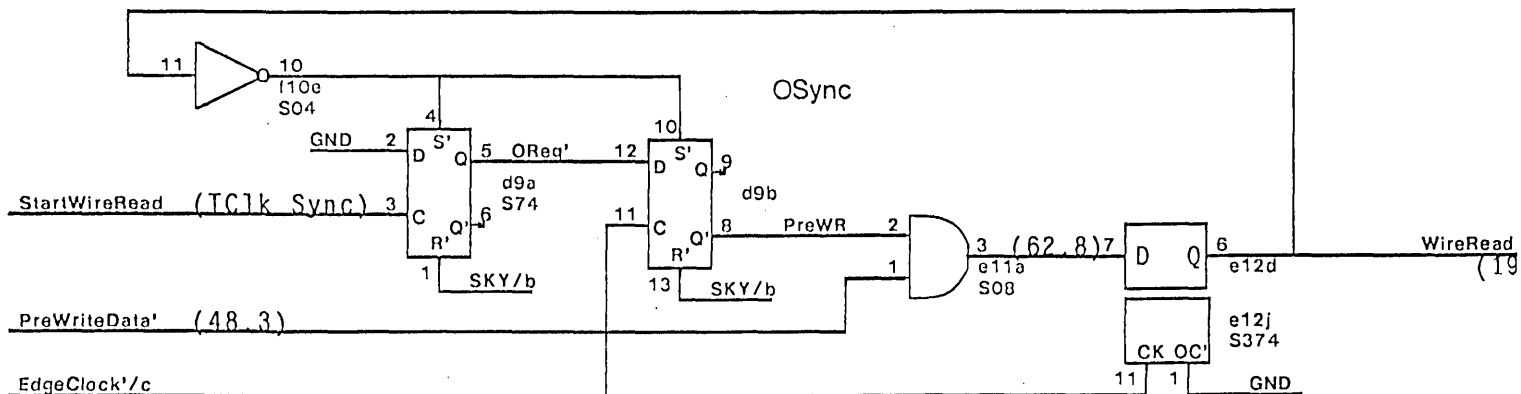


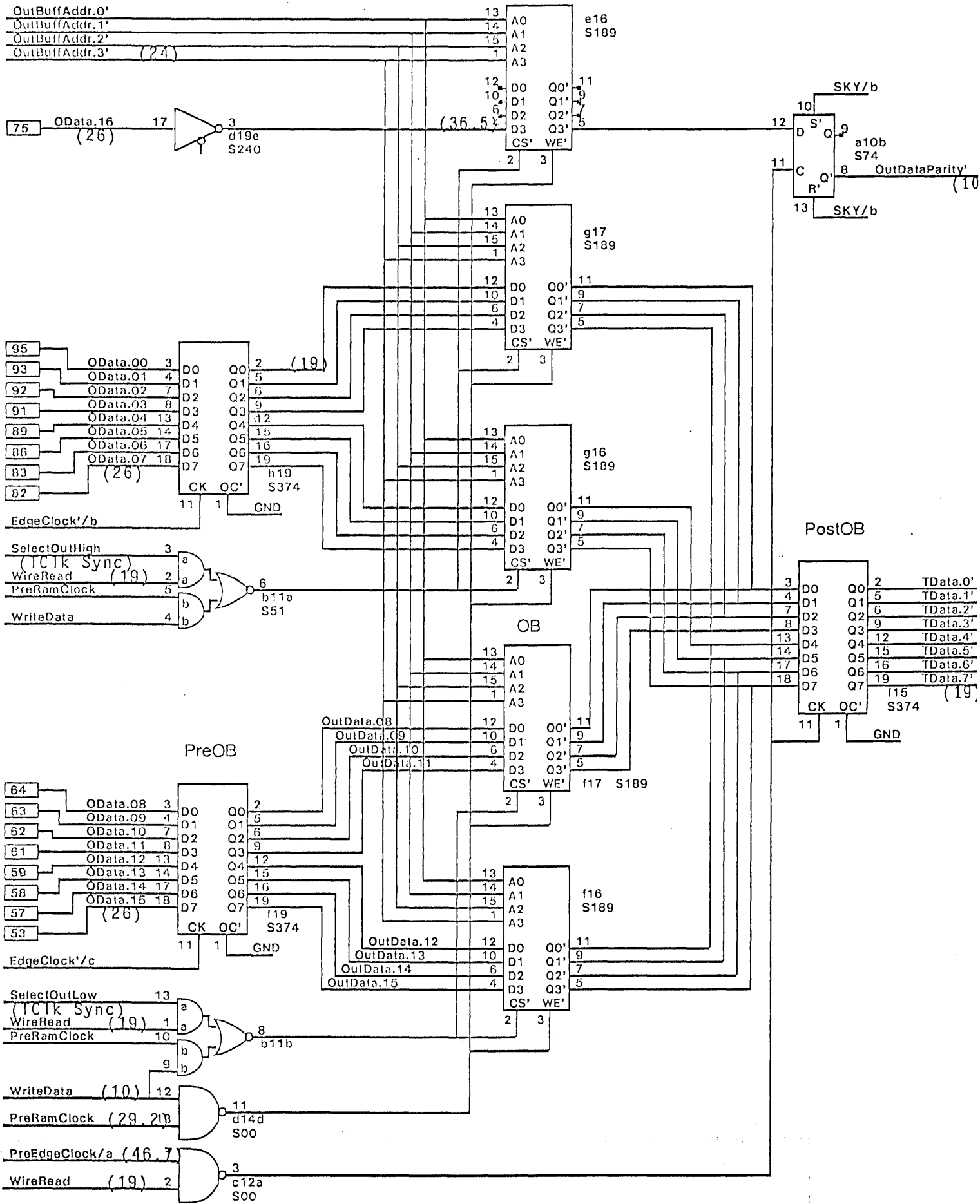
Note: IAddr  
 00 D0 Ethernet Device ID high byte = 6 for output and 7 for input. Low byte is alwa  
 01 Alto EtherNet ID (This simulates the number the Alto EtherNet obtains from the AI  
 10 Status-State  
 11 Input Data  
 Device ID Modifier [0:7] = 00 000 11x Where x = 0 for output and x = 1 for input task.  
 Device ID [8:15] = 00 000 000  
 ThusOutput ID = 3000 (octal)  
 Input ID = 3400 (octal)

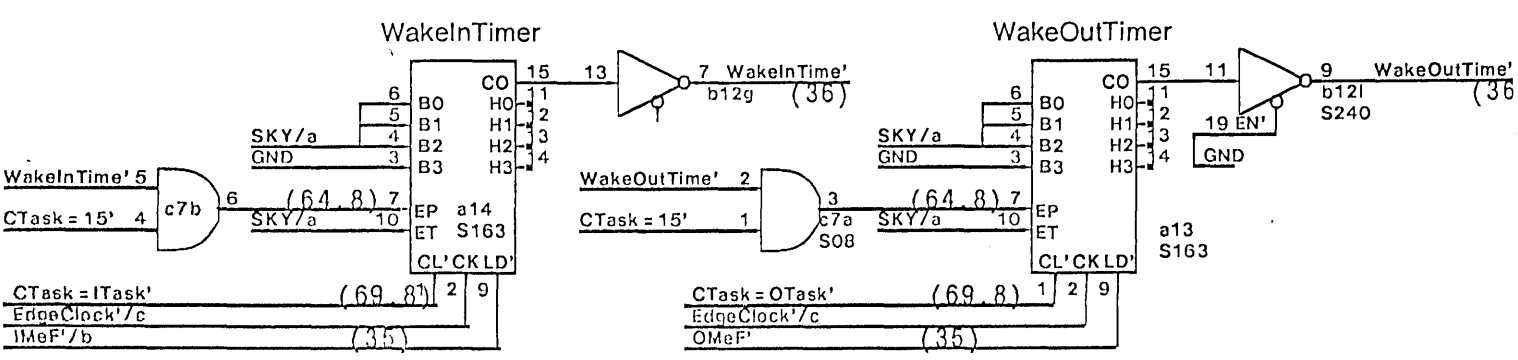
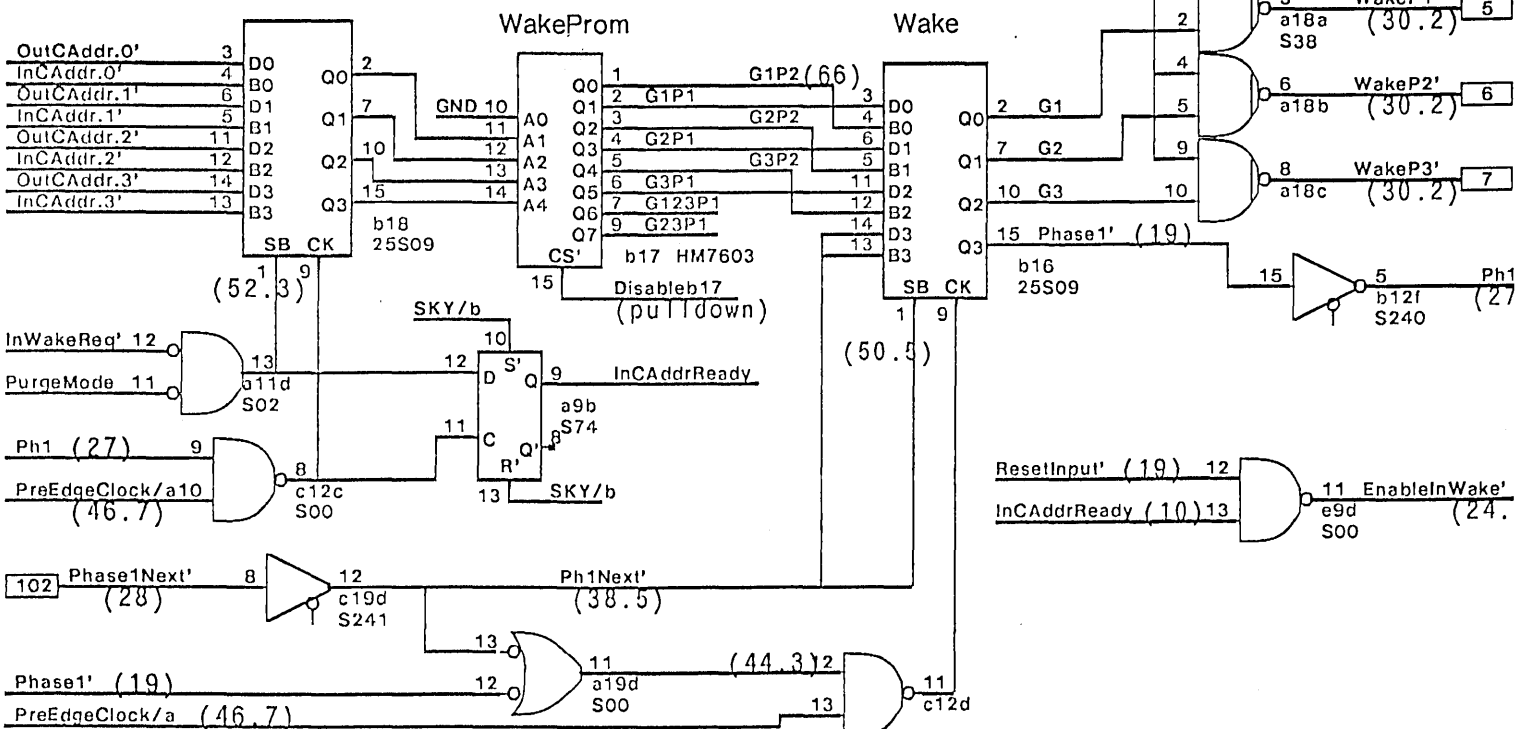
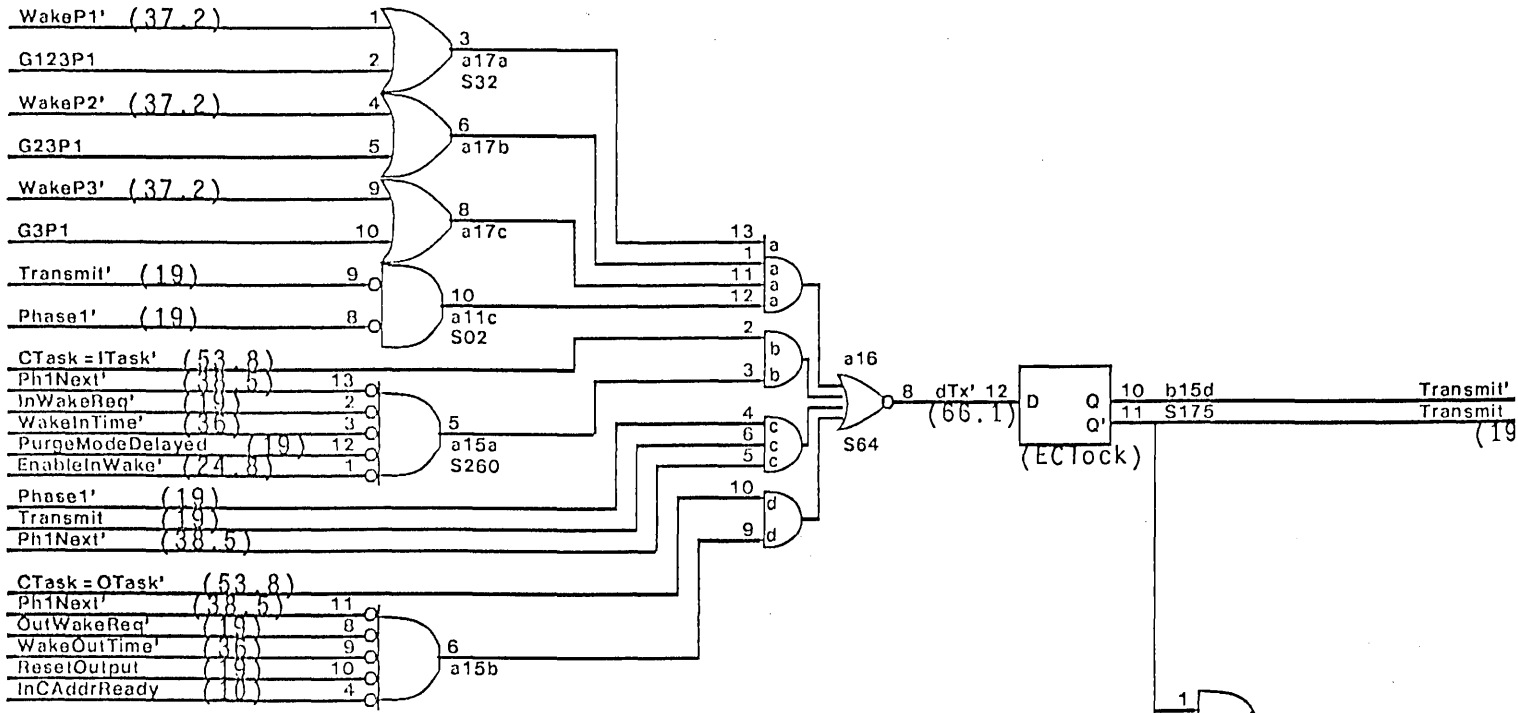




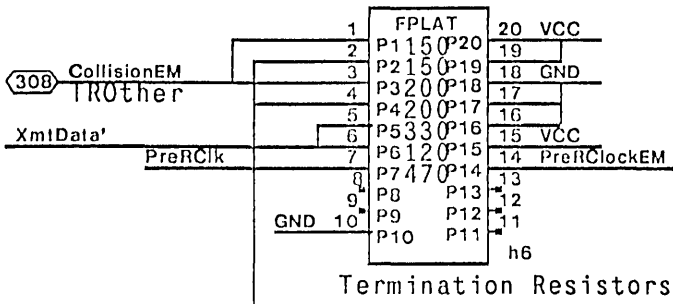




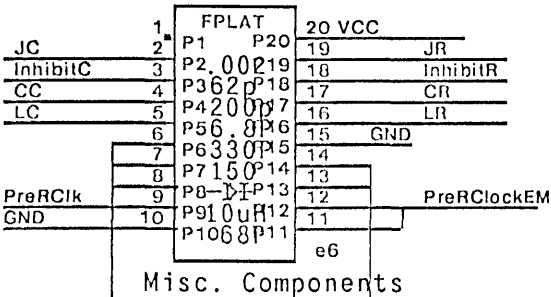
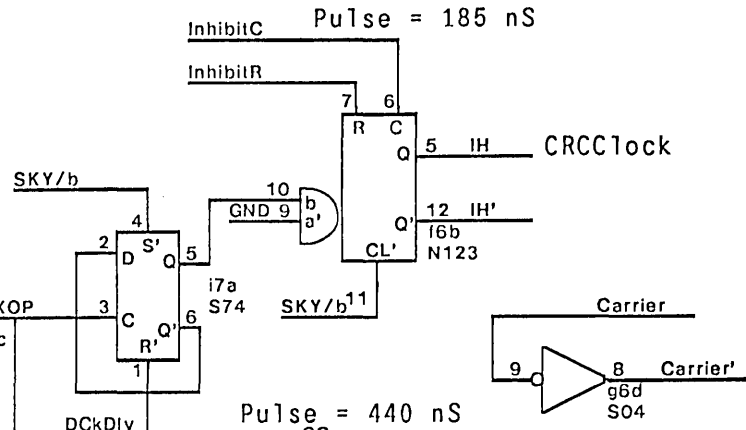
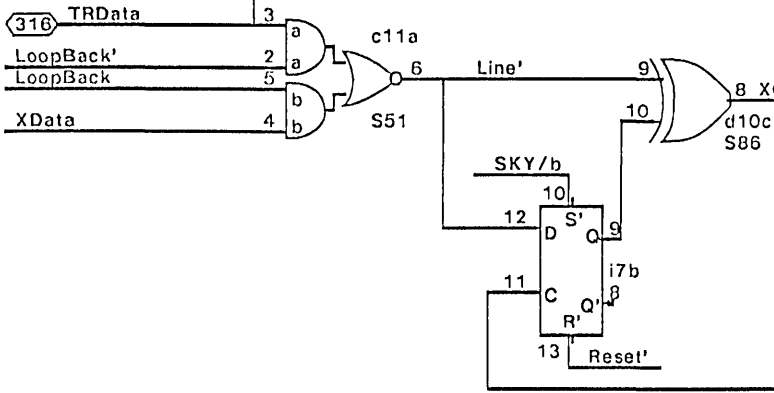




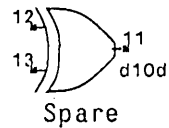
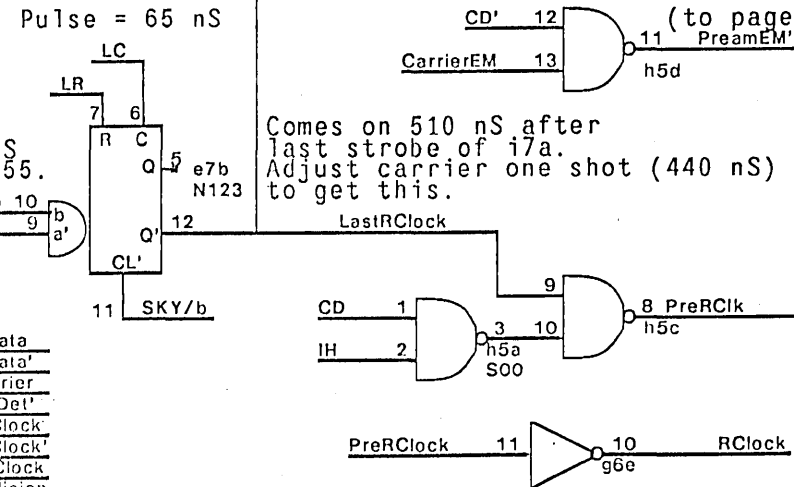
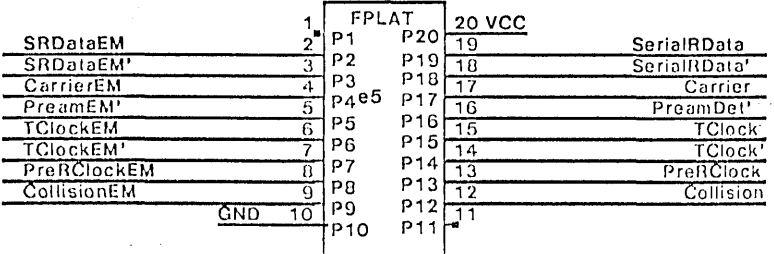
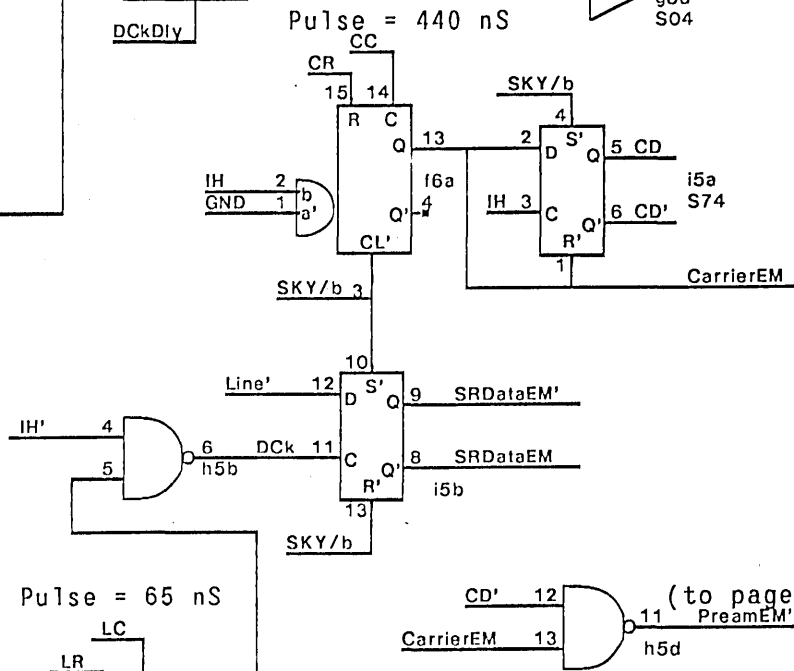
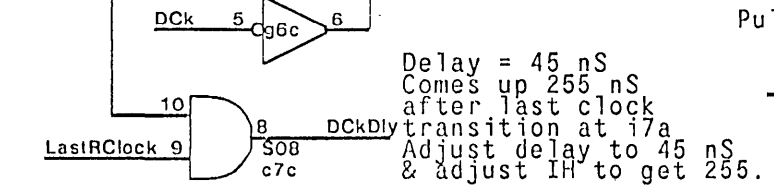


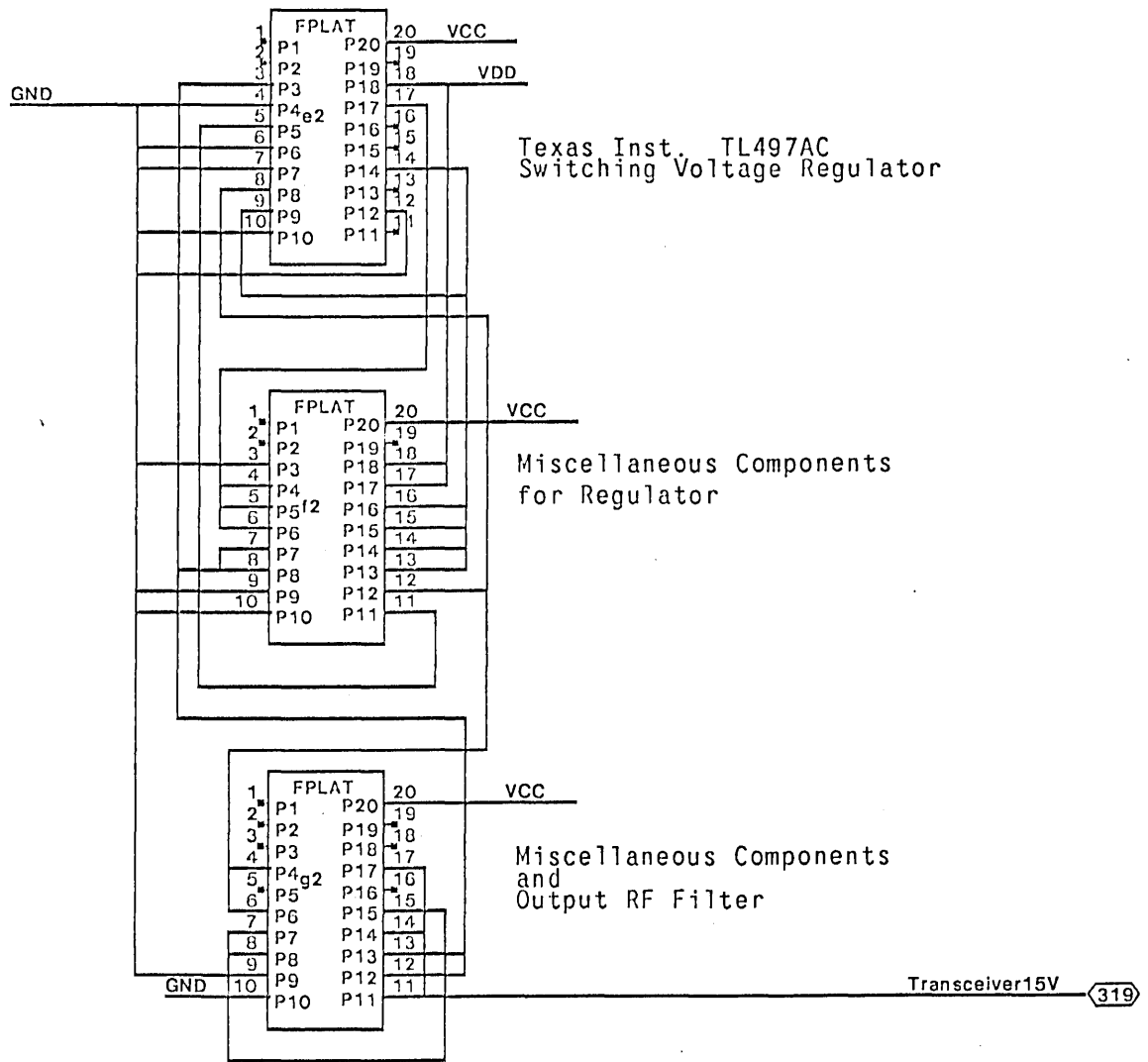


Termination Resistors

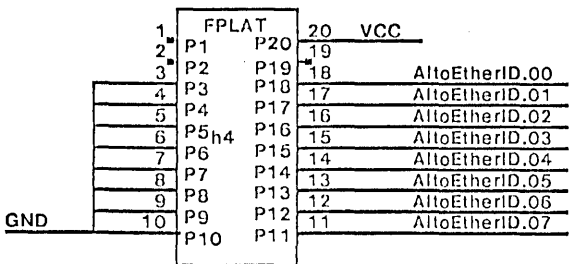


Misc. Components



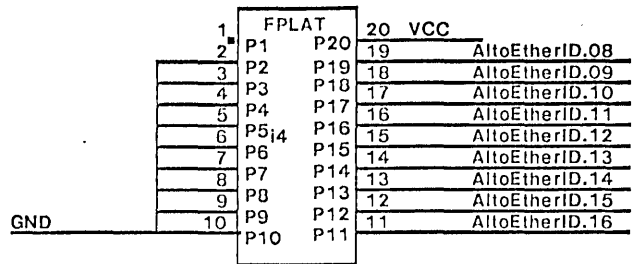


DIP Switches

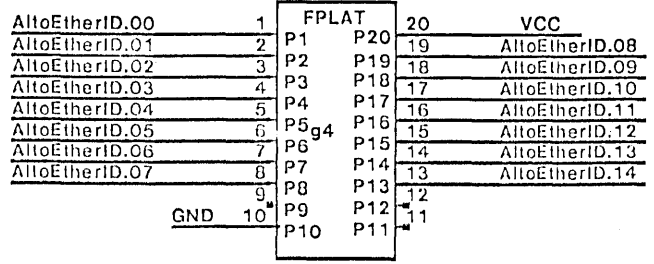


Set these switches to "ON" = logic 0.

DIP Switches

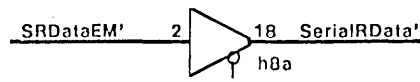
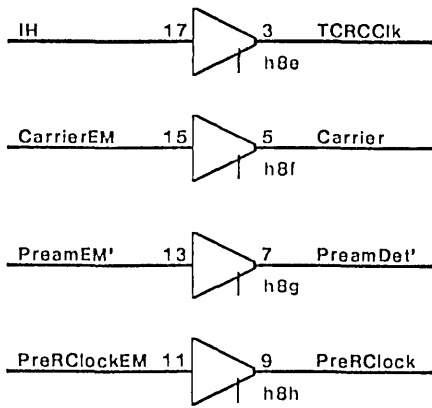


Set these switches to ID number and od P2 is MSB of ID number and P9 is LSB.  
Switch ON = 0  
Switch OFF = 1

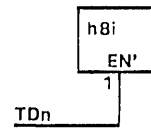
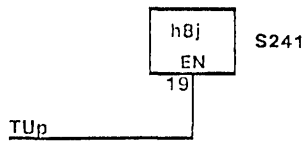
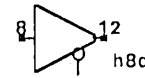
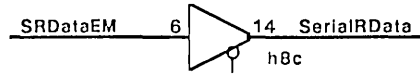


5.1K Pull-up Resistors

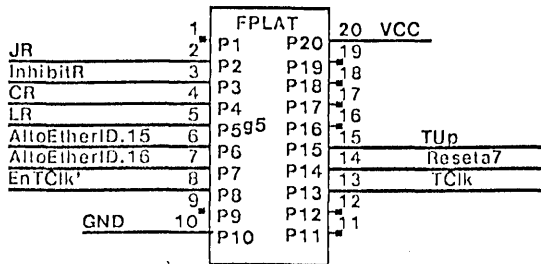




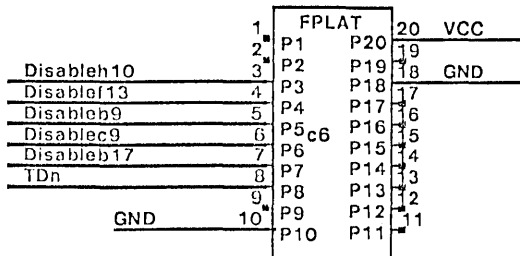
BadCRC on page 6



Note: When testing on the D0 Card tester, chip h8 (S241) must be removed as well as the jumper platform e5.



5.1K Pull-up Resistors  
16 pin package



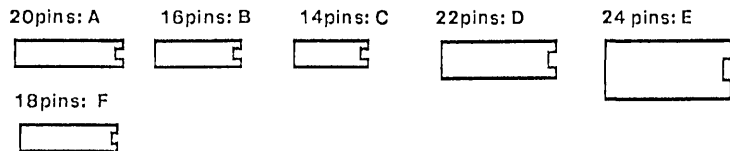
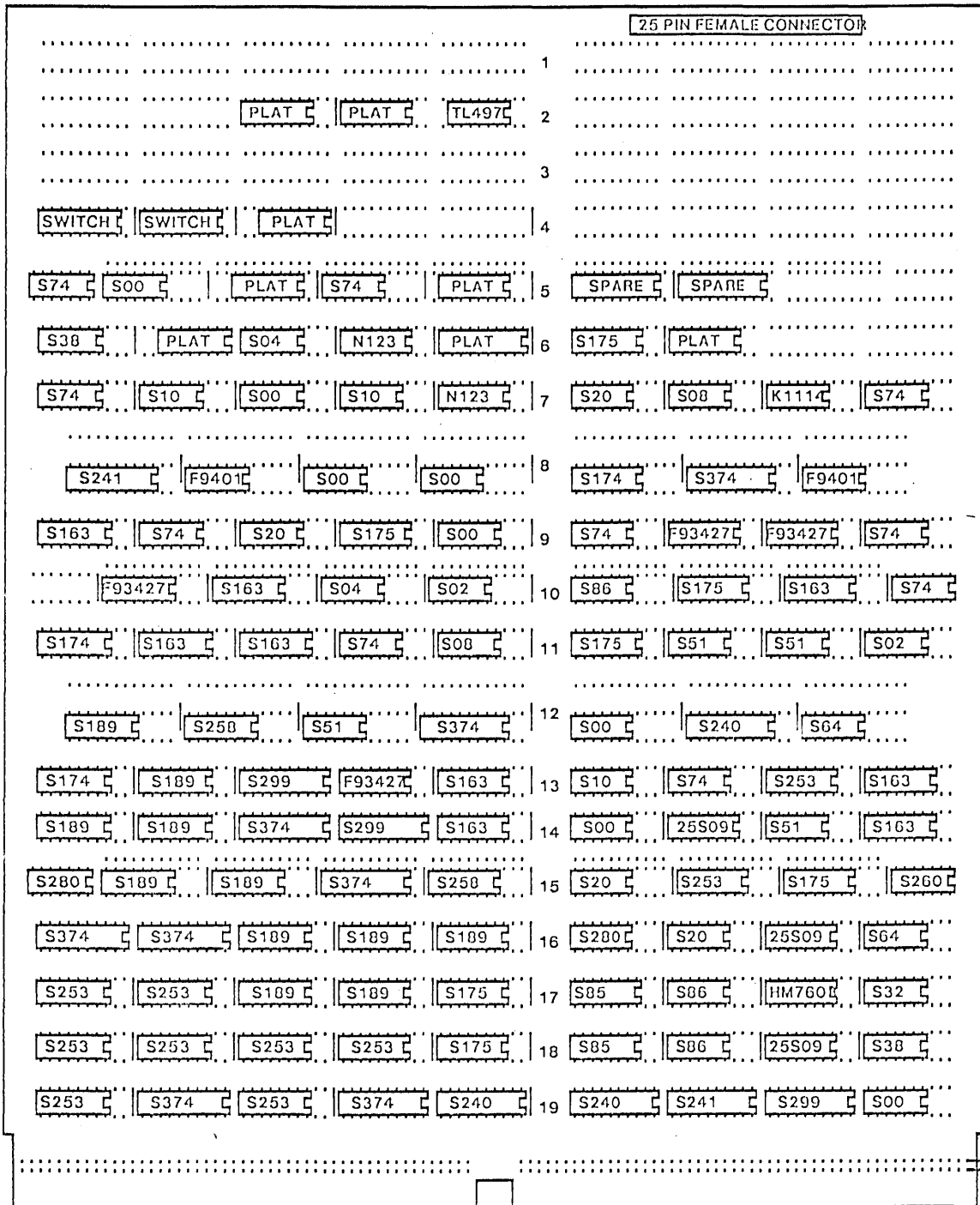
100 ohm pull down resistors  
16 pin package

Revision Ga generated from SDD revision N on 4/12/79 by CT.

- 1) Renamed D0En23.sil to D0En17.sil
  - 2) Added standard files for platforms.
- The following were done to eliminate ROUTE trace cuts:
- 3) Added VCC to clock plat at b7 (p14).
  - 4) moved 470 ohm resistor from plat e6 (1-20) to h6 (7-14), and added VCC to e6 (p15).
  - 5) Coalesced all sections of plat g5 (pg15,16,17) to pg17.
  - 6) Added VCC & GND to plat e5 (pg15).
  - 7) Added GND to plat g4, VCC to h4,i4,g2,f2 (p16).
  - 8) Moved TL497C up one position in pattern e2, added VCC & GND (pg 16).
  - 9) Added VCC, GND to plats c6, g5 (pg 17).

XEROX CSL	Project E Net	Changes	File D0EnChanges.sil	Designer Crane	Rev Ga	Date 4/12/79	Page 1
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I H G F E D C B A



Note: The short vertical lines indicate filter capacitor locations.

ML	Drawing No.	Rev. N
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MATERIAL LIST

Rev.	Drawing Title	<p>These drawings and specifications, and the data contained therein, are the exclusive property of Xerox Corporation and or Rank Xerox, Ltd. issued in strict confidence and shall not, without the prior written permission of Xerox Corporation Rank Xerox, Ltd., be reproduced, copied or used for any purpose whatsoever, except the manufacture of articles for Xerox Corporation or Rank Xerox, Ltd.</p>			
Dwg. No.	<p>D0 Ethernet Controller          (DOENPL01.sil)          EMS VERSION</p>				
		<table border="1"> <tr> <td>Model No.</td> <td>Date 4/13/79</td> <td>Sheet 1 of 3</td> </tr> </table>	Model No.	Date 4/13/79	Sheet 1 of 3
Model No.	Date 4/13/79	Sheet 1 of 3			

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
	Integrated Circuit	SN74S00	8	
		SN74S02	2	
		SN74S04	2	
		SN74S08	2	
		SN74S10	3	
		SN74S20	4	
		SN74S32	1	
		SN74S38	2	
		SN74S51	4	
		SN74S64	2	
		SN74S74	10	
		SN74S85	2	
		SN74S86	3	
		SN74123 TI only	2	This is timing component. Use only Texas Instruments
		SN74S163	9	
		SN74S174	3	
		SN74S175	7	
		SN74S189	11	
		SN74S240	3	
		SN74S241	2	
		SN74S253	10	
		SN74S258	2	
		SN74S260	1	
		SN74S280	2	
		SN74S299	3	
		SN74S374	8	
		AM25S09	3	
		F93427 PROM	4	Bit patterns detailed in Prom listings
		F9401	2	
	Integrated Circuit	HM7603-5 PROM	1	Bit Pattern detailed in Prom listings

ML

ML	Drawing No.	Rev. N
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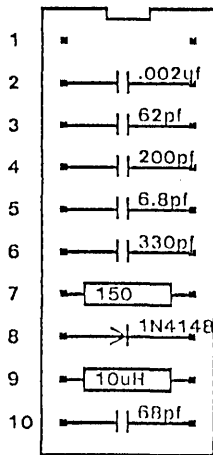
MATERIAL LIST

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Dwg. No.	D0 Ethernet Controller (DOENPL02.sil) EMS VERSION	Model No.	Date	Sheet
			4/13/79	2 of 3
Item No.	Drawing Title	Drawing No.	No. Recd.	Remarks
	Integrated Circuit Texas Inst. TL497AC		1	e2
	Clock package (14 pin) Motorola K1114A or equiv. Clock Frequency = 5.88 MHz		1	b7
ML	Timing Capacitors NPO Temperature 5% Coefficient 6.8 pF 10V		1	e6 Corning CAC02COG 6R8
	62 pF 10V		1	e6 Corning CAC02COG 620
	200 pF 10V		1	e6 Corning CAC02COG 201
	330 pF 10V		1	e6 Corning CAC02COG 331
	.002 10V		1	e6 Corning CAC03COG 202
	Capacitor 10% 10 pF 25V		1	f2
	Capacitor 10% 68 pF 25V		2	f2 , e6
	Capacitor 10% .1 uF 25V		1	g2
	Capacitor, Tantalum Electrolytic 10 uF 25V		5	f2, g2 2 of these are for board filter caps.
	Diode 1N4148		2	e6, f2
	Inductor, non-ferrous core 68 uH 4 ohms or less (Nyttronics SWD-68) DC resistance		1	g2 Inductor must not saturate @ 100 mA
	Inductor, non-ferrous core 220 uH 10 ohms or less (Miller 70F254AT 250 uH) DC resistance		1	f2 Inductor must not saturate @ 300 mA
	Carbon Composition Resistor .25 Watt 5% 120 ohms		1	h6
	150 ohms		2	h6
	200 ohms		2	h6
	330 ohms		1	h6
	1K ohm		1	f2
	Resistor .5 Watt 5% 2.2 ohm		1	f2 Allen Bradley RC20GF2R2J
	Resistor .25 Watt 1% 150 ohms		1	e6 Allen Bradley RN55D 1500F
	499 ohm		1	g2 Allen Bradley RN55D 4990F
	1.21 K ohm		1	g2 Allen Bradley RN55D 1211F
	13.3 K ohm		1	g2 Allen Bradley RN55D 1332F
	Resistor Network 16 pin 15 pullup resistors 5.1K 2% (Allen Bradley 316A512 or equiv.)		2	g4 g5 These resistors are used for timing.
	Resistor Network 16 pin 15 pullup resistors 100 ohm (Allen Bradley 316A101 or equiv.)		1	c6
	DIP Switch Package 9 SPST switches, 18 pin package		2	h4, i4 CTS 206-9
	16 pin DIP platform		4	e5, f2, g2, h6 Augat 616-DG5
	25 pin female D connector (DB25-S) with right angle printed circuit board mount		1	AMP 206584-1
	Locking posts, nuts, & washers for D Connector (available from Cannon)		2	Cannon D53018



Platform e6:

Capacitors are 5%, NPO T.C.



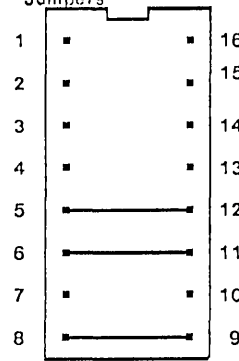
One-shot times:

R	T	Function
5.1k	3uS	Jam
5.1k	185nS	Inhibit
5.1k	440nS	Carrier
5.1k	65nS	LastRClock

Part of 45nS delay. Resistor is 1%

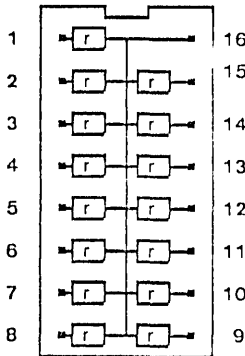
Platform e5:

Jumpers



Platform c6:

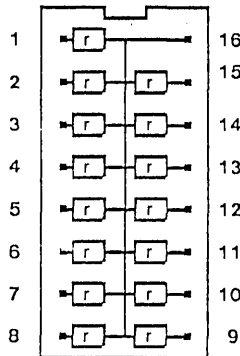
r = 100 ohm  
Allen-Bradley 316A101



Platform g4,

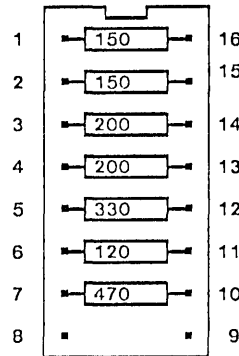
Platform g5:

r = 5.1k, 2%  
Allen-Bradley 316A512



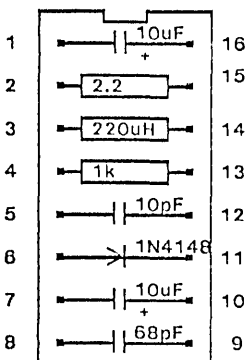
Platform h6:

Termination resistors  
.25 W, 10%



Platform f2:

Regulator components



Platform g2:

More regulator

