

## Interface to D0 chip tester

.G.T.T. Pgrp . Data .  
1 2 5 8

G -- Go bit (if on, start clocks following this instr.)

TT -- Type of instr:

- 0 -- Other (Pgrp is further decoded, see below)
- 1 -- Load Data into "Enable" reg. for indicated Pgrp
- 2 -- Load Data into "Data A" reg. for indicated Pgrp
- 3 -- Load Data into "Data B" reg. for indicated Pgrp

Pgrp -- Pin Group. Selects (except in "Other" type instrs) the group of 8 pins affected by the instruction.

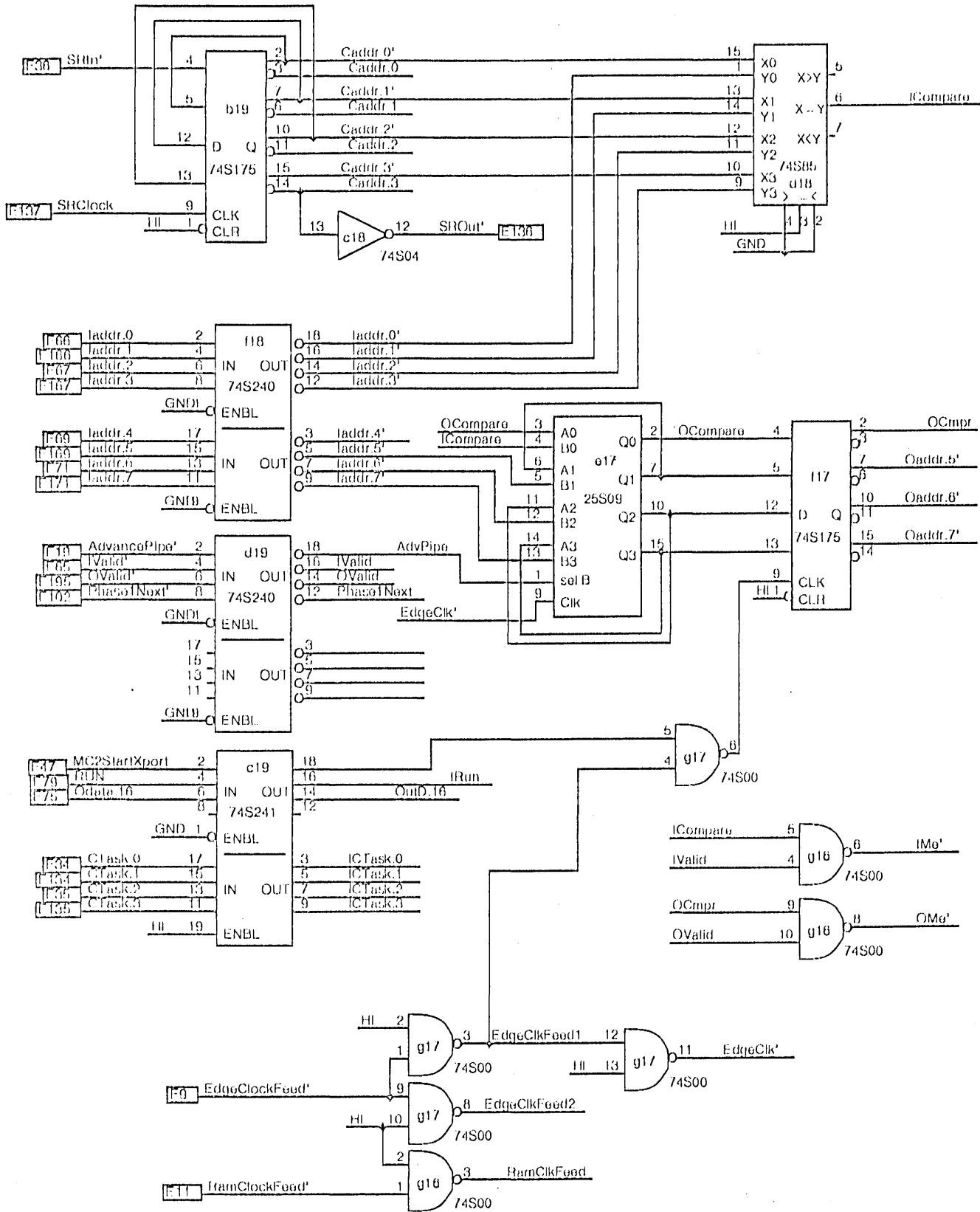
Other group:

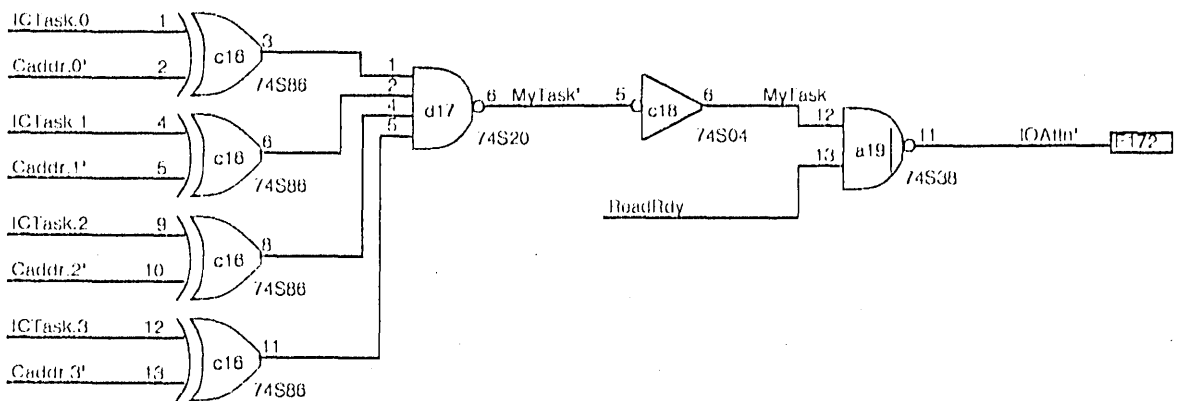
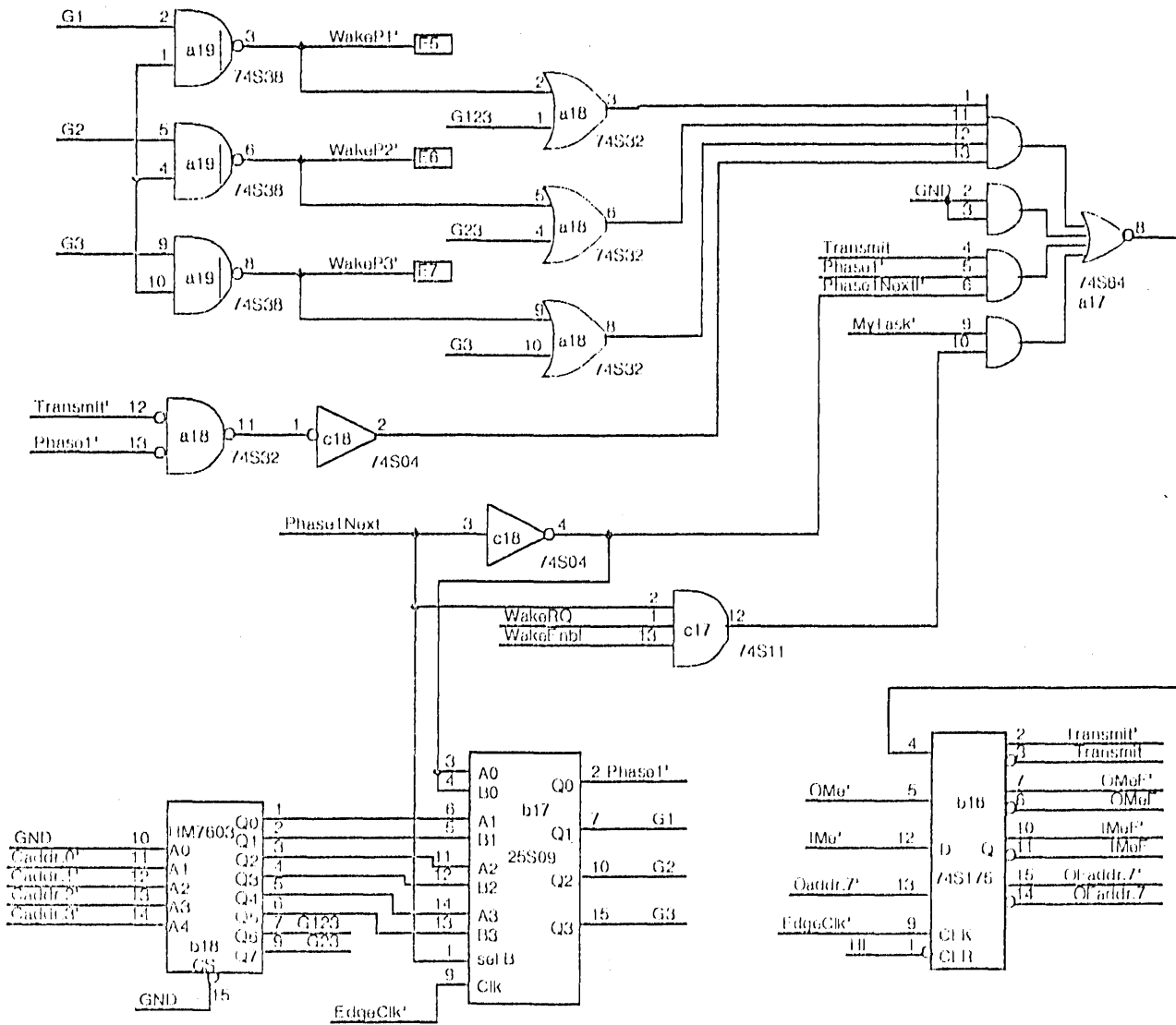
Pgrp: .X.X.I.C.C.

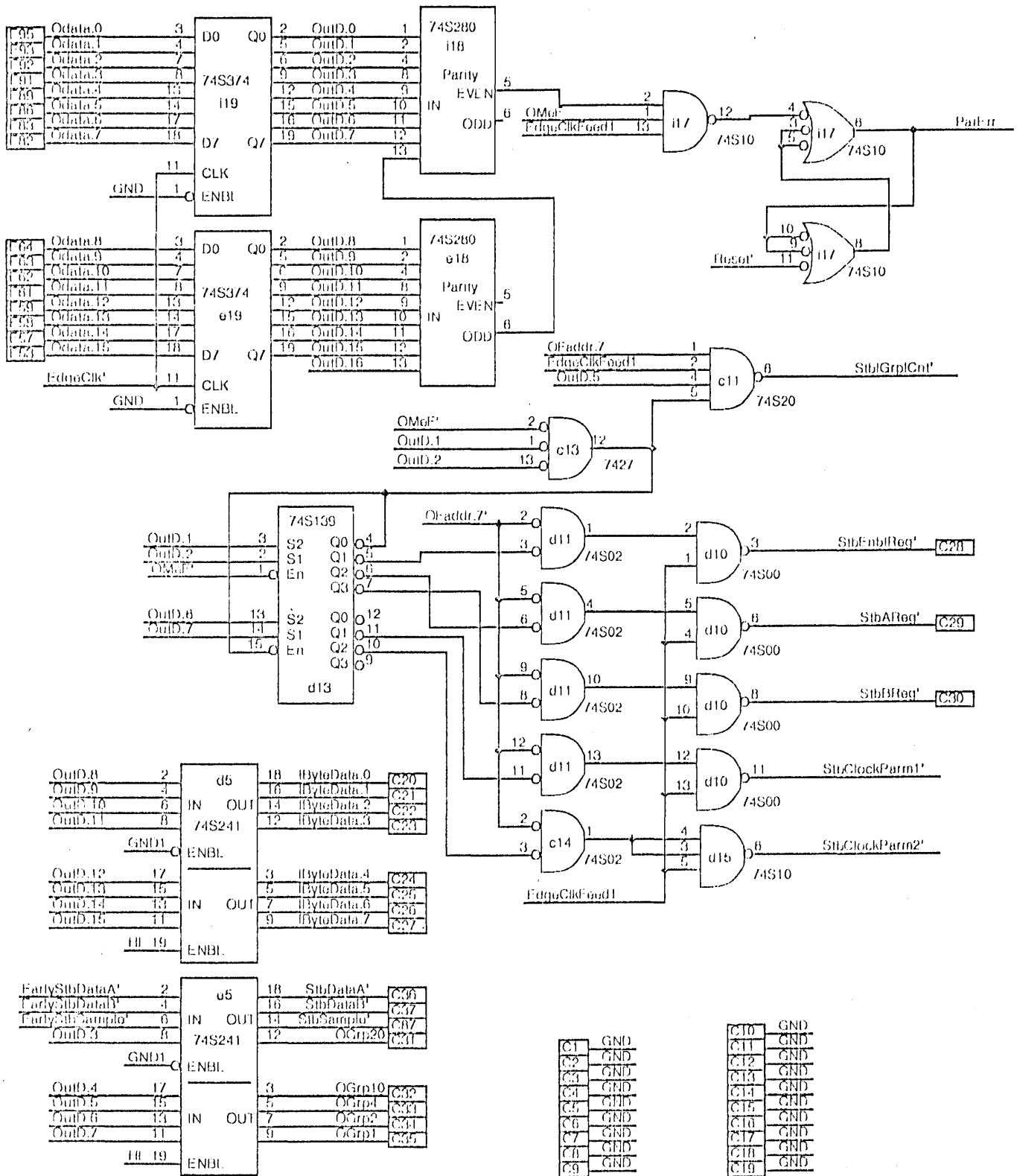
CC -- Clock parameter select:

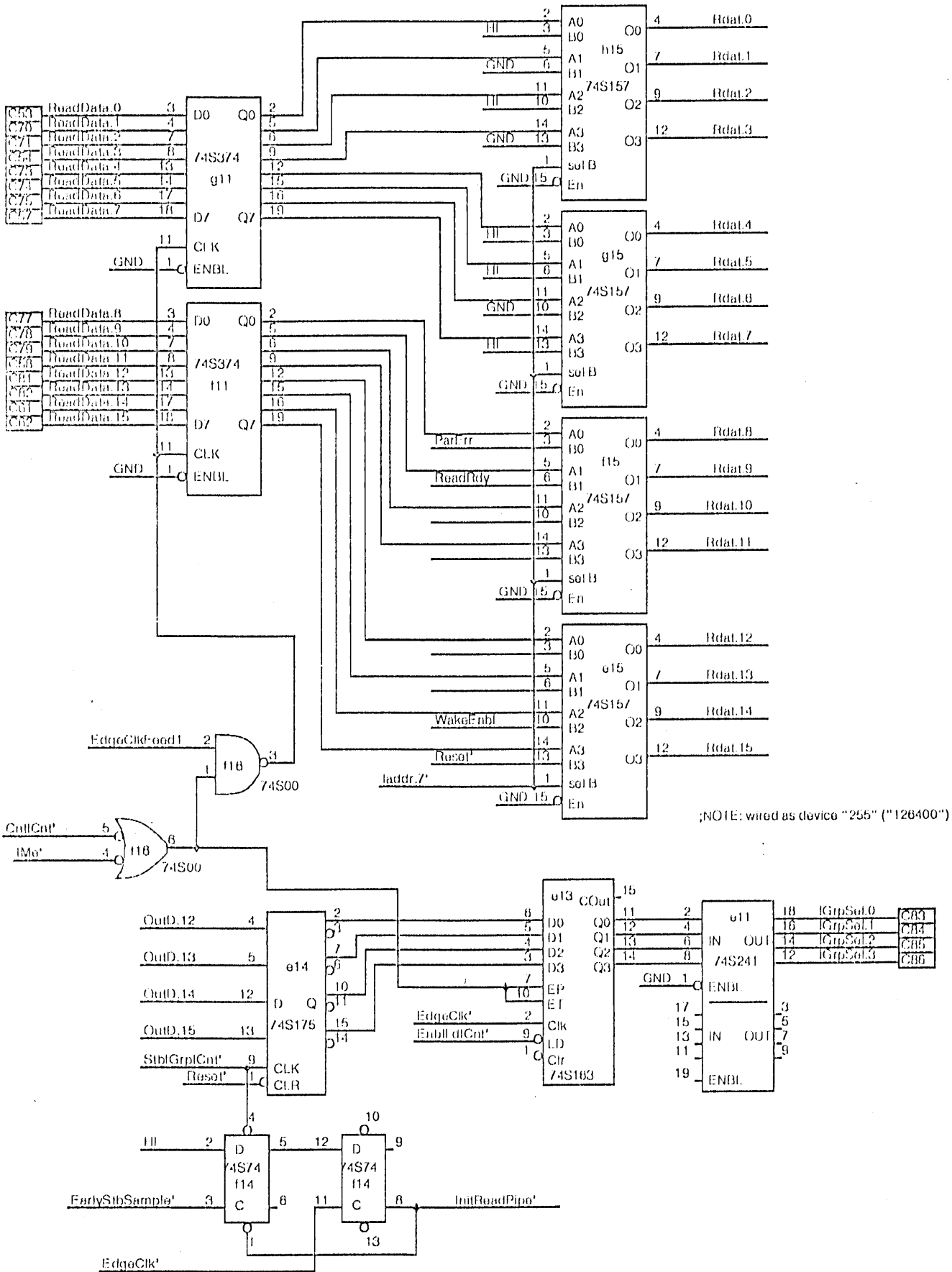
- 0 -- None (nop)
- 1 -- Load Data into clock Parameter Reg. 1
- 2 -- Load Data into clock Parameter Reg. 2
- 3 -- Load Data into clock Parameter Reg. 3

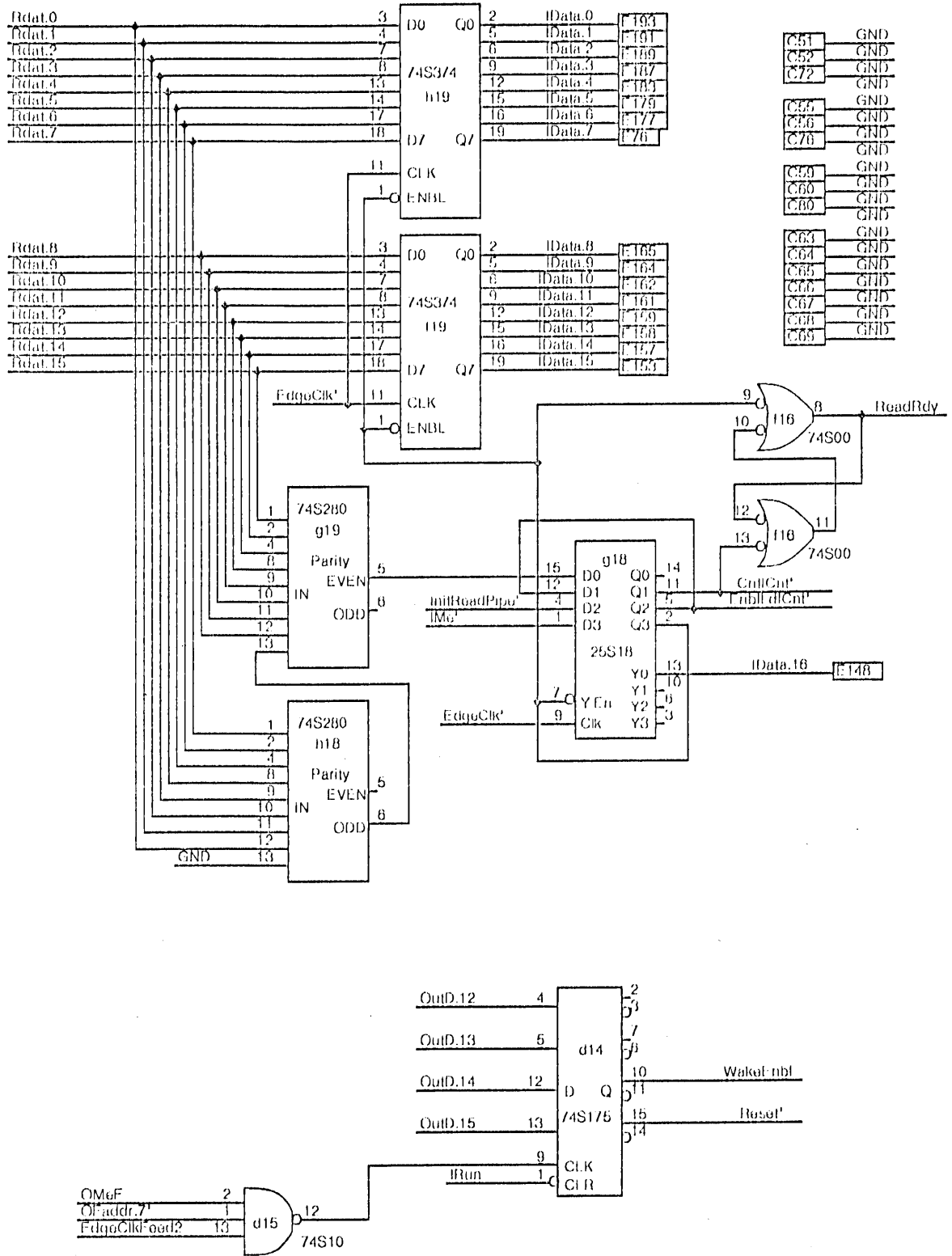
I -- Load Data into Input Group Select Counter

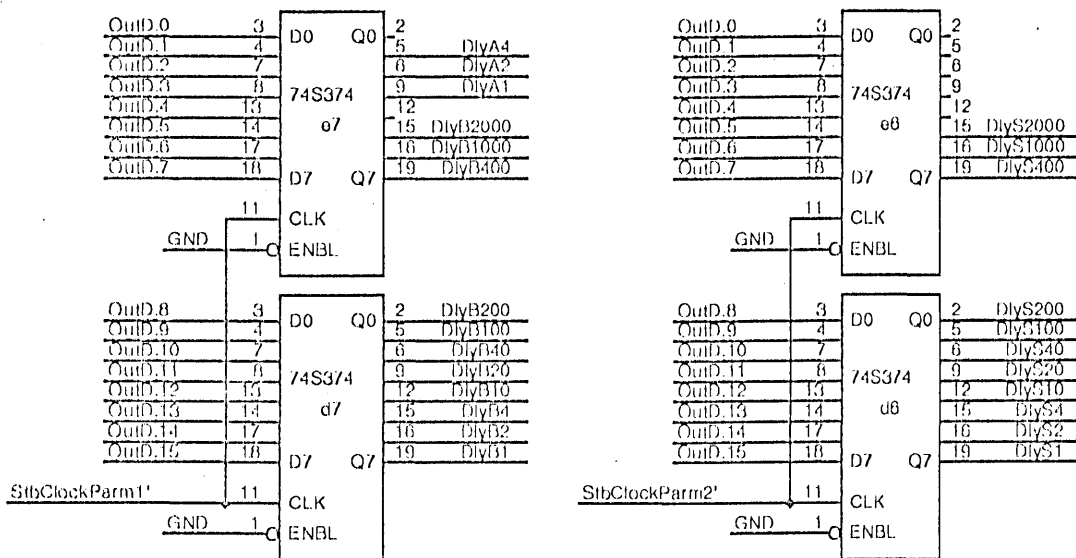
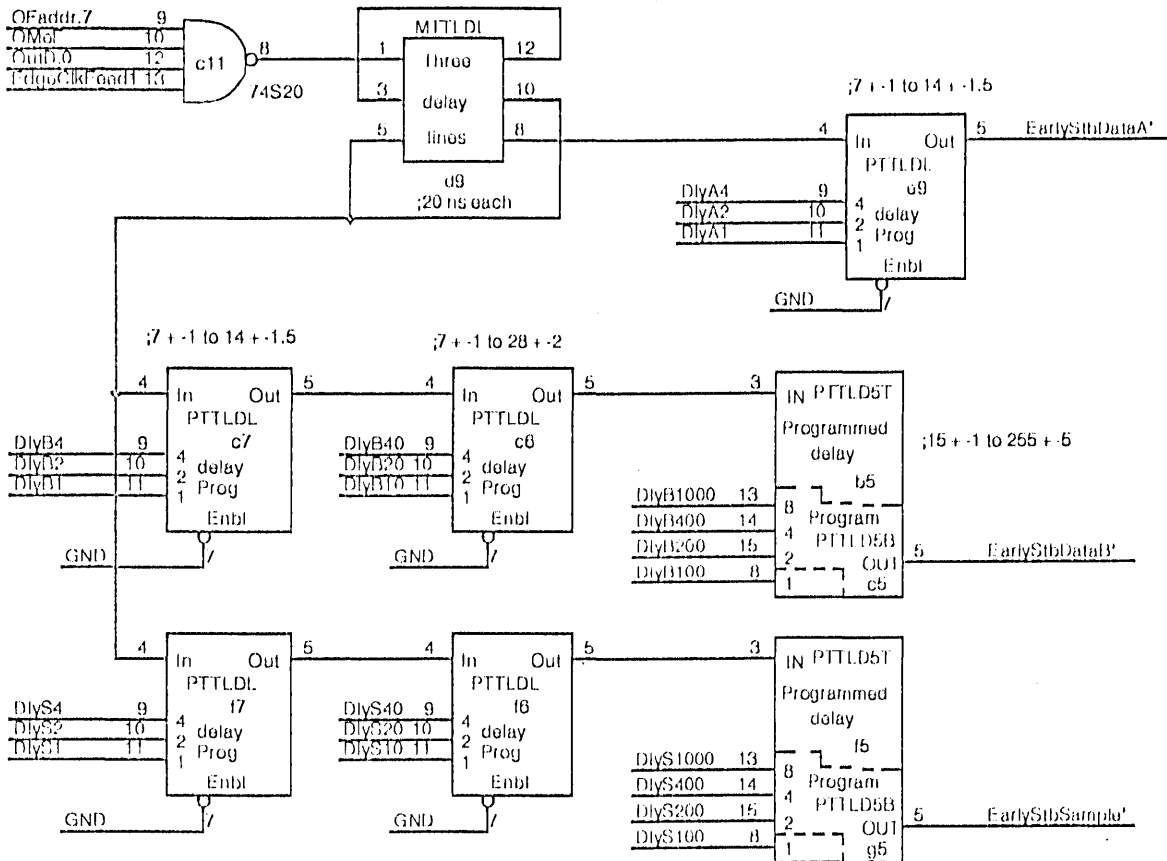




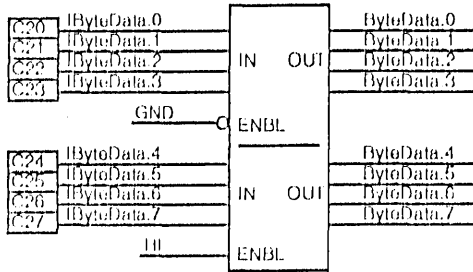




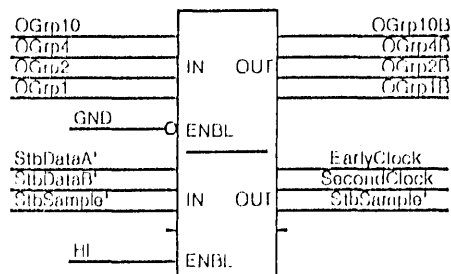




C63	RoadData.0
C76	RoadData.1
C71	RoadData.2
C54	RoadData.3
C73	RoadData.4
C74	RoadData.5
C75	RoadData.6
C57	RoadData.7



C77	RoadData.8
C78	RoadData.9
C79	RoadData.10
C58	RoadData.11
C81	RoadData.12
C82	RoadData.13
C61	RoadData.14
C62	RoadData.15



StbEnblReq'	C28
StbAReq'	C29
StbBReq'	C30

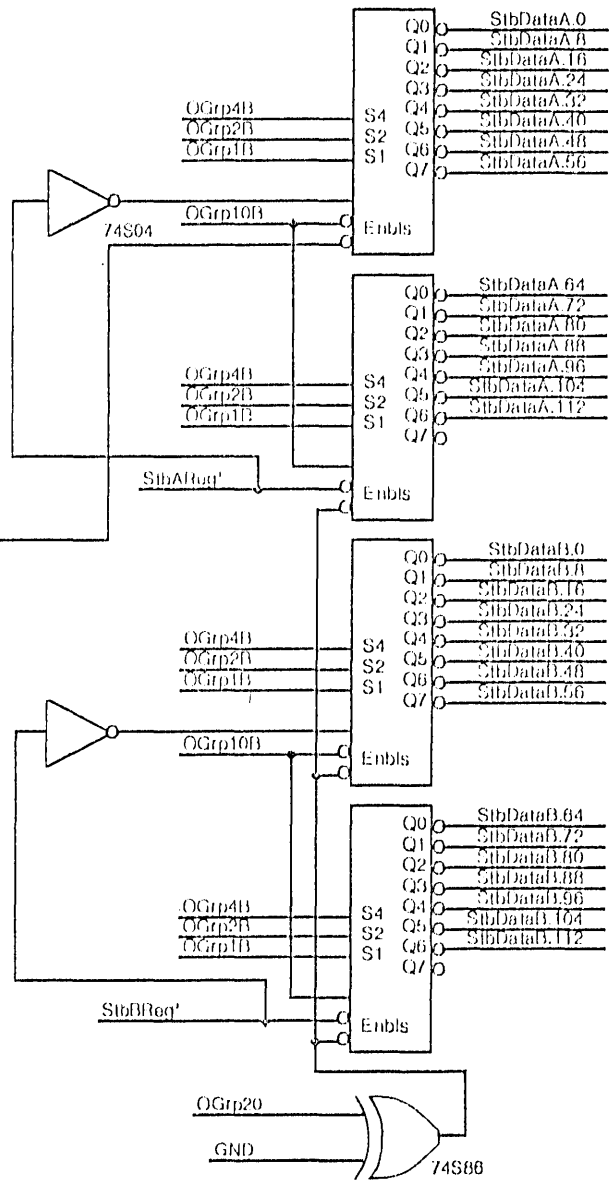
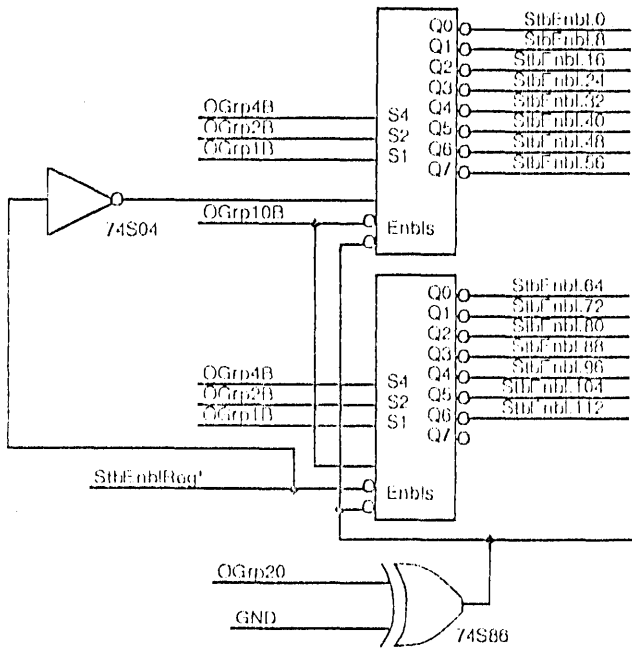
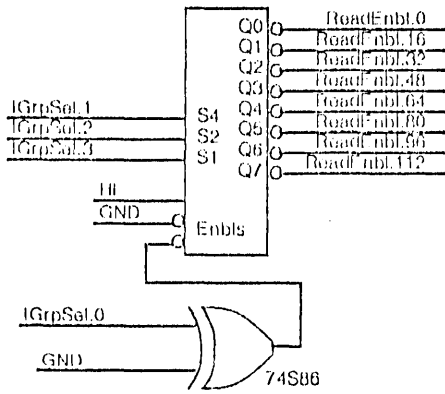
IGrpSel.0	C83
IGrpSel.1	C84
IGrpSel.2	C85
IGrpSel.3	C86

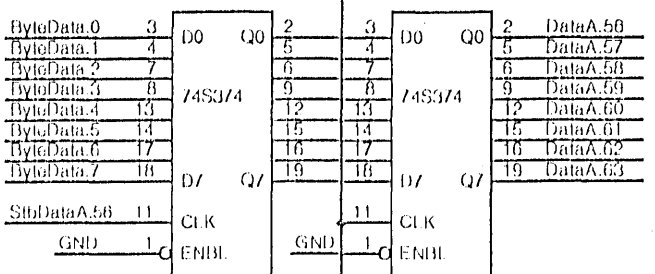
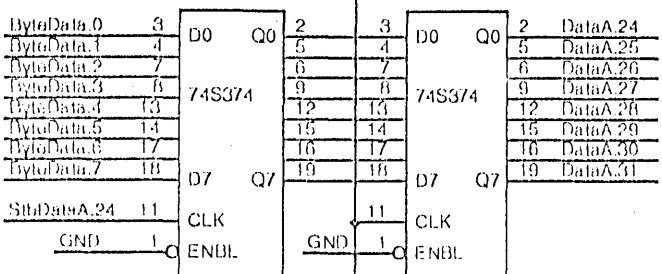
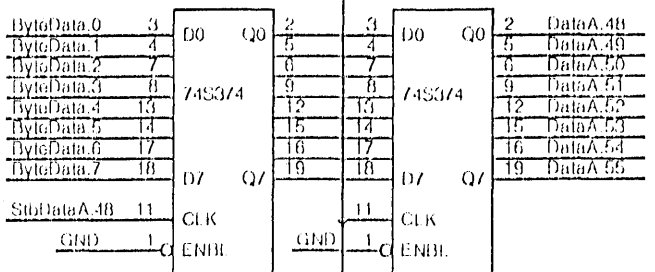
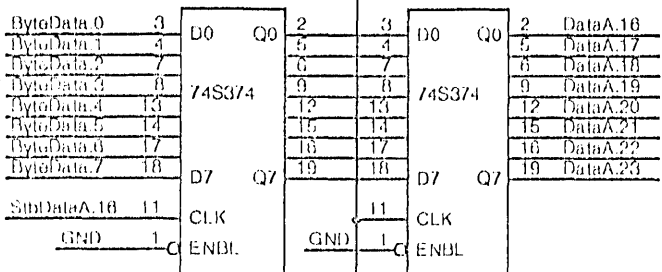
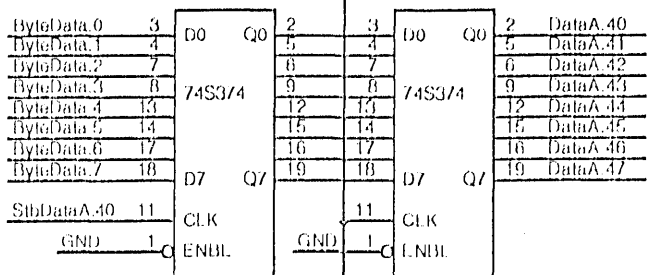
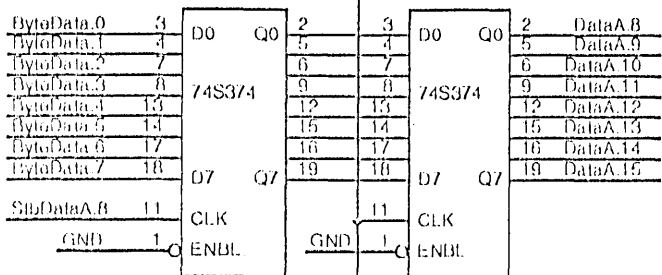
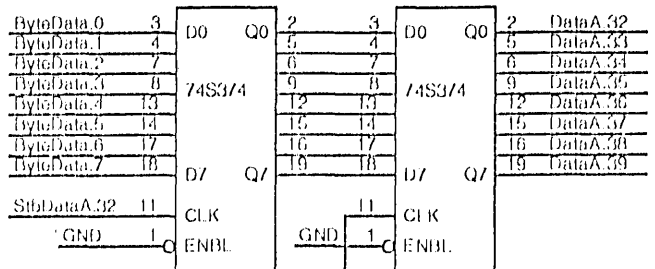
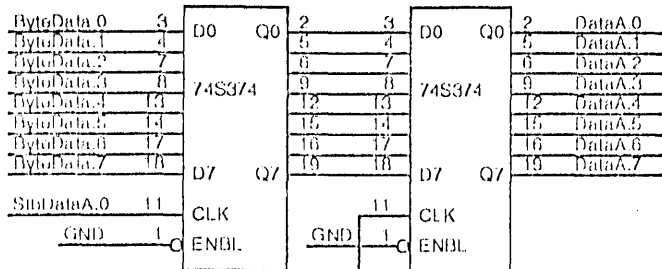
StbDataA'	C36
StbDataB'	C37
StbSample'	C37
OGrp20	C31

OGrp10	C32
OGrp4	C33
OGrp2	C34
OGrp1	C35

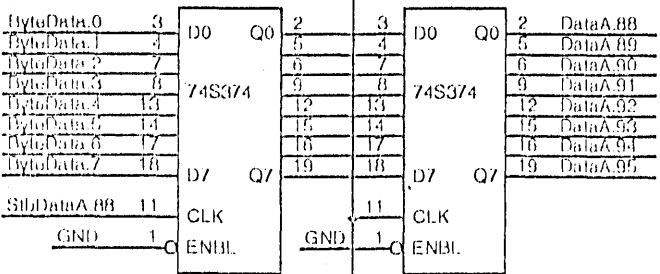
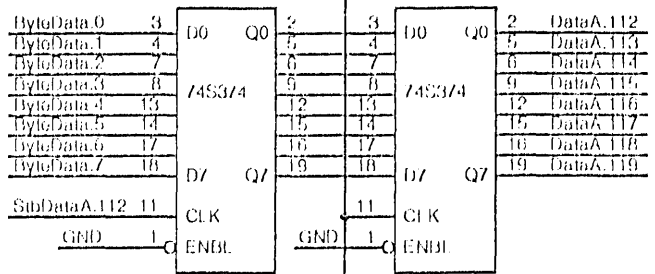
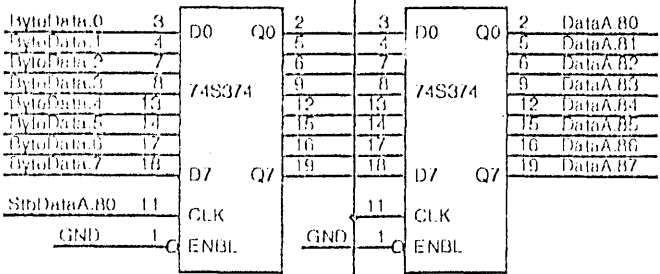
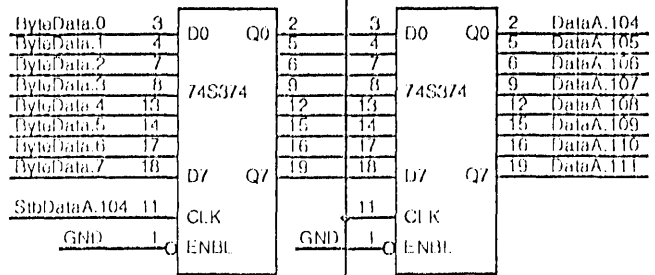
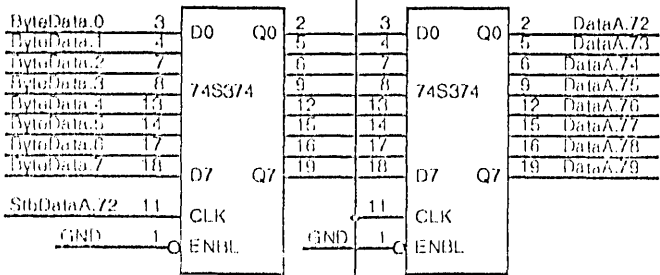
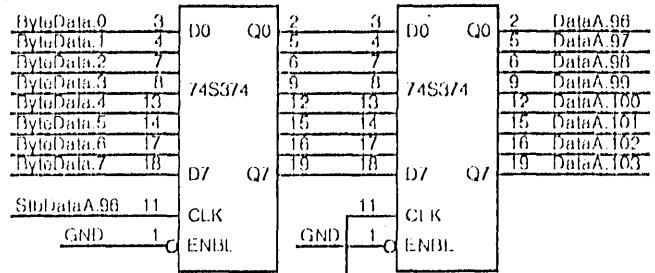
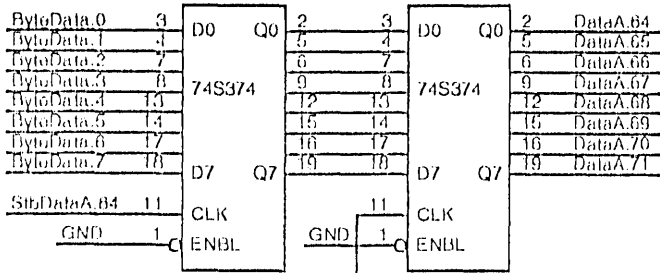
C1	GND	C51	GND
C2	GND	C52	GND
C3	GND	C72	GND
C4	GND		GND
C5	GND	C55	GND
C6	GND	C56	GND
C7	GND	C76	GND
C8	GND		GND
C9	GND		GND
C10	GND	C59	GND
C11	GND	C60	GND
C12	GND	C60	GND
C13	GND		GND
C14	GND	C63	GND
C15	GND	C64	GND
C16	GND	C65	GND
C17	GND	C66	GND
C18	GND	C67	GND
C19	GND	C68	GND
		C69	GND



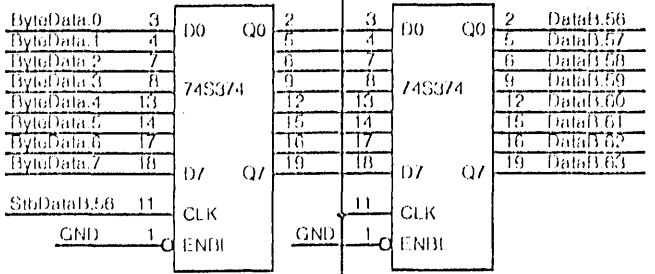
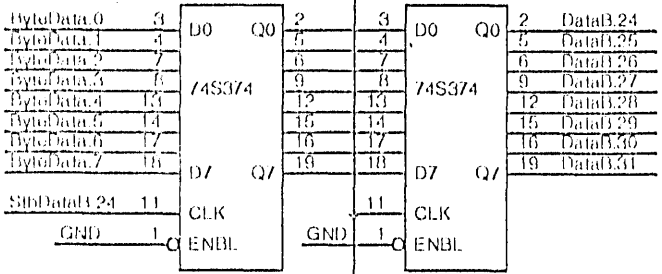
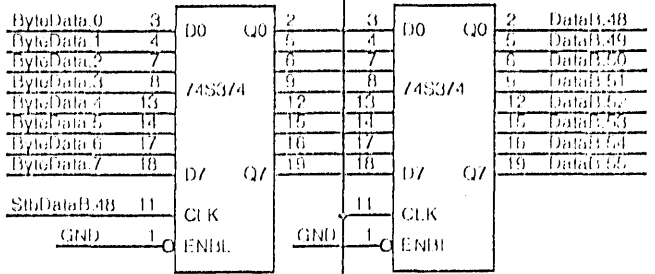
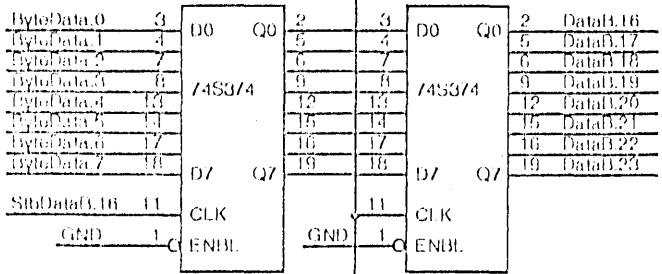
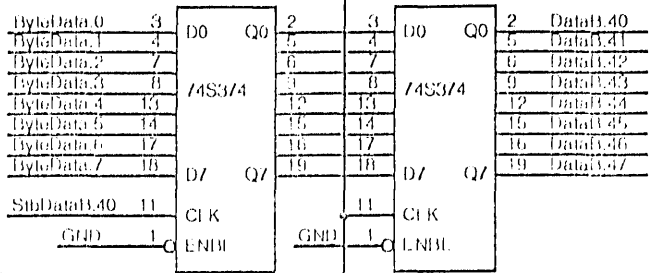
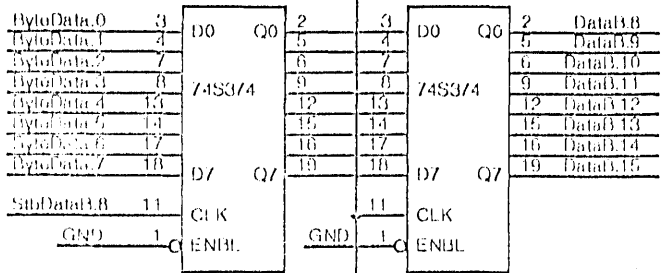
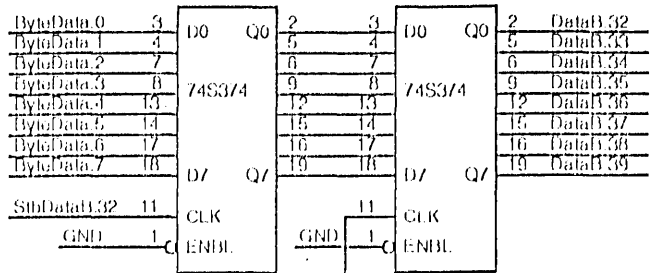
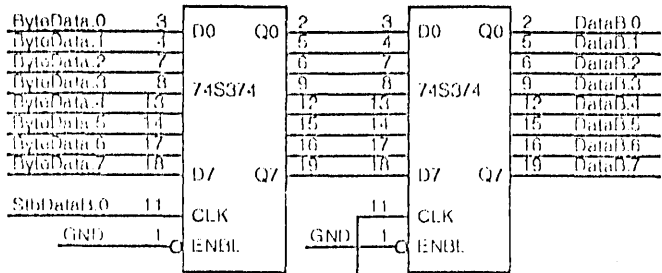




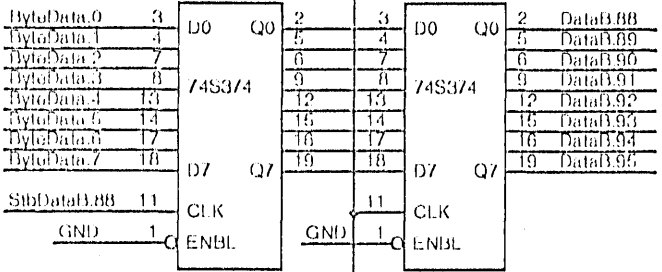
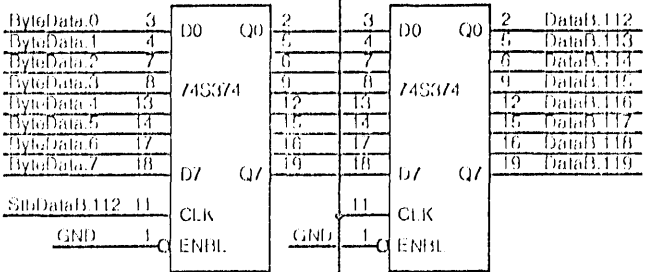
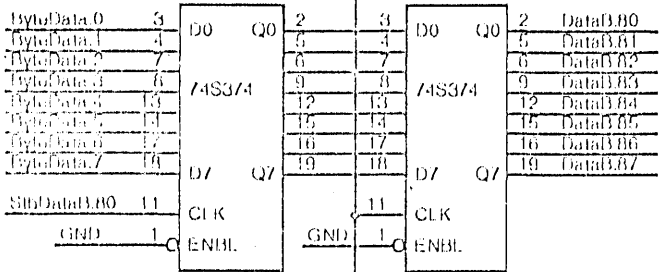
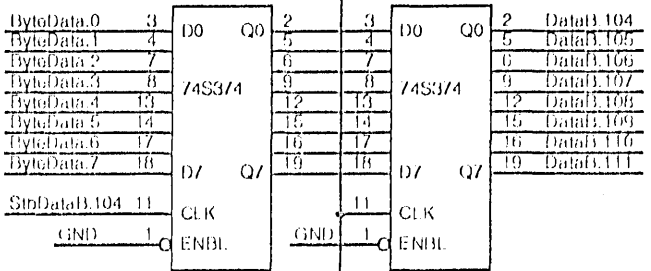
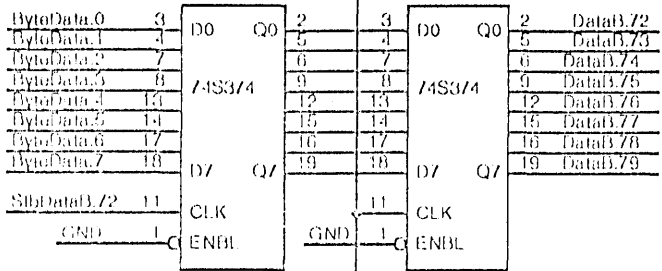
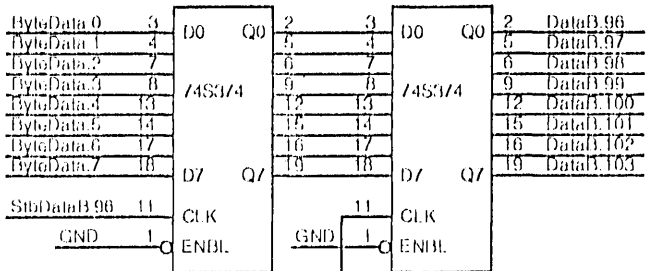
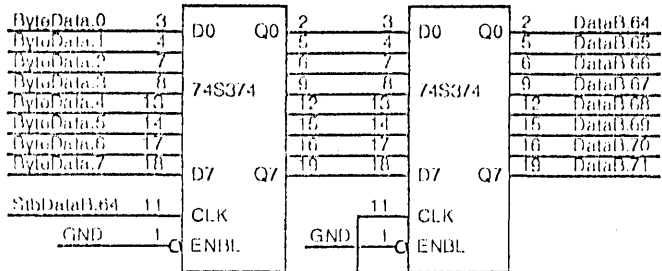
EarlyClock



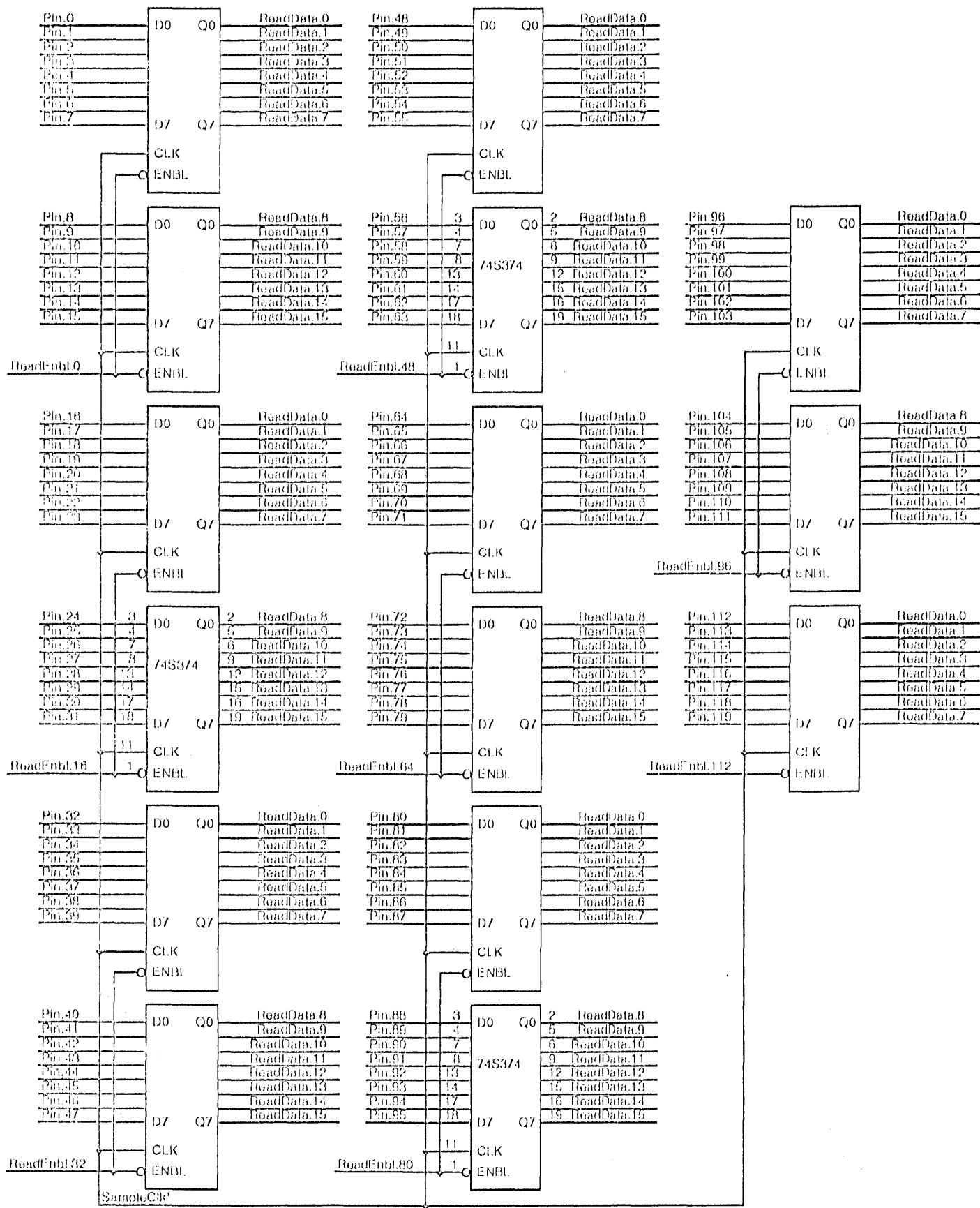
EarlyClock



SecondClock



SecondClock



FILE: CTST34

TITLE: Chip tester

Board:

Press File Written:15 Oct 80 18:49:11

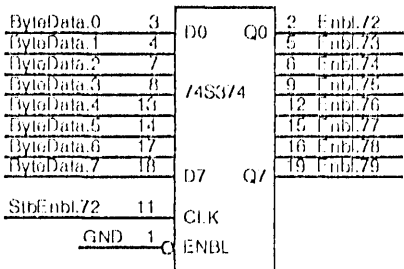
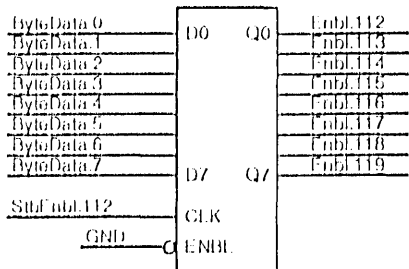
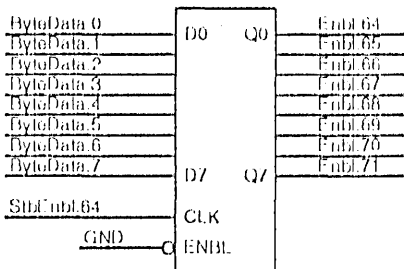
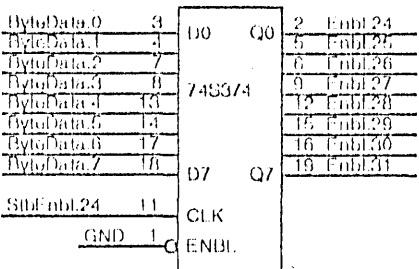
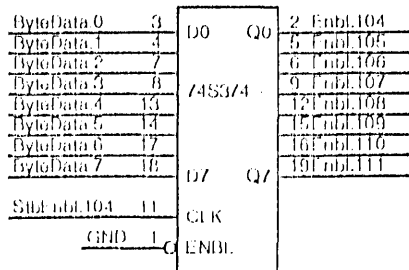
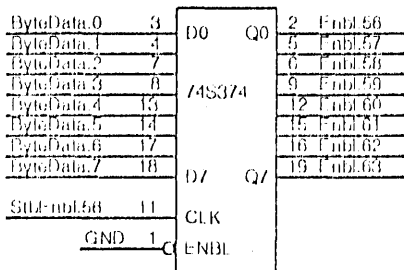
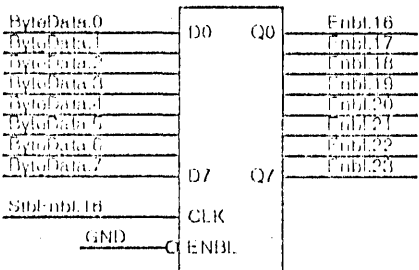
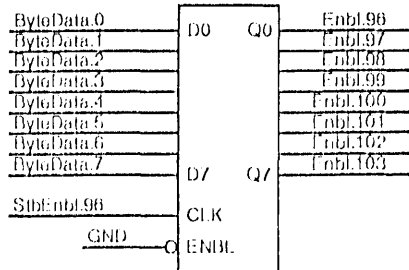
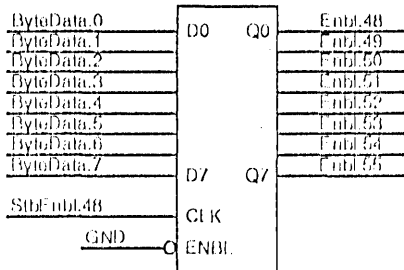
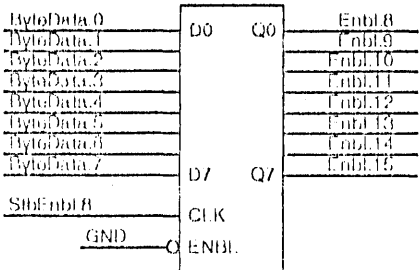
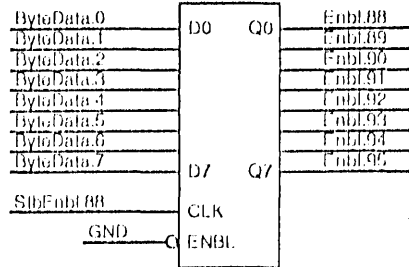
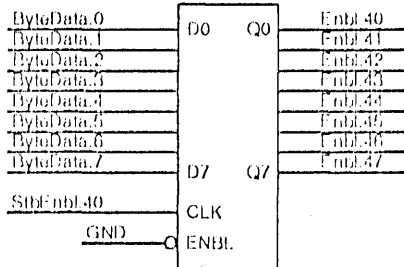
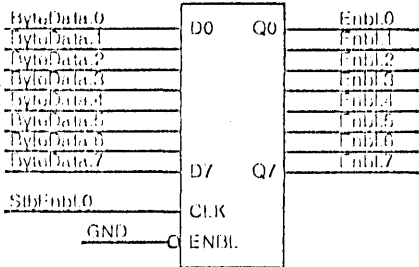
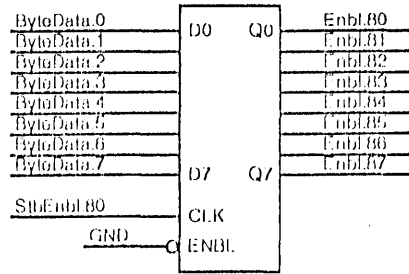
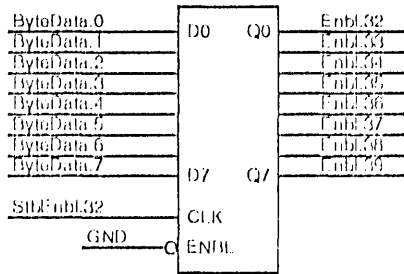
DATE:15-Oct-80 18:48

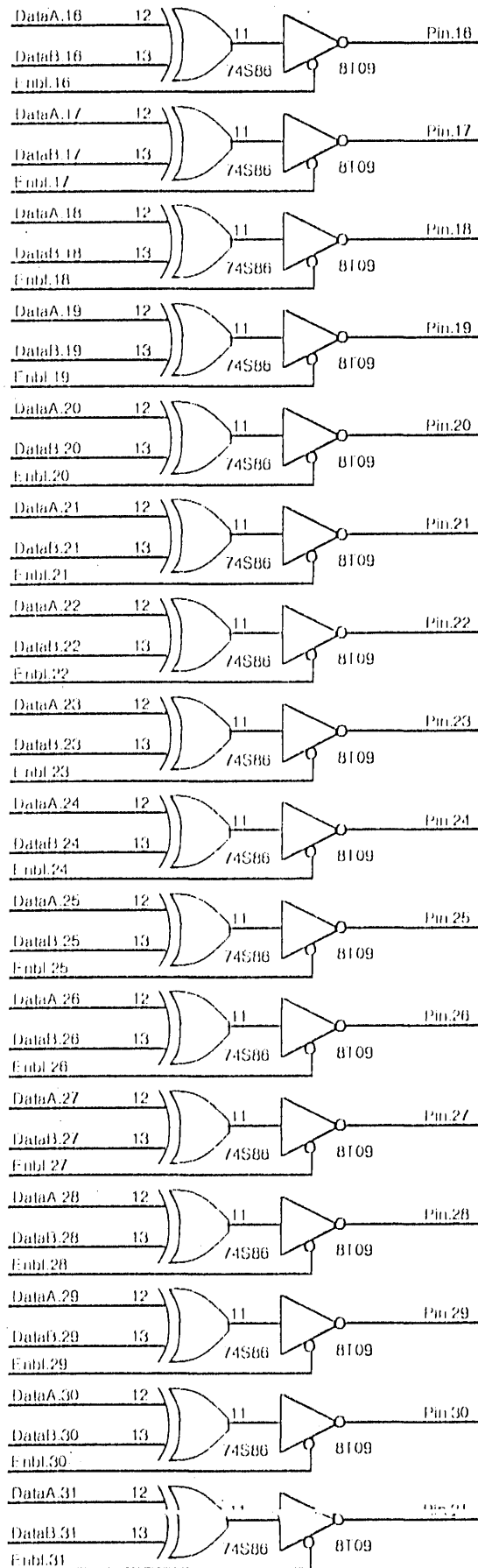
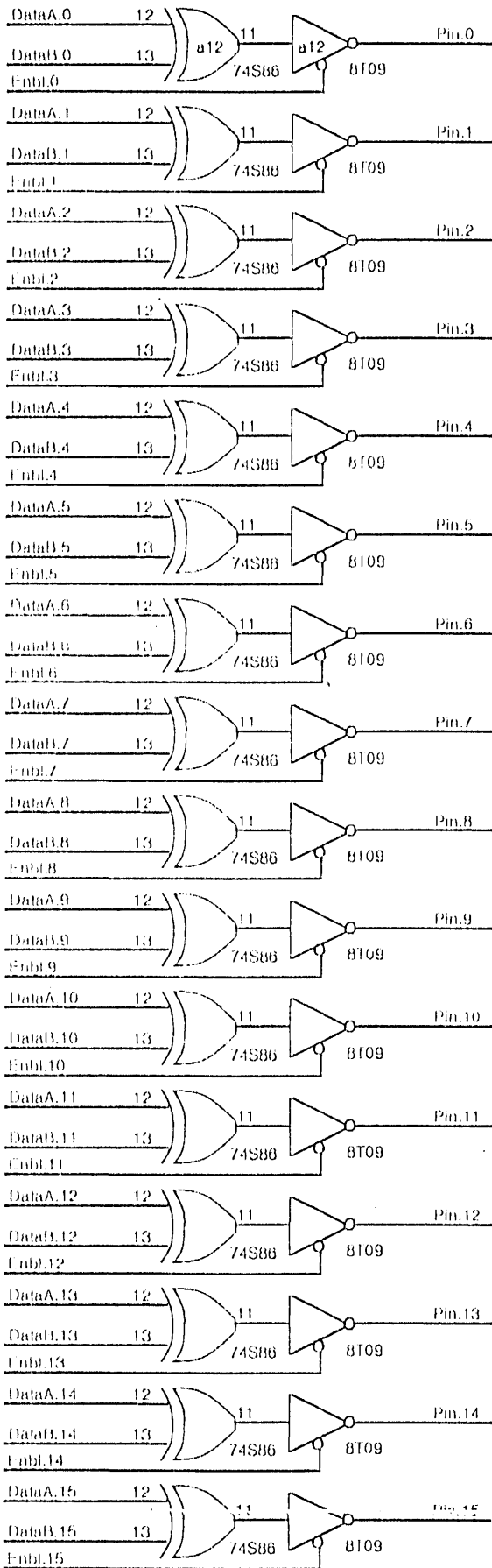
Chip Pin Enables  
Chip Pin Catch Reg

Ctest-2

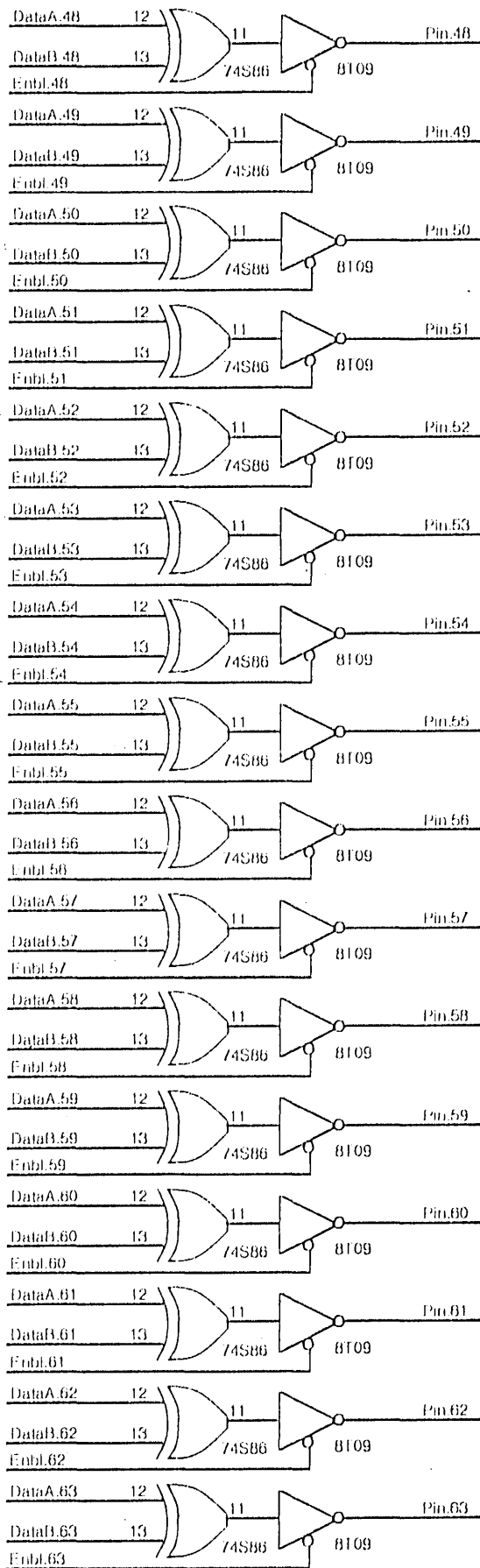
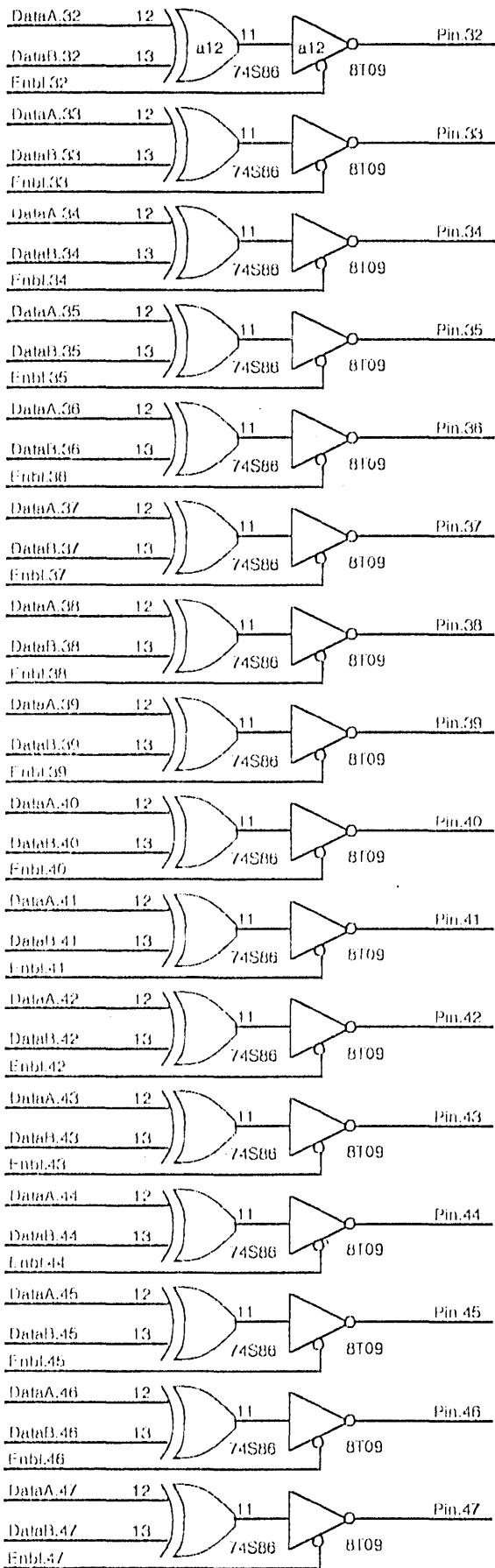
LIBRARY: TTL

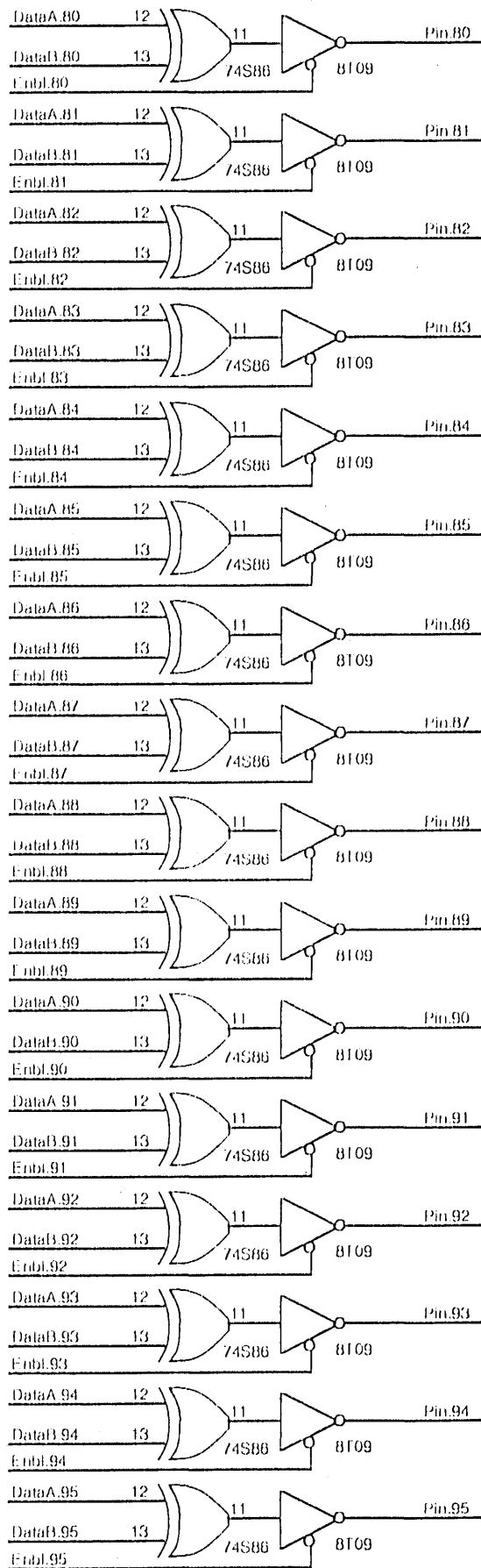
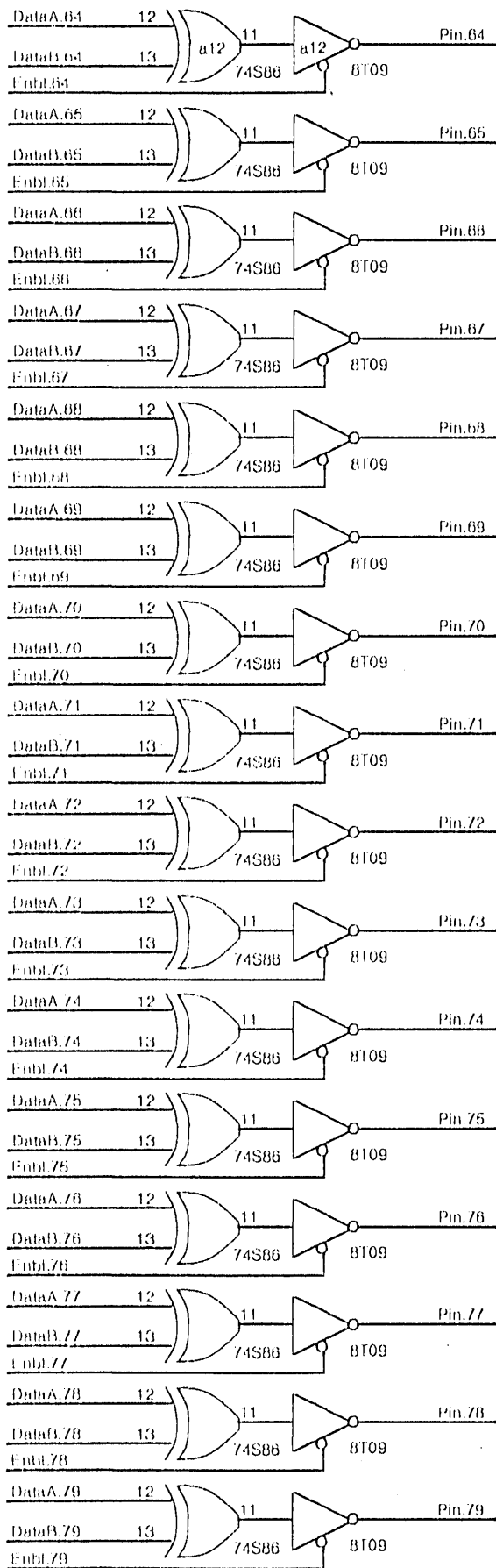
Drawn by PARSNIP

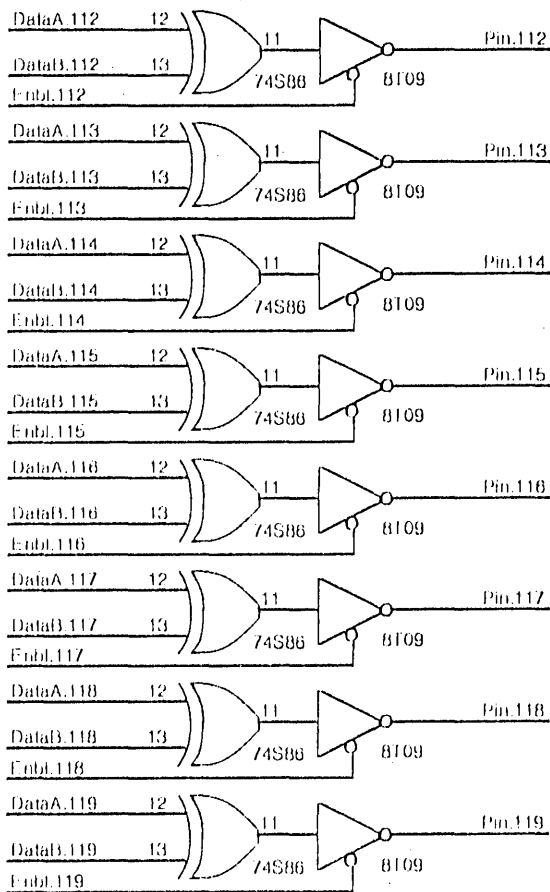
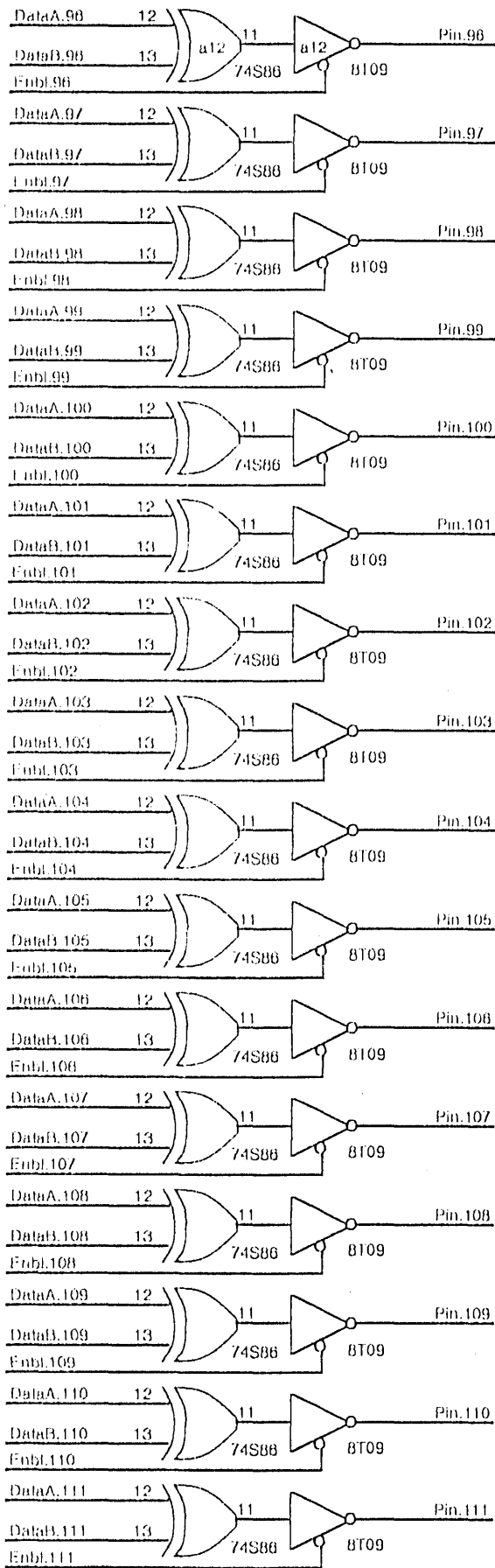












Pin.0	F2	Pin.64	F102
Pin.1	F3	Pin.65	F103
Pin.2	F4	Pin.66	F104
Pin.3	F5	Pin.67	F105
Pin.4	F6	Pin.68	F106
Pin.5	F7	Pin.69	F107
Pin.6	F8	Pin.70	F108
Pin.7	F9	Pin.71	F109
Pin.8	F10	Pin.72	F110
Pin.9	F11	Pin.73	F111
Pin.10	F12	Pin.74	F112
Pin.11	F13	Pin.75	F113
Pin.12	F14	Pin.76	F114
Pin.13	F15	Pin.77	F115
Pin.14	F16	Pin.78	F116
Pin.15	F17	Pin.79	F117
Pin.16	F18	Pin.80	F118
Pin.17	F19	Pin.81	F119
Pin.18	F20	Pin.82	F120
Pin.19	F21	Pin.83	F121
Pin.20	F22	Pin.84	F122
Pin.21	F23	Pin.85	F123
Pin.22	F24	Pin.86	F124
Pin.23	F25	Pin.87	F125
Pin.24	F26	Pin.88	F126
Pin.25	F27	Pin.89	F127
Pin.26	F28	Pin.90	F128
Pin.27	F29	Pin.91	F129
Pin.28	F30	Pin.92	F130
Pin.29	F31	Pin.93	F131
Pin.30	F32	Pin.94	F132
Pin.31	F33	Pin.95	F133
Pin.32	F34	Pin.96	F134
Pin.33	F35	Pin.97	F135
Pin.34	F36	Pin.98	F136
Pin.35	F37	Pin.99	F137
Pin.36	F38	Pin.100	F138
Pin.37	F39	Pin.101	F139
Pin.38	F40	Pin.102	F140
Pin.39	F41	Pin.103	F141
Pin.40	F42	Pin.104	F142
Pin.41	F43	Pin.105	F143
Pin.42	F44	Pin.106	F144
Pin.43	F45	Pin.107	F145
Pin.44	F46	Pin.108	F146
Pin.45	F47	Pin.109	F147
Pin.46	F48	Pin.110	F148
Pin.47	F49	Pin.111	F149
Pin.48	F50	Pin.112	F150
Pin.49	F51	Pin.113	F151
Pin.50	F52	Pin.114	F152
Pin.51	F53	Pin.115	F153
Pin.52	F54	Pin.116	F154
Pin.53	F55	Pin.117	F155
Pin.54	F56	Pin.118	F156
Pin.55	F57	Pin.119	F157
Pin.56	F58	Pin.120	F158
Pin.57	F59	Pin.121	F159
Pin.58	F60	Pin.122	F160
Pin.59	F61	Pin.123	F161
Pin.60	F62	Pin.124	F162
Pin.61	F63	Pin.125	F163
Pin.62	F64	Pin.126	F164
Pin.63	F65	Pin.127	F165

Pin Numbers Wrong!

FILE: CTST29

TITLE: Chip tester

DATE:15-Oct-80 19:05

Chip Pin Enables  
Chip Pin Catch Reg

Board:  
Ctest-2

Press File Written:15 Oct 80 19:30:56  
LIBRARY: TTL  
Drawn by PARSNIP