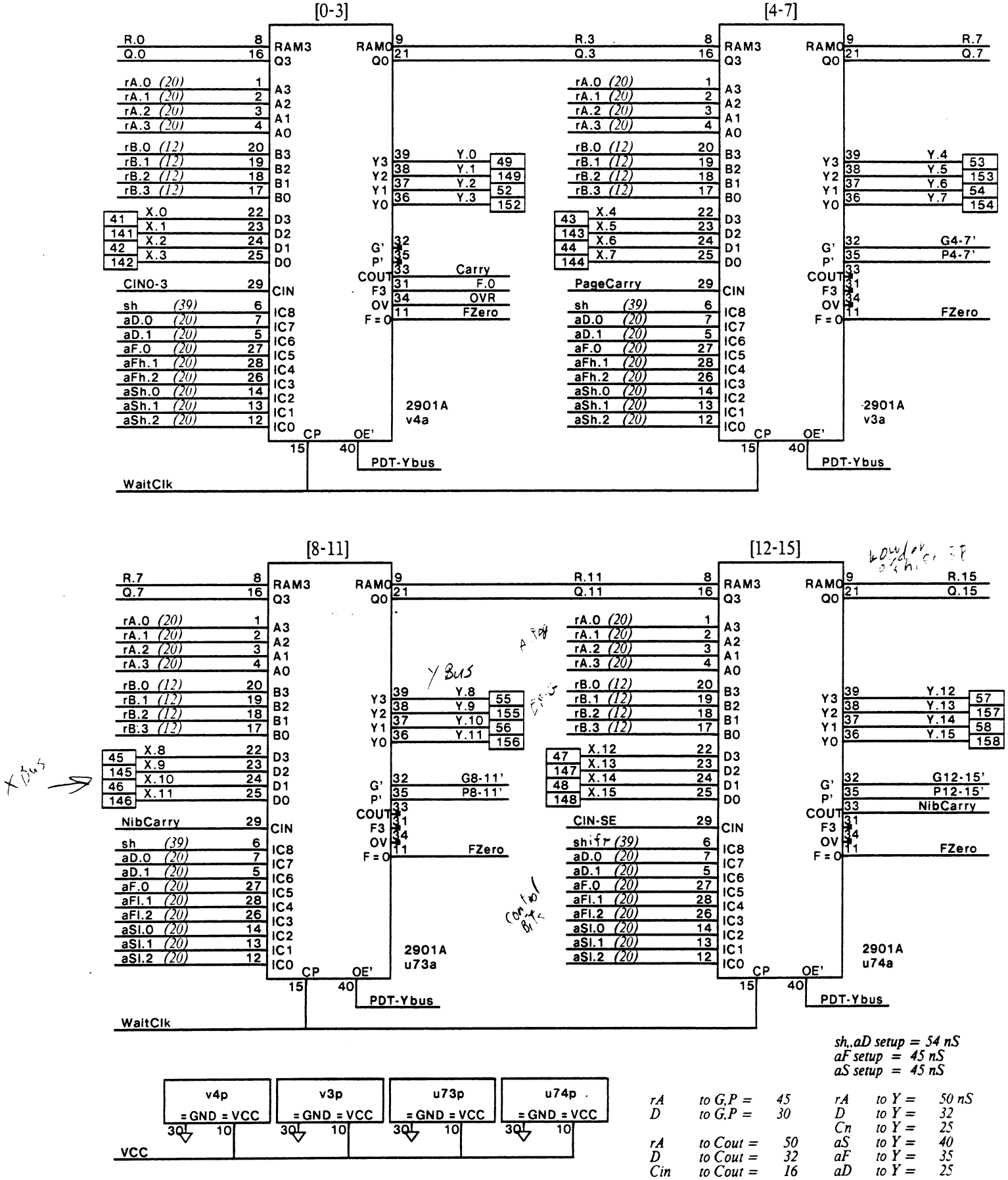
Dandelion Central Processor (CP)

pLionHead# #.sil are the printed circuit board schematics.
sLionHead# #.sil are the stichweld board schematics.
LionHead# #.sily are documentation pages.

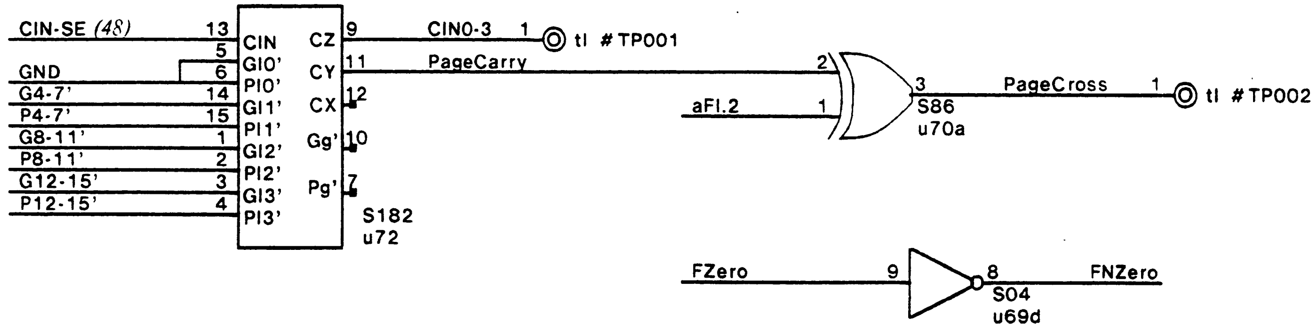
Also see:

[Iris]<Workstation>LH># LionHead-M.press	-- s or p schematics
[Iris]<Workstation>LH>CPProms-K.dm	--Proms
[Iris]<Workstation>LH>DMR.press	--Dandelion Microcode Reference
[Iris]<Workstation>LH>CPCheckOut.press	
[Iris]<Workstation>LH>DLionIORules.press	--Rules for IO controllers



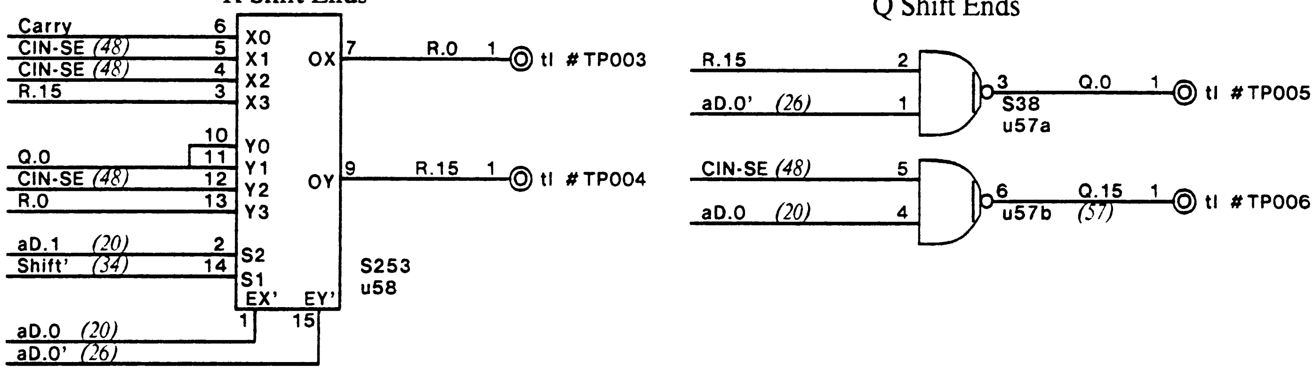
XEROX SDD	Project Dandelion	2901 chips	File pLionHead01.sil	Designer Garner	Rev M	Date 8/23/80	Page 01

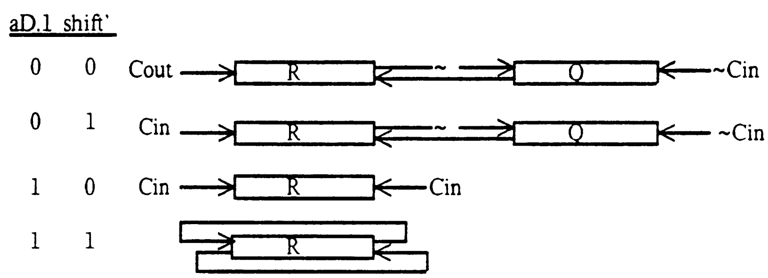
2901 Carry Lookahead



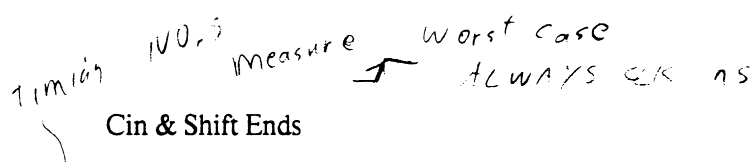
R Shift Ends

Q Shift Ends

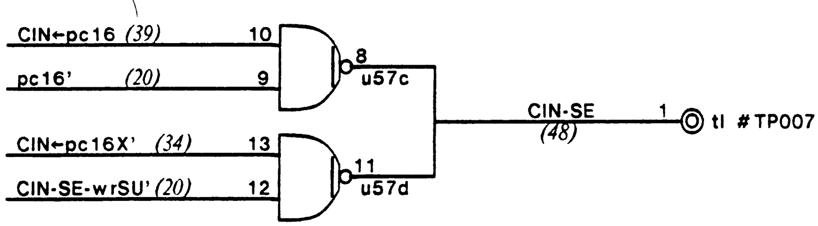




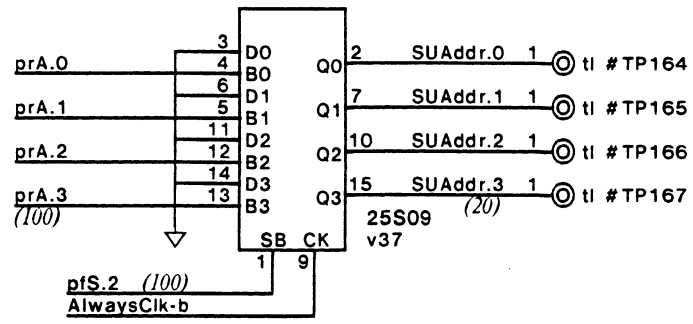
aD.0 = 0 implies right shift

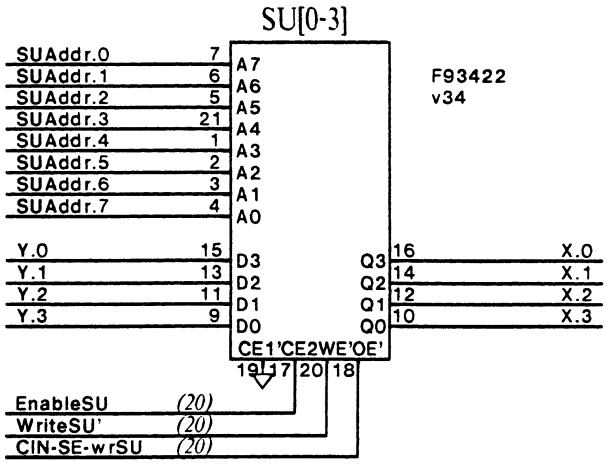


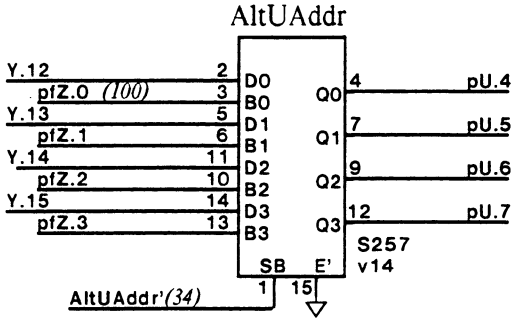
Cin & Shift Ends

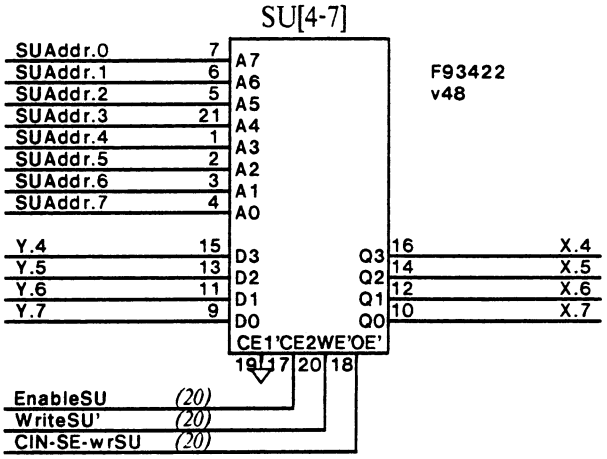


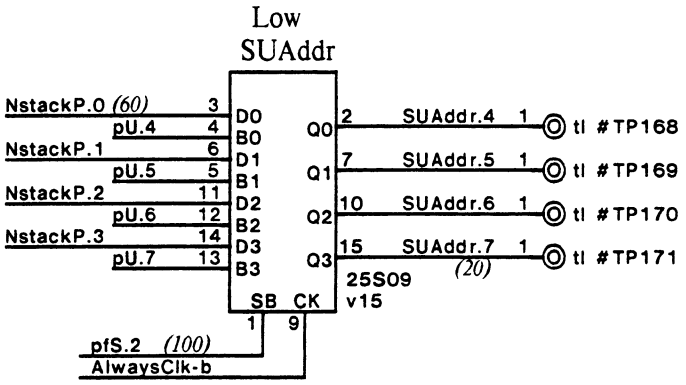
XEROX SDD	Project Dandelion	Lookahead. Shift Ends. Cin	File pLionHead02.sil	Designer Garner	Rev M	Date 8/23/80	Page 02

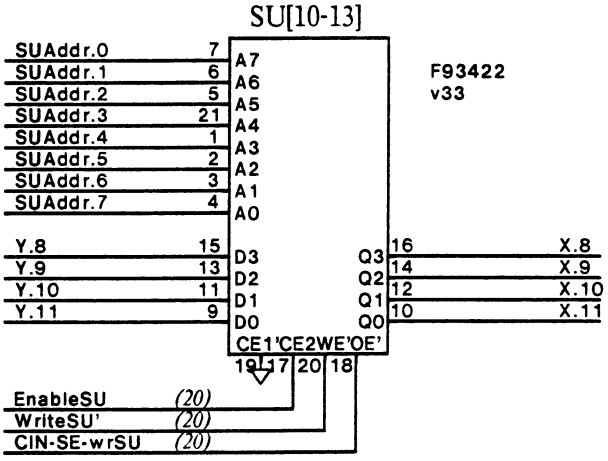












SU X-bus disable

15[3] ↑ to CIN-SE-wrSU (tPLH)
30 Output Disable
10 X-bus
55[3] = 58 nS

XBus ← SU = max(75,60) nS

17[3] ↑ to SUAddr
45 tAA
10 X-bus
72[3] = 75 nS

17[3] ↑ to CIN-SE-wrSU/EnableSU
30 F93422 OE'/CE2 to X-bus
10 X-bus
57[3]=60 nS

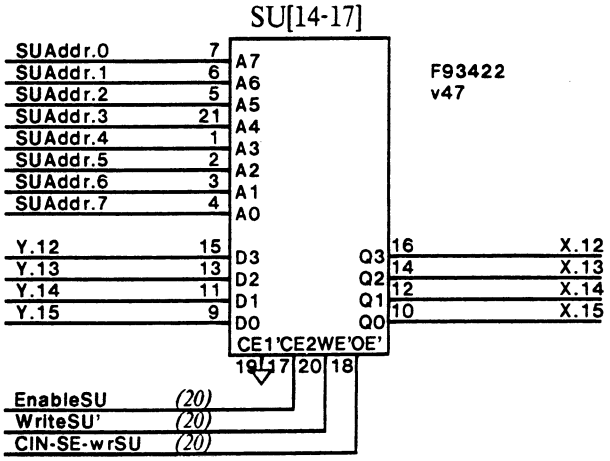
SU write setup

5[1] Data setup
39 WE
44[1] = 45 nS

AltUAddr setup

5[1] 25S09 setup
8[1] Y -> pU
13[2] = 15 nS (26 if LS257)

F93422 data t-hold = 5 nS



XEROX SDD	Project Dandelion	SU	File pLionHead03.sil	Designer Garner	Rev M	Date 12/4/80	Page 03

RH Setup

7[1]	S240
25[3]	S189 setup

32[4] = 36 nS

If the S189 must be used intead of the 29701, then place S240 between Xbus & S189 inputs.

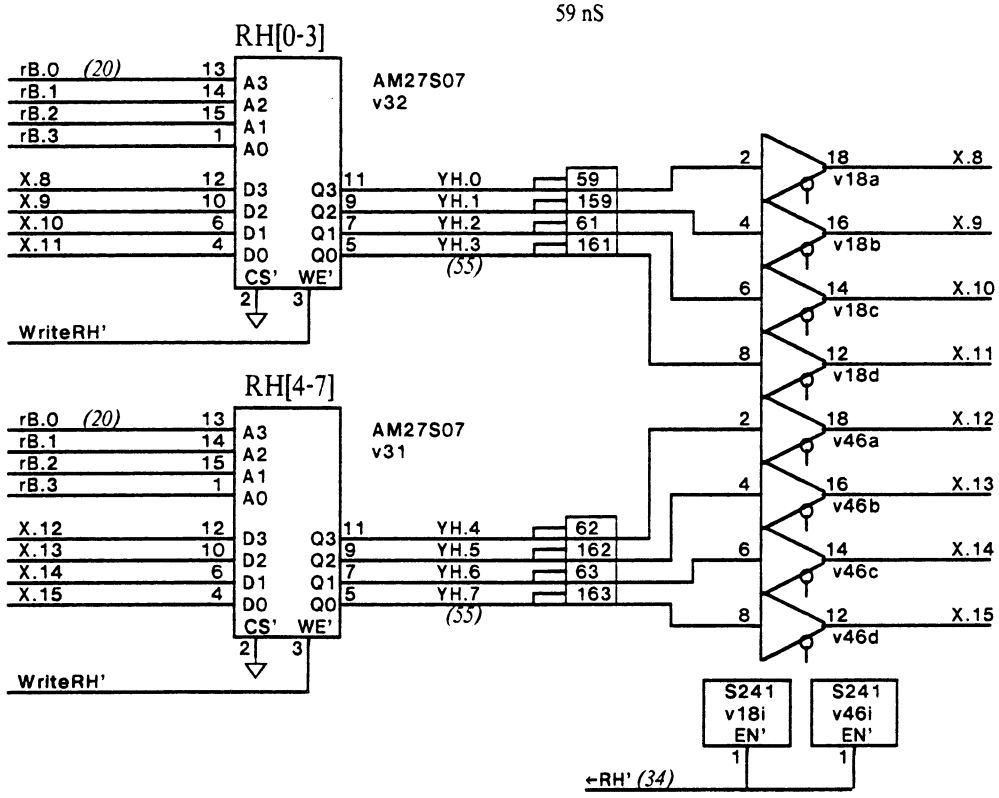
XBus ← RH = max(64, 59) nS

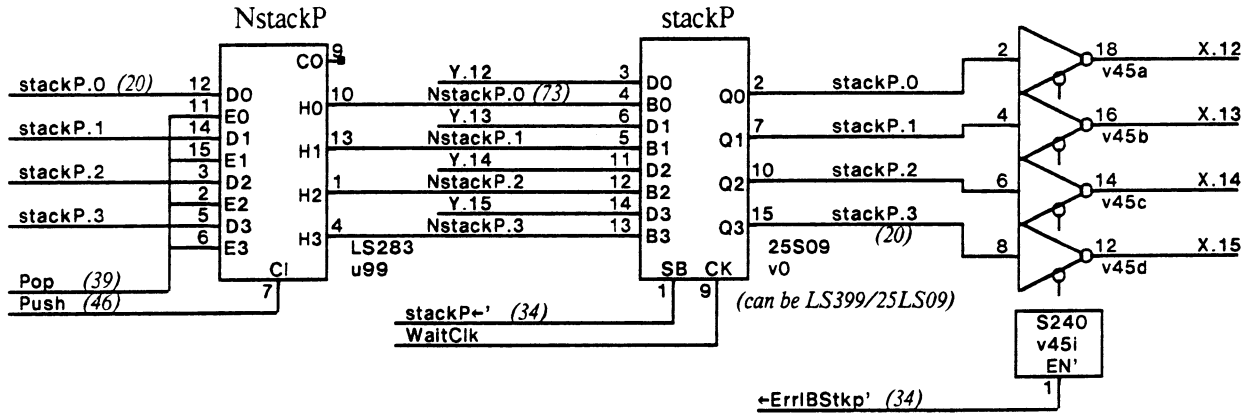
17[3]	↑ to rB'
35	S189 tAA (wr recovery = 35 nS)
9	YH to X
10	X-bus

71[3] = 74 nS

34	↑ to ←RH'
15	S241 EN' to X-bus
10	X-bus

59 nS





XBus ← stackP = max(59, 38) nS

17[3]	↑ to stackP
7	S240 data to X-bus
10	X-bus

34[3] = 38 nS

34	↑ to ←ErrIntstackP'
15	S240 EN' to X-bus
10	X-bus

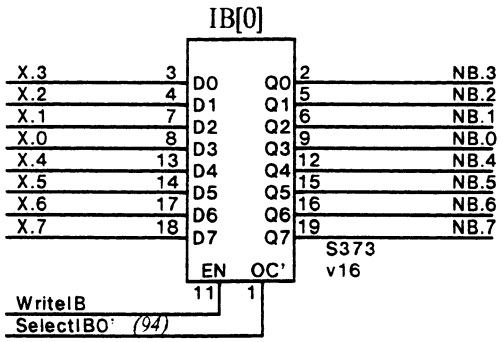
59 nS

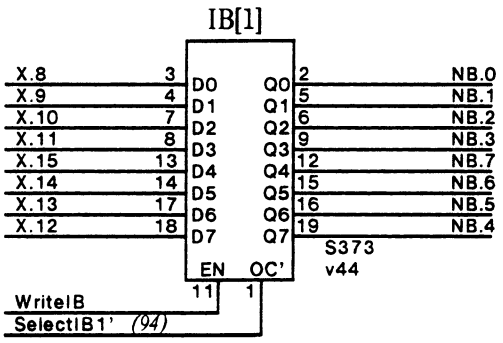
push timing

46	↑ to Push
24[3]	Push to NstackP
5[1]	25S09 setup

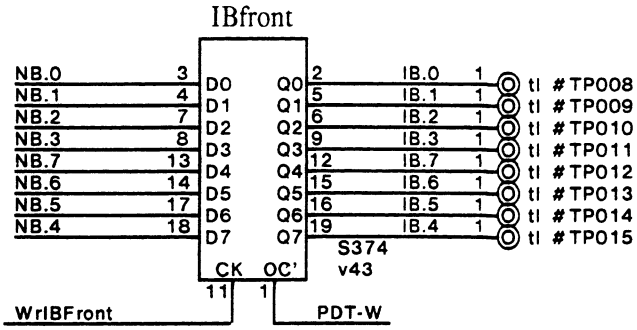
75[4] = 79 nS

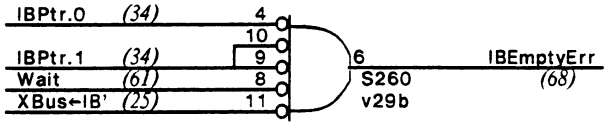
XEROX SDD	Project Dandelion	RH, stackP	File plLionHead04.sil	Designer Garner	Rev M	Date 8/24/80	Page 04





S373 t-hold = 10 nS. t-setup = 0 nS. (falling edge of WriteIB occurs 4 nS before rising edge of Clk.)

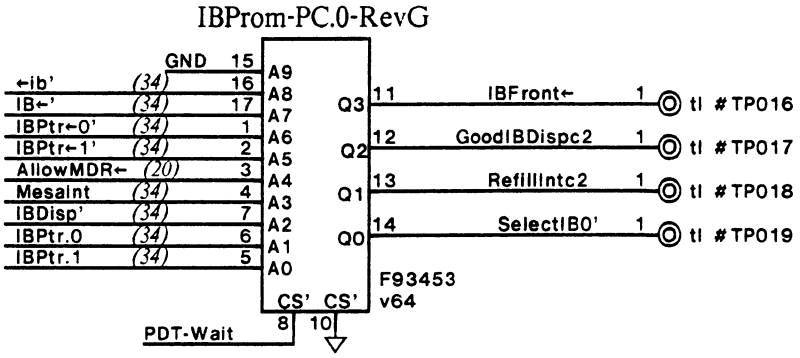


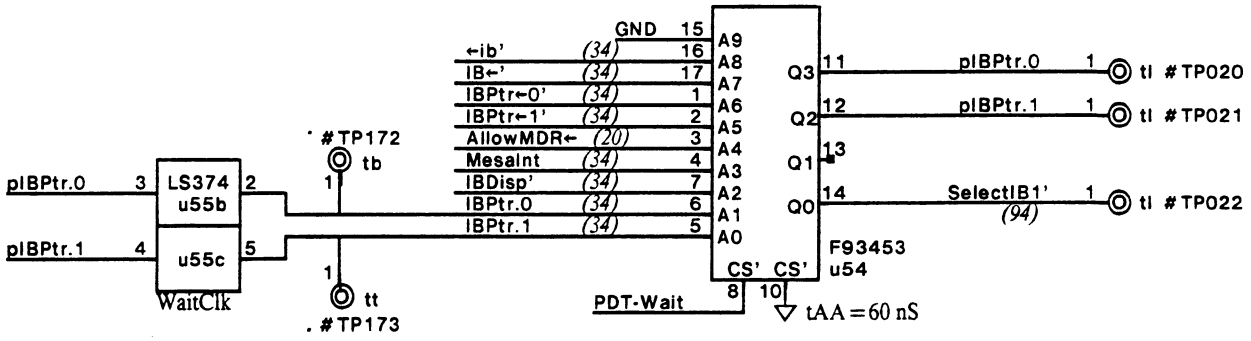


IBfront←IB[1]

34	↑ to IBPtr←1'
60	tAA
18[2]	SelectIB1' to NB
20[2]	LS374 setup

132[4] = 136 nS





IBProm-PC.4-RevG

Timing for HM7649 IBProm:

IBFront ← Xbus = (x + 37, x + 36) nS

x	Xbus to IB
43	WriteIB rises 43 nS before end of cycle
-6	Difference between S373 "EN to Q" and "Data to Q" = 18[2] - 13[1] = 6 nS. Data can arrive 6 nS after WriteIB goes high.
x + 37 nS	

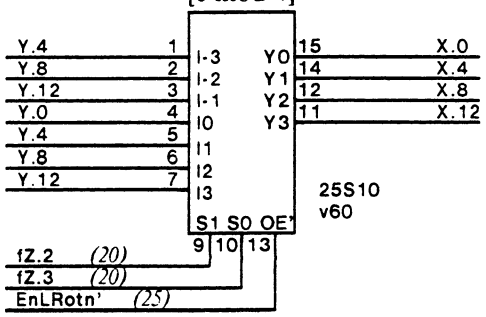
x	Xbus to IB
13[1]	S373 Data to NB
20[2]	LS374 setup
x + 36 nS	

94	WriteIB rises
18[2]	S373 EN to NB
20[2]	LS374 setup
132[4] = 136 nS	

XEROX SDD	Project Dandelion	IB	File pLionHead05.sil	Designer Garner	Rev M	Date 12/4/86	Page 05

LRotn

[0 mod 4]



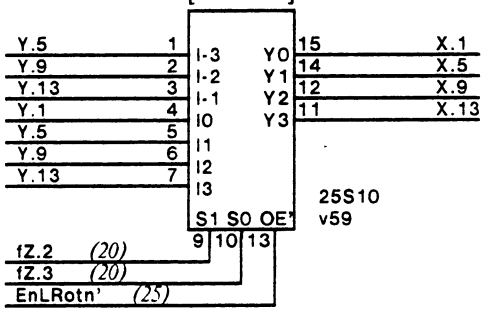
Zero disable X-bus

30	↑ to Xhigh←0
15	S241 EN to X-bus
10	X-bus
55 nS	

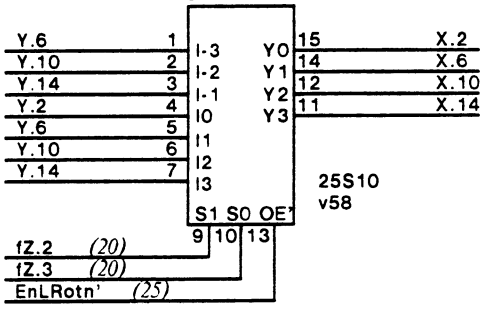
Xbus[0-7] ← 0

30	↑ to Xhigh←0
15	S241 OE
10	X-bus
55 nS	

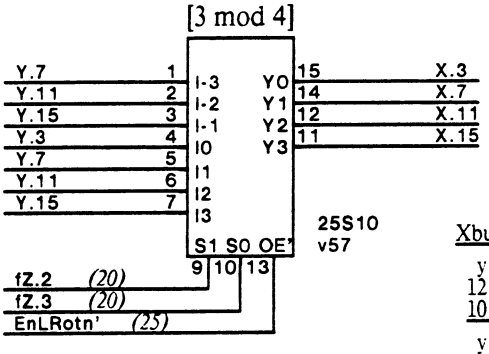
[1 mod 4]



[2 mod 4]

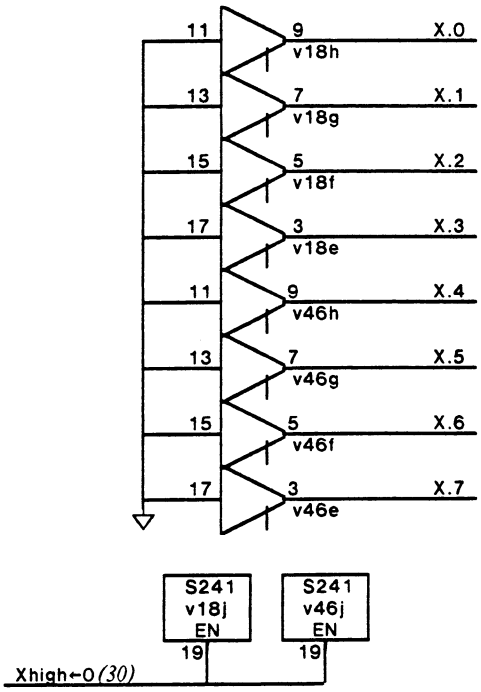


[3 mod 4]



fZ.2	fZ.3	
0	0	Left 0
0	1	Left 12
1	0	Left 8
1	1	Left 4

Zero High XBus



Xbus ← Y LRotn = max (y + 22, 56, 50) nS

y	↑ to Y bus
12	25S10 data in to out
10	X-bus
y + 22 nS	
25	↑ to EnLRotn'
21	25S10 OE
10	X-bus
56 nS	
20	↑ to fZ.2
20	25S10 Select to X-bus
10	X-bus
50 nS	

LRotn disable X-bus

25	↑ to EnLRotn'
15	25S10 OE' to X-bus
10	X-bus
50 nS	

XEROX SDD	Project Dandelion	X Bus: LRotn, RH, ZeroHighX	File pLionHead06.sil	Designer Garner	Rev M	Date 8/24/80	Page 06

IB disable X-bus

25	↑ to XBus←IB'
14	S257 E' to X-bus
10	X-bus
49 nS	

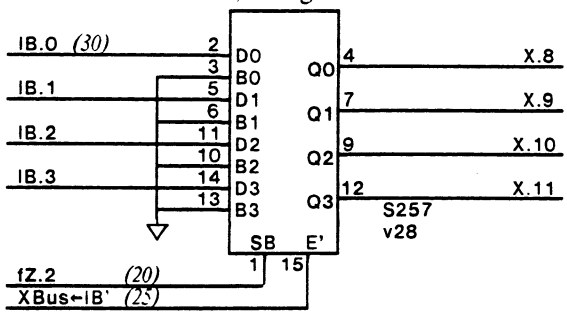
Byte disable X-bus

25	↑ to Nibble'
14	S257 E' to X-bus
10	X-bus
49 nS	

Nibble disable X-bus

25	↑ to Nibble'
15	S241 EN' to X-bus
10	X-bus
50 nS	

0, ibHigh



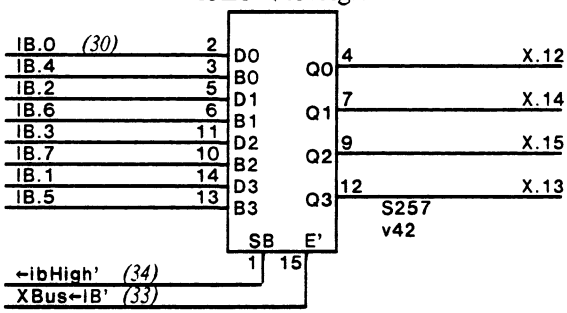
Xbus←IB=max(56,56,59) nS

34[4]	↑ to IB
8	S257 data to Xbus
10	X-bus
52[4] = 56 nS	

25	↑ to Xbus←IB'
21	S257 E' to Xbus
10	X-bus
56 nS	

34	↑ to←ibHigh'
15	S257 SB to Xbus
10	X-bus
59 nS	

ibLow, ibHigh

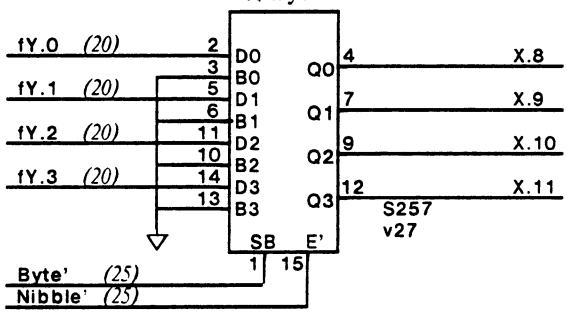


Xbus ← Nibble = max(39, 50) nS

20	↑ to fZ
9	S241 data to X-bus
10	X-bus
39 nS	

25	↑ to Nibble'
15	S241 EN' to X-bus
10	X-bus
50 nS	

0, Byte



Xbus ← Byte = max(38, 56,50) nS

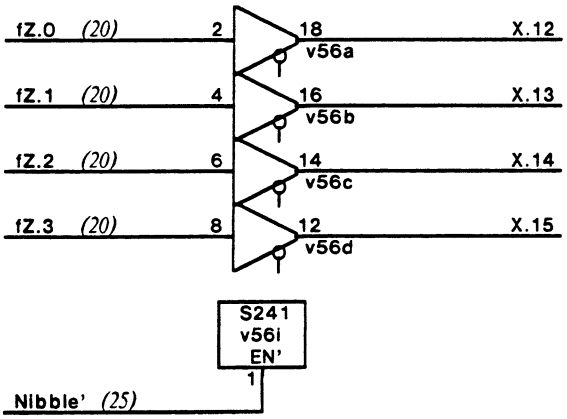
20	↑ to fY
8	S257 data to X-bus
10	X-bus
38 nS	

25	↑ to Nibble'
21	S257 E' to X-bus
10	X-bus
56 nS	

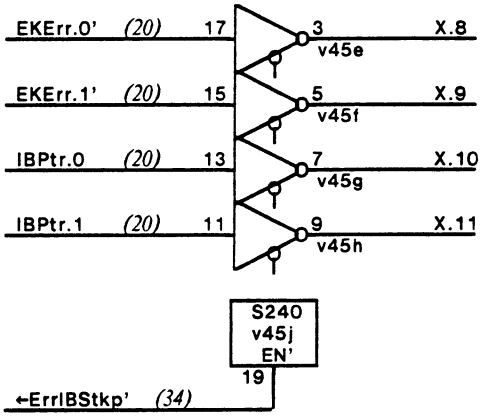
25	↑ to Byte'
15	S257 SB to Xbus
10	X-bus
50 nS	

See stackP timings for ErrIBPtr

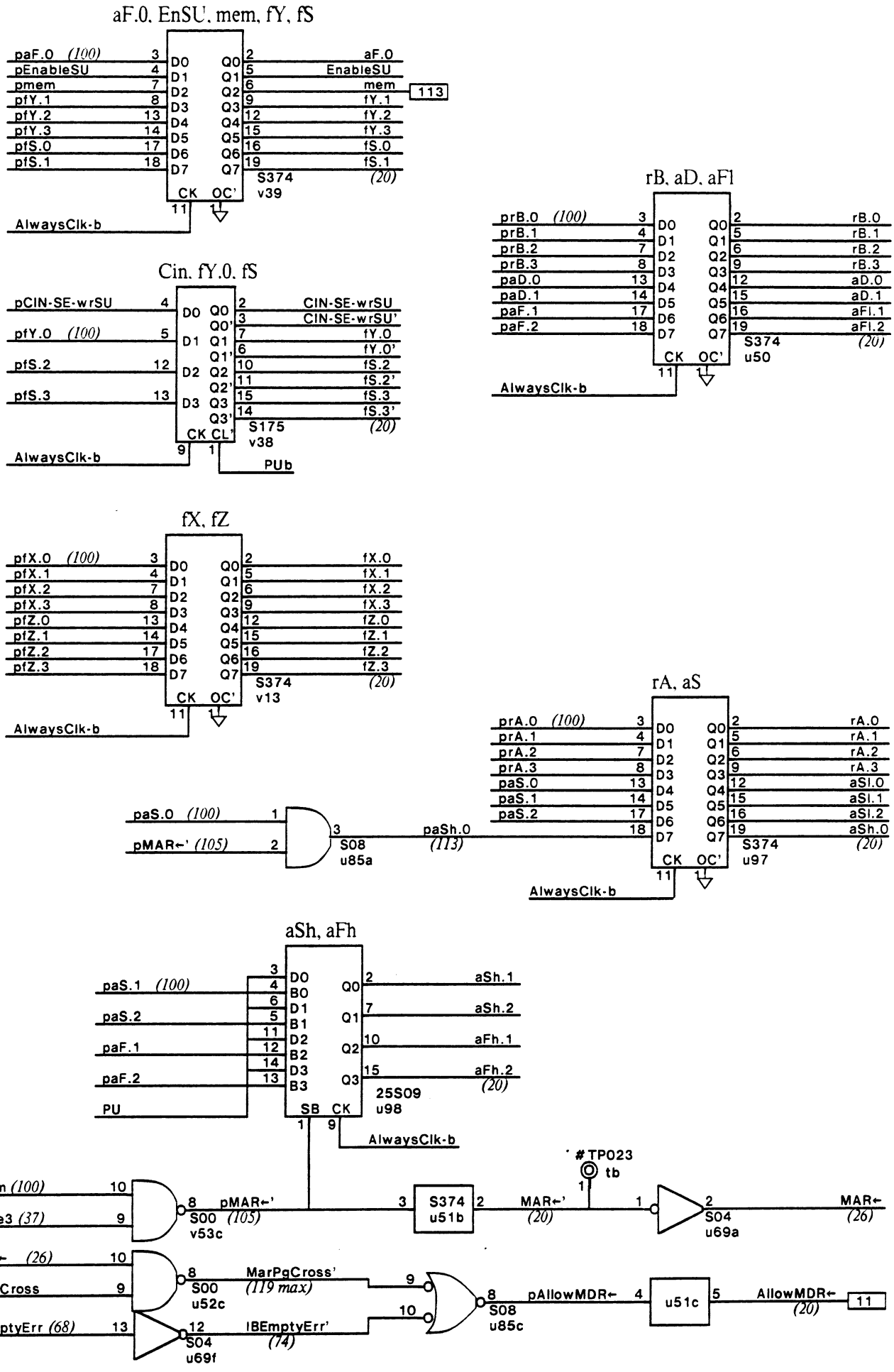
Nibble



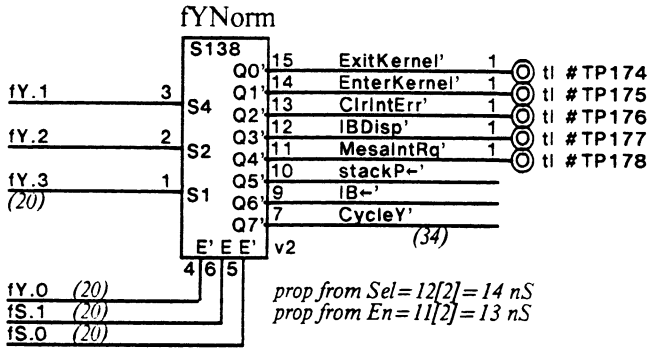
ErrIBPtr

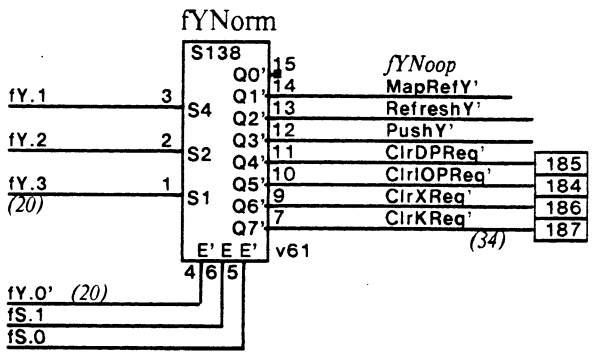


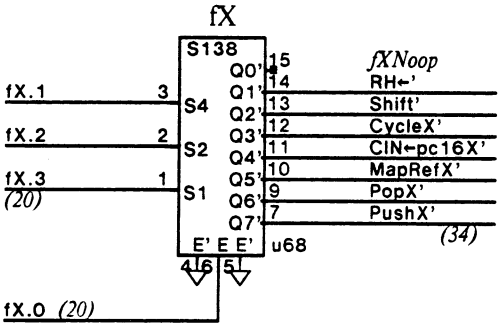
XEROX SDD	Project Dandelion	X Bus: IB. constants, ErrIntstackP	File pLionHead07.sil	Designer Garner	Rev M	Date 8/24/80	Page 07

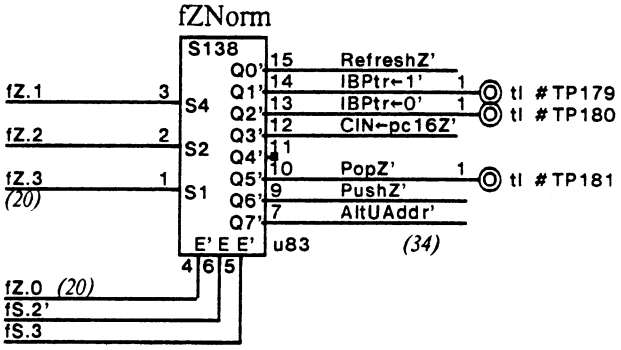


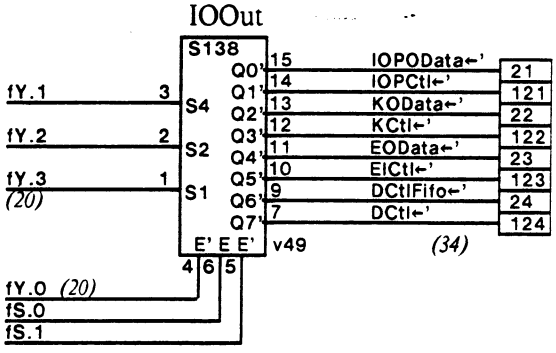
XEROX SDD	Project Dandelion	MIR	File pLionHead08.sil	Designer Garner	Rev M	Date 8/24/80	Page 08

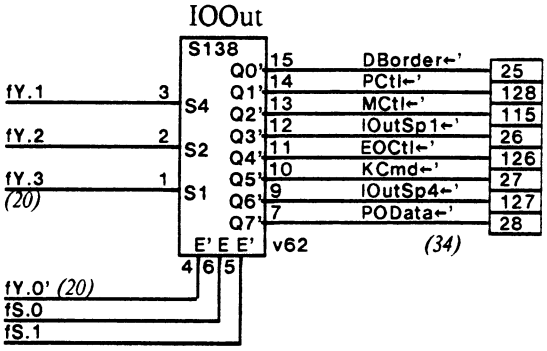


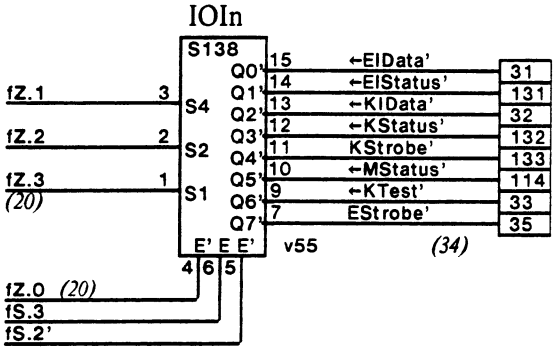


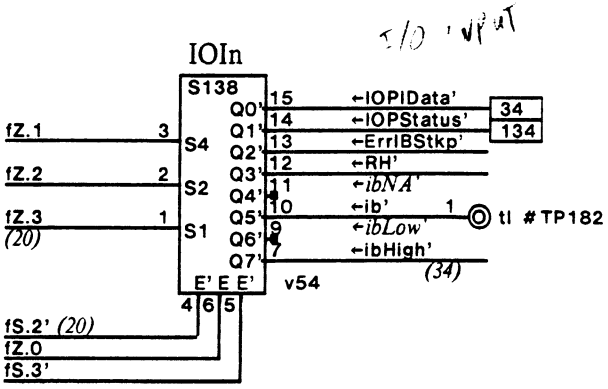




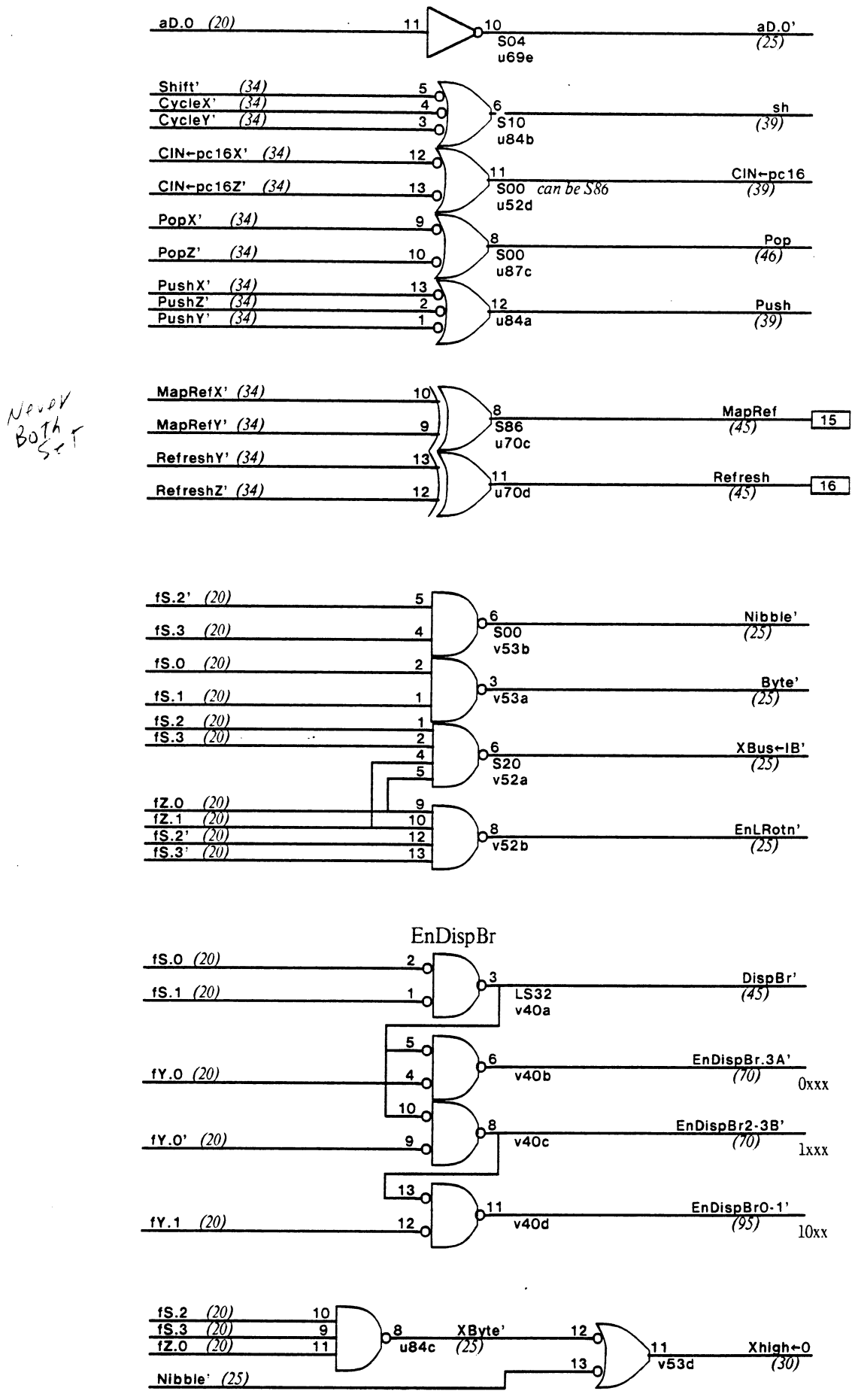








XEROX SDD	Project Dandelion	MIR Decoding I	File pLionHead09.sil	Designer Garner	Rev M	Date 12/4/80	Page 09



XEROX SDD	Project Dandelion	MIR Decoding II	File pLionHead10.sil	Designer Garner	Rev M	Date 4/3/91	Page 10

DispBr[0-1] = max(c+32,69,133)

20	↑ to fY
24[3]	S151 select to DispBr
18	DispBr' setup

64[3]=69

95	↑ to EnDispBr0-1'
18[2]	S151 E' to DispBr
18	DispBr' setup

131[2] = 133 nS

c	condition source
12[2]	S151 data to DispBr
18	DispBr' setup

c+30[2]= c+32

DsipBr setup

5	S00 in to pTC
6[1]	S64 in to pNIA
5[1]	25S09/S374 setup

18 nS

DispBr[2-3]=max(c+26,55,103)

20	↑ to fY
15[2]	S151 select to DispBr
18	DispBr' setup

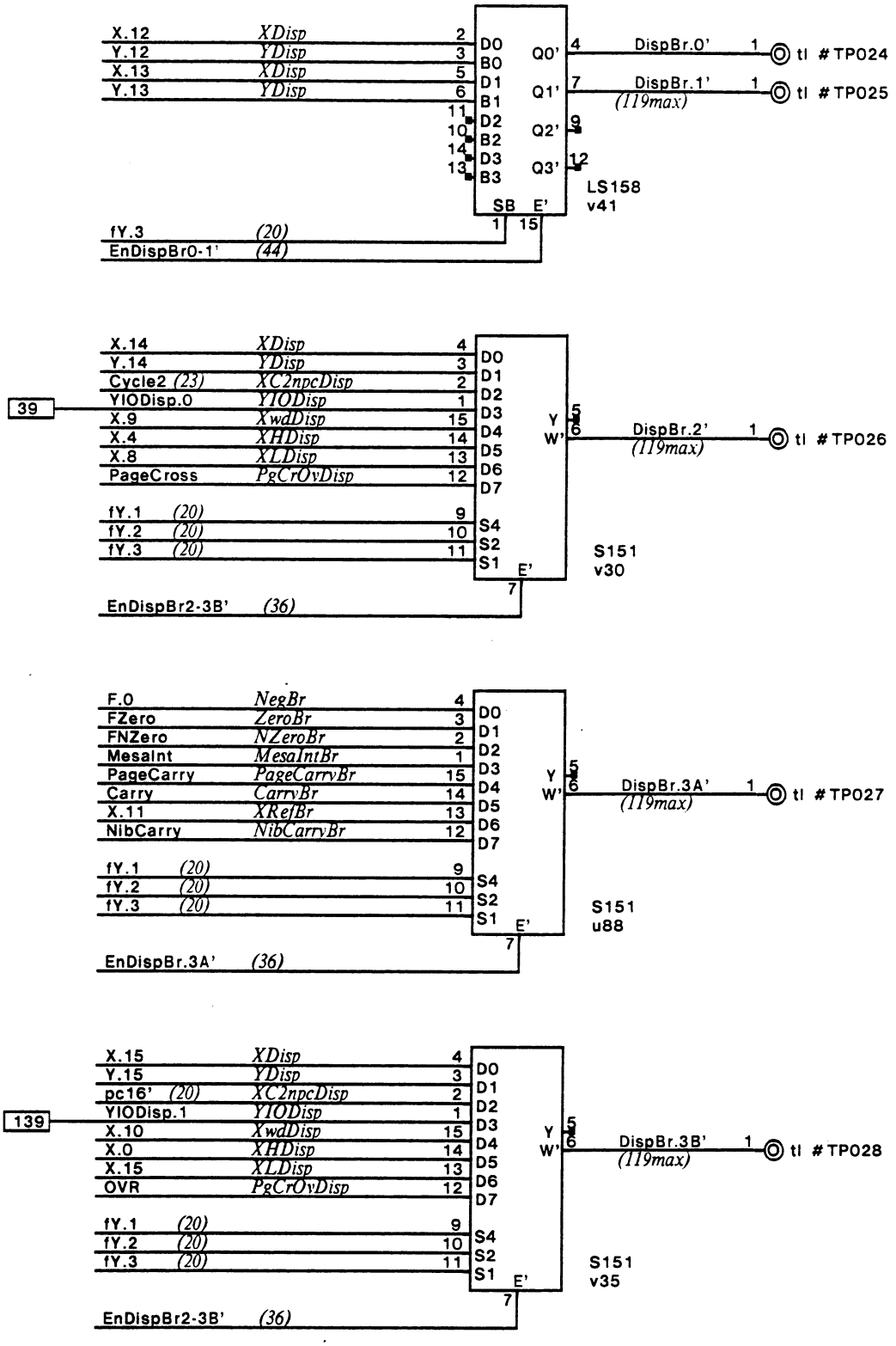
51[4]=55 nS

70	↑ to EnDispBr.3A'
13[2]	S151 E' to DispBr
18	DispBr' setup

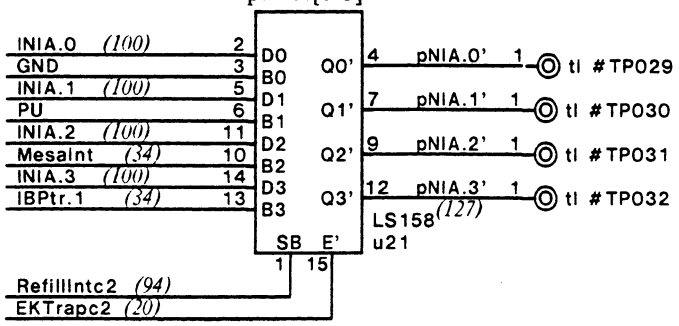
101[2] = 103 nS

c	condition source
7[1]	S151 data to DispBr
18	DispBr' setup

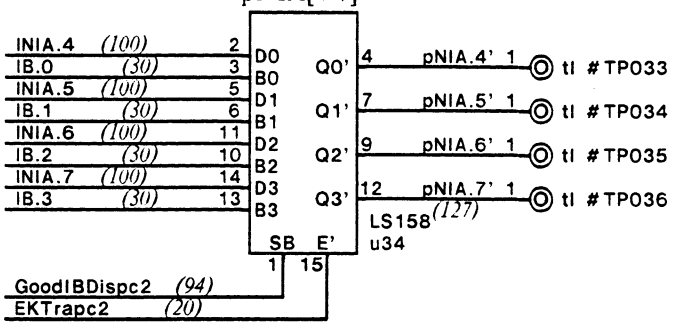
c+23[3]=c+26 nS



pNIA[0-3]



pNIA[4-7]

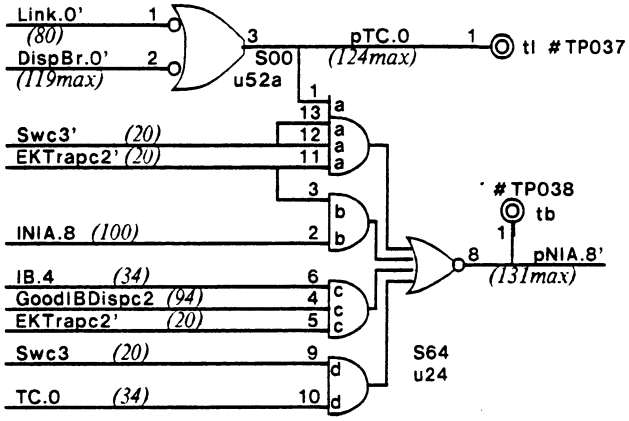


pNIA[0-7] = max(127, 120, 46) nS

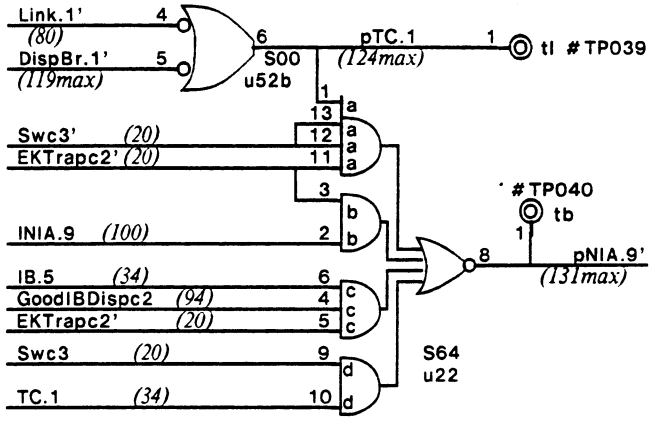
94	↑ to RefillIntc2		100	↑ to INIA		20	↑ to EKErrc2
24[3]	LS158 SB to pNIA'		12[2]	LS158 data to pNIA'		18[2]	LS158 E' to pNIA'
5[1]	25S09/S374 setup		5[1]	25S09/S374 setup		5[1]	25S09/S374 setup
123[4] = 127 nS			117[3] = 120 nS			43[3] = 46nS	

(See page 11 for pNIA[8-11] timing)

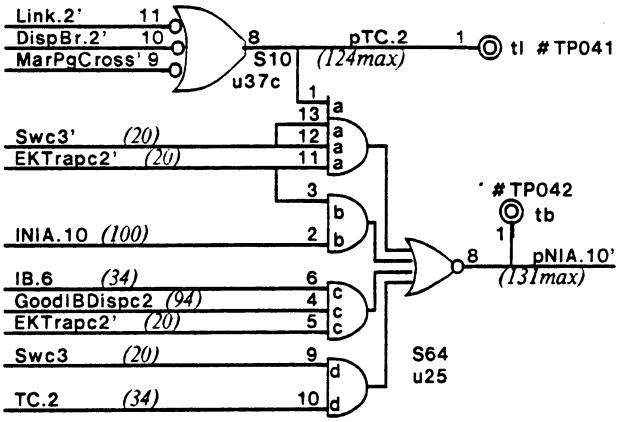
pNIA.8



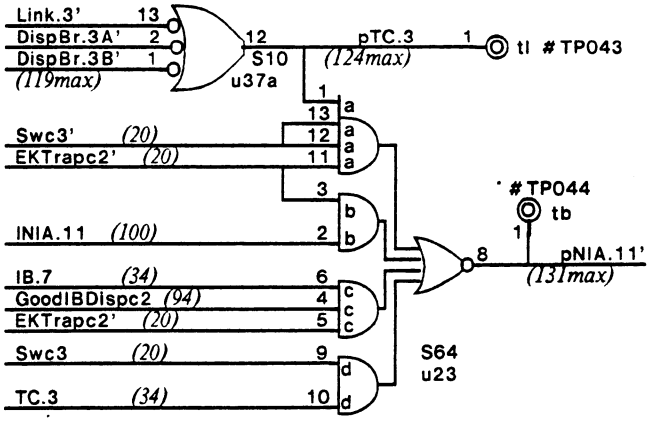
pNIA.9

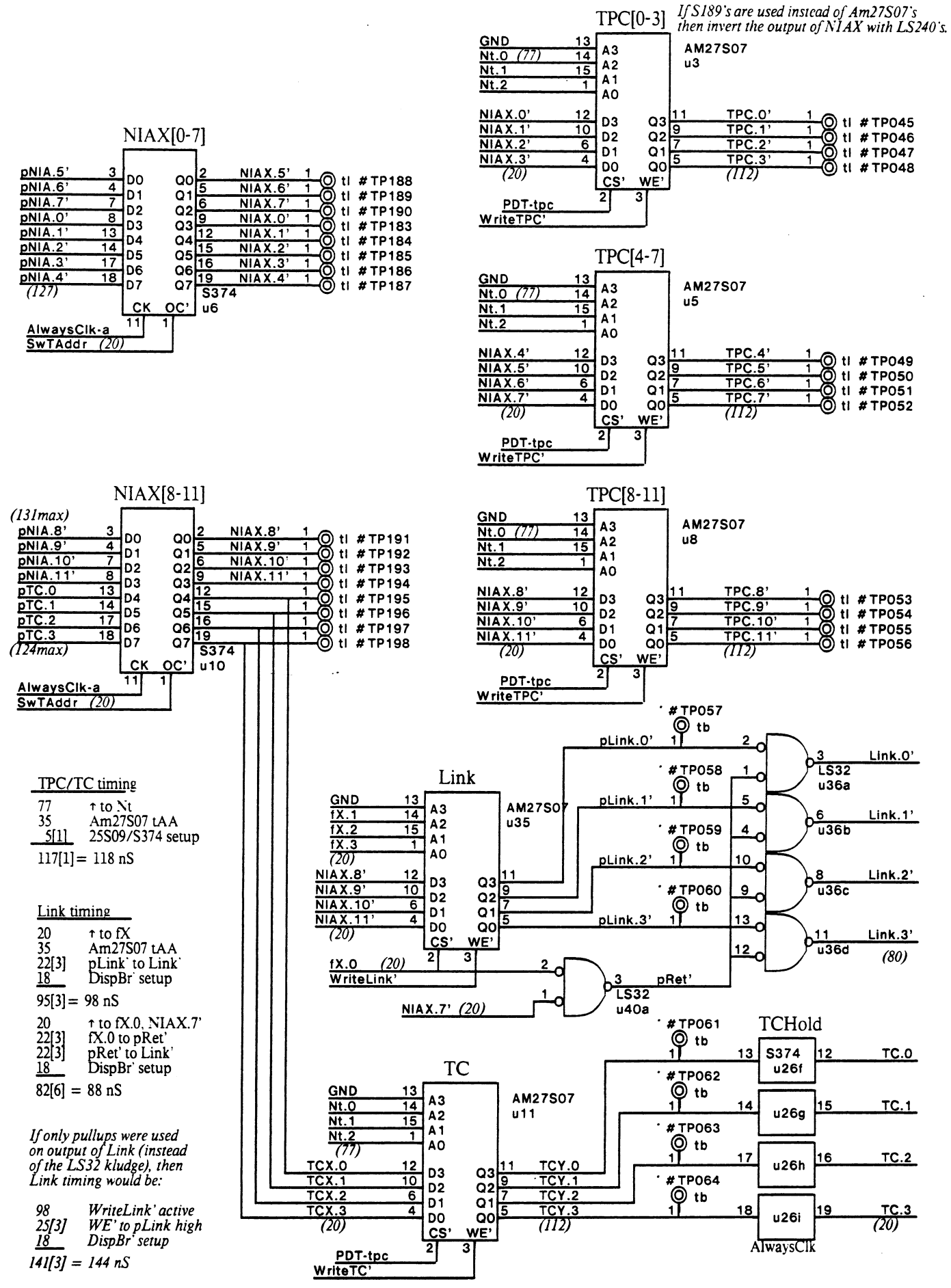


pNIA.10

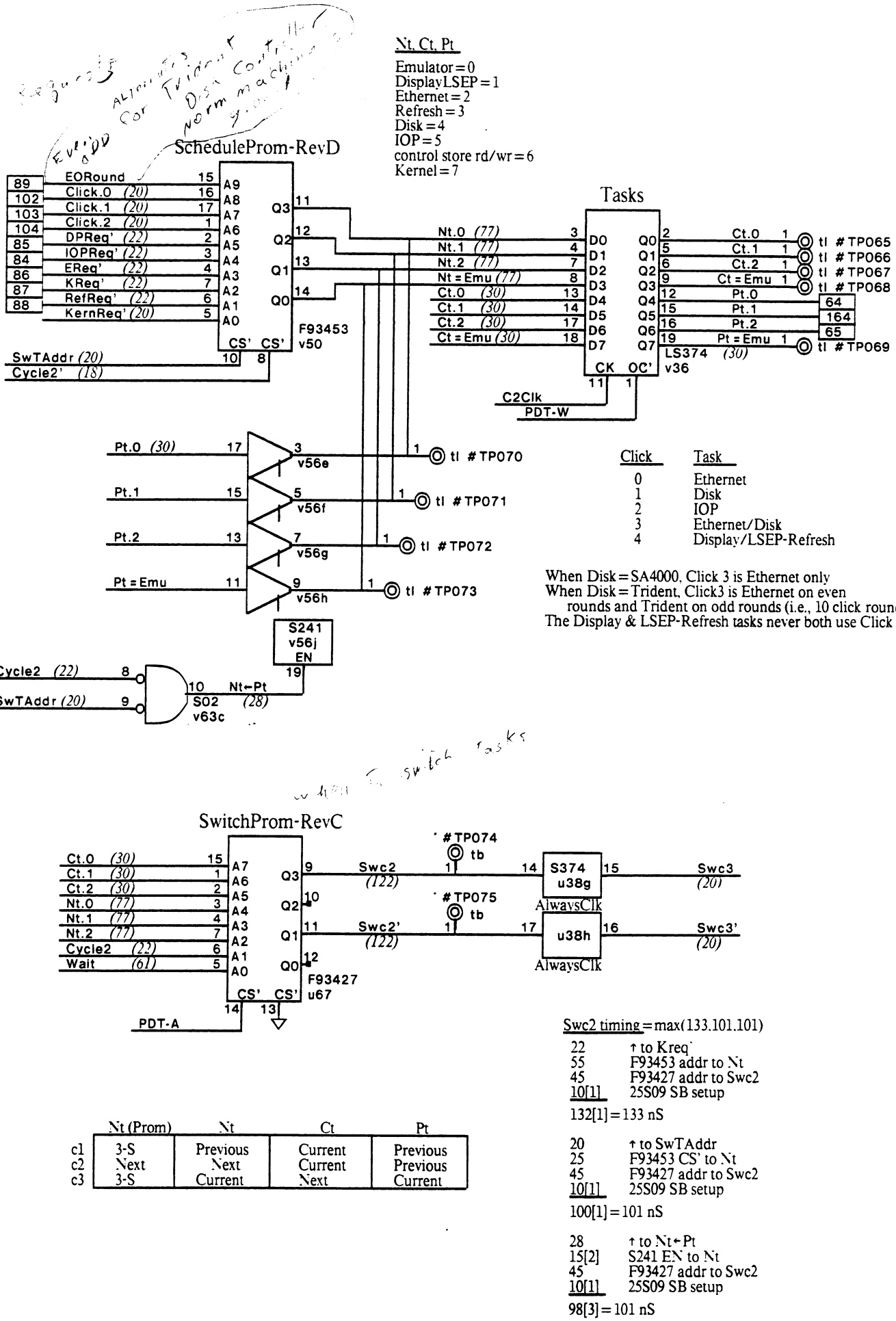


pNIA.11

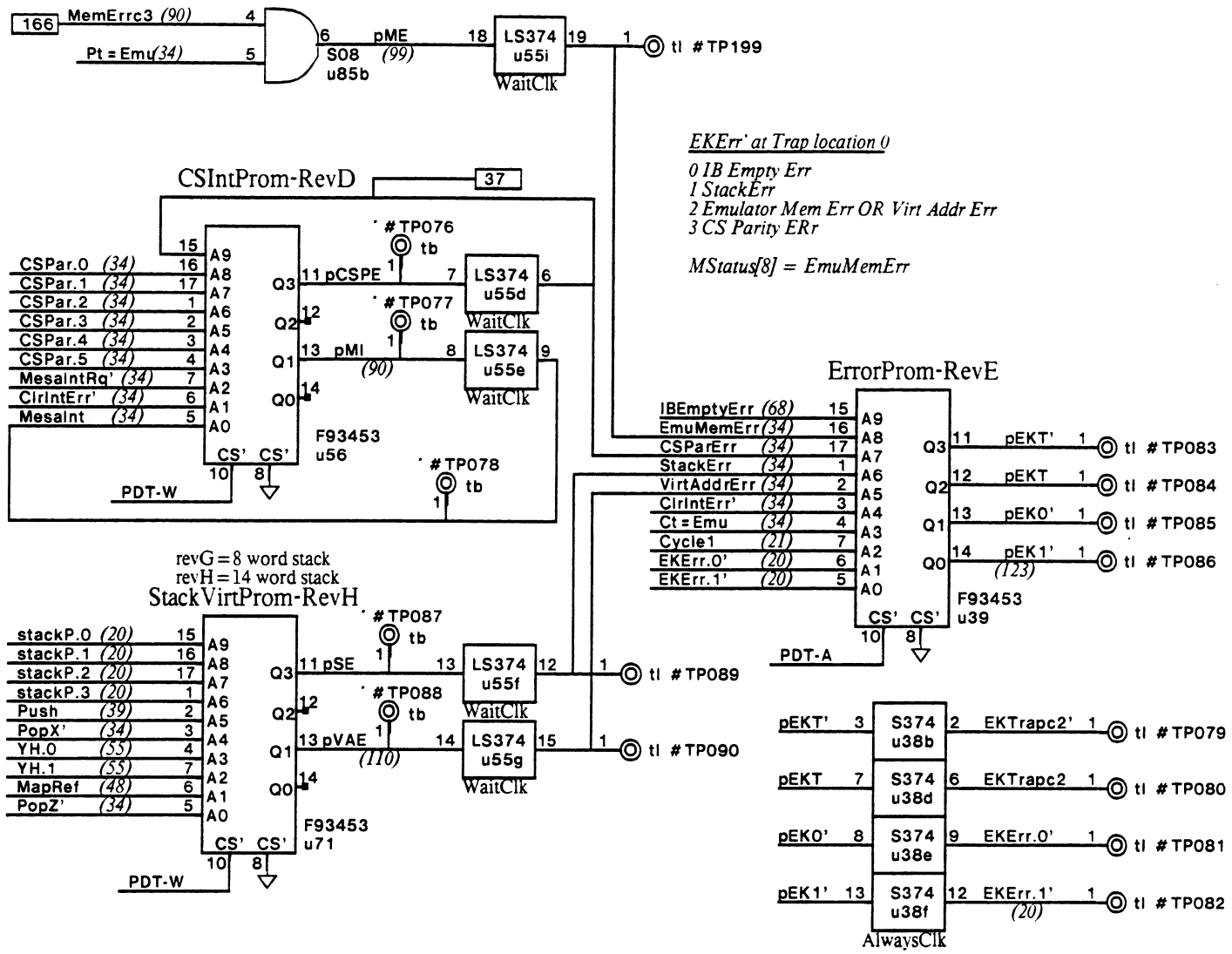




XEROX SDD	Project Dandelion	TPC, TC, & Link	File pLionHead13.sil	Designer Garner	Rev M	Date 12/4/80	Page 13

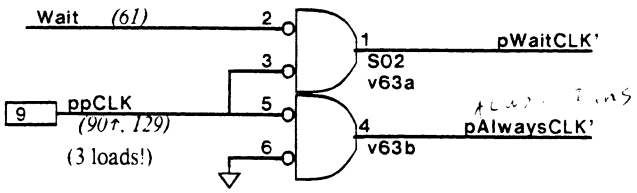


	Nt (Prom)	Nt	Ct	Pt
c1	3-S	Previous	Current	Previous
c2	Next	Next	Current	Previous
c3	3-S	Current	Next	Current

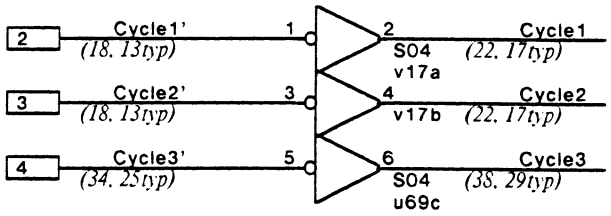


XEROX SDD	Project Dandelion	Error, Emulator, & Kernel Proms	File pLionHead15.sil	Designer Garner	Rev M	Date 12/4/80	Page 15

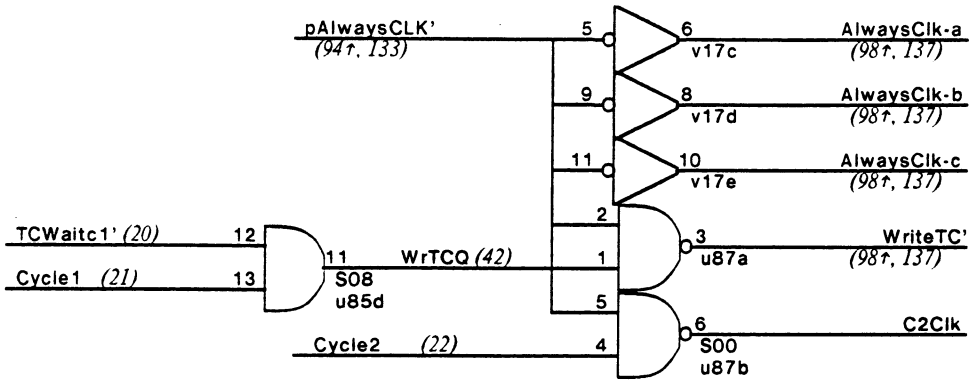
Clock Receivers

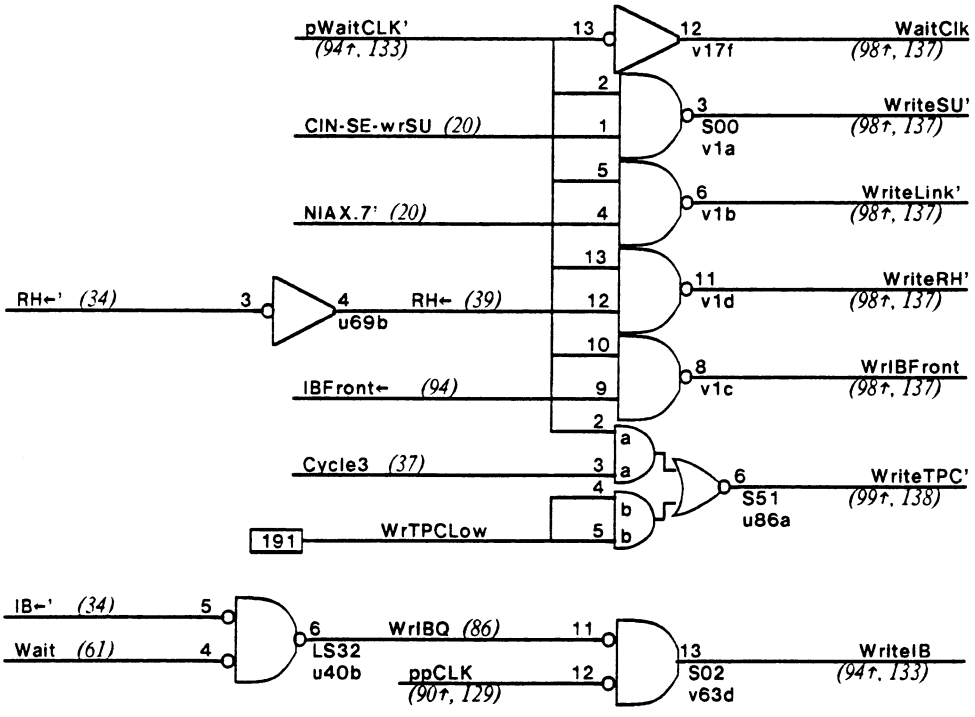


Cycles

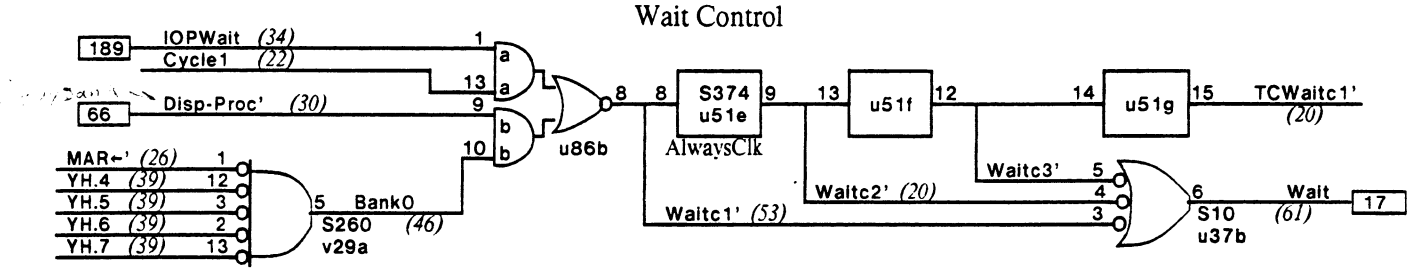


Qualified Clocks

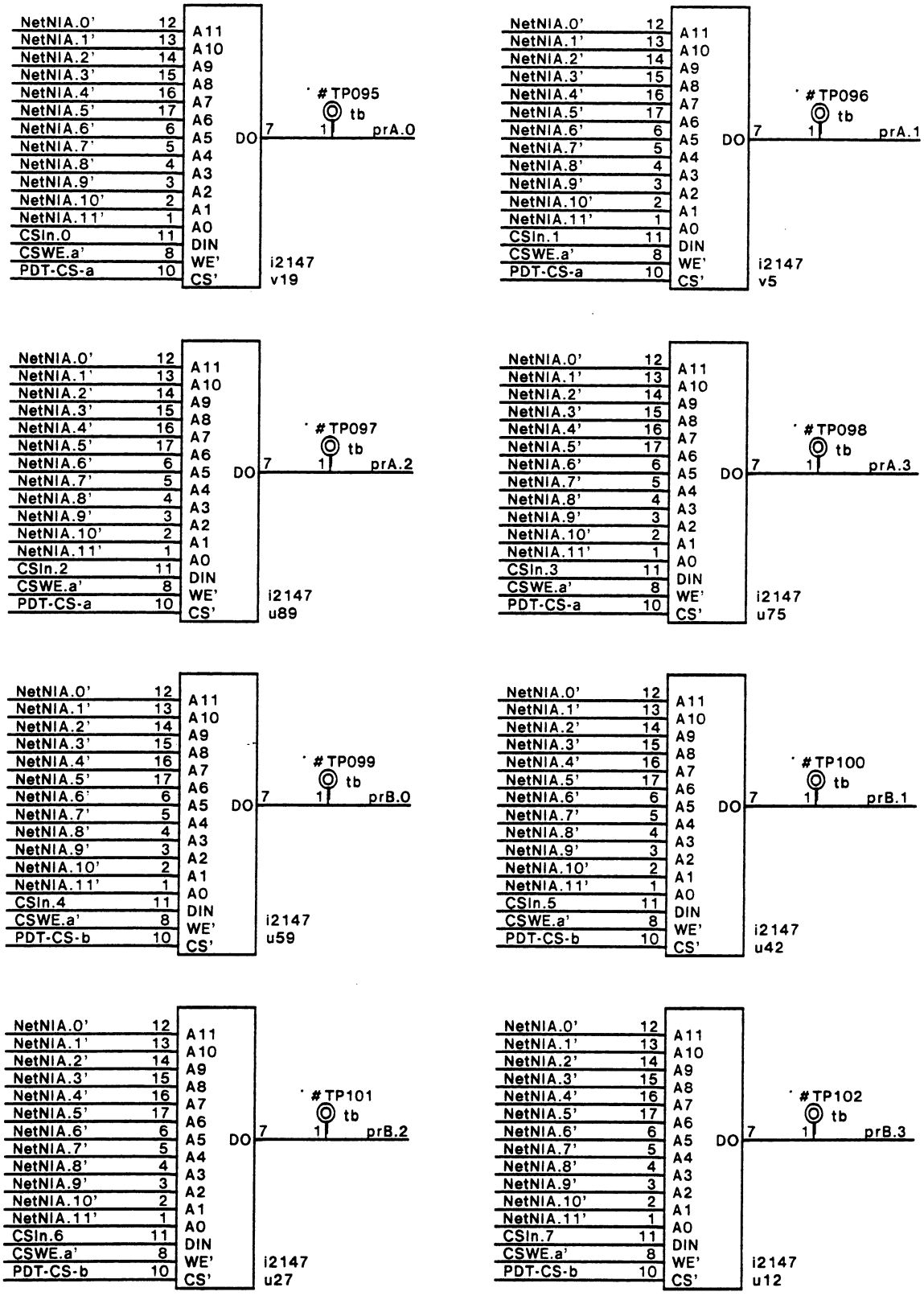




Wait Control

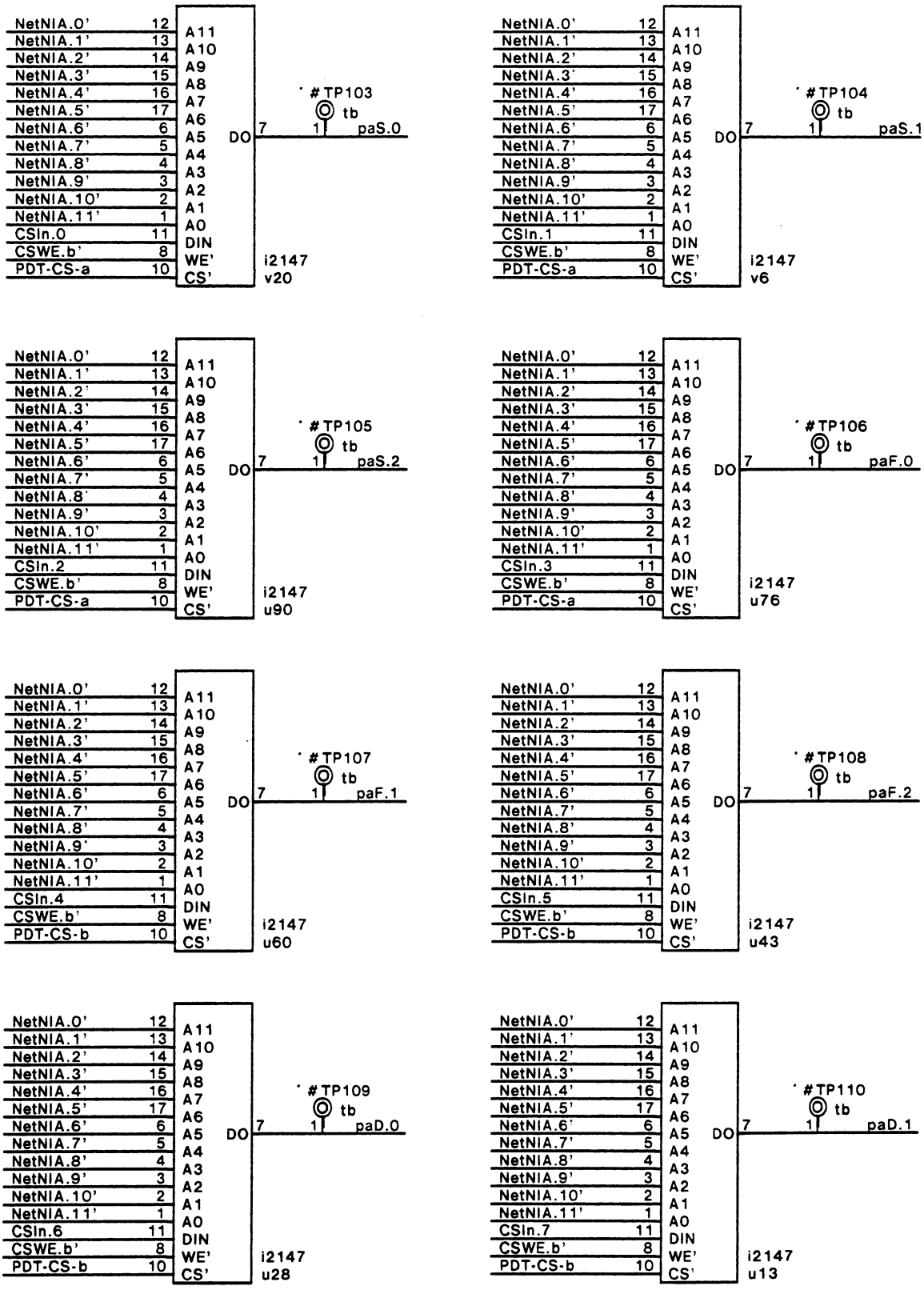


Detects low bank for max 1024K mem.



CS Timing

17	↑ to NIA'
13	transmission delay
70	tAA 2147L
100 nS	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NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.0 11
CSWE.b' 8
PDT-CS-a 10
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A0
DIN
WE'
CS'
DO
7
i2147
v20
#TP103
tb
1
paS.0
NetNIA.0' 12
NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.1 11
CSWE.b' 8
PDT-CS-a 10
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DIN
WE'
CS'
DO
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v6
#TP104
tb
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paS.1
NetNIA.0' 12
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NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.2 11
CSWE.b' 8
PDT-CS-a 10
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CS'
DO
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NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.3 11
CSWE.b' 8
PDT-CS-a 10
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CS'
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NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.4 11
CSWE.b' 8
PDT-CS-b 10
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CS'
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#TP107
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paF.1
NetNIA.0' 12
NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
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NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.5 11
CSWE.b' 8
PDT-CS-b 10
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paF.2
NetNIA.0' 12
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NetNIA.2' 14
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NetNIA.5' 17
NetNIA.6' 6
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NetNIA.9' 3
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NetNIA.11' 1
CSIn.6 11
CSWE.b' 8
PDT-CS-b 10
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CS'
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NetNIA.0' 12
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NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.7 11
CSWE.b' 8
PDT-CS-b 10
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CS'
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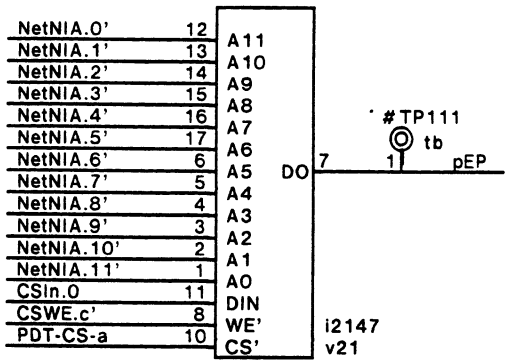
paD.1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NetNIA.2' 14
NetNIA.3' 15
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NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.0 11
CSWE.c' 8
PDT-CS-a 10
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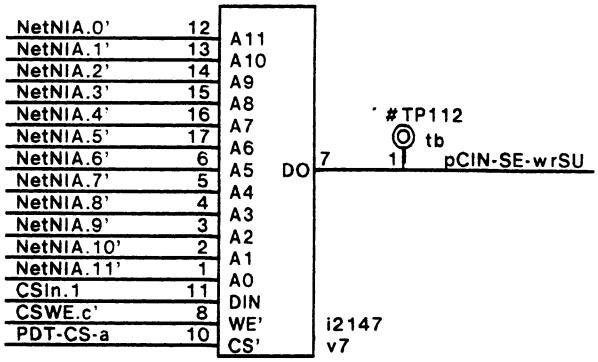
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NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.1 11
CSWE.c' 8
PDT-CS-a 10
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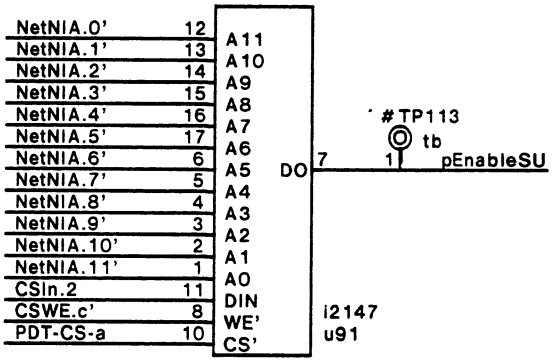
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NetNIA.11' 1
CSIn.2 11
CSWE.c' 8
PDT-CS-a 10
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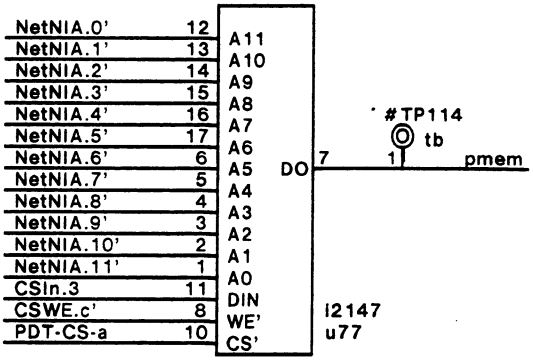
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NetNIA.11' 1
CSIn.3 11
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PDT-CS-a 10
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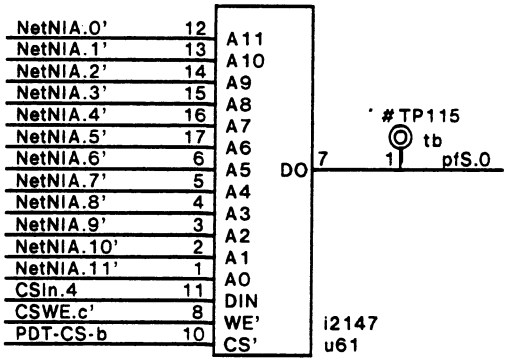
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NetNIA.11' 1
CSIn.4 11
CSWE.c' 8
PDT-CS-b 10
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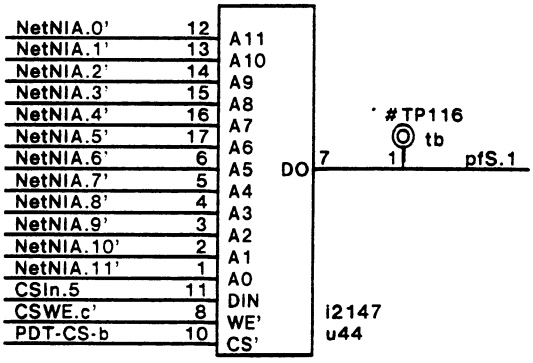
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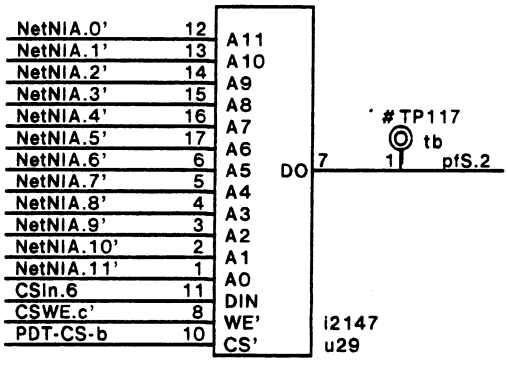
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NetNIA.8' 4
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NetNIA.11' 1
CSIn.6 11
CSWE.c' 8
PDT-CS-b 10
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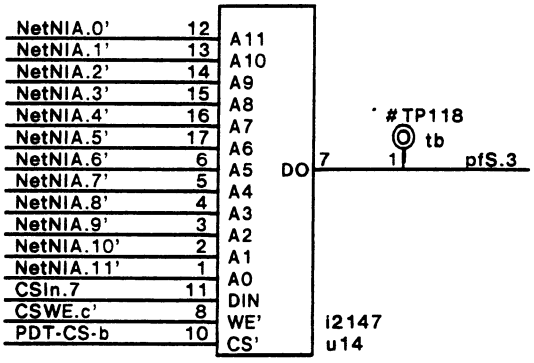
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NetNIA.3' 15
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NetNIA.5' 17
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NetNIA.7' 5
NetNIA.8' 4
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NetNIA.10' 2
NetNIA.11' 1
CSIn.7 11
CSWE.c' 8
PDT-CS-b 10
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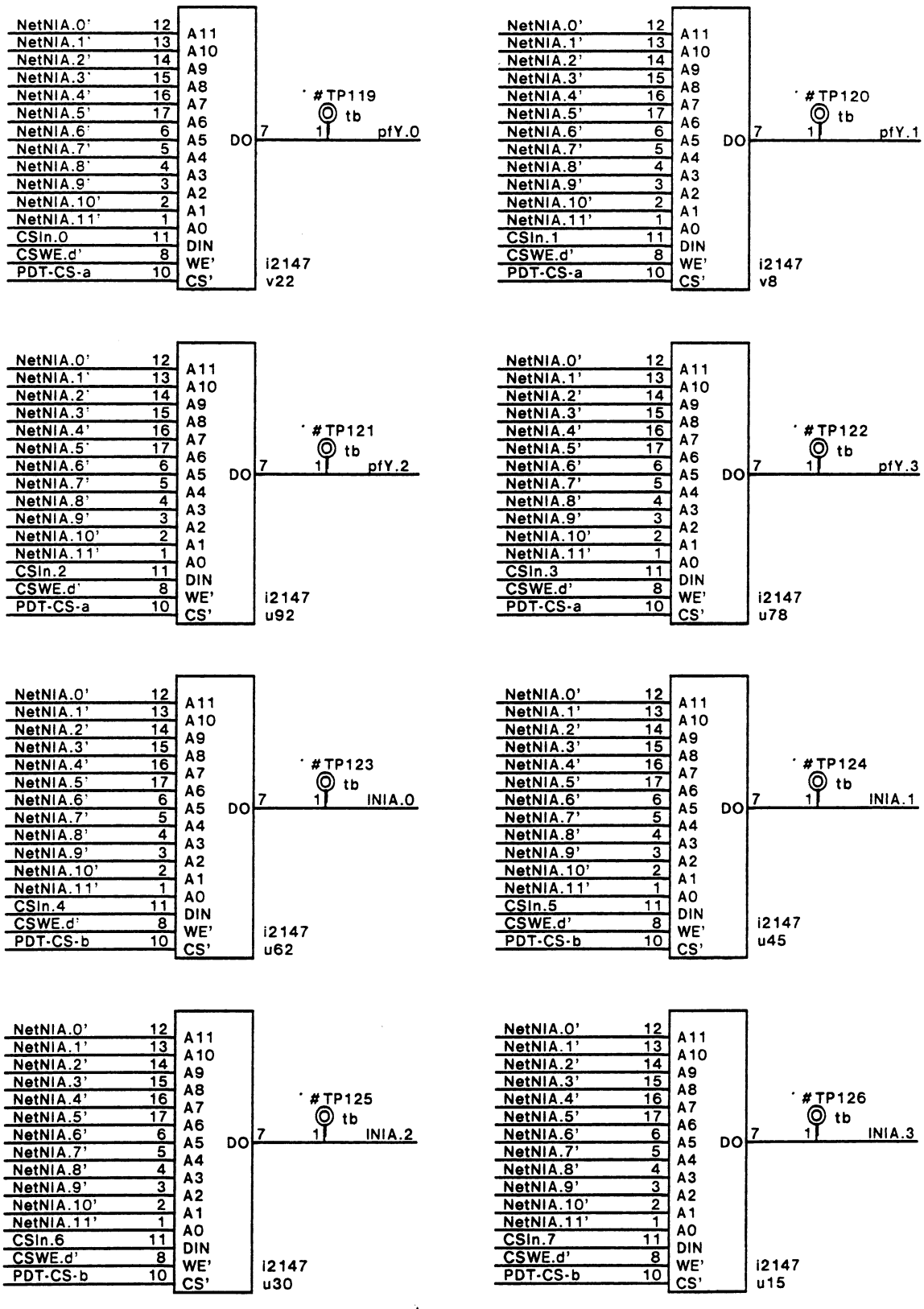
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NetNIA.3' 15
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NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.0 11
CSWE.d' 8
PDT-CS-a 10
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v22
#TP119
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pfY.0
NetNIA.0' 12
NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.1 11
CSWE.d' 8
PDT-CS-a 10
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NetNIA.0' 12
NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.2 11
CSWE.d' 8
PDT-CS-a 10
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pfY.2
NetNIA.0' 12
NetNIA.1' 13
NetNIA.2' 14
NetNIA.3' 15
NetNIA.4' 16
NetNIA.5' 17
NetNIA.6' 6
NetNIA.7' 5
NetNIA.8' 4
NetNIA.9' 3
NetNIA.10' 2
NetNIA.11' 1
CSIn.3 11
CSWE.d' 8
PDT-CS-a 10
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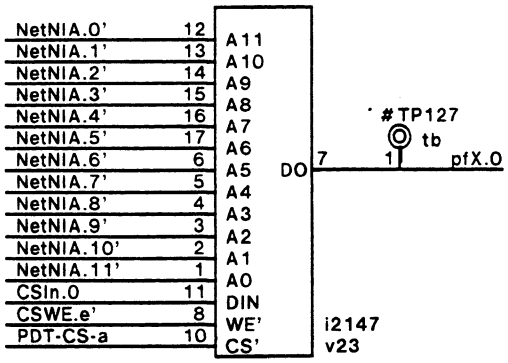
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CSIn.0 11
CSWE.e' 8
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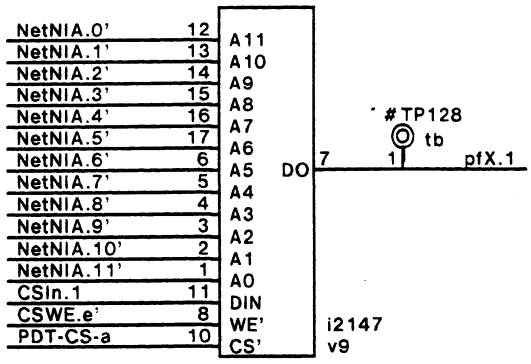
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NetNIA.11' 1
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CSWE.e' 8
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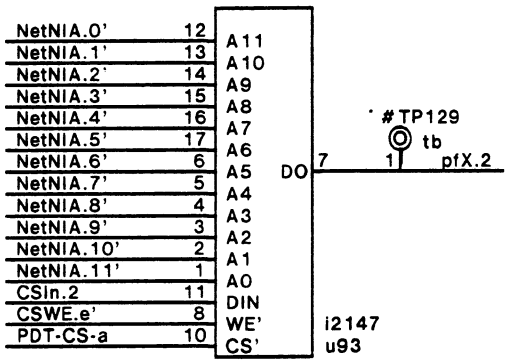
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NetNIA.11' 1
CSIn.2 11
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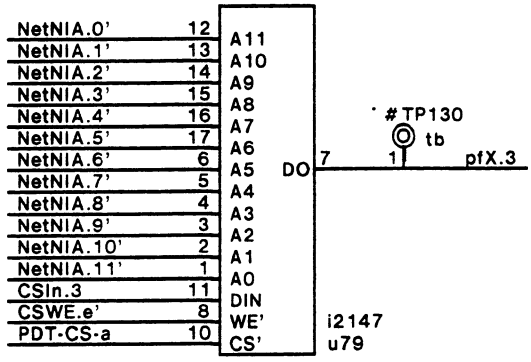
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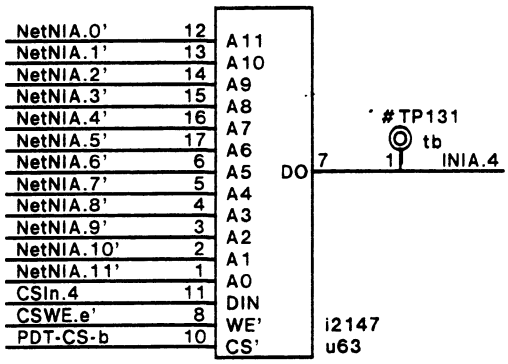
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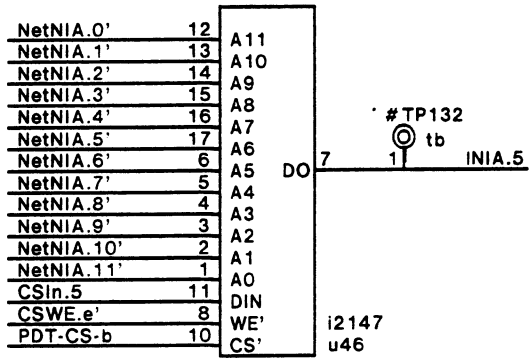
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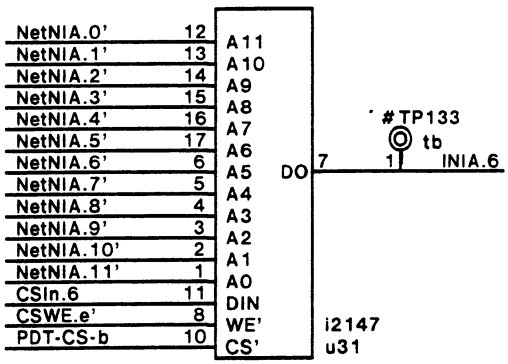
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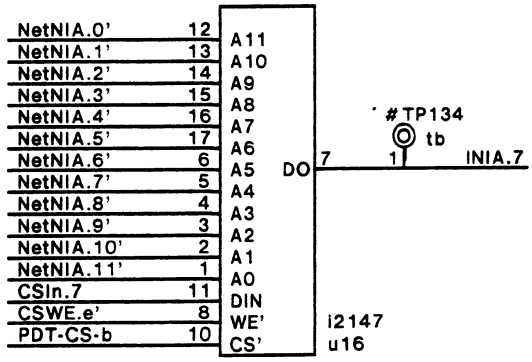
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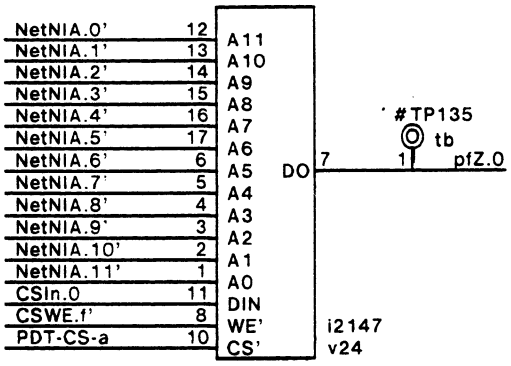
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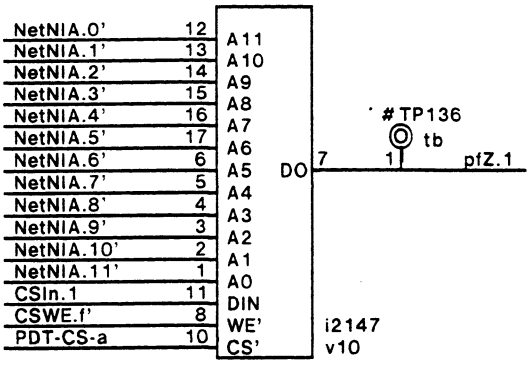
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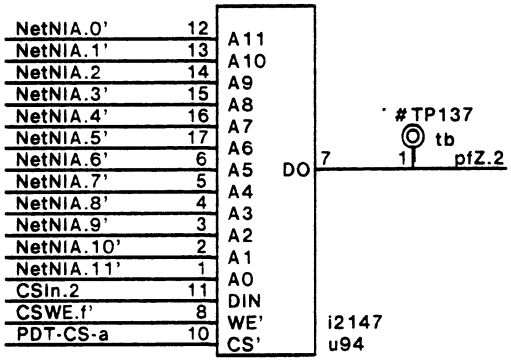
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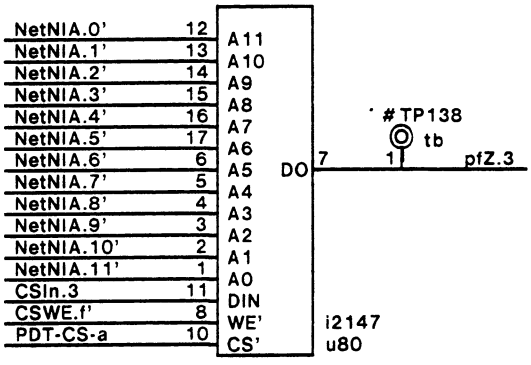
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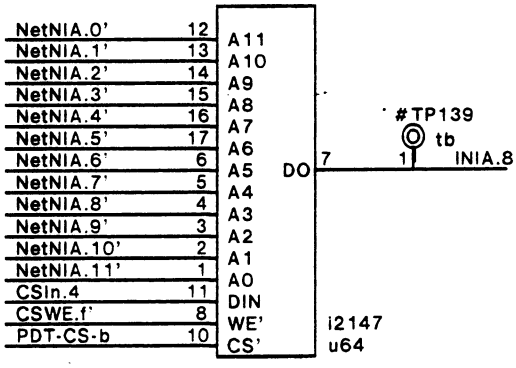
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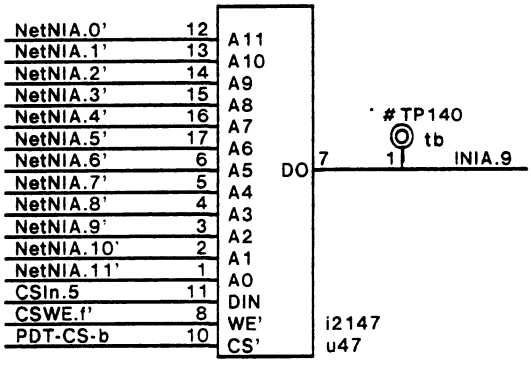
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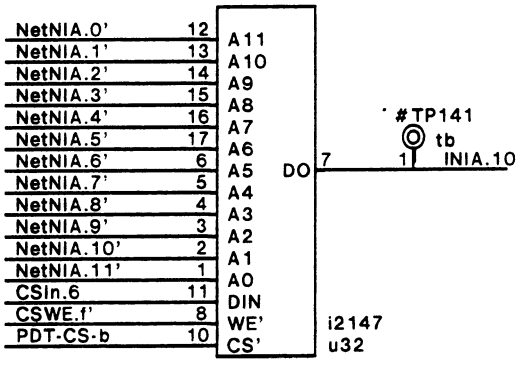
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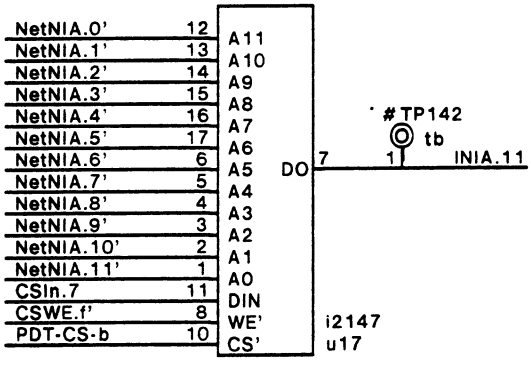
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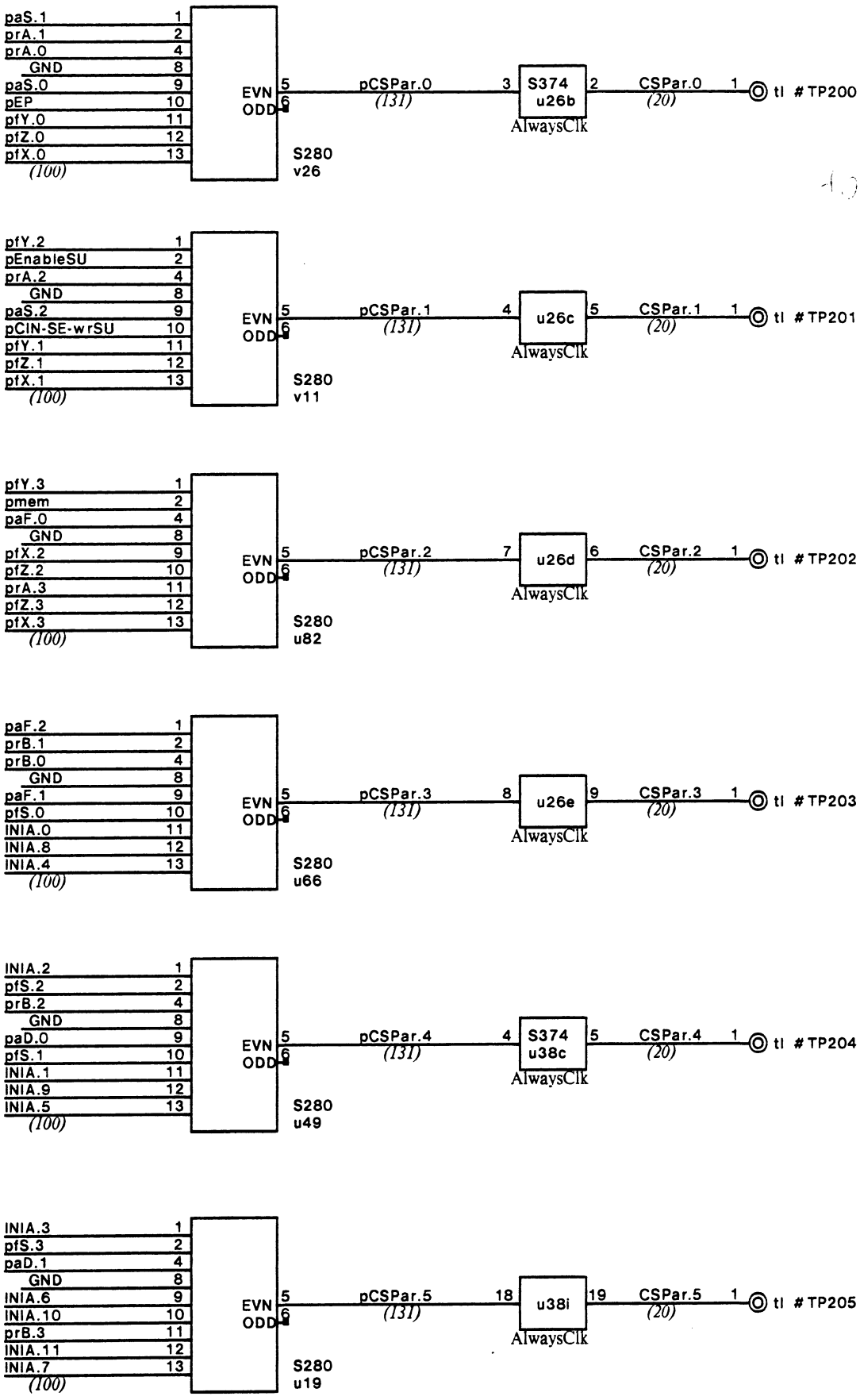

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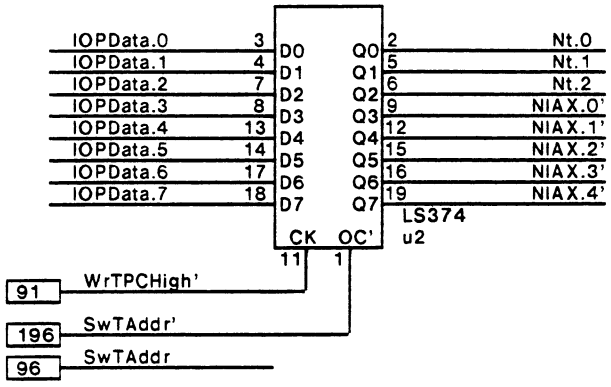

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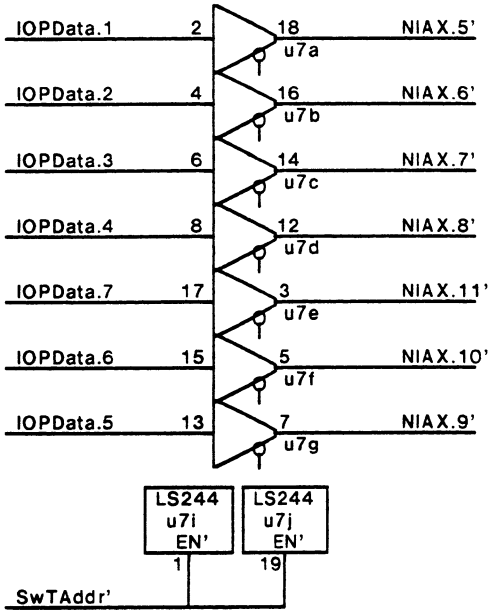

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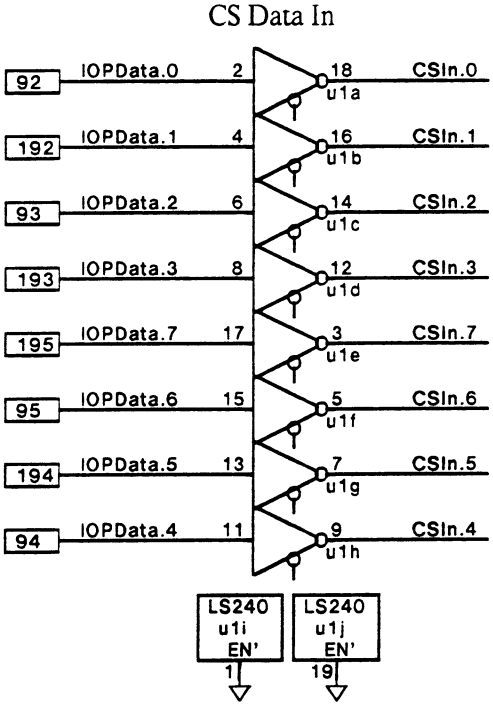

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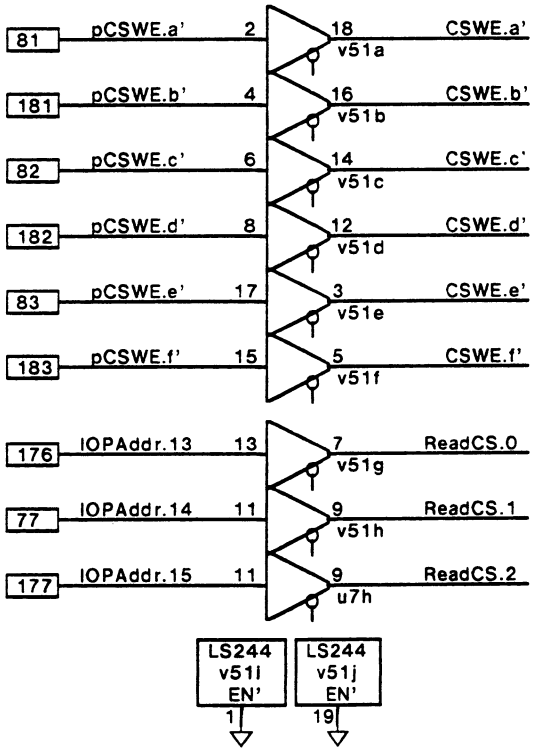
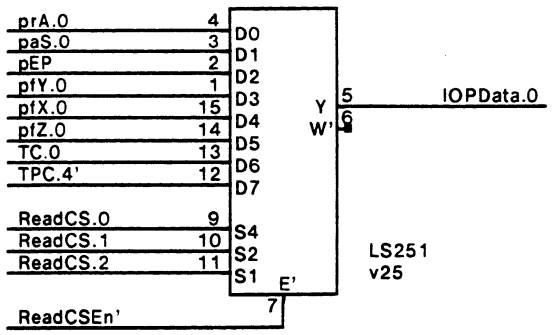
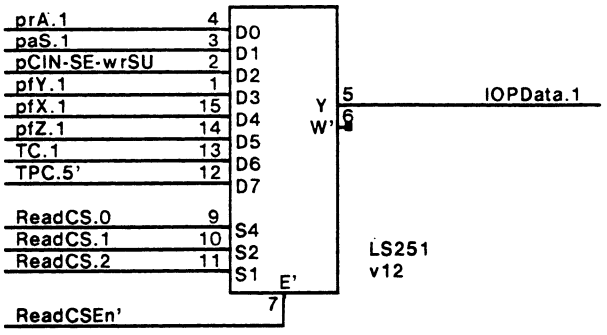
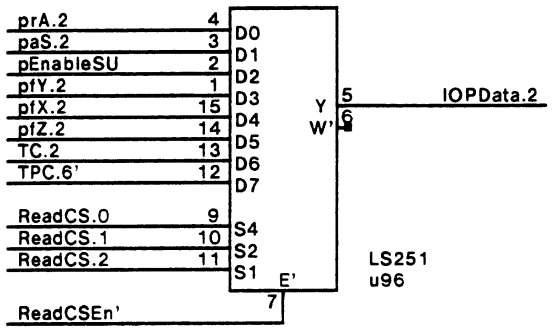
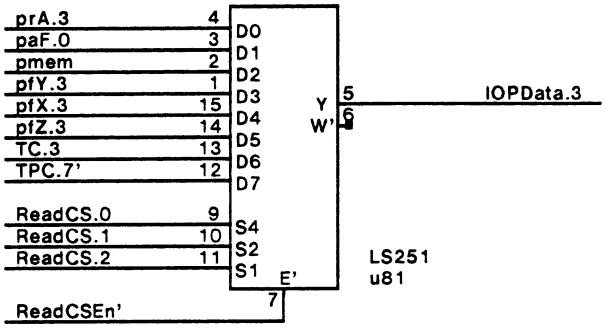
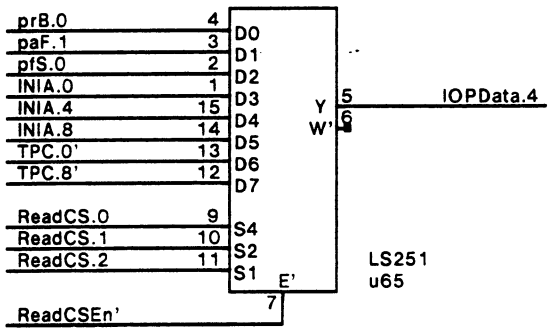


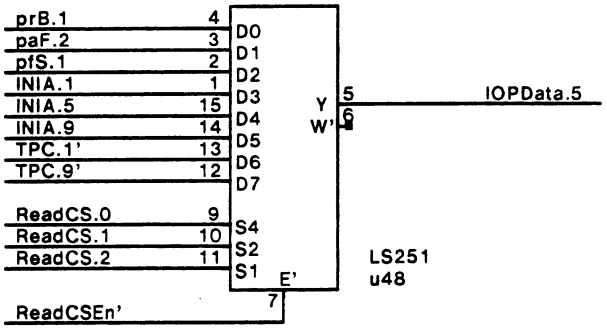


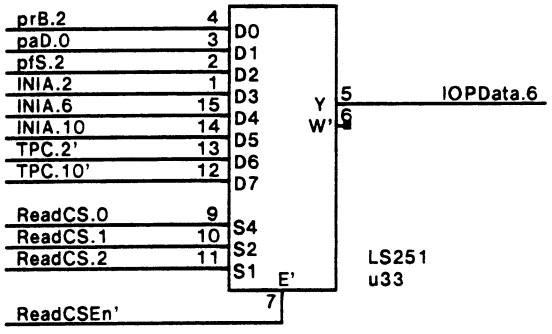


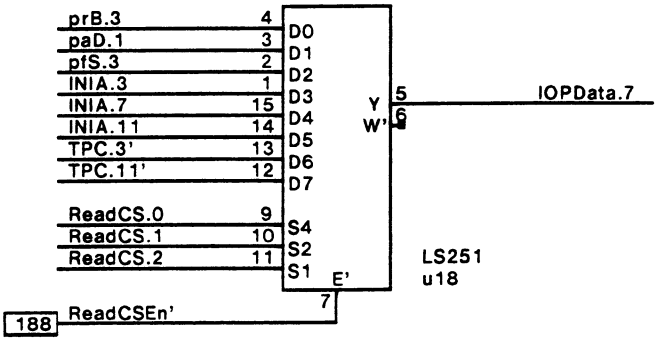




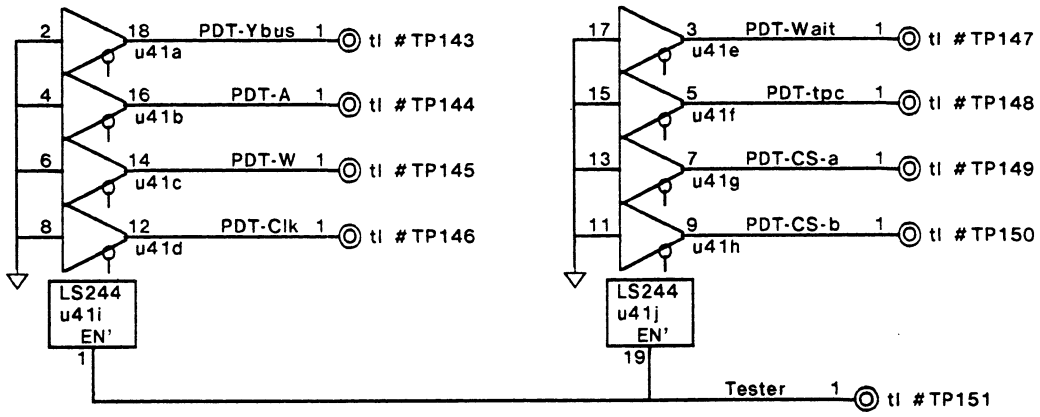








XEROX SDD	Project Dandelion	CS Read	File pLionHead25.sil	Designer Garner	Rev M	Date 8/23/80	Page 25



The Control Store can be read & written via backplane pins. Once tested, instructions (or parts of instructions), can be loaded in order to test additional features. For instance, all X-bus sources can be disabled by loading a 6 into CS bits 16-23 (controlled by CSWE.c'). Simple programs to test the 2901's can also be executed in this way.

The SU & RH registers can be loaded by controlling EnableSU, CIN-SE-wrSU, & RH← from a microinstruction.

stackP, IB, High SU Addr, & Low SU Addr can be similarly tested.

The MIR & MIR decoding can be tested by loading instructions into the CS.

PDT-Ybus is used to test devices attached to the Y bus.

PDT-A is used to disable registers or Proms whose outputs go to a register clocked by AlwaysClk.

PDT-W is similarly used for WaitClk.

PDT-Clk & PDT-Wait disable the outputs of AlwaysClk & WaitClk'd registers.

The following steps cause a CS byte to be written. It is assumed that the TPC has been written with the required CS address.

```
PDT-Clk ← 1; Swc3←1:                {cause NIA to come from TPC}
IOPWait ← 1;
SwTAddr' ← 0; SwTAddr ← 1:                {init code}
    IOPData ← data
    CSWE.x' ← 0; CSWE.x' ← 1;
```

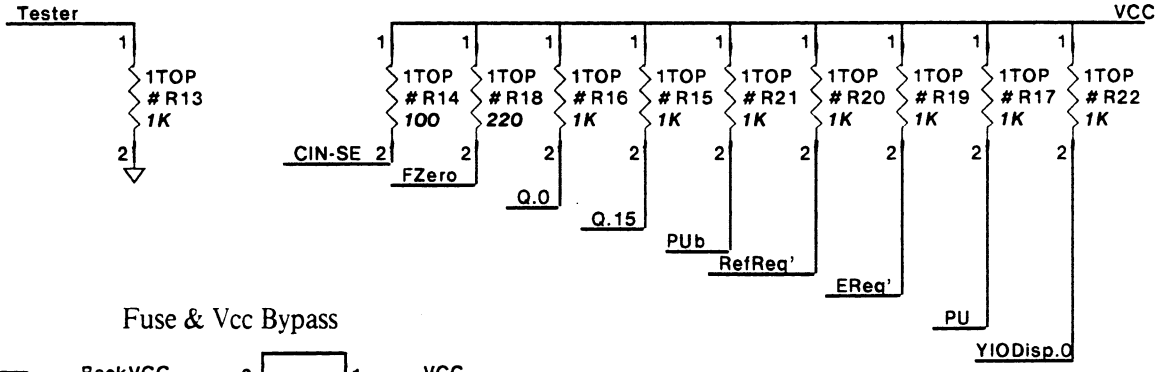
If IOPWait is left high, the CP will not execute the instruction which has been loaded into the CS. Instead, the CP will be frozen in a state where the instruction is totally decoded, but the result will no be loaded into any register. Thus, all the microinstruction register (MIR) decoding logic can be tested without even executing an instruction.

The following steps cause the TPC to be written:

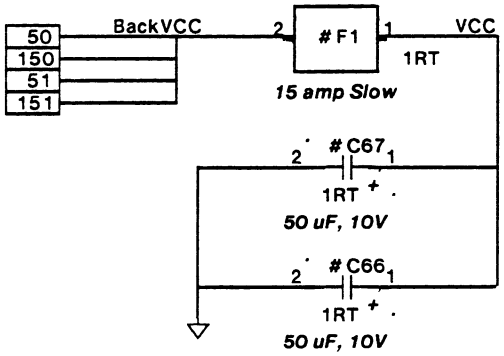
```
IOPWait ← 1:                                {init code}
SwTAddr' ← 0; SwTAddr ← 1:
    IOPData ← (addr lshift5) or (data rshift7):        {set TPC addr & high 5 bits of data}
    WrTPCHigh' ← 0; WrTPCHigh' ← 1:
    IOPData ← data and 7F'x:                {write low 7 bits}
    WrTPCLow ← 0; WrTPCLow ← 1:
```

D0 card test programs for reading & writting TPC & CS available on [Iris]<Workstation>LH>CardTest.dm

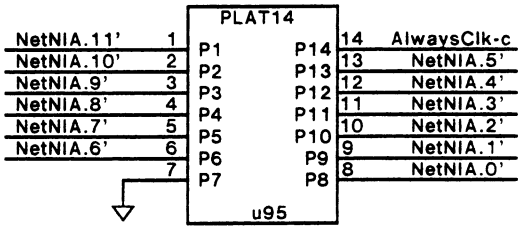
Pullups



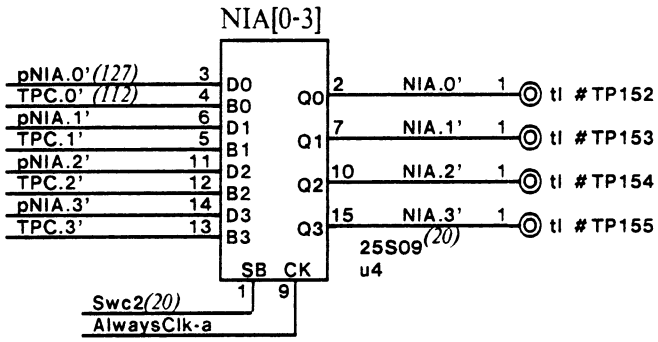
Fuse & Vcc Bypass



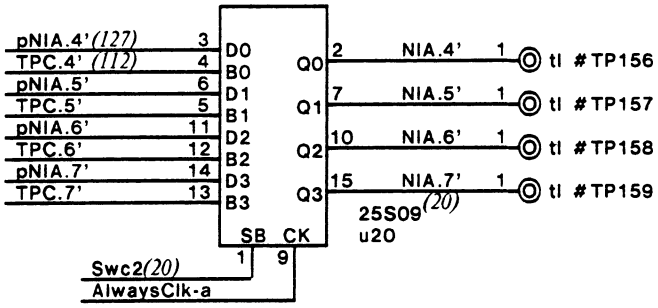
CS NIA Logic Analyzer Connector



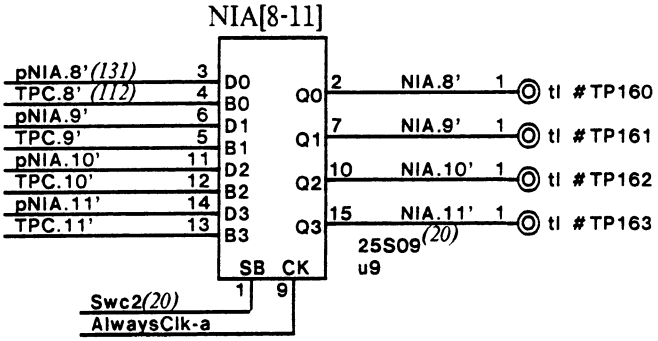
NIA[0-3]



NIA[4-7]

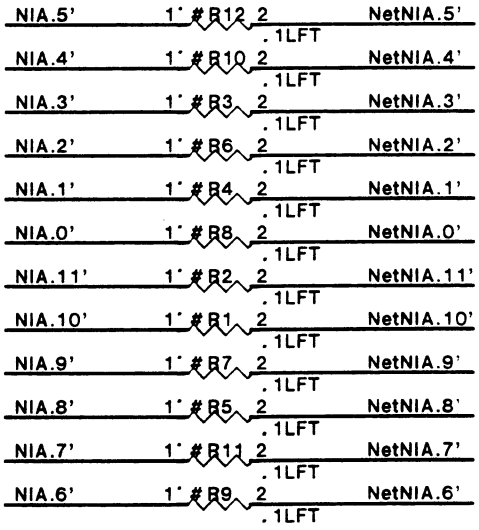


NIA[8-11]



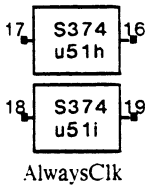
CS NIA Line Matching

15 ohms

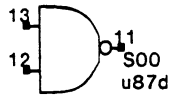


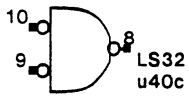
XEROX SDD	Project Dandelion	PC Discretes & NIA	File pLionHead27.sil	Designer Garner	Rev M	Date 10/30/80	Page 27

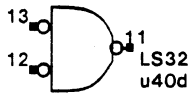
Unused Parts



AlwaysClk



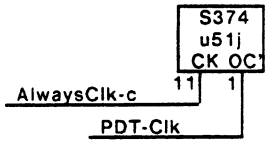




Junk 374 Allocation

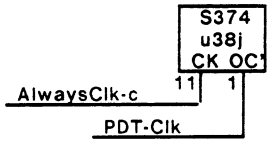
S374
g15 - Always Clock

b MAR←
c AllowMDR←
d KernReq`
e WaitC2
f WaitC3
g TCWait
h
i



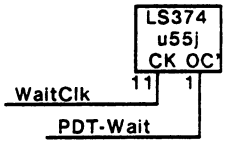
S374
h16 - Always Clock

b EKTrapc2`
c CSPar.4 *PC only*
d EKTrapc2
e EKErr.0`
f EKErr.1`
g Swc3
h Swc3`
i CSPar.5 *PC only*



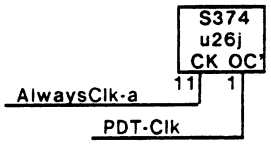
LS374
h17 - Wait Clock

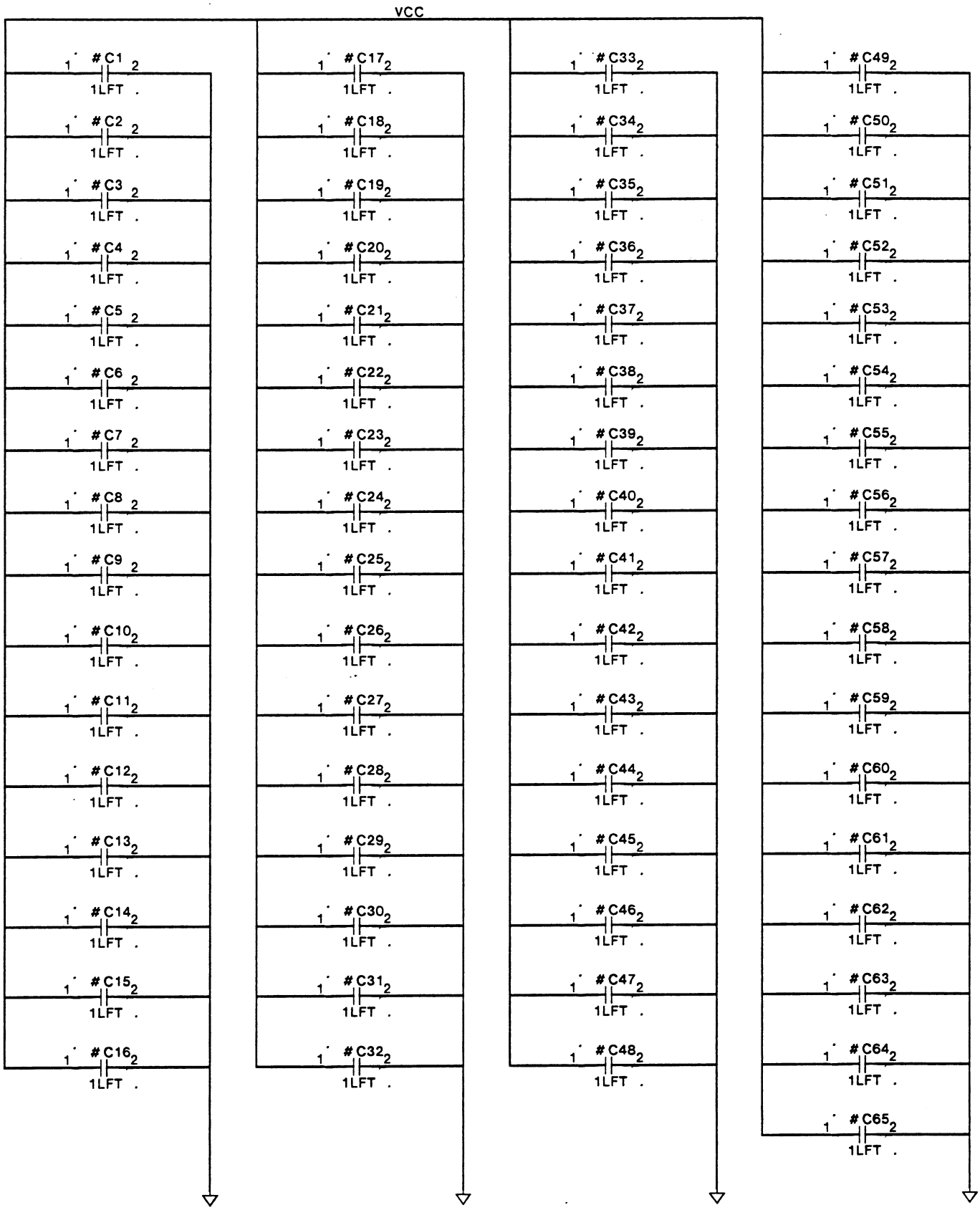
b IBPtr.0
c IBPtr.1
d CSParErr
e MesaInt
f StackErr
g VirtAddrErrc2
h pc16`
i MemErrc3



S374
f9 - Always Clock

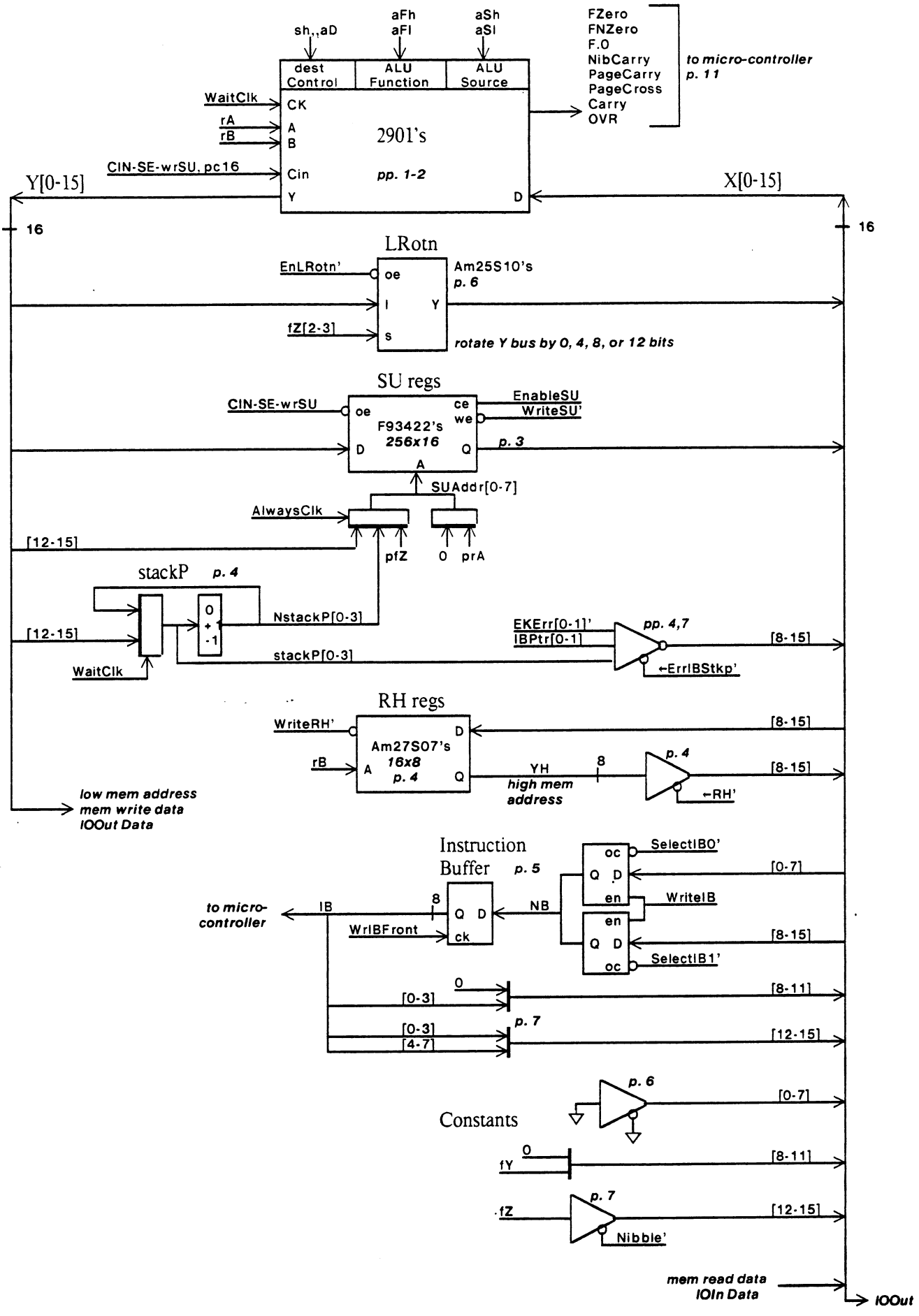
b CSPar.0
c CSPar.1
d CSPar.2
e CSPar.3
f TC.0
g TC.1
h TC.2
i TC.3



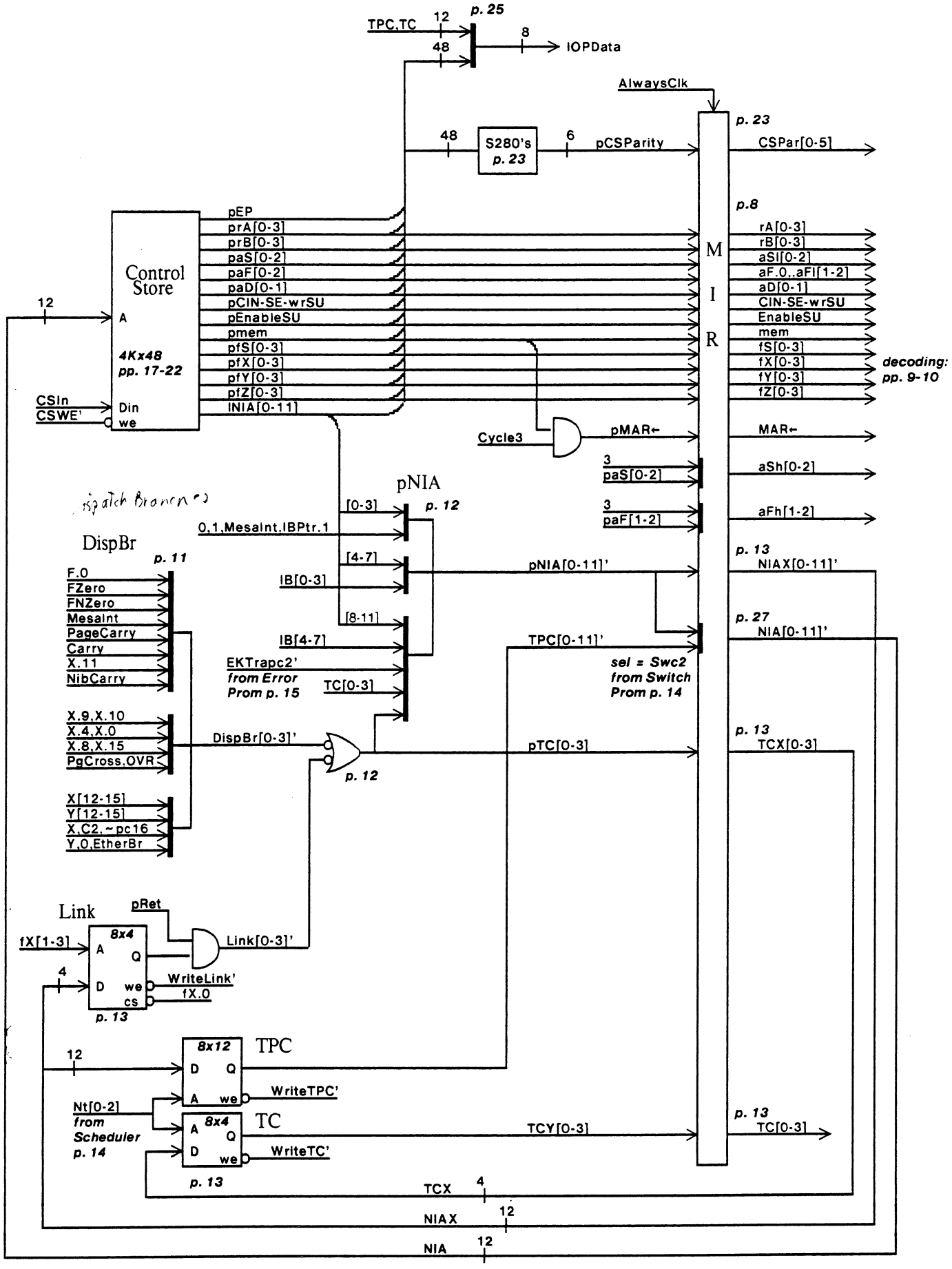


NOTE: C1-C65, CAP., CERAM, 50V, .10UF, PART NO. 702W05218

XEROX	Project		File	Designer	Rev	Date	Page
ED	Dandelion	Filter Capacitors	pLionHead29.sil	Lin	M	8/23/80	29

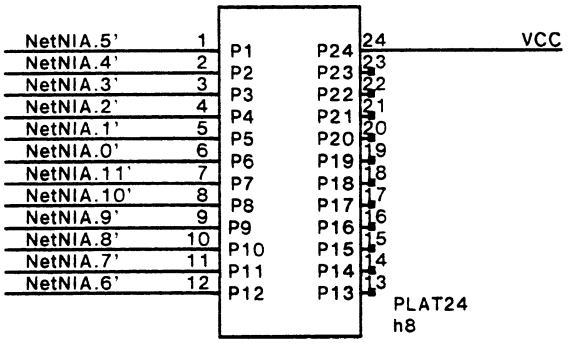


XEROX SDD	Project Dandelion	Block Diagram I	File LionHead38.sily	Designer Garner	Rev K	Date 30 Oct 80	Page 38

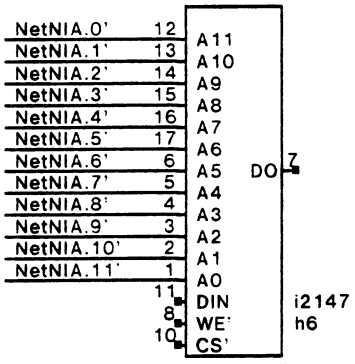


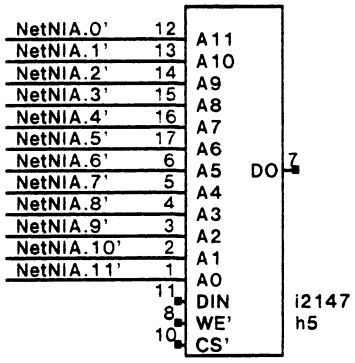
XEROX SDD	Project Dandelion	Block Diagram II	File LionHead39.sily	Designer Garner/ W.H.	Rev K	Date 30 Oct 80	Page 39

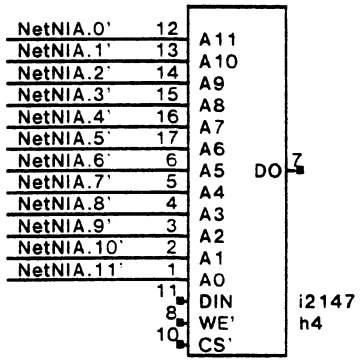
This diagram defines the NetNIA.wl wirelist. This list should be wired before LionHead.wl.
Except for the first entry in each net, each node should be welded off center and towards the closest edge of the board

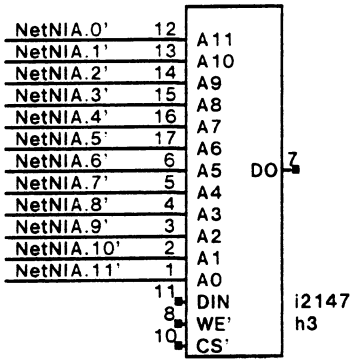


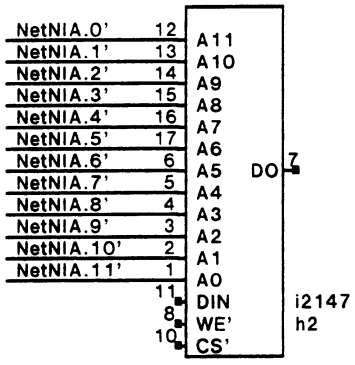
Just cut the ground connection (which is really a NetNIA line),
the LionHead wire list will cut the VCC connection.
(The LionHead wire list should not try to cut the GND again,
since it will have been connected to NetNIA.11')

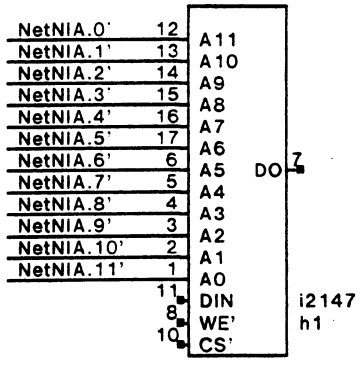












Rev A to Rev B (9 Oct 79)

1. Added timing info to all pages. Divided page 14 into 14 and 15, renumbering original 15-25.
Page 2: a. 1K pullup pack changed to 22-330 resistor pullup/pulldown. Ground to P8.
b. S09 changed to S03. Bits into Q ends inverted now. CIN-SE-wrSU' and pc16' necessary for CIN-SE.
Page 4: a. stackP read (instead of NstackP) onto X-bus (alllows stackP in arithmetic operations).
b. RH[0-3] moved to d17.
Page 5: a. IBProm changed: SelIB0' and SelIB1' are now used to immediately select either IB[0] or IB[1].
IB←' input removed and replaced with EKErrc2 (to cancel GoodIBDispc2, instead of at the pNIA S64's.
Interchanged IBPtr.0 and IBPtr.1, deleted IBPtr.1'.
Page 6: a. Changed pin4 of f19 from Y.4 to Y.3
b. Interchanged fZ.3 and fZ.2 on 25S10's
Page 7: a. Changed ErrInt Status to ErrIBPtr, i.e. subsituted IBPtr.0 for MesaInt' and IBPtr.1 for CSParErr'.
Page 8: a. Changed mem from pin 14 to pin 113.
b. Moved CIN-SE-wrSU from c9 to b9, creating CIN-SE-wrSU'. paF.0 took CIN's place. aD.0 was moved to aD.1, and aD.1 to aF.0
c. Changed MAR← to MAR←', discontected MAR← from backplane.
Page 9: a. On b11(fZNorm), changed AlwaysNI' to IBPtr←0'; fS.2 to fS.2'; and moved all outputs up one position.
Page 10: a. Added S04 inverter for aD.0', moved RH← to page 16.
b. Changed S20's to S08 + S10's, opening up an S10 for use.
Page 11: a. Replaced Cycle1 test with CSParErr and NibCarry test with MesaInt.
Page 12: a. at pNIA[0-3] changed pin 6 from GND to HIGH (to distinquish no interrupt, empty buffer from error trap at 0)
b. Rearranged pNIA[8-11] S64 inputs: EKErrc2 should have zeroed the dispatch/branch bits also.
Page 13: a. Moved Link.3' connection to pullup pack since it is now 220-330 Pullup-down.
b. Changed NIA's SB inputs from Swc3 to Swc2.
Page 14: a. Enlarged Schedule Prom, adding RefReq' input. Pullup connections to requests from Options board.
b. Changed all inputs to SwitchProm (see programs).
Page 15: a. MemCSErrProm renamed CSIntProm since MemErr moved out to S08 and MesaInt moved in.
b. StackVirtErrProm renamed StackVirtProm, ClrIntErr' input not needed.
c. ErrorProm inputs changed: Nt = Emu to Ct = Emu.
d. KEProm renamed KernPC16Prom since MesaInt moved out. KernReq' an input now.
Page 16: a. WriteIB qualifier changed from S08 to S260 with ppCLK--reduced IB's large hold time.
b. WrTPCLow inverted, RH← moved here.
c. Detection of Low bank changed to S260 (freeing up and S02 and S08).
Page 25: a. LS251 inputs rearranged so read data is identical to write data format.

Rev B to Rev C (17 Dec 79)

Page 2: a. Changed S1 of R Shift Ends from Cycle' to Shift' (to accomodate new fY = Cycle). Switched inputs to mux.
c. Added S86 PageCross.
Page 3: a. Added LS257 AltUAddr allowing low SU address to come from Y bus.
Page 5: a. EKErrc2 input to IBProm changed back to IB←'. PgCarryDly replaced by AllowMDR←. IBFront inverted.
Page 8: a. rB's S74's replaced by S374.
b. aS, aFh's S374 + S32 replaced by 25S09
c. Added MarPgCross' & AllowMDR← (to pin 11 backplane)
Page 9: a. Added Cycle to fY; AltUAddr to fY; PushNT to fZ
b. Inverted S.2 and S.3 values used to select IOIn.
Page 10: a. With new fY cycle, changed sh's S00 to S10; changed Pop's S00 to S86; With PushNT, changed Push's S00 to S10. changed MapRef's S00 to S86.
Page 11: a. Changed 4:1 mux for DispBr[0-1]' to 2:1 S258.
b. XC2npcDisp ← IODispA[2-3]; YIODisp ← IODispB[2-3]; IODisp ← XpcDisp; [] ← XwdDisp; PgCrossBr ← PgCarryBr; NibCarryBr ← DirtyBr;
Page 12: a. Interchanged TC's and IB's contection to pNIA[8-11], so that IB is blocked by EKTrapc2 (renamed from EKErrc2).
b. EKTrapc2 doesn't zero pNIA.11 (reduces loading on EKTrapc2 below max)
c. pTC.2 changed from S00 to S10 adding MarPgCross'
Page 14: a. SpareReq' added to ScheduleProm & Pullups. Task reqister enabled by Cycle2' now.
b. Nt = Emu from Pt = Emu established.
c. Waitc2' changed to Wait in SwitchProm.
Page 15: a. MemErr not gated by Pt = Emu any longer. Connected to ErrorProm instead.
b. CSParErr connected to BP pin 37.
Page 16: a. WriteTC = pAlwaysClk AND Cycle1 AND TCWait'. TCWait' added beyond Waitc3.
b. IOPWait gated with cycle1 now (so Stop correctly works).
Page 24: a. SwTAddr, SwTAddr', & IOPWait temporarily synched by Clock until IOP card does it.

Rev C to Rev D (1 Feb 80)- Rev D submitted for 1st etch.

Page 1: Added PDT-Y bus for testability; Moved the 2901's to free up 3 board positions.
Page 2: Q.0 & Q.15 pullups now 1K; Cin's pullup is 100 ohms; S03 replaced with S38 (used on HSIO board)
Page 5: IBFront changed to LS374; added PDT for testability; h17 now LS374.
Page 7: Byte inverted => D & B inputs interchanged on S257.
Page 8: rA & rB swapped (for layout); S08 to LS08; HIGH-a to PU
Page 9: fYNorm, fZNorm updated; fX moved to c13.
Page 10: PushY' added to Push; Refresh is now RefreshY or RefreshZ; S32 to LS32; XBus←IB' now S20 (so MAR←IB works)
Byte S08 changed to S00; fZHigh eliminated
Page 11: S258 changed to LS158; PgCrOvDisp, YOddBr added; PageCross changed back to PageCarry.
Page 12: EKTrap zeros pNIA.11 (again).
Page 13: Am29700 changed to Am29701 and LS32 gates output.
Page 14: Tasks reg changed to LS374; PDT added for testability.
Page 15: Now Switchweld & PC version of page 15: Sw version does not have CSPar.4 & CSPar.5 to CSIntProm--now a F93453
PDt added for testability; h17 & g15 now LS374; PopX' replaces Pop & Popz' added to StackProm.
Page 16: WrIBFront and C2Clk qualifiers added; WrTPCLow no longer inverted.
Page 23: Now Switchweld & PC version of page 23: Sw version uses 93S48 12-input parity chips & PC version uses S280's.
Page 24: IOPWait, SwTAddr, SwTAddr' no longer temporarily clocked; IOPBus renamed IOPData; LS241 replaced with LS244.
Page 25: IOPBus renamed IOPData
Page 26: LS244 added for testability
Page 27: Discrete page for PC & Sw versions--PC versions includes fuse & supply caps.
Page 28: Unused parts

Rev D to E (13 Feb 80) -- version actually used for 1st PC etch

5	SelectIB0 swapped with SelectIB1' (name change only)
9	←IOInSp1' changed to ←KTest' (name change only)
10	changed S86 to S00 which generates Pop since both PopX' and PopZ' can be active now..
17-22	For the PC version only, the NIA.#a', NIA.#b', NIA.#c', NIA.#d', NIA.#e', and NIA.#f' nets were replaced by NetNIA.#' This change was made for PC only.
p27	NIA.#' was swapped with NetNIA.#' on the resistors so the error messages would go away...
28	S86 now spare instead of S00.

Rev E to F (15 March 80) -- updates made to 1st PC etch.

2	S04 at c14d used to form FNZero
5	S260 at d16b now used to generate IBEmptyErr. IBProm now rev E.
8	LS08 gate producing BrMAR← from MAR← & IgnorePgCr added.
9	MapRefZ' deleted and MapRefY' added. changed name of DOAData←' & DOBData←' to DCtlFifo←' & DBorder←' IgnorePgCr' replaces MapRefZ'
10	MapRefZ' replaced with MapRefY'
11	IODisp replaced with XwdDisp. YOddBr replaced with NZeroBr.
12	IBPtr.1 replaced with IBPtr.0 (due to renumbering ibPtr states).
13	Per Testability Review, added PDT-tpc. Link pRet enable kludge made worse by ading LS32 producing pRet'.
15	IBEmptyErr replaces Pt = Emu in ErrorProm. MemErrC3 now gated with a LS08. ErrorProm now Rev D. Moved 374 clocks and enables to page28.
16	WriteIB now comes from S02 at a19d and LS32 at e14b (an ADDITIONAL PART).
17-22	Per Testability Review, PDT-CS-a and PDT-CS-b were added to the control store chips.
26	Per Testability Review, PDT-tpc, PDT-CS-a and PDT-CS-b added to LS244.
28	Moved Junk 374 clocks & enabled here, including the one for f9 (WHICH WAS FORGOTTEN in Rev E). Only one LS08, one S04 spare now. two LS32's gates spare.

Rev F to G (15 April 80) -- updates made to 1st etch.

	LS08 at b13 changed to S08; LS374 at g15 changed to S374
8	pAllowDMR← added: No mem write on IBEmtpyErr OR MarPgCross; IgnorePgCr eliminated
9	IgnorePgCr' eliminated.
12	pNIA.3' fed by IBPtr.1 instead of IBPtr.0 (above fix wrong)
15	StackVirtProm & ErrorProm now Rev E.
p27,s27	NetNIA', AlwaysClk, & GND connected to 14 pin plat at i5 for Logic Analyzer
28	S04 at c14f no longer unused.
49y	Printer registers
51y	S08, S374 parts change

Rev G to H (14 May 80) -- updates made to 1st etch

	163 test points were added
13	PDT-tpc connected to g9.2 (CS'). NIA moved to page 27.

Rev H to I (July 80) -- changes made by Richard Johnson (ED) to 1st etch layout (hand changes) plus other name/part changes
-- There were 8 Rev I boards manufactured. They require fixes to the incorrect changes below described.

	Am29701's replaced by Am27S07's
4	half of S241 at c18 and half S241 at d18 changed (inadvertently) into an S244. e17e-h swapped with a-d.
5	g17(v16)b-e reverse ordered. g16(v44)f-i reverse ordered. f16(v43)f-i reverse ordered, LS374 changed to S374.
6	half of S241 at c18 and half of S241 at d18 changed (inadvertently) into an S241-like chip with 2 EN inputs.
7	f18c got swapped inputs of f18d, f18d got swapped inputs of f18e, f18e got swapped inputs of f18c. Swapping inputs to the S257 multiplexer was (moderately) incorrect!!
9	XOData,XCtl,XIData.XStatus,IOOutSp1,IOOutSp2,IOOutSp3,PStatus,IOInSp2 renamed
13	Swapped inputs of i4.
14	SpareReq' renamed EORound
24	e8e-h reverse ordered. i13e interchanged with i13g.
27	i5.14 replaced with AlwaysClk-c

Rev I to J (24 Aug 80) -- changes made for etch 1.5 (Never built)

4,6	u146 & u118 (c18,d18) reconnected as in Rev. H
7	u142 (f18) reconnected as in Rev. H
10	u70b connected in order to invert Refresh (This change was not made on the MCtl card as directed)
27	R21 connected to u138.1 instead of SpareReq' (renamed to EORound)

Rev J to K (30 Oct 80) -- etch 2 definition

5	IBProm (HM7649) split into two F93453's.
14	XReq' renamed EReq'
24	LS244 @u1 (CSDataIn) changed to LS240 (to prevent ringing). -- requires change in IOP Kernel

Rev K to L (3 Dec 80) -- changes made to 2nd etch

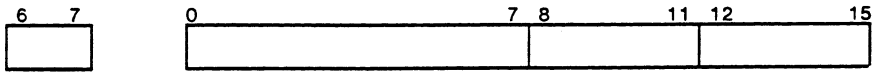
3, 5, 9, 13, 15, 23	Added test points according to D. Adams, ES

Rev L to M (2 April 81) -- etch 3 definition

10	u70b removed so that Refresh is no longer inverted (reality wins over politics)

YH,,Y Bus MAR← timing:

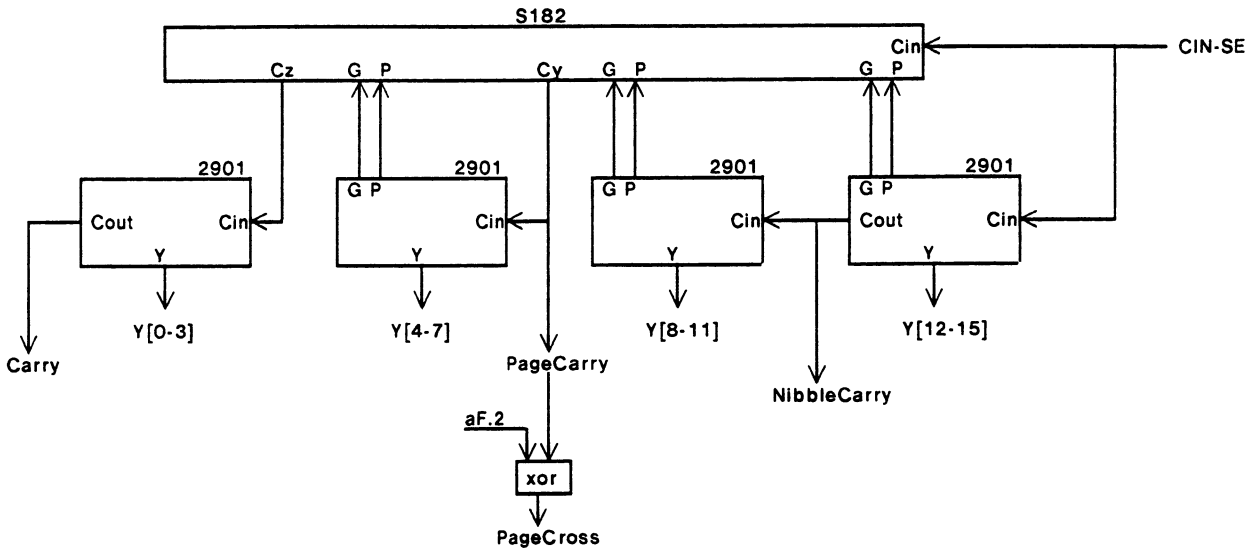
For high-half ALU, operation is 0 or B.



17[3]	Clk -> rB		59	disable X	59	disable X (See X bus timing)
35	rB -> YH	80 nS	67	D -> Y	42	D -> Y (See Y bus arithmetictiming)
5	YH bus	(See Ybus logic timing)	126	nS	101	nS
57[3]	= 60 nS					

Y bus Arith timing:

Ripple carry is used in low half of ALU, and lookahead in high half.



X bus arithmetic: Ybus ← XBus + A

x	Xbus time
30	D -> G,P[4-11]
7[2]	G,P -> Cin.7, Cin.3
25	Cin -> Y[0-7]
10	Y bus
72[2]	= (74 + x) nS

x	Xbus time
32	D -> Cout[12-15]
25	Cin -> Y[8-11]
10	Y bus
(67 + x) nS	

x	Xbus time
32	D -> Y[12-15]
10	Y bus
(42 + x) nS	

Register Arithmetic: Ybus ← A + B

max(109, 95)

17[3]	↑ -> rB
45	rB -> G,P
7[2]	G,P -> Cin.7, Cin.3
25	Cin -> Y[0-7]
10	Y bus
104[5]	= 109 nS

48	↑ -> CIN-SE (see p. 2)
11[1]	S182 Cin -> Cin.7, Cin.3
25	Cin -> Y[0-7]
10	Y bus
94[1]	= 95 nS

max(105, 99)

17[3]	↑ -> rB
50	rB -> Cout[12-15]
25	Cin -> Y[8-11]
10	Y bus
102[3]	= 105 nS

48	↑ -> CIN-SE (see p. 2)
16	Cin[12-15] -> Cout
25	Cin -> Y[8-11]
10	Y bus
99	nS

max(83, 80)

17[3]	↑ -> rB
50	rB -> Y[12-15]
10	Y bus
77[3]	= 80 nS

48	↑ -> CIN-SE (see p. 2)
25	Cin -> Y[12-15]
10	Y bus
83	nS

Ybus Logic Timing:

Xbus Logic
Ybus ← Xbus .or. 0

x	X bus
32	D -> Y
10	Ybus
(42 + x) nS	

Register Logic:
Ybus ← A .or. B

17[3]	↑ -> rA, rB
50	rB -> Y
10	Ybus
77[3] = 80 nS	

A pass around (aD=2):
Ybus ← A

17[3]	↑ -> rA
40	rA -> Y (via A bypass)
10	Ybus
67[3] = 69 nS	

Xbus Source timing:

Xbus ← A LRotn {A bypass}	69 ↑ -> Y (see above) 12 25S18 prop 10 Xbus 91 nS	(Xbus to Ybus time = 22 nS)	Disable = 56 nS
Xbus ← (A or B) LRotn	80 + 22 = 102 nS		Disable = 56 nS
Xbus ← (A + B) LRotn	109 + 22 = 131 nS	105 + 22 = 127 nS	83 + 22 = 105 nS
Xbus ← SU	75 nS (see p. 3)		Disable = 58 nS
Xbus ← RH[B]	74 nS (see p. 4)		Disable = 59 nS
Xbus ← IB	59 nS (see p. 5)		Disable = 49 nS
Xbus ← MD	97 nS max		Disable = 17[3] + 3 (BP) + 5 + 15 + 10(Xubs) = 53 nS
Xbus ← 4-bit constant	50 nS (see p. 7)		Disable = 50 nS
Xbus ← 8-bit constant	56 nS (see p. 7)		Disable = 49 nS
Xbus ← ErrIBStkP	59 nS (see p. 4)		Disable = 59 nS
Xbus[0-7] ← 0	55 nS (see p. 7)		Disable = 55 nS
Xbus ← IOIn	34 ↑ -> ← IOIn' 3 backplane 15 S240 EN' to X 10 Xbus 62 nS	34 ↑ -> ← IOIn' 3 backplane 18 S374 EN' to X 10 Xbus 65 nS	Disable = 59 nS

External Register Write Setups:

SU Write Setup (SU ← Ybus):

5[1]	F93422 data setup (from beginning of write pulse)
39	WE pulse width
44[1] = 45 nS	

RH Write Setup (RH ← Xbus): 36 nS (see p. 4)

IB Write Setup (IB ← Xbus): 37 nS (see p. 5)

IOOut Write Setup (IOOut ← Xbus): equals setup time of receiving reg.
data setup for LS374/LS273 = 20[2] = 22 nS

Dispatch/Branch Condition Bits Setup:

```
7[1]    S151/S258 in -> DispBr
5       DispBr -> pTC
6[1]    pTC -> pNIA
5[1]    25S09/S374 setup
23[3] = 26 nS
```

D-input Setup Times:

Logic
B ← Xbus or 0
B ← Xbus or A

40 nS

Logic & Branch
B ← Xbus .xor. A, ZeroBr

```
32   D -> F.0, F = 0
26   DispBr setup
58 nS
```

Logic & YDisp
B ← Xbus .xor. A, YDisp

```
32   D -> Y
10   Ybus
26   DispBr setup
68 nS
```

Logic & Single-Bit Shifting
B ← Xbus .or. A, LShift1

```
35   D -> R.3
15   RAM3 setup
50 nS
```

Logic & Single-Bit Rotates
B ← Xbus .or. A, LRot1

```
35     D -> R.15
9[1]   S253 in to R.0
15     RAM0 setup
59[1] = 60 nS
```

Logic & Double-Bit Shift/Rotate
B ← DRShift1 B

```
35   D -> R.15
20   S38 in to Q.0
10   RAM3 setup
65 nS
```

	Xbus[0-7]	Xbus[8-11]	Xbus[12-15]
Register Arithmetic B ← Xbus + A	30 D -> G,P 7[2] G,P -> Cin.3, Cin.7 35 Cin setup 72[4] = 74 nS	32 D -> Cout[12-15] 35 Cin.11 setup 67 nS	40 nS (Logic setup)
Register Arithmetic & ZeroBr B ← Xbus + A, ZeroBr B ← Xbus + A, NZeroBr	30 D -> G,P 7[2] G,P -> Cin.3, Cin.7 30 Cin -> F = 0 26 DispBr setup 93[2] = 95 nS max(95, 86, 58)	32 D -> Cout[12-15] 30 Cin -> F = 0 26 DispBr setup 88 nS Add 5 nS for NZeroBr	58 nS (Logic&Branch)
Register Arithmetic & NegBr B ← Xbus + A, NegBr	22 Cin -> F.0 = 95-8 = 87 nS		
Register Arithmetic & OvBr B ← Xbus + A, OvBr	25 Cin -> Ovr = 95-5 = 90 nS		max(58 + x, 90) nS
Register Arith & Carry branches B ← Xbus + A, NibCarryBr B ← Xbus + A, PgCrossBr B ← Xbus + A, CarryBr	30 D -> G,P 7[2] G,P -> Cin 16 Cin -> Cout.0 26 DispBr setup 79[2] = 81 nS (CarryBr)	30 D -> G,P 7[2] G,P -> PgCarry 11[1] PgCarry -> PgCross 26 DispBr setup 74[3] = 77 nS (PgCrossBr) (MarPgCrossBr = 75 nS)	32 D -> Cout 26 DispBr setup 58 nS (NibCarryBr) 48 ↑ -> CIN-SE 16 Cin -> Cout 26 DispBr setup 90 nS
Arithmetic & YDisp B ← Xbus + A, YDisp	Timing for X[0-7] does not affect YDisp		68 nS (Logic&YDisp)
Arithmetic & Single-Bit Shifting B ← Xbus + A, RShift1	30 D -> G,P 7[2] G,P -> Cin.3, Cin.7 35 Cin -> R.3 15 RAM3 setup 87[2] = 89 nS	30 D -> Cout[12-15] 35 Cin -> R.3 15 RAM3 setup 80 nS	50 nS (Logic&Shifting)
Arithmetic & Singl-Bit Rotating B ← Xbus + A, RRot1	89 + 10 = 99 nS	80 + 10 = 90 nS	60 nS (Logic&Rotating)
Arithmetic & Double-Bit Shift/Rotate B ← DARShift1 B	30 D -> G,P 7[2] G,P -> Cin 16 Cin -> Cout.0 9[1] S253 to R.0 15 RAM0 setup 77[3] = 80 nS		

R Register Cycle Times

Register Logic
B ← A .and. B

```
17[3]  ↑ -> rA
 60    rA setup
77[3] = 80  nS
```

Register Logic & Branch
B ← A .xor. B, ZeroBr,
B ← A .xor. B, NegBr,

```
17[3]  ↑ -> rA
55     rA -> F = 0
26     DispBr setup
98[3] = 101  nS
```

```
17[3]  ↑ -> rA
50     rA -> F.0
26     DispBr setup
93[3] = 96  nS  (NegBr)
```

Register Logic & YDisp
B ← A .xor. B, YDisp,

```
80     Ybus ← A .xor. B
26     DispBr setup
106  nS
```

A Bypass & YDisp
[] ← A, YDisp

```
69     Ybus ← A
26     DispBr setup
95   nS
```

Register Logic & Shifting
B ← A .or. B, LShift1

```
17[3]  ↑ -> rA
55     rA -> R.3
15     RAM3 setup
87[3] =  90  nS
```

```
17[3]  ↑ -> rA
55     rA -> R.3
20     S38 to Q.0
10     Q0 setup
102[3] = 105 nS
       (DRShift1)
```

```
30     ↑ -> Q.0
 9[1]  S253 to R.15
15     RAM3 setup
54[1] = 55 nS
       (DLShift1)
```

Register Logic & Rotating
B ← A .or. B, LRot1

```
17[3]  ↑ -> rA
55     rA -> R.3
 9[1]  S253 in to R.0
15     RAM0 setup
96[4] = 100  nS
```

	bits[0-7]	bits[8-11]	bits[12-15]
	max(109, 98)	max(105, 99)	
Register Arithmetic B ← A + B	17[3] ↑ -> rA 45 rA -> G,P 7[2] G,P -> Cin.3, Cin.7 35 Cin setup 104[5] = 109 nS	17[3] ↑ -> rA 50 rA -> Cout[12-15] 35 Cin.11 setup 102[3] = 105 nS	80 nS (Reg Logic)
	48 ↑ -> CIN-SE 11[2] CIN-SE -> Cin.3(S182) 35 Cin setup 94[2] = 98 nS	48 ↑ -> CIN-SE 16 CIN-SE -> Cout[12-15] 35 Cin.11 setup 99 nS	
Register Arithmetic & Branch B ← A + B, ZeroBr B ← A + B, NZeroBr B ← A + B, NegBr B ← A + B, OvBr B ← A + B, CarryBr, B ← A + B, PgCrossBr, B ← A + B, NibCarryBr,	17[3] ↑ -> rA 45 rA -> G,P 7[2] G,P -> Cin.3, Cin.7 30 Cin -> F = 0 26 DispBr setup 127[5] = 132 nS (ZeroBr)	17[3] ↑ -> rA 30 rA -> Cout[12-15] 30 Cin -> F = 0 26 DispBr setup 103[3] = 106 nS (ZeroBr)	101 nS (Logic&Branch) Add 5 nS for NZeroBr
	22 Cin -> F.0 = => 124 nS (NegBr)	22 Cin -> PgCarry 11[1] PgCarry -> PgCross 33[1] = 34 nS = => 110 nS (PgCrossBr)	48 ↑ -> CIN-SE 16 CIN-SE -> NibCarry 26 DispBr setup 90 nS (NibCarryBr)
	25 Cin -> OVR = => 127 nS (OvBr)		
	16 Cin -> Carry = => 118 nS (CarryBr)		
Arithmetic & YDisp B ← A + B, YDisp	Timing for X[0-11] does not affect YDisp		104 nS (Logic&YDisp)
Arithmetic & Shifting B ← A + B, RShift1	17[3] ↑ -> rA 30 rA -> G,P 7[2] G,P -> Cin.3, Cin.7 35 Cin -> R.3 15 RAM3 setup 107[5] = 112 nS	17[3] ↑ -> rA 30 rA -> Cout[12-15] 35 Cin -> R.3 15 RAM3 setup 97[3] = 100 nS	90 nS (Logic&Shifting)
Arithmetic & Rotating B ← A + B, RRot1	112 + 10 = 122 nS	100 + 10 = 110 nS	100 nS (Logic&Rotating)

			X Source										
		D setup	SU	MD	* RH	* Nibble	* Byte	* IB	* ErrIBStkP	IOIn	A LRotn	(A .or. B) LRotn	(A+B) LRotn
	X ←		75	97	74	50	56	59	59	63	91	102	
	max (59, X←)		75	97	74	59	59	59	59	63	91	102	131 127 105
X Operation	B←X or A	40	115	137	114	99	99	99	99	103	131	—	—
	[]←X or A, ZeroBr	58	133	*155*	132	117	117	117	117	121	*149*	—	—
	[]←X or A, NZeroBr	63	138	*160*	137	122	122	122	122	126	*154*	—	—
	[]←X or A, NegBr	58	133	*155*	132	117	117	117	117	121	*149*	—	—
	[]←X .or.A, YDisp	68	*143*	*165*	*142*	127	127	127	127	131	*159*	—	—
	B←X .or. A, LShift1	50	125	*147*	124	109	109	109	109	113	—	—	—
	B←X .or. A, LRot1	60	135	*157*	134	119	119	119	119	123	—	—	—
	MAR←X .or. A	78	*153*	—	*152*	137	137	137	137	*141*	—	—	—
	MDR←X .or. A	45	120	—	119	104	104	104	104	108	—	—	—
	SU←X .or. A	87	—	*184*	*161*	*146*	*146*	*146*	*146*	*150*	—	—	—
	IOYOut←X .or. A	64	139	*161*	138	123	123	123	123	127	—	—	—
	B←X + A	74 66 40	*149* *141* 115	*171* *163* 137	*143* 140 114	133 125 99	133 125 99	133 125 99	133 125 99	137 129 103	*165* *157* 131	—	—
	[]←X + A, ZeroBr	95	*170*	*192*	*169*	*154*	*154*	*154*	*154*	*158*	*186*	—	—
	[]←X + A, NegBr	87	*162*	*184*	*161*	*146*	*146*	*146*	*146*	*150*	*178*	—	—
	[]←X + A,OvBr	90	*165*	*187*	*164*	*149*	*149*	*149*	*149*	*153*	*181*	—	—
	[]←X + A,NibCarry	58	133	*155*	132	117	117	117	117	121	*149*	—	—
	[]←X + A,PgCarryBr	65	140	*162*	139	124	124	124	124	128	—	—	—
	[]←X + A,PgCrossBr	77	*152*	*174*	*151*	136	136	136	136	140	*168*	—	—
	[]←X + A,CarryBr	81	*156*	*172*	*155*	140	140	140	140	*144*	*171*	—	—
	[]←X + A,YDisp	68	*143*	*165*	*142*	127	127	127	127	131	*159*	—	—
	B←X + A, RShift1	89 80 50	*164* *155* 124	*186* *177* *147*	*163* *154* 124	*148* 139 109	*148* 139 109	*148* 139 109	*148* 139 109	*152* *143* 113	—	—	—
	B←X + A, RRot1	99 90 60	*174* *165* 135	*196* *187* *157*	*173* *164* 134	*158* *149* 119	*158* *149* 119	*158* *149* 119	*158* *149* 119	*162* *153* 123	—	—	—
	MAR←X + A	- 78 78	*153*	—	*152*	137	137	137	137	*141*	—	—	—
	MDR←X + A	77 70 45	*152* *145* 120	—	*151* *144* 119	136 129 104	136 129 104	136 129 104	136 129 104	135 133 108	—	—	—
	SU←X + A	119 112 87	—	*216* *209* *184*	*193* *186* *161*	*178* *171* *146*	*178* *171* *146*	*178* *171* *146*	*178* *171* *146*	*182* *174* *150*	—	—	—
	IOYOut←X + A	80 73 48	*155* *148* 123	*177* *170* *145*	*154* *147* 122	139 132 107	139 132 107	139 132 107	139 132 107	*143* 136 111	—	—	—
	[] ← X, XDisp	32	107	129	106	91	91	91	91	94	123	134	*163* *159* 137
	RH ← X	36	111	133	110	95	95	95	95	99	127	138	*167* *163* *146*
	IB ← X	37	112	134	111	96	96	96	96	100	128	139	*168* *164* *148*
	IOXOut←X (LS374)	22	97	117	96	79	79	79	79	83	111	122	*153* *149* 127

* Timing for bits[0-7] of these sources is that of Nibble
The 3 numbers for arithmetic operations correspond to bits[0-7], bits[8-11], & bits[12-15], respectively.
stackP← has timing of the slow IOYOut.

		Y Source		
	setup	A .or. B	A (bypass)	A + B
Y ←		**80**	**69**	**109** **105** **83**
Y Operation: MAR ← *	**36** **11** **36**	116 91 116	105 80 105	114 116 119
Y Operation: MDR←	**3**	83	72	112 108 86
Y Operation: SU←	**45**	125	114	***154*** ***150*** 128
Y Operation: stackP←	**6**	86	75	115 112 89
Y Operation: []← . YDisp	**32**	112	101	121
Y Operation: Uaddr[4-7]←	**15**	95	84	124 120 98
Y Operation: IOYOut← (S374)	**6**	86	75	115 112 89

* Bits[0-7] have timing of Y ← (B .or. 0), except in the A bypass case.

The 3 numbers for arithmetic operations correspond to bits[0-7], bits[8-11], & bits[12-15], respectively.

X bus Loading & Estimated Capacitance

(for X[12-15] since these bits have the greatest loading & length)

Capacitances are based on experimental measurements (see p. 55)

Source	Sink	Part	Source Drive	Sink Load	Capacitance (pF)
	D-input	IDM2901A-1		.4/.18	4
	RH	Am27S07		.2/.125	4
	IB	S373		1/.125	4
	XDisp	S151		1/1	4
	XLDisp	S151		1/1	4
	"HSIO"	S241		1/.2	8
	"Option"	S241		1/.2	8
	IOPOData	LS374		.4/.2	4
	IOPCtl	LS273		.4/.2	4
SU		93422	104/4	1/.025	5
LRotn		Am25S10	130/10	1/.025	9
ErrIBStkp		S240	60/32	1/.025	11
RH		S241	60/32	1/.025	11
IB		S257	130/10	1/.025	5
Nibble		S241	60/32	1/.025	11
MD		S240	60/32	1/.025	11
IOPIData		S374	130/10	1/.025	5
IOPStatus		S240	60/32	1/.025	11
XIData		S374	130/10	1/.025	5
XStatus		S240	60/32	1/.025	11
KIData		S374	130/10	1/.025	5
KStatus		S240	60/32	1/.025	11
KTest		S240	60/32	1/.025	11
MStatus		S240	60/32	1/.025	11
Min Source Drive		S240/93422	60/4		
Total Sink Load				22/3.7	

Total Component Capacitance	177 pF
Etch @ 50" (CP=20, HSIO=10, MCtl=8, Opt=5, IOP=4, BP=3)	150 pF
Total X bus Capacitance	327 pF

Table Entries: High U.L./ Low U.L.
1 High U.L. = 50 uA
1 Low U.L. = 2.0 mA

Y[0-7] Bus loading

Source	Sink	Part	Source Drive	Sink Load
Y-output		IDM2901A-1	32/10	
	LRotn	Am25S10		1.5/1.5
	SU	93442		.8/.15
Y.4	MAR	S253		3(1/1)
	MDR	S373		1/.125
	MCtl	S138		1/1
	DCtlFifo	S373		1/.125
	DBorder	LS374		.4/.2
Total Sink Load				8.7/6.1

Y[8-15] Bus loading

Source	Sink	Part	Source Drive	Sink Load
Y-output		IDM2901A-1	32/10	
	LRotn	Am25S10		1.5/1.5
	SU	93442		.8/.15
	stackP	25S09		1/1
	AltUAddr	S257		1/1
Y.12	MAR	S253		2(1/1)
	MDR	S373		1/.125
	MCtl	LS374		.4/.2
	DCtlFifo	S373		1/.125
	DBorder	LS374		.4/.2
	YDisp	S151		1/1
Total Sink Load				10.5/7.4

Table Entries: High U.L./ Low U.L.

1 High U.L. = 50 uA
1 Low U.L. = 2.0 mA

PC version:	#	I_{typ}	I_{total}	
IDM2901A-1	4	160	640	
Am27S07	7	75	525	
AM25S09	7	75	525	
AM25S10	4	60	240	
i2147L	48	100	4800	
F93422	4	95	380	
F93427	2	85	170	
F93453	4	120	480	
HM7649	1	120	120	
SN74S00	4	15	60	
SN74S02	1	22	22	
SN74S04	2	23	46	
SN74S08	1	25	25	
SN74S10	2	12	24	
SN74S20	1	6	6	
SN74S38	1	32	32	
SN74S51	1	11	11	
SN74S64	4	8	32	
SN74S86	1	50	50	
SN74S138	8	49	392	
SN74S151	3	45	135	
SN74S175	1	60	60	
SN74S182	1	69	69	
SN74S240	1	90	90	
SN74S241	3	108	324	
SN74S253	1	55	55	
SN74S257	4	52	208	
SN74S260	1	22	22	
SN74S280	6	67	402	
SN74S373	2	105	210	
SN74S374	7	90	630	
SN74LS32	3	4	12	
SN74LS158	3	5	15	
SN74LS244	4	20	80	
SN74LS251	8	7	56	
SN74LS283	1	20	20	
SN74LS374	1	27	27	
	156		11.0 Amps	(70 mA/chip)

Stichweld only:				
Am93S48	4	57	228	
	154		10.8 Amps	(70 mA/chip)

1 10 20 30 40 50 51 60 70 80 90 100
101 150 151 200

Am29701 can be used instead of Am27S07

	a	b	c	d	e	f	g	h	i	
19	S02 pWait,pAlws Pt, WrIB	S257 0, Byte	25S10 LRotn.0	25S10 LRotn.1	25S10 LRotn.2	25S10 LRotn.3	LS374 Tasks	F93453 SchedProm	LS244 CS-IOP Recv	19
18	S138 IOOut	S138 IOIn	S241 0,RH[0-3]	S241 0,RH[4-7]	S241 Nibble, Pt	S257 ibLow. ibHigh	HM7649 IBProm	F93453 ErrorProm	F93427 SwProm	18
17	S138 IOOut	S138 IOIn	F93453 StackVirtErr	AM27S07 RH[0-3]	S240 ErrIBStkp	S257 0, ibHigh	S373 IB[1]	LS374 WaitClks	LS244 Tester	17
16	S257 AltUAddr	LS283 NstackP	25S09 stackP	S260 ProcLow, IBEmptyErr	AM27S07 RH[4-7]	S374 IBFront	S373 IB[0]	S374 AlwaysClks	F93427 Kpc16Prom	16
15	S00 Byte',Nib' pMAR',X←0	25S09 SUAddrHigh	F93422 SU[0-3]	F93422 SU[4-7]	F93422 SU[8-11]	F93422 SU[12-15]	S374 @ AlwaysClks	F93453 CSIntProm		15
14	S138 fYNorm(Req)	25S09 SUAddrLow	S04 Mar←,RH←,c3, F#0,aD.0,ibE	S00 WrSU,WrLink, WrIBf,WrRH	LS32 @ Link, WrIB, ..., ...	S00 @ WrTC,C2Clk, Pop, ...	S253 R Ends	S38 Q Ends, CIN-SE	LS374 IOPTPCHigh	14
13	S138 fYNorm	S08 paShO,MemErr pAllow,TCWt	S138 fX	S04 AlwysClk(3), WaitClk,C1,c2	S51 WriteTPC', Waitc1'	LS32 Link	S182 LookAhead	18Pin Plat Resistors	LS244 IOPTPCLow	13
12	q12 a IDM2901A-1 [0-3]	m12 b IDM2901A-1 [4-7]	c		n12 e IDM2901A-1 [8-11]	f	p12 g IDM2901A-1 [12-15]	h		12
11	S20 XBus←IB, LRotn	S138 fZNorm	S10 push,sh,Xbyte	S10 pTC.3,Wait, pTC.2	S151 DispBr.3A	S151 DispBr.2	S64 pNIA.8	S64 pNIA.9	S64 pNIA.10	11
10	S86 PgCr,Ref' Map,Ref	25S09 aSh,aFh	S374 rA, aS	S00 pTC.0,1, PgCross,Cinpc	S151 DispBr.3B	LS158 DispBr.01	LS158 pNIA[4-7]	LS158 pNIA[0-3]	S64 pNIA.11	10
9	S374 fX, fZ	S175 Cin',fY.0,fS	S374 Misc,fY,fS	S374 rB,aD,aFl	AM27S07 Link	S374 TC, CSPar	AM27S07 TC	S374 NIAX[8-11]	25S09 NIA[8-11]	9
8	a LS251 IOPBus.0	b 93S48 pCSPar.0	c 93S48 pCSPar.1		e LS244 CSIn	f 93S48 pCSPar.2	g 93S48 pCSPar.3	h 18 ohm resistors		8
7	i2147L pfZ.0	LS251 IOPBus.1	LS251 IOPBus.2	LS251 IOPBus.3	LS251 IOPBus.4	LS251 IOPBus.5	LS251 IOPBus.6	LS251 IOPBus.7	25S09 NIA[0-3]	7
6	i2147L pfX.0	i2147L pfZ.1	i2147L pfZ.2	i2147L pfZ.3	i2147L INIA.8	i2147L INIA.9	i2147L INIA.10	i2147L INIA.11	25S09 NIA[4-7]	6
5	LS32 EnDispBr	i2147L pfX.1	i2147L pfX.2	i2147L pfX.3	i2147L INIA.4	i2147L INIA.5	i2147L INIA.6	i2147L INIA.7	PLAT logic analyzer	5
4	i2147L pfY.0	i2147L pfY.1	i2147L pfY.2	i2147L pfY.3	i2147L INIA.0	i2147L INIA.1	i2147L INIA.2	i2147L INIA.3	S374 NIAX[0-7]	4
3	i2147L pEP	i2147L pCIN-SE-WrSU	i2147L pEnSU	i2147L pmem	i2147L pfS.0	i2147L pfS.1	i2147L pfS.2	i2147L pfS.3	AM27S07 TPC[8-11]	3
2	i2147L paS.0	i2147L paS.1	i2147L paS.2	i2147L paF.0	i2147L paF.1	i2147L paF.2	i2147L paD.0	i2147L paD.1	AM27S07 TPC[0-3]	2
1	i2147L prA.0	i2147L prA.1	i2147L prA.2	i2147L prA.3	i2147L prB.0	i2147L prB.1	i2147L prB.2	i2147L prB.3	AM27S07 TPC[4-7]	1
	a	b	c	d	e	f	g	h	i	

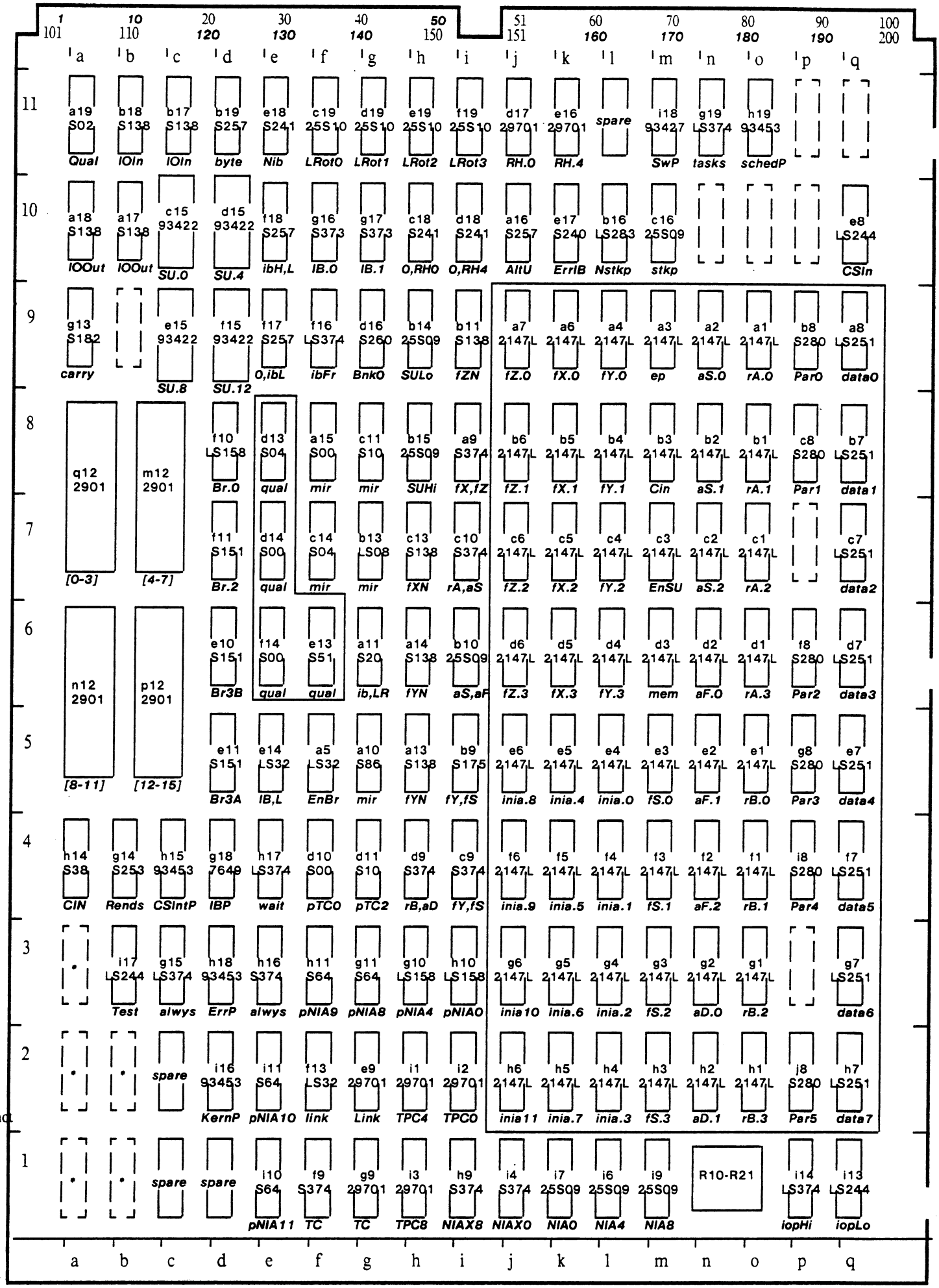
6 holes must be drilled here & nets blue-wired

DIP Orient.

I/O Connector Area (Top)

I/O Connector Area (Bottom)

XEROX SDD	Project Dandelion	Stichweld Layout	File LionHead52.sily	Designer Garner	Rev I	Date 24 [illegible] 80	Page 52



XEROX	Project		File	Designer	Rev	Date	page
SDD	Dandelion	PC Layout	LionHead53.sil	Garner	F	2/1/78	53

I. Filter caps: 1 per 3 chip positions; 2 per 2147L; 1 per 2901.

II. Don't use PC layout positions a1, b1, a2, & b2.

III. There are 5 spare positions: c1, d1, c2, b3, l11.

IV. Clock qualifiers: The qualifier chips boxed in the PC layout should be kept together & near their current location (i.e. center of "board"). The S02 at pc loc a11 should not be moved.

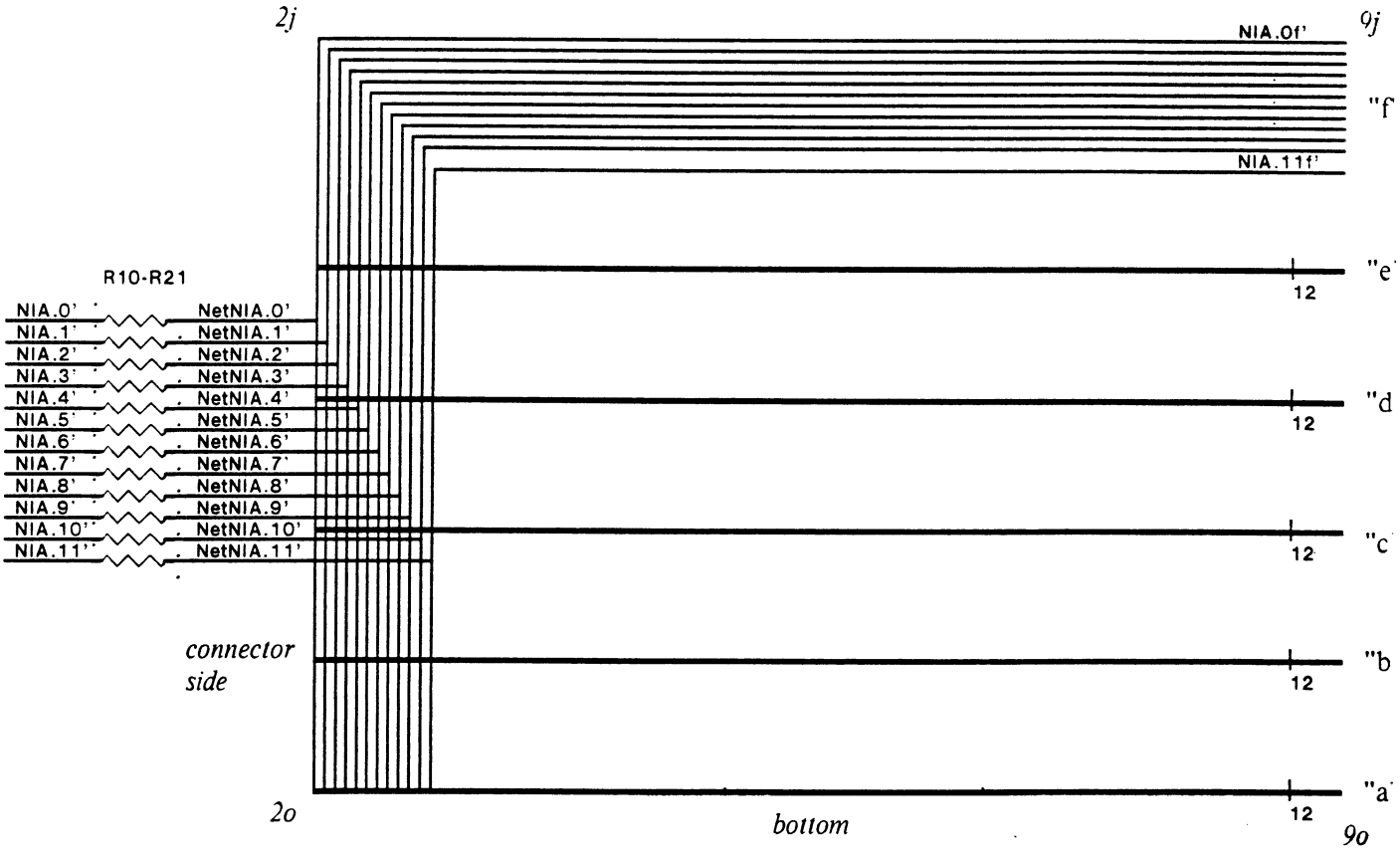
V. Control store layout

The CS is a 6 by 8 array with horizontal address lines & vertical data lines
The 8085 reads the CS from the bottom (via the LS251'), parity is computed at the bottom, and the MIR is located at the top.

Address Lines: Each horizontal row of 8 chips has its 12 address lines connected together- suffixed by "a" through "f" in the diagrams. The 8 rows are interconnected at the left side with a vertical bus, called NetNIA, which driven by the NIA register.

NetNIA is defined by the file NetNIA.sil.

R10-R21 are necessary to prevent undershooting & approximately equal the line impedance divided by 6. Electrolytic bypass caps may be necessary (2nd etch).



Calculated Delay:

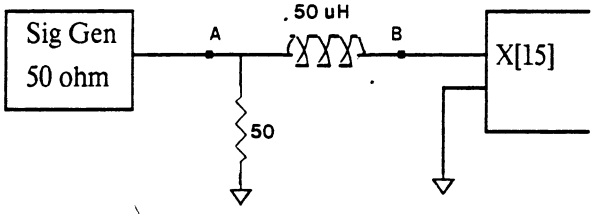
$$V = \frac{1}{C}\int i\,dt = \frac{t}{C}\left(\frac{i_{init} - i_{threshold}}{2} + i_{threshold}\right)$$

For standard Schottky, Fig. E3, p. 6-103 of the TI Data Book shows Iinit=68 mA, Ithreshold=42 mA. On page 49, the X bus capacitance is estimated at 327 pF. Therefore,

X bus delay = t = CV/I = (327 pF)(1.3 V)/(.055 A) = 8 nS

Measured Capacitance & Delay:

Using the following circuit, the capacitance of the X bus has been measured at 337 pF (for 2 PC-Dandelions @25 C)



Adjust frequency so that voltage @B is maximum.
Voltage @A is .4 Vpp centered above 2V.
All bus driver outputs are disabled.

$$C = \frac{1}{4\,(3.14)^2 f^2 L} = \frac{T^2}{1.97 \times 10^{-3}}$$

Using a high-BW scope, the following delays were observed for X[15]:

w/ S240 drivers:	w/ S257 driver:	
7 nS	8 nS	On CP board (between driver and 2901 D input)
10 nS	11 nS	On backplane
16 nS	21 nS	On backplane w/ CP on card extender