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SUBJECT: TCB-3 (128K) Specifications

This memorandum is an updated version of the TCB-3 Specifications dated April 19, 1982. This updated information reflects three major changes:

1) The mechanical specifications for the RS-449/X.21 connector interface board and associated ribbon cable have been finalized.

2) The X.21 protocol dictated a hardware change involving a specific switch setting (SW1) for X.21.

3) The hardware has been modified to allow the X.21 software to detect a "Break" condition more easily.

The TCB-3 Telecommunications Processor is functionally similar to the TCB-1 but contains 128K bytes of memory space as compared to 64K in the TCB-1. This memorandum contains specifications for the memory organization and control only. Refer to Technical Memorandum HM 28 for detailed information concerning the operation of the TCB-1.

There are two differences between the TCB-1 and TCB-3 other than the memory space available.

A) In the TCB-3 three conditions generate a non-maskable interrupt (NMI):

1) Detection of a memory parity error (MPE).
2) Expiration of the "Deadman" Timer (DMT).
3) Detection of an incorrect second opcode in a dual opcode instruction (IPA--illegal PROM address).

A status register is provided to allow software to determine which condition produced the NMI. An IN X'71' reads the status register which is configured as shown below. An OUT X'72' clears the status register.

ERROR	D0	D1	D2
MPE	1	X	X
IPA	X	1	X
DMT	X	X	1

The DMT and IPA are enabled or disabled by I/O commands. Either or both may be prevented from generating an NMI. After a reset condition, both DMT and IPA are disabled. An OUT X'56' with D3 = '1' enables the IPA. An OUT X'56' with D3 = '0' disables the IPA. The IPA Latch is automatically cleared after the NMI is generated. Enabling the DMT remains the same as in the TCB-1.

B) In the TCB-3 a memory parity error does not generate NOP's. This allows the problem to be rectified by debugging.

MEMORY ORGANIZATION (ref: Figure 1)

The TCB-3 memory space is organized similar to that in the OIS 140 CPU and the CIU (Cable Interface Unit). Memory is divided into two 64K sections (HM4864-3 64K RAM's are used) referred to as I-space (instruction space) and D-space (data space).

Normally, I-space stores the software instruction code and D-space stores variables, pointers, tables, stack, etc. This is referred to as I/D-mode. See following explanation.) I-space also contains the master/slave communication area.

MODES OF OPERATION

The actual non-restricted storage area in the TCB-3 is 63K bytes in each memory section for a total of 126K bytes. The lower 1K of D-space is not accessible due to the master/slave communication area residing in I-space at locations 0000-03FF.

The TCB-3 can operate in three software-selectable modes.

1) I-mode: All memory operations access I-space. The TCB-3 defaults to I-mode after any reset.

2) D-mode: All memory operations access D-space.

3) I/D-mode: Both I-space and D-space are utilized. Control circuitry selects the appropriate memory section for each data transfer. (See explanation of Opcode Decode PROM.)

The desired mode is selected via an OUT X'56' command as shown below.

MODE	D0	D1	D2
I/D	1	0	0
I	0	1	0
D	0	0	1

Refresh is maintained in both memory spaces regardless of the operation mode. This allows software to switch between modes without the loss of data due to memory decay.

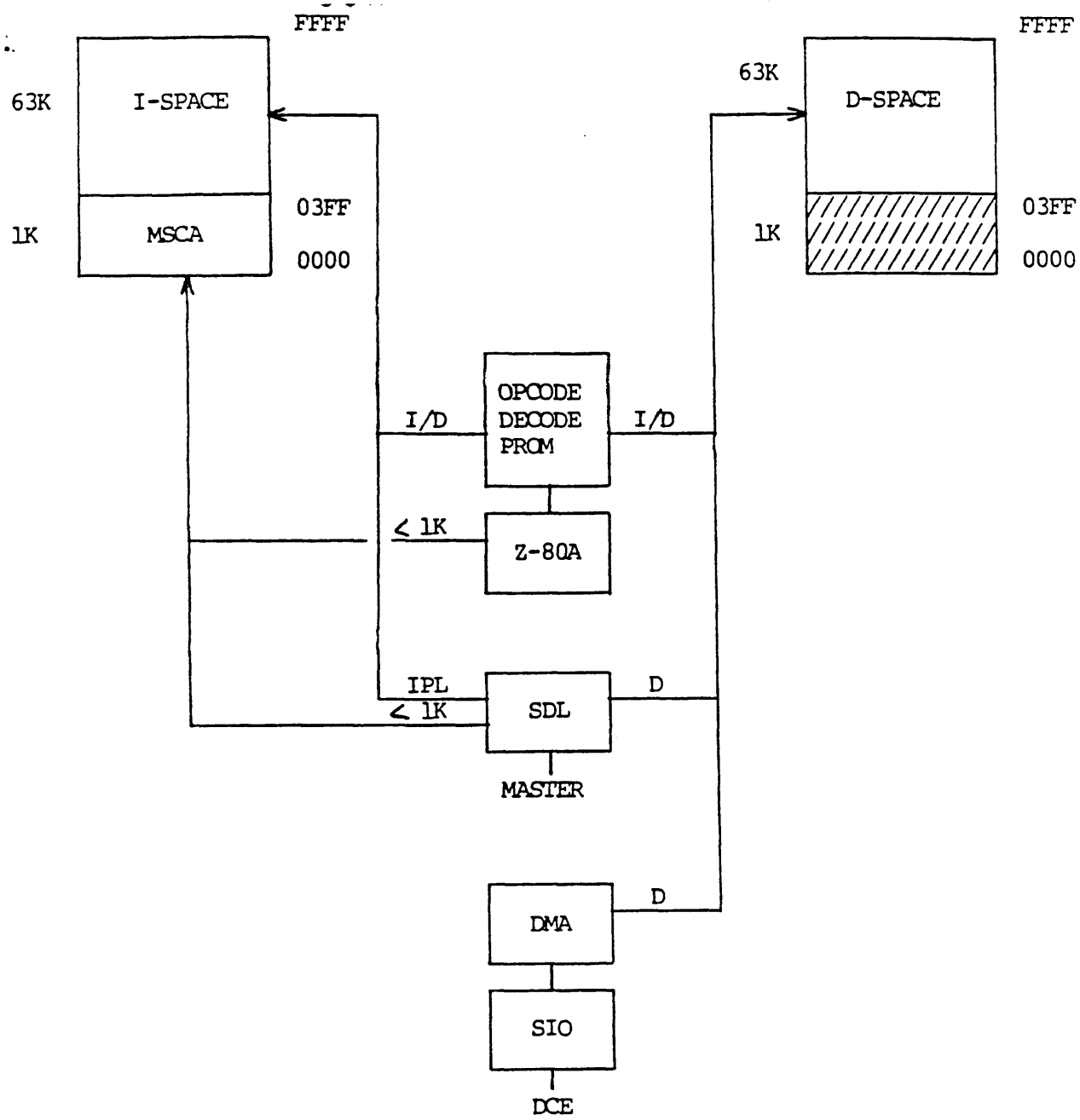

Figure 1 I/D-Mode Memory Organization

DMA TRANSFERS

When in I/D Mode, DMA transfers select D-space.

IPL

After power-on and until the first RESTART command has been received (during IPL time), the hardware traps the memory selection to I-space.

MASTER/SLAVE COMMUNICATION AREA (MSCA)

The MSCA is a software selected 1K block of memory located anywhere in I-space. The TCB-3 hardware monitors the CPU and Slave Data Link address busses, and when an address corresponding to a location in the MSCA is detected, the hardware traps memory selection to I-space. Since any address in the MSCA selects I-space, the 1K block in D-space with MSCA addresses is not accessible.

OPCODE DECODE PROM (ref: Figure 2)

When software selects the I/D-mode of operation for the TCB-3, a 2716 (2K) EPROM and some associated circuitry are responsible for steering data to/from the appropriate memory space. The sequence of events is as follows.

During an opcode fetch (M1 cycle), I-space is selected. The instruction opcode is read out of memory and applied to the inputs of a transparent latch called the Opcode Latch. The data is latched at the end of the M1 MREQ (memory request) and provides an address to page 0 in the decode PROM. At the end of the M1 cycle, the four low order bits of the PROM output code are loaded into a shift register called the Bit Shifter. Each subsequent MREQ shifts the bits out of the register providing a steering mechanism for the memory selection logic. Every time a '0' is shifted out (from QD bar), D-space is enabled, and when a '1' is shifted out, I-space is enabled. The next M1 cycle clears the Bit Shifter, and the sequence repeats.

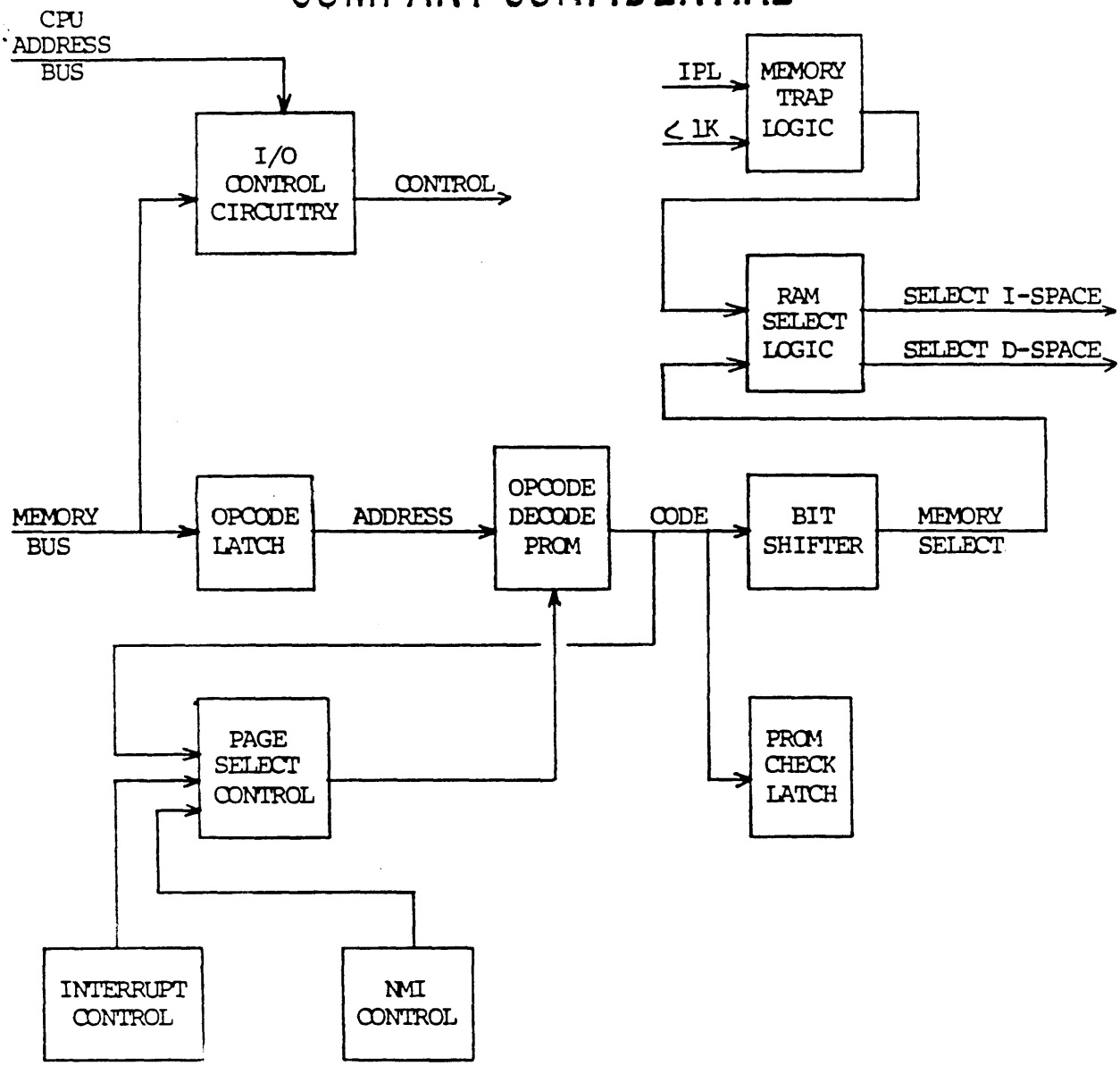

Figure 2 TCB-3 Block Diagram

The codes contained in the decode PROM were derived by examining each Z80 instruction and deciding where the next operation after the opcode fetch cycle is to take place. The entire PROM map with explanation can be found at the end of this memorandum.

If the instruction to be executed requires two opcode fetches, the PROM code addressed by the first opcode is used to change the selected PROM page. The second opcode is fetched and addresses the new PROM page which then outputs the appropriate code to the Bit Shifter.

Not all 256 HEX combinations (00-FF) are valid for the second opcode. If for some reason the second opcode is incorrect (invalid), a special code (HEX '40') is read out of the PROM and generates an illegal PROM address (IPA) NMI.

INTERRUPT HANDLING

The TCB-3 hardware is designed such that, if an interrupt occurs while in I/D-mode, D-space is selected for the duration of the interrupt acknowledge cycle. This is to allow the contents of the program counter to be stored in data memory. During a maskable interrupt (Mode 2), the interrupt service routine address is also read from D-space.

The selection of D-space during an interrupt acknowledge is controlled by the Opcode Decode PROM and the associated circuitry. When a maskable interrupt occurs, the acknowledge (M1 IORQ or INTA) selects page 1 of the decode PROM. All 256 locations of page 1 contain the same code which is read out and loaded/shifted through the Bit Shifter selecting D-space for the remaining memory accesses during the acknowledge cycle. When an NMI occurs, the NMI signal selects page 2 of the decode PROM. The code output from the PROM steers the program counter PUSH to D-space.

X.21 INTERFACE

The TCB-3 utilizes the RS-449 interface to support X.21. An adapter board (w/ribbon cable) has been designed to route the X.21 circuits to/from the appropriate pin on the TCB-3 RS-449 edge connector and the correct pin of the 15-pin "D" connector.

The output structure for the Line Control Register (OUT '40') has been modified as follows.

LINE CONTROL	D0	D1	D2	D3	D4
RX CLK EXT	1	X	X	X	X
RX CLK INT	0	X	X	X	X
TX CLK/EXT	X	1	X	X	X
TX CLK/INT	X	0	X	X	X
NRZ	X	X	1	X	X
NRZI	X	X	0	X	X
RS-449	X	X	X	0	0
RS-232-C	X	X	X	1	0
X.21	X	X	X	0	1

The X.21 protocol requires that a SPACE condition be present on the transmit data line at power on and until the unit is ready to receive. To meet this requirement, switch number seven (7) of switchbank SW1 must be placed in the ON position. (This implies that the device address for a TCB-3 with X.21 is HEX 870.)

When power is applied to the TCB-3, the secondary channel of the SIO is used for diagnostic use (internal loopback). If and when the software selects X.21 mode, the secondary channel of the SIO is available to monitor the primary channel's received data for a "Break" indication.

DIAGNOSTIC CAPABILITY

A PROM Check Latch has been provided to allow partial verification of the Opcode Decode PROM. Before performing a checksum on the decode PROM, I-Mode or D-Mode must be selected to disable the Opcode Latch at M1 MREQ time. Once this has been accomplished an OUT X'54' will provide an address to the decode PROM. The data (D0-D7) output during the command is the address. During the next M1 cycle, the PROM code is clocked into the check latch where it can be read via an IN X'55' command and checked for validity.

The following table is a summary of the I/O commands that have been added to the existing TCB-1 I/O structure to comprise the TCB-3 structure.

ADDRESS	I/O	ACTIVE DATA BIT	FUNCTION
X'52'	OUT	N/A	Clear Memory Parity Error Latch
X'54'	OUT	D0-D7	Set Opcode Decode PROM address (diag. use)
X'55'	IN	D0-D7	Read decode PROM code (diag. use)
X'56'	OUT		Memory control
		D0	Select I/D-mode
		D1	Select I-mode
		D2	Select D-mode
		D3	Enable IPA NMI
X'71'	IN		Read NMI Status Register
		D0	MPE (memory parity error)
		D1	IPA (illegal PROM address)
		D2	DMT ("Deadman" Timer)
X'72'	OUT	N/A	Clear NMI Status Register

The following table contains a map of the Opcode Decode PROM. Included within the table is the instruction opcode, the number of T states, the type of M cycles performed, the number of M cycles, and the expanded memory PROM code.

Listed below are the M cycle codes that are used throughout the opcode map.

IO = Internal CPU operation
MR = Memory read
MRH = Memory read of high byte
MRL = Memory read of low byte
MW = Memory write
MWH = Memory write of high byte
MWL = Memory write of low byte
OCF = Opcode fetch
ODH = Operand data read of high byte
ODL = Operand data read of low byte
PR = Port read
PW = Port write
SRH = Stack read of high byte
SRL = Stack read of low byte
SWH = Stack write of high byte
SWL = Stack write of low byte

The 2716 decode PROM has the following internal structure:

PAGE	CODES FOR
0	Opcodes 00-FF
1	Maskable interrupt (Mode 2)
2	Non-maskable interrupt
3	Unused page
4	X'CB' (dual M1 cycle instructions)
5	X'DD' (dual M1 cycle instructions)
6	X'ED' (dual M1 cycle instructions)
7	X'FD' (dual M1 cycle instructions)

All unused locations contain a X'40' code, which indicates an illegal PROM address.

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
00	NOP	4	OCF	1	00
01	LD BC,nn	10	OCF ODL ODH	3	00
02	LD (BC),A	7	OCF MW	2	08
03	INC BC	6	OCF	1	00
04	INC B	4	OCF	1	00
05	DEC B	4	OCF	1	00
06	LD B,N	7	OCF OD	2	00
07	RLCA	4	OCF	1	00
08	EX AF,AF'	4	OCF	1	00
09	ADD HL,BC	11	OCF IO IO	3	00
0A	LD A,(BC)	7	OCF MR	2	08
0B	DEC BC	6	OCF	1	00
0C	INC C	4	OCF	1	00
0D	DEC C	4	OCF	1	00
0E	LD C,N	7	OCF OD	2	00
0F	RRCA	4	OCF	1	00
10	DJNZ e	13	OCF OD IO	3	00
11	LD DE,NN	10	OCF ODL ODH	3	00
12	LD (DE),A	7	OCF MW	2	08
13	INC DE	6	OCF	1	00
14	INC D	4	OCF	1	00
15	DEC D	4	OCF	1	00
16	LD D,N	7	OCF OD	2	00
17	RLA	4	OCF	1	00
18	JR e	12	OCF OD IO	[illegible]	00
19	ADD HL,DE	11	OCF IO IO	[illegible]	00
1A	LD A,(DE)	7	OCF MR	2	08
1B	DEC DE	6	OCF	1	00
1C	INC E	4	OCF	1	00
1D	DEC E	4	OCF	1	00
1E	LD E,N	7	OCF OD	2	00
1F	RRA	4	OCF	1	00
20	JR NZ,e	12	OCF OD IO	3	00
21	LD HL,NN	10	OCF ODL ODH	3	00
22	LD(NN),HL	16	OCF ODL ODH MWL MWH	5	03
23	INC HL	6	OCF	1	00
24	INC H	4	OCF	1	00
25	DEC H	4	OCF	1	00
26	LD H,N	7	OCF OD	2	00
27	DAA	4	OCF	1	00
28	JR Z,e	12	OCF OD IO	3	00
29	ADD HL,HL	11	OCF IO IO	3	00
2A	LD HL,(NN)	16	OCF ODL ODH MRL MRH	5	03
2B	DEC HL	6	OCF	1	00
2C	INC L	4	OCF	1	00
2D	DEC L	4	OCF	1	00
2E	LD L,N	7	OCF OD	2	00
2F	CPL	4	OCF	1	00
30	JR NC,e	12	OCF OD IO	3	00
31	LD SP,NN	10	OCF ODL ODH	3	00
32	LD (NN),A	13	OCF ODL ODH MW	4	02
33	INC SP	6	OCF	1	00
34	INC (HL)	11	OCF MR MW	3	0C

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
35	DEC (HL)	11	OCF MR MW	3	0C
36	LD (HL),N	10	OCF OD IO	3	04
37	SCF	4	OCF	1	00
38	JR C,e	12	OCF OD IO	3	00
39	ADD HL,SP	11	OCF IO IO	3	00
3A	LD A,(NN)	13	OCF ODL ODH MR	4	02
3B	DEC SP	6	OCF	1	00
3C	INC A	4	OCF	1	00
3D	DEC A	4	OCF	1	00
3E	LD A,N	7	OCF OD	2	00
3F	CCF	4	OCF	1	00
40	LD B,B	4	OCF	1	00
41	LD B,C	4	OCF	1	00
42	LD B,D	4	OCF	1	00
43	LD B,E	4	OCF	1	00
44	LD,B,H	4	OCF	1	00
45	LD B,L	4	OCF	1	00
46	LD B,(HL)	7	OCF MR	2	08
47	LD B,A	4	OCF	1	00
48	LD C,B	4	OCF	1	00
49	LD C,C	4	OCF	1	00
4A	LD C,D	4	OCF	1	00
4B	LD C,E	4	OCF	1	00
4C	LD C,H	4	OCF	1	00
4D	LD C,L	4	OCF	1	00
4E	LD C,(HL)	7	OCF MR	2	08
4F	LD C,A	4	OCF	1	00
50	LD D,B	4	OCF	1	00
51	LD D,C	4	OCF	1	00
52	LD D,D	4	OCF	1	00
53	LD D,E	4	OCF	1	00
54	LD D,H	4	OCF	1	00
55	LD D,L	4	OCF	1	00
56	LD D,(HL)	7	OCF MR	2	08
57	LD D,A	4	OCF	1	00
58	LD E,B	4	OCF	1	00
59	LD E,C	4	OCF	1	00
5A	LD E,D	4	OCF	1	00
5B	LD E,E	4	OCF	1	00
5C	LD E,H	4	OCF	1	00
5D	LD E,L	4	OCF	1	00
5E	LD E,(HL)	7	OCF MR	2	08
5F	LD E,A	4	OCF	1	00
60	LD H,B	4	OCF	1	00
61	LD H,C	4	OCF	1	00
62	LD H,D	4	OCF	1	00
63	LD H,E	4	OCF	1	00
64	LD H,H	4	OCF	1	00
65	LD H,L	4	OCF	1	00
66	LD H,(HL)	7	OCF MR	2	08
67	LD H,A	4	OCF	1	00
68	LD L,B	4	OCF	1	00
69	LD L,C	4	OCF	1	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
6A	LD L,D	4	OCF	1	00
6B	LD L,E	4	OCF	1	00
6C	LD L,H	4	OCF	1	00
6D	LD L,L	4	OCF	1	00
6E	LD L, (HL)	7	OCF MR	2	08
6F	LD L,A	4	OCF	1	00
70	LD (HL) ,B	7	OCF MW	2	08
71	LD (HL) ,C	7	OCF MW	2	08
72	LD (HL) ,D	7	OCF MW	2	08
73	LD (HL) ,E	7	OCF MW	2	08
74	LD (HL) ,H	7	OCF MW	2	08
75	LD (HL) ,L	7	OCF MW	2	08
76	HALT	4	OCF	1	00
77	LD (HL) ,A	7	OCF MW	2	08
78	LD A,B	4	OCF	1	00
79	LD A,C	4	OCF	1	00
7A	LD A,D	4	OCF	1	00
7B	LD A,E	4	OCF	1	00
7C	LD A,H	4	OCF	1	00
7D	LD A,L	4	OCF	1	00
7E	LD A, (HL)	7	OCF MR	1	08
7F	LD A,A	4	OCF	1	00
80	ADD A,B	4	OCF	1	00
81	ADD A,C	4	OCF	1	00
82	ADD A,D	4	OCF	1	00
83	ADD A,E	4	OCF	1	00
84	ADD A,H	4	OCF	1	00
85	ADD A,L	4	OCF	1	00
86	ADD A, (HL)	7	OCF MR	2	08
87	ADD A,A	4	OCF	1	00
88	ADC A,B	4	OCF	1	00
89	ADC A,C	4	OCF	1	00
8A	ADC A,D	4	OCF	1	00
8B	ADC A,E	4	OCF	1	00
8C	ADC A,H	4	OCF	1	00
8D	ADC A,L	4	OCF	1	00
8E	ADC A, (HL)	7	OCF MR	2	08
8F	ADC A,A	4	OCF	1	00
90	SUB B	4	OCF	1	00
91	SUB C	4	OCF	1	00
92	SUB D	4	OCF	1	00
93	SUB E	4	OCF	1	00
94	SUB H	4	OCF	1	00
95	SUB L	4	OCF	1	00
96	SUB (HL)	7	OCF MR	2	08
97	SUB A	4	OCF	1	00
98	SBC A,B	4	OCF	1	00
99	SBC A,C	4	OCF	1	00
9A	SBC A,D	4	OCF	1	00
9B	SBC A,E	4	OCF	1	00
9C	SBC A,H	4	OCF	1	00
9D	SBC A,L	4	OCF	1	00
9E	SBC A, (HL)	7	OCF MR	2	08

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
9F	SBC A,A	4	OCF	1	00
A0	AND B	4	OCF	1	00
A1	AND C	4	OCF	1	00
A2	AND D	4	OCF	1	00
A3	AND E	4	OCF	1	00
A4	AND H	4	OCF	1	00
A5	AND L	4	OCF	1	00
A6	AND (HL)	7	OCF MR	2	08
A7	AND A	4	OCF	1	00
A8	XOR B	4	OCF	1	00
A9	XOR C	4	OCF	1	00
AA	XOR D	4	OCF	1	00
AB	XOR E	4	OCF	1	00
AC	XOR H	4	OCF	1	00
AD	XOR L	4	OCF	1	00
AE	XOR (HL)	7	OCF MR	2	08
AF	XOR A	4	OCF	1	00
B0	OR B	4	OCF	1	00
B1	OR C	4	OCF	1	00
B2	OR D	4	OCF	1	00
B3	OR E	4	OCF	1	00
B4	OR H	4	OCF	1	00
B5	OR L	4	OCF	1	00
B6	OR (HL)	7	OCF MR	2	08
B7	OR A	4	OCF	1	00
B8	CP B	4	OCF	1	00
B9	CP C	4	OCF	1	00
BA	CP D	4	OCF	1	00
BB	CP E	4	OCF	1	00
BC	CP H	4	OCF	1	00
BD	CP L	4	OCF	1	00
BE	CP (HL)	7	OCF MR	2	08
BF	CP A	4	OCF	1	00
C0	RET NZ	11	OCF SRL SRH	3	0C
C1	POP BC	10	OCF SRL SRH	3	0C
C2	JP NZ,NN	10	OCF ODL ODH	3	00
C3	JP NN	10	OCF ODL ODH	3	00
C4	CALL NZ,NN	17	OCF ODL ODH SWH SWL	5	03
C5	PUSH BC	11	OCF SWH SWL	3	0C
C6	ADD A,N	7	OCF OD	2	00
C7	RST 0	11	OCF SWH SWL	3	0C
C8	RET Z	11	OCF SRL SRH	3	0C
C9	RET	10	OCF SRL SRH	3	0C
CA	JP Z,NN	10	OCF ODL ODH	3	00
*CB			*Addr 'CB' is in pg 4		*80
CC	CALL Z,NN	17	OCF ODL ODH SWH SWL	5	03
CD	CALL NN	11	OCF ODL ODH SWH SWL	5	03
CE	ADC A,N	7	OCF OD	2	00
CF	RST 8	11	OCF SWH SWL	3	0C
D0	RET NC	11	OCF SRL SRH	3	0C
D1	POP DE	10	OCF SRL SRH	3	0C

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
D2	JP NC,NN	10	OCF ODL ODH	3	00
D3	OUT N,A	11	OCF OD PW	3	00
D4	CALL NC,NN	17	OCF ODL ODH SWH SWL	5	03
D5	PUSH DE	11	OCF SWH SWL	3	0C
D6	SUB N	7	OCF MR	2	00
D7	RST 10h	11	OCF SWH SWL	3	0C
D8	RET C	10	OCF SRL SRH	3	0C
D9	EXX	4	OCF	1	00
DA	JP C,NN	10	OCF ODL ODH	3	00
DB	IN A,N	11	OCF OD PR	3	00
DC	CALL C,NN	17	OCF ODL ODH SWH SWL	5	03
*DD			*Addr 'DD' is in pg 5		*90
DE	SBC A,N	7	OCF OD	2	00
DF	RST 18h	11	OCF SWH SWL	3	0C
E0	RET PO	10	OCF SRL SRH	3	0C
E1	POP HL	10	OCF SRL SRH	3	0C
E2	JP PO,NN	10	OCF ODL ODH	3	00
E3	EX (SP),HL	19	OCF SRL SRH SWH SWL	5	0F
E4	CALL PO,NN	17	OCF ODL ODH SWH SWL	5	03
E5	PUSH HL	11	OCF SWH SWL	3	0C
E6	AND N	7	OCF MR	2	00
E7	RST 20h	11	OCF SWH SWL	3	0C
E8	RET PE	10	OCF SRL SRH	3	0C
E9	JP (HL)	4	OCF	1	00
EA	JP PE,NN	10	OCF ODL ODH	3	00
EB	EX DE,HL	4	OCF	1	00
EC	CALL PE,NN	17	OCF ODL ODH SWH SWL	5	03
*ED			*Addr 'ED' is in pg 6		*A0
EE	XOR N	7	OCF MR	2	00
EF	RST 28h	11	OCF SWH SWL	3	0C
F0	RET P	10	OCF SRL SRH	3	0C
F1	POP AF	10	OCF SRL SRH	3	0C
F2	JP P,NN	10	OCF ODL ODH	3	00
F3	DI	4	OCF	1	00
F4	CALL P,NN	17	OCF ODL ODH SWH SWL	5	03
F5	PUSH AF	11	OCF SWH SWL	3	0C
F6	OR N	7	OCF MR	2	00
F7	RST 30h	11	OCF SWH SWL	3	0C
F8	RET M	10	OCF SRL SRH	3	0C
F9	LD SP,HL	6	OCF	1	00
FA	JP M,NN	10	OCF ODL ODH	3	00
FB	EI	4	OCF	1	00
FC	CALL M,NN	17	OCF ODL ODH SWH SWL	5	03
*FD			*Addr 'FD' is in pg 7		*B0
FE	CP N	7	OCF MR	2	00
FF	RST 38h	11	OCF SWH SWL	3	0C

Page 1 contains 256 bytes of X'0F' (Mode 2 interrupt response)

Page 2 contains 256 bytes of X'0C' (non-maskable interrupt response)

Page 3 contains 256 bytes of X'40' (unused locations)

Page 4 contains codes for all X'CB' addresses (dual M1 cycle) as follows:

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
CB00	RLC B	8	OCF OCF	1	00
CB01	RLC C	8	OCF OCF	1	00
CB02	RLC D	8	OCF OCF	1	00
CB03	RLC E	8	OCF OCF	1	00
CB04	RLC H	8	OCF OCF	1	00
CB05	RLC L	8	OCF OCF	1	00
CB06	RLC (HL)	15	OCF OCF MR MW	3	0C
CB07	RLC A	8	OCF OCF	1	00
CB08	RRC B	8	OCF OCF	1	00
CB09	RRC C	8	OCF OCF	1	00
CB0A	RRC D	8	OCF OCF	1	00
CB0B	RRC E	8	OCF OCF	1	00
CB0C	RRC H	8	OCF OCF	1	00
CB0D	RRC L	8	OCF OCF	1	00
CB0E	RRC (HL)	15	OCF OCF MR MW	3	0C
CB0F	RRC A	8	OCF OCF	1	00
CB10	RL B	8	OCF OCF	1	00
CB11	RL C	8	OCF OCF	1	00
CB12	RL D	8	OCF OCF	1	00
CB13	RL E	8	OCF OCF	1	00
CB14	RL H	8	OCF OCF	1	00
CB15	RL L	8	OCF OCF	1	00
CB16	RL (HL)	15	OCF OCF MR MW	3	0C
CB17	RL A	8	OCF OCF	1	00
CB18	RR B	8	OCF OCF	1	00
CB19	RR C	8	OCF OCF	1	00
CB1A	RR D	8	OCF OCF	1	00
CB1B	RR E	8	OCF OCF	1	00
CB1C	RR H	8	OCF OCF	1	00
CB1D	RR L	8	OCF OCF	1	00
CB1E	RR (HL)	15	OCF OCF MR MW	3	0C
CB1F	RR A	8	OCF OCF	1	00
CB20	SLA B	8	OCF OCF	1	00
CB21	SLA C	8	OCF OCF	1	00
CB22	SLA D	8	OCF OCF	1	00
CB23	SLA E	8	OCF OCF	1	00
CB24	SLA H	8	OCF OCF	1	00
CB25	SLA L	8	OCF OCF	1	00
CB26	SLA (HL)	15	OCF OCF MR MW	3	0C
CB27	SLA A	8	OCF OCF	1	00
CB28	SRA B	8	OCF OCF	1	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
CB29	SRA C	8	OCF OCF	1	00
CB2A	SRA D	8	OCF OCF	1	00
CB2B	SRA E	8	OCF OCF	1	00
CB2C	SRA H	8	OCF OCF	1	00
CB2D	SRA L	8	OCF OCF	1	00
CB2E	SRA (HL)	15	OCF OCF MR MW	3	0C
CB2F	SRA A	8	OCF OCF	1	00
CB38	SRL B	8	OCF OCF	1	00
CB39	SRL C	8	OCF OCF	1	00
CB3A	SRL D	8	OCF OCF	1	00
CB3B	SRL E	8	OCF OCF	1	00
CB3C	SRL H	8	OCF OCF	1	00
CB3D	SRL L	8	OCF OCF	1	00
CB3E	SRL (HL)	15	OCF OCF MR MW	3	0C
CB3F	SRL A	8	OCF OCF	1	00
CB40	BIT 0,B	8	OCF OCF	1	00
CB41	BIT 0,C	8	OCF OCF	1	00
CB42	BIT 0,D	8	OCF OCF	1	00
CB43	BIT 0,E	8	OCF OCF	1	00
CB44	BIT 0,H	8	OCF OCF	1	00
CB45	BIT 0,L	8	OCF OCF	1	00
CB46	BIT 0,(HL)	15	OCF OCF MR	3	08
CB47	BIT 0,A	8	OCF OCF	1	00
CB48	BIT 1,B	8	OCF OCF	1	00
CB49	BIT 1,C	8	OCF OCF	1	00
CB4A	BIT 1,D	8	OCF OCF	1	00
CB4B	BIT 1,E	8	OCF OCF	1	00
CB4C	BIT 1,H	8	OCF OCF	1	00
CB4D	BIT 1,L	8	OCF OCF	1	00
CB4E	BIT 1,(HL)	15	OCF OCF MR	3	08
CB4F	BIT 1,A	8	OCF OCF	1	00
CB50	BIT 2,B	8	OCF OCF	1	00
CB51	BIT 2,C	8	OCF OCF	1	00
CB52	BIT 2,D	8	OCF OCF	1	00
CB53	BIT 2,E	8	OCF OCF	1	00
CB54	BIT 2,H	8	OCF OCF	1	00
CB55	BIT 2,L	8	OCF OCF	1	00
CB56	BIT 2,(HL)	15	OCF OCF MR	3	08
CB57	BIT 2,A	8	OCF OCF	1	00
CB58	BIT 3,B	8	OCF OCF	1	00
CB59	BIT 3,C	8	OCF OCF	1	00
CB5A	BIT 3,D	8	OCF OCF	1	00
CB5B	BIT 3,E	8	OCF OCF	1	00
CB5C	BIT 3,H	8	OCF OCF	1	00
CB5D	BIT 3,L	8	OCF OCF	1	00
CB5E	BIT 3,(HL)	15	OCF OCF MR	3	08
CB5F	BIT 3,A	8	OCF OCF	1	00
CB60	BIT 4,B	8	OCF OCF	1	00
CB61	BIT 4,C	8	OCF OCF	1	00
CB62	BIT 4,D	8	OCF OCF	1	00
CB63	BIT 4,E	8	OCF OCF	1	00
CB64	BIT 4,H	8	OCF OCF	1	00
CB65	BIT 4,L	8	OCF OCF	1	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
CB66	BIT 4,(HL)	15	OCF OCF MR	3	08
CB67	BIT 4,A	8	OCF OCF	1	00
CB68	BIT 5,B	8	OCF OCF	1	00
CB69	BIT 5,C	8	OCF OCF	1	00
CB6A	BIT 5,D	8	OCF OCF	1	00
CB6B	BIT 5,E	8	OCF OCF	1	00
CB6C	BIT 5,H	8	OCF OCF	1	00
CB6D	BIT 5,L	8	OCF OCF	1	00
CB6E	BIT 5,(HL)	15	OCF OCF MR	3	08
CB6F	BIT 5,A	8	OCF OCF	1	00
CB70	BIT 6,B	8	OCF OCF	1	00
CB71	BIT 6,C	8	OCF OCF	1	00
CB72	BIT 6,D	8	OCF OCF	1	00
CB73	BIT 6,E	8	OCF OCF	1	00
CB74	BIT 6,H	8	OCF OCF	1	00
CB75	BIT 6,L	8	OCF OCF	1	00
CB76	BIT 6,(HL)	8	OCF OCF MR	3	08
CB77	BIT 6,A	8	OCF OCF	1	00
CB78	BIT 7,B	8	OCF OCF	1	00
CB79	BIT 7,C	8	OCF OCF	1	00
CB7A	BIT 7,D	8	OCF OCF	1	00
CB7B	BIT 7,E	8	OCF OCF	1	00
CB7C	BIT 7,H	8	OCF OCF	1	00
CB7D	BIT 7,L	8	OCF OCF	1	00
CB7E	BIT 7,(HL)	15	OCF OCF MR	3	08
CB7F	BIT 7,A	8	OCF OCF	1	00
CB80	RES 0,B	8	OCF OCF	1	00
CB81	RES 0,C	8	OCF OCF	1	00
CB82	RES 0,D	8	OCF OCF	1	00
CB83	RES 0,E	8	OCF OCF	1	00
CB84	RES 0,H	8	OCF OCF	1	00
CB85	RES 0,L	8	OCF OCF	1	00
CB86	RES 0,(HL)	15	OCF OCF MR MW	3	0C
CB87	RES 0,A	8	OCF OCF	1	00
CB88	RES 1,B	8	OCF OCF	1	00
CB89	RES 1,C	8	OCF OCF	1	00
CB8A	RES 1,D	8	OCF OCF	1	00
CB8B	RES 1,E	8	OCF OCF	1	00
CB8C	RES 1,H	8	OCF OCF	1	00
CB8D	RES 1,L	8	OCF OCF	1	00
CB8E	RES 1,(HL)	15	OCF OCF MR MW	1	0C
CB8F	RES 1,A	8	OCF OCF	1	00
CB90	RES 2,B	8	OCF OCF	1	00
CB91	RES 2,C	8	OCF OCF	1	00
CB92	RES 2,D	8	OCF OCF	1	00
CB93	RES 2,E	8	OCF OCF	1	00
CB94	RES 2,H	8	OCF OCF	1	00
CB95	RES 2,L	8	OCF OCF	1	00
CB96	RES 2,(HL)	15	OCF OCF MR MW	3	0C
CB97	RES 2,A	8	OCF OCF	1	00
CB98	RES 3,B	8	OCF OCF	1	00
CB99	RES 3,C	8	OCF OCF	1	00
CB9A	RES 3,D	8	OCF OCF	1	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
CB9B	RES 3,E	8	OCF OCF	1	00
CB9C	RES 3,H	8	OCF OCF	1	00
CB9D	RES 3,L	8	OCF OCF	1	00
CB9E	RES 3,(HL)	15	OCF OCF MR MW	3	0C
CB9F	RES 3,A	8	OCF OCF	1	00
CBA0	RES 4,B	8	OCF OCF	1	00
CBA1	RES 4,C	8	OCF OCF	1	00
CBA2	RES 4,D	8	OCF OCF	1	00
CBA3	RES 4,E	8	OCF OCF	1	00
CBA4	RES 4,H	8	OCF OCF	1	00
CBA5	RES 4,L	8	OCF OCF	1	00
CBA6	RES 4,(HL)	15	OCF OCF MR MW	3	0C
CBA7	RES 4,A	8	OCF OCF	1	00
CBA8	RES 5,B	8	OCF OCF	1	00
CBA9	RES 5,C	8	OCF OCF	1	00
CBAA	RES 5,D	8	OCF OCF	1	00
CBAB	RES 5,E	8	OCF OCF	1	00
CBAC	RES 5,H	8	OCF OCF	1	00
CBAD	RES 5,L	8	OCF OCF	1	00
CBAE	RES 5,(HL)	15	OCF OCF MR MW	3	0C
CBAF	RES 5,A	8	OCF OCF	1	00
CBB0	RES 6,B	8	OCF OCF	1	00
CBB1	RES 6,C	8	OCF OCF	1	00
CBB2	RES 6,D	8	OCF OCF	1	00
CBB3	RES 6,E	8	OCF OCF	1	00
CBB4	RES 6,H	8	OCF OCF	1	00
CBB5	RES 6,L	8	OCF OCF	1	00
CBB6	RES 6,(HL)	15	OCF OCF MR MW	3	0C
CBB7	RES 6,A	8	OCF OCF	1	00
CBB8	RES 7,B	8	OCF OCF	1	00
CBB9	RES 7,C	8	OCF OCF	1	00
CBBA	RES 7,D	8	OCF OCF	1	00
CBBB	RES 7,E	8	OCF OCF	1	00
CBBC	RES 7,H	8	OCF OCF	1	00
CBBD	RES 7,L	8	OCF OCF	1	00
CBBE	RES 7,(HL)	15	OCF OCF MR MW	3	0C
CBBF	RES 7,A	8	OCF OCF	1	00
CBC0	SET 0,B	8	OCF OCF	1	00
CBC1	SET 0,C	8	OCF OCF	1	00
CBC2	SET 0,D	8	OCF OCF	1	00
CBC3	SET 0,E	8	OCF OCF	1	00
CBC4	SET 0,H	8	OCF OCF	1	00
CBC5	SET 0,L	8	OCF OCF	1	00
CBC6	SET 0,(HL)	15	OCF OCF MR MW	3	0C
CBC7	SET 0,A	8	OCF OCF	1	00
CBC8	SET 1,B	8	OCF OCF	1	00
CBC9	SET 1,C	8	OCF OCF	1	00
CBCA	SET 1,D	8	OCF OCF	1	00
CBCB	SET 1,E	8	OCF OCF	1	00
CBCC	SET 1,H	8	OCF OCF	1	00
CBCD	SET 1,L	8	OCF OCF	1	00
CBCE	SET 1,(HL)	15	OCF OCF MR MW	3	0C
CBCF	SET 1,A	8	OCF OCF	1	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
CBD0	SET 2,B	8	OCF OCF	1	00
CBD1	SET 2,C	8	OCF OCF	1	00
CBD2	SET 2,D	8	OCF OCF	1	00
CBD3	SET 2,E	8	OCF OCF	1	00
CBD4	SET 2,H	8	OCF OCF	1	00
CBD5	SET 2,L	8	OCF OCF	1	00
CBD6	SET 2,(HL)	15	OCF OCF MR MW	3	0C
CBD7	SET 2,A	8	OCF OCF	1	00
CBD8	SET 3,B	8	OCF OCF	1	00
CBD9	SET 3,C	8	OCF OCF	1	00
CBDA	SET 3,D	8	OCF OCF	1	00
CBDB	SET 3,E	8	OCF OCF	1	00
CBDC	SET 3,H	8	OCF OCF	1	00
CBDD	SET 3,L	8	OCF OCF	1	00
CBDE	SET 3,(HL)	15	OCF OCF MR MW	3	0C
CBDF	SET 3,A	8	OCF OCF	1	00
CBE0	SET 4,B	8	OCF OCF	1	00
CBE1	SET 4,C	8	OCF OCF	1	00
CBE2	SET 4,D	8	OCF OCF	1	00
CBE3	SET 4,E	8	OCF OCF	1	00
CBE4	SET 4,H	8	OCF OCF	1	00
CBE5	SET 4,L	8	OCF OCF	1	00
CBE6	SET 4,(HL)	15	OCF OCF MR MW	3	0C
CBE7	SET 4,A	8	OCF OCF	1	00
CBE8	SET 5,B	8	OCF OCF	1	00
CBE9	SET 5,C	8	OCF OCF	1	00
CBEA	SET 5,D	8	OCF OCF	1	00
CBEB	SET 5,E	8	OCF OCF	1	00
CBEC	SET 5,H	8	OCF OCF	1	00
CBED	SET 5,L	8	OCF OCF	1	00
CBEE	SET 5,(HL)	15	OCF OCF MR MW	3	0C
CBEF	SET 5,A	8	OCF OCF	1	00
CBF0	SET 6,B	8	OCF OCF	1	00
CBF1	SET 6,C	8	OCF OCF	1	00
CBF2	SET 6,D	8	OCF OCF	1	00
CBF3	SET 6,E	8	OCF OCF	1	00
CBF4	SET 6,H	8	OCF OCF	1	00
CBF5	SET 6,L	8	OCF OCF	1	00
CBF6	SET 6,(HL)	15	OCF OCF MR MW	3	0C
CBF7	SET 6,A	8	OCF OCF	1	00
CBF8	SET 7,B	8	OCF OCF	1	00
CBF9	SET 7,C	8	OCF OCF	1	00
CBFA	SET 7,D	8	OCF OCF	1	00
CBFB	SET 7,E	8	OCF OCF	1	00
CBFC	SET 7,H	8	OCF OCF	1	00
CBFD	SET 7,L	8	OCF OCF	1	00
CBFE	SET 7,(HL)	15	OCF OCF MR MW	3	0C
CBFF	SET 7,A	8	OCF OCF	1	00

Page 5 contains codes for all X'DD' addresses (dual M1 cycle) as follows:

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
DD09	ADD IX,BC	15	OCF OCF IO IO	3	00
DD19	ADD IX,DE	15	OCF OCF IO IO	3	00
DD21	LD IX,NN	20	OCF OCF ODL ODH MRL MRH	5	00
DD22	LD (NN),IX	20	OCF OCF ODL ODH MRL MRH	5	03
DD23	INC IX	10	OCF OCF	1	00
DD29	ADD IX,IX	15	OCF OCF IO IO	3	00
DD2A	LD IX,(NN)	20	OCF OCF ODL ODH MRL MRH	5	03
DD2B	DEC IX	10	OCF OCF	1	00
DD34	INC (IX+IND)	23	OCF OCF OD IO MR MW	5	06
DD35	DEC (IX+IND)	23	OCF OCF OD IO MR MW	5	06
DD36	LD (IX+IND),N	19	OCF OCF OD IO MW	4	03
DD39	ADD IX,SP	15	OCF OCF IO IO	3	00
DD46	LD B,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD4E	LD C,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD56	LD D,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD5E	LD E,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD66	LD H,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD6E	LD L,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD70	LD (IX+IND),B	19	OCF OCF OD IO MW	4	04
DD71	LD (IX+IND),C	19	OCF OCF OD IO MW	4	04
DD72	LD (IX+IND),D	19	OCF OCF OD IO MW	4	04
DD73	LD (IX+IND),E	19	OCF OCF OD IO MW	4	04
DD74	LD (IX+IND),H	19	OCF OCF OD IO MW	4	04
DD75	LD (IX+IND),L	19	OCF OCF OD IO MW	4	04
DD77	LD (IX+IND),A	19	OCF OCF OD IO MW	4	04
DD7E	LD A,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD86	ADD A,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD8E	ADC A,(IX+IND)	19	OCF OCF OD IO MR	4	04
DD96	SUB (IX+IND)	19	OCF OCF OD IO MR	4	04
DD9E	SBC A,(IX+IND)	19	OCF OCF OD IO MR	4	04
DDA6	AND (IX+IND)	19	OCF OCF OD IO MR	4	04
DDAE	XOR (IX+IND)	19	OCF OCF OD IO MR	4	04
DDB6	OR (IX+IND)	19	OCF OCF OD IO MR	4	04
DDBE	CP (IX+IND)	19	OCF OCF OD IO MR	4	04
DDE1	POP IX	14	OCF OCF SRH SRL	3	0C
DDE3	EX (SP),IX	22	OCF OCF SRL SRH SWH SWL	5	0F
DDE5	PUSH IX	15	OCF OCF SWH SWL	3	0C
DDE9	JP (IX)	8	OCF OCF	1	00
DDF9	LD SP,IX	10	OCF OCF	1	00

The following opcodes have the prefix X'DDCB'

XX06	RLC (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX0E	RRC (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX16	RL (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX1E	RR (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX26	SLA (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX2E	SRA (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX3E	SRL (IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX46	BIT 0,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX4E	BIT 1,(IX+IND)	20	OCF OCF OD IO MR	4	03

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
XX56	BIT 2,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX5E	BIT 3,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX66	BIT 4,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX6E	BIT 5,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX76	BIT 6,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX7E	BIT 7,(IX+IND)	20	OCF OCF OD IO MR	4	03
XX86	RES 0,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX8E	RES 1,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX96	RES 2,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XX9E	RES 3,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXA6	RES 4,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXAE	RES 5,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXB6	RES 6,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXBE	RES 7,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXC6	SET 0,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXCE	SET 1,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXD6	SET 2,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXDE	SET 3,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXE6	SET 4,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXEE	SET 5,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXF6	SET 6,(IX+IND)	23	OCF OCF OD IO MR MW	5	03
XXFE	SET 7,(IX+IND)	23	OCF OCF OD IO MR MW	5	03

Page 6 contains codes for all X'ED' addresses (dual M1 cycle) as follows:

ED40	IN B,(C)	12	OCF OCF PR	2	00
ED41	OUT (C),B	12	OCF OCF PW	2	00
ED42	SBC HL,BC	15	OCF OCF IO IO	3	00
ED43	LD (NN),BC	20	OCF OCF ODL ODH MWL MWH	5	03
ED44	NEG	8	OCF OCF	1	00
ED45	RETN	14	OCF OCF SRL SRH	3	0C
ED46	IM 0	8	OCF OCF	1	00
ED47	LD I,A	9	OCF OCF	1	00
ED48	IN C,(C)	12	OCF OCF PR	2	00
ED49	OUT (C),C	12	OCF OCF PW	2	00
ED4A	ADC HL,BC	15	OCF OCF IO IO	3	00
ED4B	LD BC,(NN)	20	OCF OCF ODL ODH MRL MRH	5	03
ED4D	RETI	14	OCF OCF SRL SRH	3	0C
ED4F	LD R,A	9	OCF OCF	1	00
ED50	IN D,(C)	12	OCF OCF PR	2	00
ED51	OUT (C),D	12	OCF OCF PW	2	00
ED52	SBC HL,DE	15	OCF OCF IO IO	3	00
ED53	LD (NN),DE	20	OCF OCF ODL ODH MWL MWH	5	03
ED56	IM 1	8	OCF OCF	1	00
ED57	LD A,I	9	OCF OCF	1	00
ED58	IN E,(C)	12	OCF OCF PR	2	00
ED59	OUT (C),E	12	OCF OCF PW	2	00
ED5A	ADC HL,DE	15	OCF OCF IO IO	3	00
ED5B	LD DE,(NN)	20	OCF OCF ODL ODH MRL MRH	5	03
ED5E	IM 2	8	OCF OCF	1	00
ED5F	LD A,R	9	OCF OCF	1	00
ED60	IN H,(C)	12	OCF OCF PR	2	00
ED61	OUT (C),H	12	OCF OCF PW	2	00

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
ED62	SBC HL,HL	15	OCF OCF IO IO	3	00
ED67	RRD	18	OCF OCF MR IO MW	4	0C
ED68	IN L,(C)	12	OCF OCF PR	2	00
ED69	OUT (C),L	12	OCF OCF PW	2	00
ED6A	ADC HL,HL	15	OCF OCF IO IO	3	00
ED6F	RLD	18	OCF OCF MR IO MW	4	0C
ED72	SBC HL,SP	15	OCF OCF IO IO	3	00
ED73	LD (NN),SP	20	OCF OCF ODL ODH MWL MWH	5	03
ED78	IN A,(C)	12	OCF OCF PR	2	00
ED79	OUT (C),A	12	OCF OCF PW	2	00
ED7A	ADC HL,SP	15	OCF OCF IO IO	3	00
ED7B	LD SP,(NN)	20	OCF OCF ODL ODH	3	03
EDA0	LDI	16	OCF OCF MR MW	3	08
EDA1	CPI	16	OCF OCF MR MW	3	08
EDA2	INI	16	OCF OCF PR MW	3	04
EDA3	OUTI	16	OCF OCF MR PW	3	08
EDA8	LDD	16	OCF OCF MR MW	3	08
EDA9	CPD	16	OCF OCF MR MW	3	08
EDAA	IND	16	OCF OCF PR MW	3	04
EDAB	OUTD	16	OCF OCF MR PW	3	08
EDB0	LDIR	21	OCF OCF MR MW IO	4	0C
EDB1	CPIR	21	OCF OCF MR MW IO	4	08
EDB2	INIR	21	OCF OCF PR MW IO	4	04
EDB3	OTIR	21	OCF OCF MR PW IO	4	08
EDB8	LDDR	21	OCF OCF MR MW IO	4	0C
EDB9	CPDR	21	OCF OCR MR MW IO	4	08
EDBA	INDR	21	OCF OCF PR MW IO	4	04
EDBB	OTDR	21	OCF OCF MR PW IO	4	08

Page 7 contains codes for all X'FD' addresses (dual M1 cycle) as follows:

FD09	ADD IY,BC	15	OCF OCF IO IO	3	00
FD19	ADD IY,DE	15	OCF OCF IO IO	3	00
FD21	LD IY,NN	14	OCF OCF ODL ODH	3	00
FD22	LD (NN),IY	20	OCF OCF ODL ODH MWL MWH	5	03
FD23	INC IY	8	OCF OCF	1	00
FD29	ADD IY,IY	15	OCF OCF IO IO	3	00
FD2A	LD IY,(NN)	20	OCF OCF ODL ODH MRL MRH	5	03
FD2B	DEC IY	8	OCF OCF	1	00
FD34	INC (IY+IND)	23	OCF OCF OD IO MR MW	5	06
FD35	DEC (IY+IND)	23	OCF OCF OD IO MR MW	5	06
FD36	LD (IY+IND),N	19	OCF OCF OD IO MW	4	03
FD39	ADD IY,SP	15	OCF OCF IO IO	3	00
FD46	LD B,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD4E	LD C,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD56	LD D,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD5E	LD E,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD66	LD H,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD6E	LD L,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD70	LD (IY+IND),B	19	OCF OCF OD IO MW	4	04
FD71	LD (IY+IND),C	19	OCF OCF OD IO MW	4	04
FD72	LD (IY+IND),D	19	OCF OCF OD IO MW	4	04
FD73	LD (IY+IND),E	19	OCF OCF OD IO MW	4	04

OPCODE	INSTRUCTION	T STATES	TYPE OF M CYCLE	M CYCLES	CODE
FD74	LD (IY+IND),H	19	OCF OCF OD IO MW	4	04
FD75	LD (IY+IND),L	19	OCF OCF OD IO MW	4	04
FD77	LD (IY+IND),A	19	OCF OCF OD IO MW	4	04
FD7E	LD A,(IY+IND)	19	OCF OCF OD IO MW	4	04
FD86	ADD A,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD8E	ADC A,(IY+IND)	19	OCF OCF OD IO MR	4	04
FD96	SUB (IY+IND)	19	OCF OCF OD IO MR	4	04
FD9E	SBC A,(IY+IND)	19	OCF OCF OD IO MR	4	04
FDA6	AND (IY+IND)	19	OCF OCF OD IO MR	4	04
FDAE	XOR (IY+IND)	19	OCF OCF OD IO MR	4	04
FDB6	OR (IY+IND)	19	OCF OCF OD IO MR	4	04
FDBE	CP (IY+IND)	19	OCF OCF OD IO MR	4	04
FDE1	POP IY	14	OCF OCF SRH SRL	3	0C
FDE3	EX (SP),IY	22	OCF OCF SRL SRH SWH SWL	5	0F
FDE5	PUSH IY	15	OCF OCF SWH SWL	3	0C
FDE9	JP (IY)	8	OCF OCF	1	00
FDF9	LD SP,IY	10	OCF OCF	1	00

The following opcodes have the prefix X'FDCB'

XX06	RLC (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX0E	RRC (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX16	RL (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX1E	RR (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX26	SLA (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX2E	SRA (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX3E	SRL (IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX46	BIT 0,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX4E	BIT 1,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX56	BIT 2,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX5E	BIT 3,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX66	BIT 4,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX6E	BIT 5,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX76	BIT 6,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX7E	BIT 7,(IY+IND)	20	OCF OCF OD IO MR	4	03
XX86	RES 0,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX8E	RES 1,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX96	RES 2,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XX9E	RES 3,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXA6	RES 4,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXAE	RES 5,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXB6	RES 6,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXBE	RES 7,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXC6	SET 0,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXCE	SET 1,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXD6	SET 2,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXDE	SET 3,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXE6	SET 4,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXEE	SET 5,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXF6	SET 6,(IY+IND)	23	OCF OCF OD IO MR MW	5	03
XXFE	SET 7,(IY+IND)	23	OCF OCF OD IO MR MW	5	03