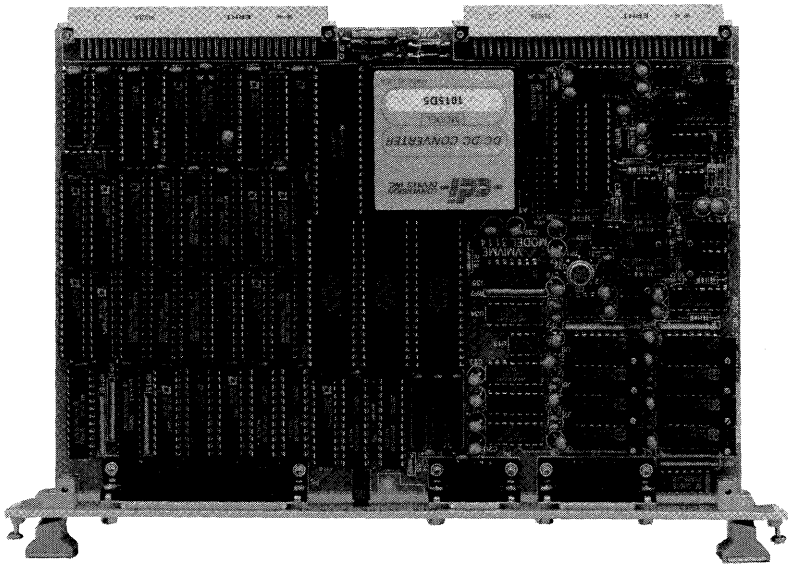
PRELIMINARY

VMIVME-3114

12-bit ANALOG INPUT BOARD WITH SIMULTANEOUS SAMPLE-AND-HOLD INPUTS, DUAL ANALOG OUTPUTS, AND 16-bit DIGITAL I/O



FEATURES

ANALOG INPUTS

- EIGHT SAMPLE-AND-HOLD SCANNING ANALOG INPUT CHANNELS
- 12-bit A/D CONVERTER, WITH RANGES OF 0 TO 10 V, ±5 V, AND ±10 V
- PGA PROVIDES PROGRAM CONTROLLED GAINS OF X1, X2, X4, X8, AND X16
- 125 kHz MAXIMUM SCAN RATE (GAIN = x1)
- DUAL 128 Kbyte DATA BUFFERS

DIGITAL I/O

- DUAL 8-bit TTL I/O PORTS, PROGRAM CONTROLLED AS INPUTS OR OUTPUTS

GENERAL

- DUAL-PORTED DATA BUFFERS APPEAR AS MEMORY TO VME HOST
- CONTINUOUS OR SYNCHRONOUS SEQUENCING
- MULTIBOARD OR INDEPENDENT SYNCHRONIZING
- INTERRUPTS

ANALOG OUTPUTS

- DUAL DEGLITCHED 12-bit SCANNING ANALOG OUTPUTS
- OUTPUT RANGES OF 0 TO +10 V, ±5 V, AND ±10 V
- 10 mA LOAD CAPACITY
- 125 kHz MAXIMUM UPDATE RATE
- DUAL 128 Kbyte DATA BUFFERS
- ON-LINE OR OFF-LINE OPERATION UNDER PROGRAM CONTROL

VME MICROSYSTEMS INTERNATIONAL CORPORATION
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Huntsville, Alabama 35803-3308
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Revised 29 May 1992

Document No.: SSS-003114-000

VMIVME-3114
ANALOG INPUT/OUTPUT BOARD

INTRODUCTION

The VMIVME-3114 is a 12-bit input/output board which provides eight analog inputs, two analog outputs, and dual 8-bit bi-directional digital input/output ports for VMEbus system applications. Dual ported data memory, on-board timers, and a program controlled bus interrupter enable the VMIVME-3114 Board to support extensive analog input and output traffic with minimum involvement of the host processor.

SPECIFICATIONS

FUNCTIONAL CHARACTERISTICS

GENERAL DESCRIPTIONS:

Sample-and-hold input amplifiers provide "snapshot" simultaneous sampling of all analog inputs at aggregate sample rates up to 125 kHz, and virtually eliminate time skewing between input channels. The VMIVME-3114 supports both *independent and multiboard synchronization*. Dual analog outputs enable the board to "close the loop" in system servo applications. The VMIVME-3114 functional block diagram is shown in Figure 1.

Analog Input data is stored sequentially in dual 64 Kword buffer memories. The host controls which of the two buffers resides in VME memory through a single toggle bit in the Control and Status Register (CSR). The host can direct the board to generate an interrupt when a scanning sequence is completed.

Dual analog output channels are deglitched to ensure minimum output noise, and can drive 10 mA loads over the maximum output range of ±10 V. Dual 64 Kword buffer memories for the analog outputs are identical to the analog input buffers, and provide the same control features. On-line or off-line (disconnected) operation is program controlled.

Analog inputs and outputs can be programmed to scan continously, or to stop at the end of a buffer. Scan rates can be provided by on-board or external clocks, or by software single-stepping. Up to seven slave boards can synchronize to a master VMIVME-3114. Input and output scan rates are independent.

The buffer memories appear as 128 Kbytes of VMEbus memory. To simplify automatic system configuring, the buffers are disabled during power-up and reset operations. To support multiple VMIVME-3114 Boards without requiring additional memory space, the buffers can be removed from VME memory entirely through a control bit in the I/O space CSR. The buffers are program locatable on any 4 0000 byte (HEX) boundary in the VMEbus memory space. Block Mode D16 data transfers (BLT) are supported.

SEQUENCE INITIATION:

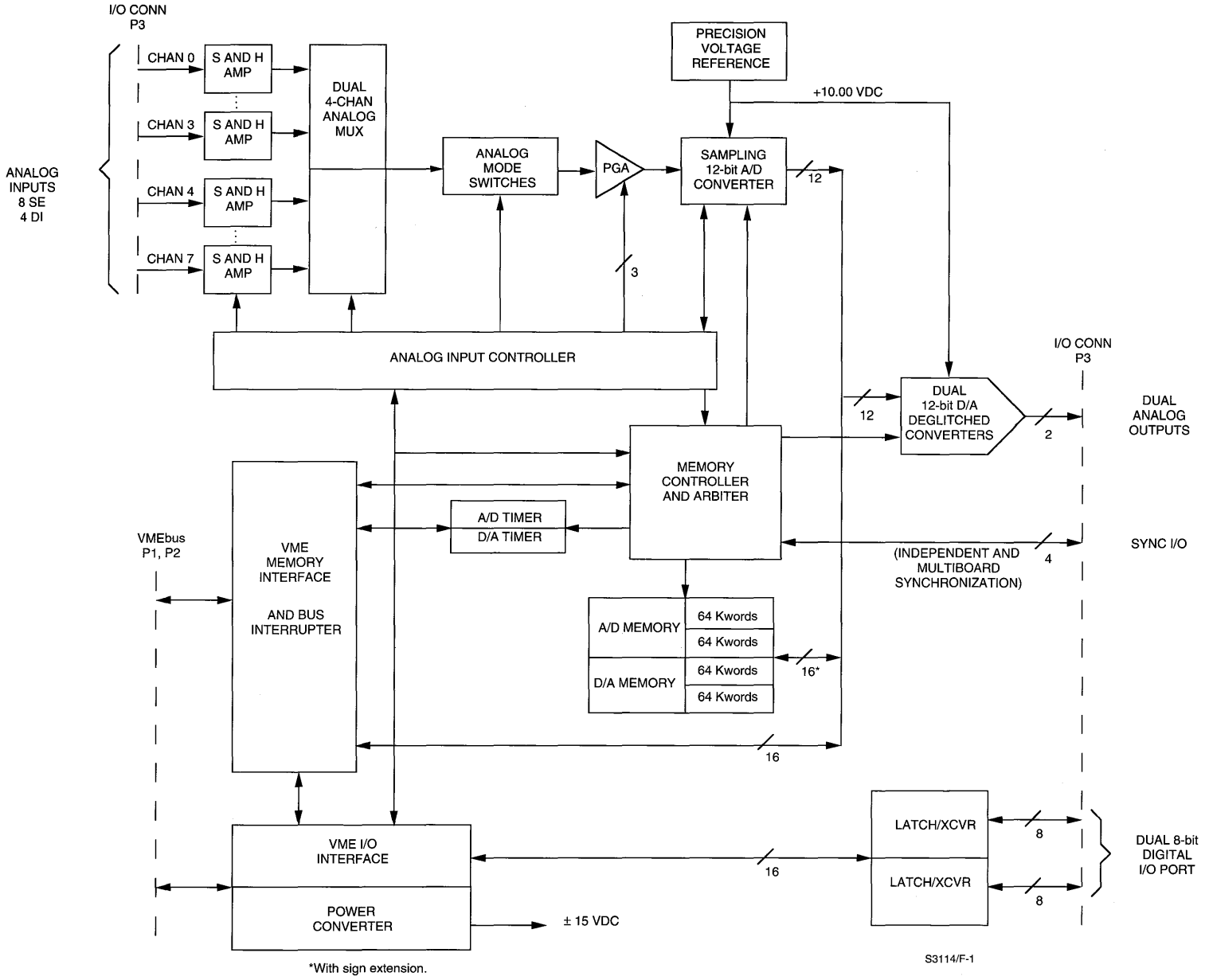
The input and output scans have separate resets. These can be used to start scans at specific moments.

DIGITAL I/O PORTS:

16-bit parallel digital input and output capability is provided by dual 8-bit TTL data ports. Each port can be program configured as either an input or output port, and is accessible in the short I/O space in which the control registers for the boards are located.

COMPLIANCE:

A32/A24/A16:D16/D08 (EO) DTB Slave: BLT D16 Slave.
Interrupters (2): I(1) to I(7) ROAK.
Interrupt Vector:D08(0).
6U form factor.



*With sign extension.

Figure 1. VMIVME-3114 Analog I/O Board Block Diagram
(8-Channel, 12-bits, Sample-and-Hold Analog Inputs)

I/O ADDRESSING: Addressable as 16 contiguous 16-bit registers, located on any 16-word boundary within the short supervisory or short nonprivileged I/O space.

MEMORY ADDRESSING: The input and output buffers appear as conventional memory to the VME host. Total memory space occupied by the board is 256 Kbytes, and can be program located on any 4 0000 byte (HEX) boundary in the VMEbus memory space. The VMIVME-3114 buffers can be removed (masked) from VME memory, by a CSR control bit, thereby permitting multiple boards to occupy the same memory space.

I/O ADDRESS SELECTION: Board address in the short I/O space is selected by on-board field selectable jumpers. Operation is supported in any slot except slot 1.

ACCESS PRIVILEGE: Address modifiers are decoded to support either supervisory or nonprivileged access, or both accesses. Jumpers are provided to support this feature, and is factory configured for either access. Decoded modifier codes include 09, 0A, 0B, 0D, 0E, 0F, 2D, 29, 39, 3A, 3B, 3D, 3E, and 3F.

VME INTERRUPT: The VMIVME-3114 can be programmed to generate separate interrupts for input and output end-of-buffer conditions. The interrupt levels ard response vectors (status/IDs) are programmable.

BOARD IDENTIFICATION: The Board Identification Register contains the VMIVME-3114 identification code.

INITIAL OPERATION: The following default conditions are established at RESET:

- Continuous operation.
- Minimum block size.
- Analog Input Gain = x1.
- Maximum conversion rate.
- Analog outputs disconnected.
- Digital ports configured as inputs.

ELECTRICAL SPECIFICATIONS (TYPICAL @ 25 °C)

ANALOG INPUTS

NUMBER OF INPUTS CHANNELS: Eight single-ended or four differential channels.

RESOLUTION: 12 bits.

VOLTAGE RANGES: 0 to +10 V, ±5 V, ±10 V; jumper-selectable.

VOLTAGE GAIN: Program-selectable as x1, x2, x4, x8, x16.

INPUT IMPEDANCE: 1 MΩ minimum.

INPUT SAMPLING: Simultaneous sampling of all analog inputs.

INTERCHANNEL PHASE SKEW: Less than 0.1° at 5 kHz.

CONVERSION RATE: 977 Hz to 125 kHz (aggregate) in 7 equal ratios of 2:1 (internally generated). Up to 125 kHz by external or software sync.

PER CHANNEL CONVERSION RATE: Up to 31,250 Hz for four channels.
Up to 15,625 Hz for eight channels.

ACQUISITION TIME: Same as conversion cycle, see Note 2.

SETTLING TIME: 3.5 µsec maximum, to 0.02 percent; Gain = x1.

CONVERSION CYCLE:
(Setting plus Conversion) 8.0 µsec maximum.

DATA CODING: Two's complement, binary or offset binary.

GAIN ERROR: ±0.05 percent maximum.

CROSSTALK REJECTION:	72 dB at 1 kHz.
INPUT OFFSET:	±2.0 mV maximum.
INPUT BIAS CURRENT:	±200 nA.
INPUT PROTECTION:	±25 V, sustained.

(1) KSPS = Thousand samples per second.
(2) Inputs are "pipelined" sample acquisition occurs while the previously acquired channel sample is digitized.

ANALOG OUTPUTS

NUMBER OF OUTPUT CHANNELS:	Two independent, deglitched analog outputs.
RESOLUTION:	12 bits.
MONOTONICITY:	12 bits over operating temperature range.
OUTPUT MODES:	On-line (output connected to I/O connector) or off-line (outputs disconnected from I/O connector).
VOLTAGE RANGES:	0 to +10 V, ±5 V, ±10 V, jumper-selectable.
OUTPUT IMPEDANCE:	Less than 0.5 Ω.
SCAN RATE:	3.8 Hz to 125 kHz in 15 equal ratios of 2:1 (internally generated). Up to 125 kHz external sync or software sync.
DATA CODING:	Two's complement, binary or offset binary.
SETTLING TIME:	20 µs maximum to 0.02 percent.
LINEARITY ERROR:	±0.03 percent maximum.
OUTPUT OFFSET:	± 5 mV maximum.
LOAD CURRENT:	± 10 mA maximum, over full output range of ±10 V.
LOAD CAPACITANCE:	3,000 pF, no oscillation.
OUTPUT PROTECTION:	Continuous short to ground; ±25 V for one second.
OFF-LINE OUTPUT LEAKAGE:	50 nA.

BUFFER MEMORIES

ANALOG INPUT BUFFER SIZE:	Two words to 64 Kwords, in 15 equal ratios of 2:1.
ANALOG OUTPUT BUFFER SIZE:	Two words to 64 Kwords, in 15 equal ratios of 2:1.
VMEbus ACCESS:	D8 or D16; conventional or block mode transfers.
VMEbus ACCESS LOCATION:	Program locatable on any 4 0000 byte (HEX) boundary from 00000000 to FFFC0000 (HEX).
CONTROL:	Disabled at power-up and during reset operations. Enabled or disabled through the short I/O space CSR.
OPERATING MODES:	Continuous or single block.

DIGITAL I/O PORTS

ORGANIZATION:	Dual 8-bit bi-directional ports.

LOGIC LEVELS:	Standard TTL levels with no inversions.
VMEbus ACCESS:	Single 16-bit register is short I/O space, D8 or D16 access.
CONTROL:	Each port is program-controlled as either an input port or an output port.

PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

TEMPERATURE:	Operating: 0 to +55 °C. Storage: 40 to +85 °C.
RELATIVE HUMIDITY:	10 to 80 percent noncondensing.
ALTITUDE:	Operation to 10,000 feet.
COOLING:	Forced air convection.
DIMENSIONS:	Standard VME double height board, 160 x 233.35 mm.
INPUT/OUTPUT CONNECTORS:	Refer to Ordering Information.
POWER REQUIREMENTS	5.1 A (typical) @ +5.0 VDC +0.25/-0.125 VDC . 7.3 A (maximum).

REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253 (602) 951-8866

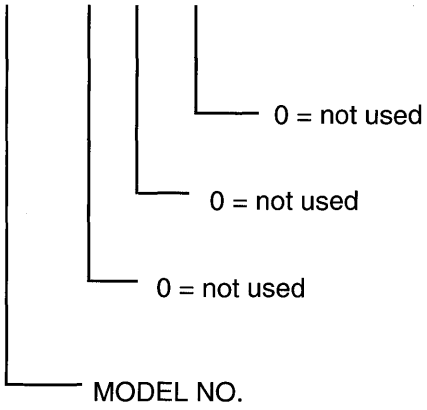
The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Board Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

VMIVME-3114 ANALOG INPUT/OUTPUT BOARD

ORDERING INFORMATION

VMIVME-3114 - A B C



I/O CONNECTOR DATA (*)

TYPICAL CONNECTING COMPONENT	P2 (PANDUIT)	P3 (AMP)	P4 (AMP)	P5 (AMP)
COMPATIBLE MATING CONNECTOR (Insulation Displacement)	120-964-435E	747945-5	747943-5	747949-5
STRAIN RELIEF (FERRULE)	100-000-032	1-747579-0	747579-8	747580-8
P.C. BOARD HEADER CONNECTOR	101-096-033A (96-pin DIN)	747841-3 (15-pin PLUG)	747840-3 (9-pin PLUG)	747843-3 (37-pin PLUG)

*P3, P4, and P5 are standard D-Subminiature connectors.

VMIVME-3114

12-bit ANALOG INPUT/OUTPUT BOARD

8 INPUT CHANNELS, 125 kHz WITH SAMPLE-AND-HOLD INPUTS AND DYNAMIC ANALOG OUTPUTS

INSTRUCTION MANUAL

DOCUMENT NO. 500-003114-000 A

4 February 1993

VME MICROSYSTEMS INTERNATIONAL CORPORATION
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NOTICE

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VMIC

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	02/03/93	Release	93-0029

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THIS OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THE PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

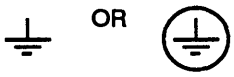
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

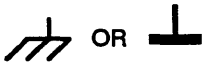
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



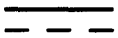
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-3114
12-bit ANALOG INPUT/OUTPUT BOARD 8 INPUT CHANNELS, 125 kHz WITH SAMPLE-AND-HOLD INPUTS AND DYNAMIC ANALOG OUTPUTS

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APPENDIX

SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-3114 (Figure 1.1-1) is a member of VMIC's extensive family of analog input/output board products for the VMEbus. The board provides automatic scanning of both analog input and output functions, and represents a complete analog input/output subsystem. Digital ports also are included for controlling and monitoring TTL interfaces. Simultaneous sampling of eight analog input channels provides the minimum skew characteristics required in modern sampled data systems. Two dynamic analog output channels are available for the generation of arbitrary analog stimulus functions.

A summary of principal features illustrates the performance and flexibility offered by the VMIVME-3114 Board:

1.1.1 VMIVME-3114 High Rate 12-bit Analog Inputs

a. Simultaneous sampling of eight single-ended or four differential analog inputs
b. Aggregate conversion rates to 125 kSPS (thousand samples per second)
c. Input ranges of 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V
d. Program controlled gains of x1, x2, x4, x8, and x16
e. Dual 64-Kword data buffers
f. High-speed 3 µsec 12-bit Analog-to-Digital Converter (ADC)
g. Program controlled input block size and scan rate
h. Continuous, burst, single-step, and multiboard synchronization
i. Bus interrupter for block-full indication
j. Loopback self-test

1.1.2 VMIVME-3114 Dual 12-bit Analog Outputs

a. Output ranges of 0 to +10 V, 0 to +5 V, ±2.5, ±5 V, and ±10 V
b. Dual 64-Kword data buffers
c. Dual, deglitched 12-bit Digital-to-Analog Converter
d. Program controlled output block size
e. Continuous, burst, single-step, and multiboard synchronization
f. 10 mA output load capacity over full output range
g. On-line or off-line operation under program control
h. Bus interrupter for end-block indication
i. Scan rates to 125 kSPS for each channel

(Photograph of VMIVME-3114)

M3114/F1.1-1

Figure 1.1-1. VMIVME-3114 Analog Input/Output Board

1.1.3 VMIVME-3114 Digital Input/Output Ports

a. Dual independent 8-bit TTL input/output ports
b. Individually program controlled as input or output ports

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-3114 (Figure 1.2-1) is a high throughput 12-bit Analog Input/Output (AIO) Board which provides eight sample-and-hold analog inputs, two dynamic analog outputs, and dual 8-bit bi-directional digital input/output ports for VMEbus system applications. Dual ported data memory, on-board rate generators, and a program controlled bus interrupter enable the board to support extensive analog input and output traffic, with minimum involvement of the host processor.

Analog input data is stored sequentially in two 64-Kword buffer memories. A bit in the Control and Status Register (CSR) selects one of the buffers for access as VME memory. VME controlled registers determine the active block size of the buffers, and the input scanning rate. The host can direct the board to generate an interrupt when an input block is filled. Input gain, active buffer size, and preset scan rate are controlled by the Input Control Register (ICR).

Analog inputs can be scanned at a preset rate or synchronized to an external signal.

Analog inputs can be sequenced either continuously, single block synchronously, or multiboard synchronously. In the continuous mode, input scanning proceeds continuously unless stopped by the host processor. The VMIVME-3114 fills one input buffer while the host reads the other. In the single block synchronous mode, a preselected input block is filled and the input sequence halts. Multiboard synchronization can be applied in either the continuous or single block modes, with a designated master controlling other VMIVME-3114 Boards.

To simplify automatic system configuring, VME access to the input and output buffers is disabled after power-up and reset operations. VME-to-buffer access is enabled by a bit in the CSR. This bit makes it possible for several VMIVME-3114 Boards to share a buffer address, thus conserving memory space. The buffer is jumper-locatable on any 20000 (HEX) word boundary in the VMEbus memory space.

Dual dynamic analog output channels can drive 10 mA loads over the maximum output range of ±10 V. On-line operation (outputs connected to I/O connector) or off-line operation (disconnected) is program controlled. Each of the two analog output channels is driven from a dedicated 64-Kword data buffer. Control and synchronization of the analog output buffers is essentially identical to that of the analog input buffers, but is independent of analog input activity.

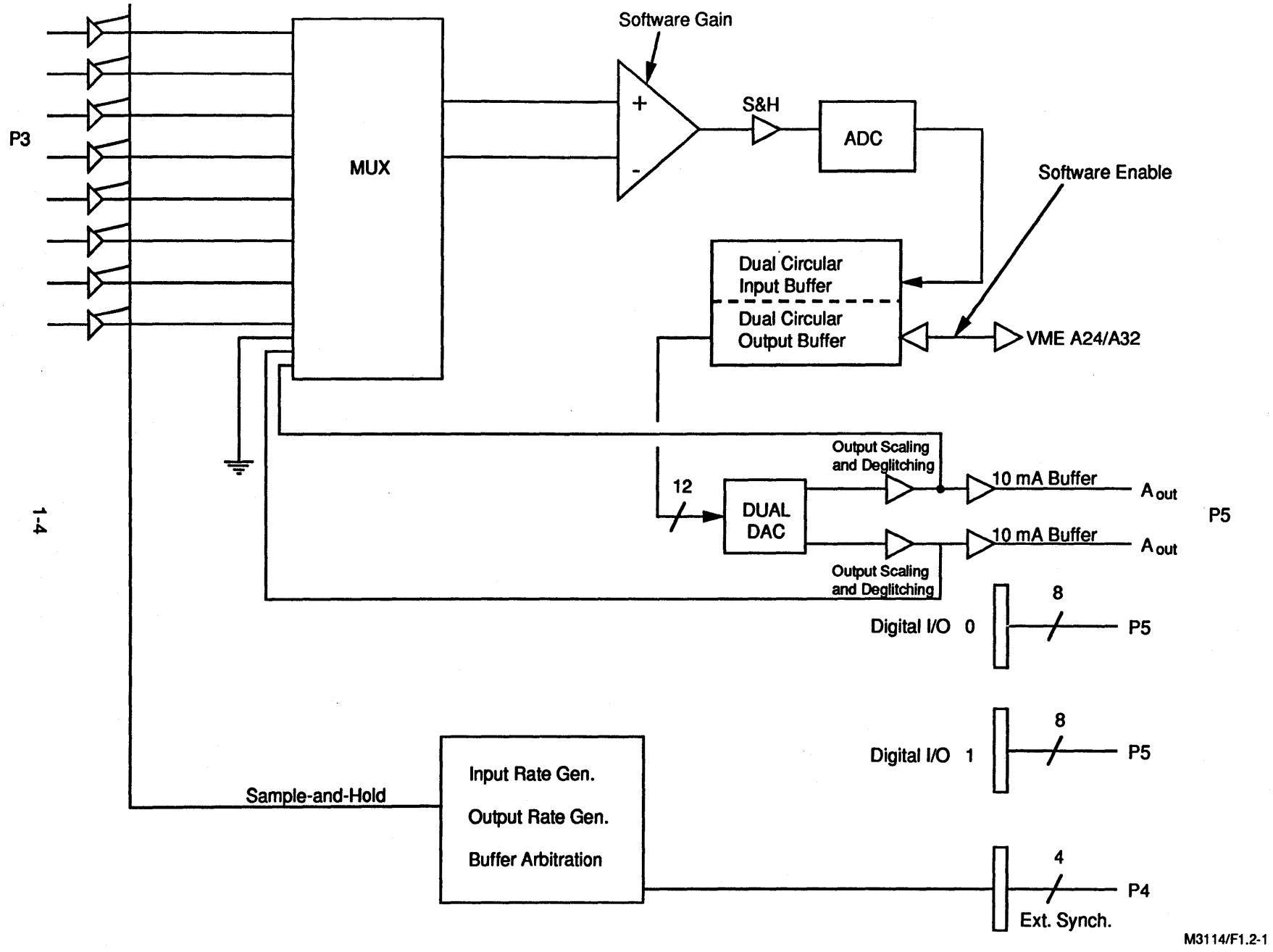

Figure 1.2-1. Functional Block Diagram

1.3 REFERENCE MATERIAL

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
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Scottsdale, AZ 85253
(602) 951-8866

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Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Product (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

SECTION 2
PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003114-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3114 Board uses a high-speed Analog-to-Digital Converter (ADC) and pipelined Sample-and-Hold Amplifiers (S&H), to achieve high rate sampling and 12-bit digitizing of eight single-ended or four differential analog inputs. All inputs are sampled simultaneously to eliminate time skewing, and their digitized values are stored sequentially in Dynamic RAM (DRAM) data buffers. Input scanning can be operated asynchronously, or can be synchronized either to an external signal or to another VMIVME-3114 Board.

Dual Digital-to-Analog Converters (DACs) convert 12-bit digital values from scanned data buffers into two dynamic analog output channels. The data buffers can be scanned automatically, or can be single-stepped or synchronized to either an external sync signal or to another VMIVME-3114 Board. A self-test multiplexer permits the analog outputs to be routed to the analog input multiplexers for loopback self-testing.

In addition to the analog input and output functions, the board provides two independent 8-bit digital I/O ports.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-3114 Board contains the following hardware functions:

a. VMEbus interface and bus interrupter
b. Input and output data buffers
c. Analog input sampling, multiplexing, and digitizing
d. Analog input synchronization
e. Analog output DACs, deglitching, switching, and protection
f. Analog output synchronization
g. Digital I/O ports
h. Power converters

The Control and Status Register (CSR) establishes the operational mode of the board. The Input Control Register (ICR) and Output Control Register (OCR) establish the sizes of the input and output memory blocks, and control the input and output scan rates. The Scan Status Register (SSR) monitors the status of input and output scanning operations.

3.3 SHORT I/O CONTROL INTERFACE

Control of data transfers between the board and the VMEbus is illustrated in Figure 3.3-1. Data transfers are supported anywhere in the VMEbus short I/O space. Address modifiers AM0 through AM5 are decoded to support both supervisory and nonprivileged access. The registers which are used to control and monitor the board occupy a 16-word block which can be located on any 16-word boundary within the VMEbus short I/O space.

3.3.1 Read/Write Operations

VMEbus data transfer requests are ignored unless the board-selection comparator detects a match between the selection jumpers and the address and address modifier lines from the backplane. When a valid match is detected, the board prepares for a data transfer, and asserts the open collector DTACK interface signal (LOW). DTACK returns to the negated (HIGH) state when the transfer has been completed.

Data Bus lines D00 through D15 are bi-directional and move data to or from the board through a 16-bit data transceiver in response to control signals from the I/O control timer. The data transceiver serves as a buffer for the internal data bus which interconnects all short I/O devices on the board. Address lines A05 through A15 map the communication registers onto an 16-word boundary within the VME short I/O space (Section 4). Data transfer control signals from the VMEbus determine whether data is moved to the board (Write) or from the board (Read). Both D8 and D16 transfers are supported.

3.3.2 Bus Interrupter

To eliminate the processing overhead usually associated with process polling, access to the VME interrupt structure is provided through a bus interrupter. If the interrupt is enabled, an interrupt is generated in response to an INTERRUPT REQUEST signal, which indicates the end of an input or output buffer. The interrupt function is implemented with a Bus Interrupter Module (BIM). Control Registers for the interrupter occupy four word locations in the short I/O space. Details of interrupter capabilities are described in Section 4.

3.4 STANDARD AND EXTENDED MEMORY DATA TRANSFERS

The data buffers can be located on any 20000 (HEX) word boundary in either standard or extended VMEbus space, depending upon the position of on-board jumpers. Detection of a match between the jumpered address and the current VMEbus address causes the memory DTACK generator to initiate a VME MEMORY REQUEST. The arbiter frees the RAM after input and output scans and refresh cycles are done. Upon completion of the data transfer, the MEM DTACK flag is combined with the I/O DTACK in the interrupt controller to produce a VMEbus DTACK.

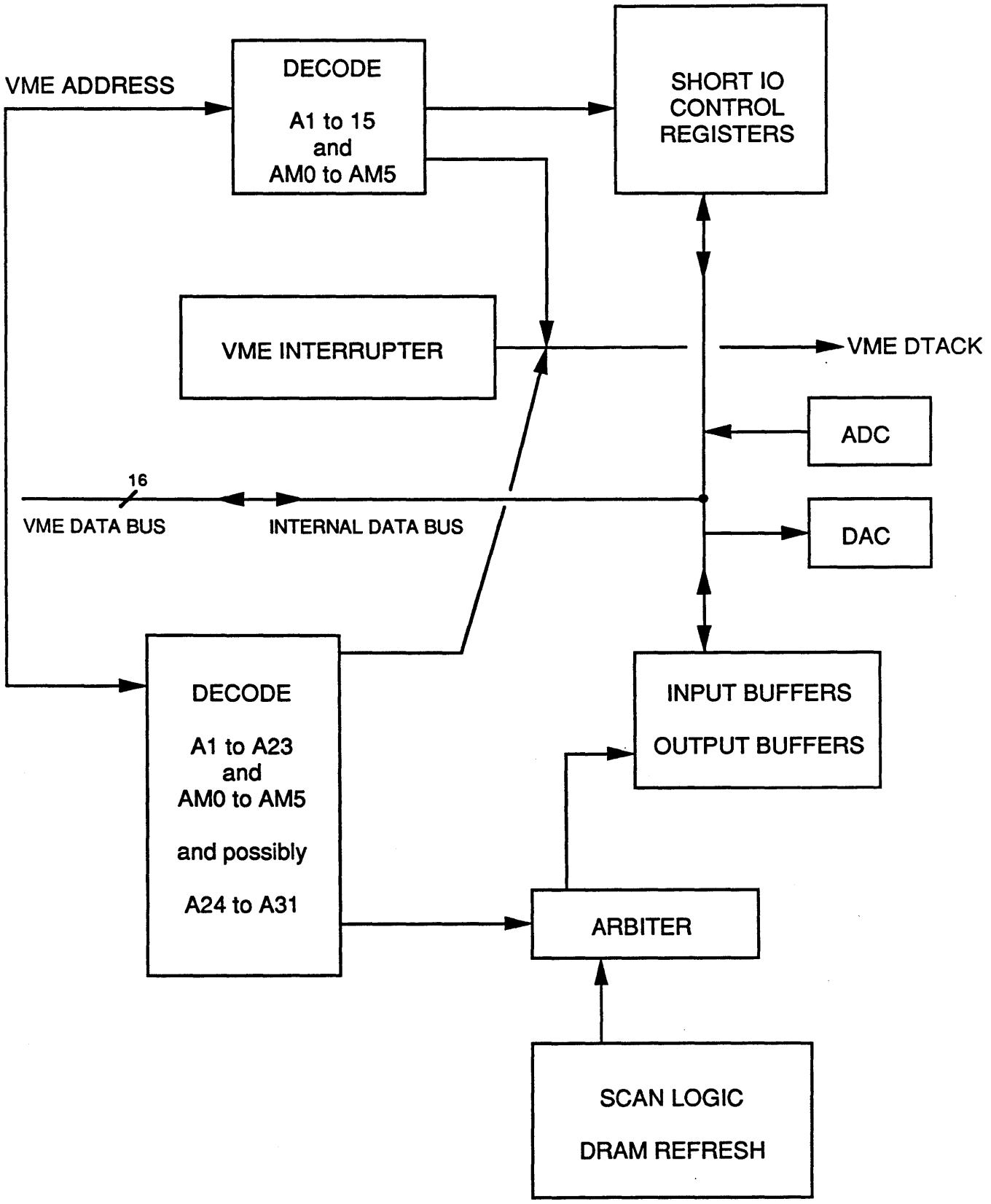


Figure 3.3-1. VMEbus Interface Logic

3.5 DATA BUFFERS

3.5.1 Input Buffers

Digitized inputs are stored in on-board dual data buffers (Figure 3.5.1-1), which share 128 Kwords of 12-bit wide Dynamic RAM (DRAM). The upper 4 bits of each data word are appended during VMEbus access as a sign extension. Digitized data accumulates within only one buffer at a time. Addressing of buffer memory is controlled by the ADC address counter for ADC access, and by the VMEbus through the VME address buffer for VMEbus access. The CSR permits either buffer to be selected for VMEbus access, or for both buffers to be removed from the VMEbus address space.

The BLOCK SIZE input from the Input Control Register (ICR) establishes the size of each buffer from 2 words to 64 Kwords, in 15 equal binary steps. Maximum scanning rate is controlled by the SCAN RATE output of the ICR from 1 kHz to 125 kHz, in seven equal binary steps. The ADC address counter halts and generates an END SCAN signal when the ADC conversion count matches the BLOCK SIZE. END ADC SCAN causes the ADC timer/sequencer to set a RST ADC ADDR flag which can be programmed to generate an interrupt request. END ADC SCAN also sets an ADC SCAN COMPL flag which is monitored through the SSR.

Buffer operation can be programmed for either single scan operation, in which A/D conversion activity ceases after a single buffer is filled, or for continuous operation, in which the accumulated data alternately fills each buffer. Data is stored in the input buffer in channel sequence starting with Channel 0 and ending when the buffer is full.

3.5.2 Output Buffers

The analog output data buffers occupy the 64-Kword space directly after the input buffers. Like the input buffers, the two analog outputs are represented by two 64-Kword buffers. Prior to operation of the analog outputs, the VME host must preload the output buffers with a sequence of 12-bit data words which represent the required analog output sequence. Analog output Channel 0 values are located in Output Buffer 0, and Channel 1 values are located in Output Buffer 1.

Control operations are the same as those available for the input buffers, except control of scanning rates is extended to the range from 3.8 Hz to 125 kHz, in 15 equal binary steps.

3.5.3 Buffer Arbitration and Refresh

Access to the data buffers is controlled by the memory arbiter/sequencer, which arbitrates requests for ADC access (ADC MEMORY REQ), DAC access (DAC MEMORY REQ), VMEbus access (VME MEMORY REQ), and memory refresh (REFR MEMORY REQ). The highest priority is placed upon DAC requests, followed in descending order of priority by ADC, VMEbus, and Refresh memory requests.

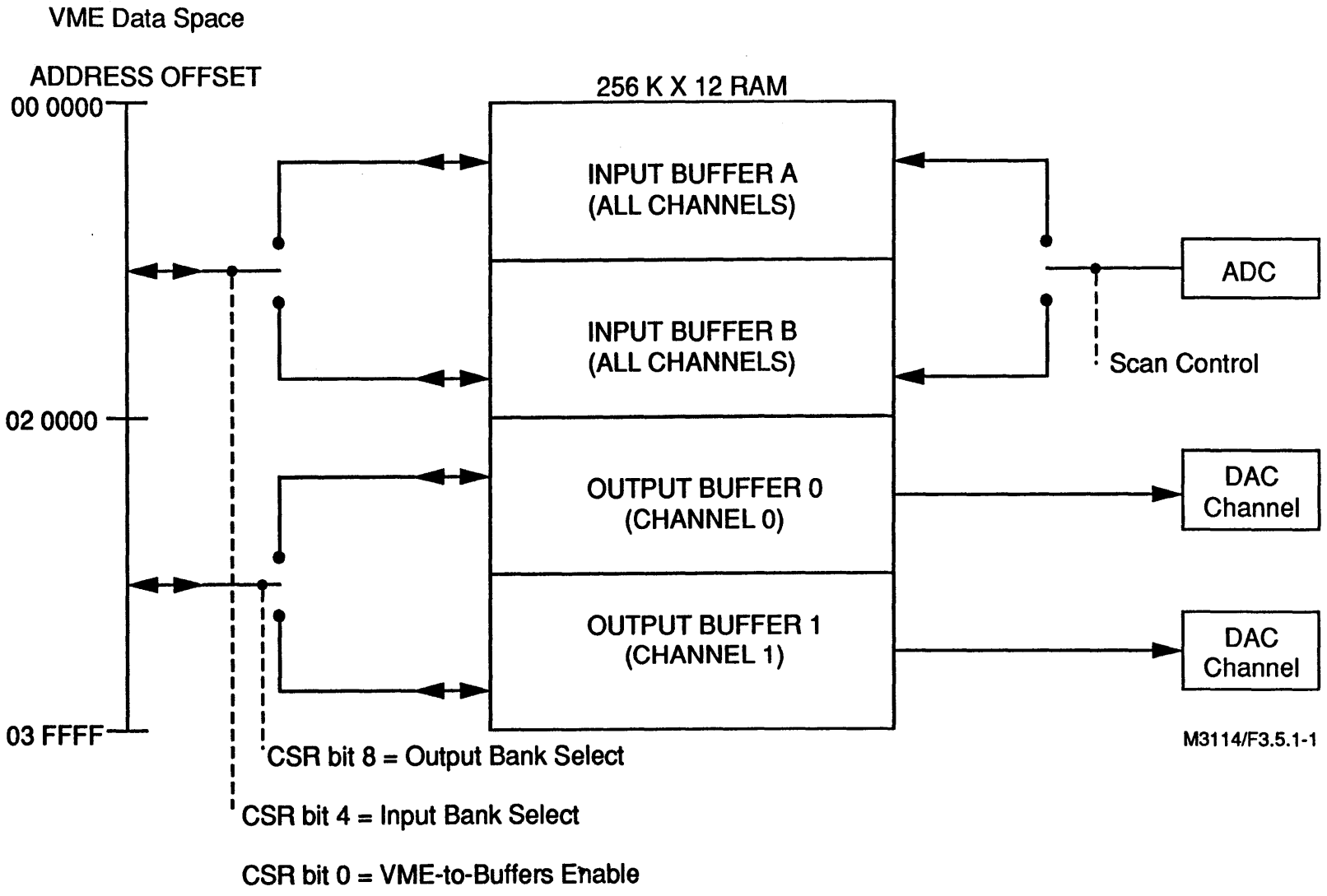


Figure 3.5.1-1. VMIVME-3114 Memory Buffers

3.6 ANALOG INPUT SYNCHRONIZATION

A sync event initiates a single sample and A/D conversion of all active input channels (4 or 8). At each sync event, all input channels are sampled, digitized, and stored in the input data buffers.

3.6.1 Sync Mode

A sync selector enables the VMIVME-3114 Board to be operated either asynchronously or synchronously, and in either continuous, single-block, or single-step mode.

3.6.2 Asynchronous Operation

In asynchronous continuous operation, external sync inputs are ignored and a sync event occurs automatically at the rate established by the SCAN RATE input from the ICR.

3.6.3 Synchronous Operation

Synchronous operation produces one conversion of each input each time a sync event occurs. External sync signals at P2 and P5 are identical, and appear at both connectors. During synchronous operation, the SCAN RATE in the ICR establishes only the maximum conversion rate; the actual rate is determined by the external sync source.

The board can be designated as either a master or a slave with the MASTER MODE control bit in the CSR (Section 4). A synchronous master is itself controlled by the EXT AD SYNC input or by CSR bit D07. An asynchronous master depends only on the programmed scan rate.

A synchronous slave ignores the EXT ADSYNC input, and instead, generates an internal sync event in response to the M/S AD SYNC signal from a master. This feature permits multiple slave boards to be synchronized to a single master. Master and slaves can be interconnected either through a ribbon cable at P5, or through backplane wiring at P2. As many as seven slaves can be controlled by a single master.

3.7 ANALOG INPUT PROCESSING

3.7.1 Sampling, Multiplexing, and Digitizing

The VMIVME-3114 Board can be jumper-configured to accept either eight single-ended or four differential analog inputs. All inputs are sampled simultaneously. They are multiplexed and gain-adjusted before being digitized by the ADC (Figure 3.7.1-1). Input sampling can be programmed to occur each time

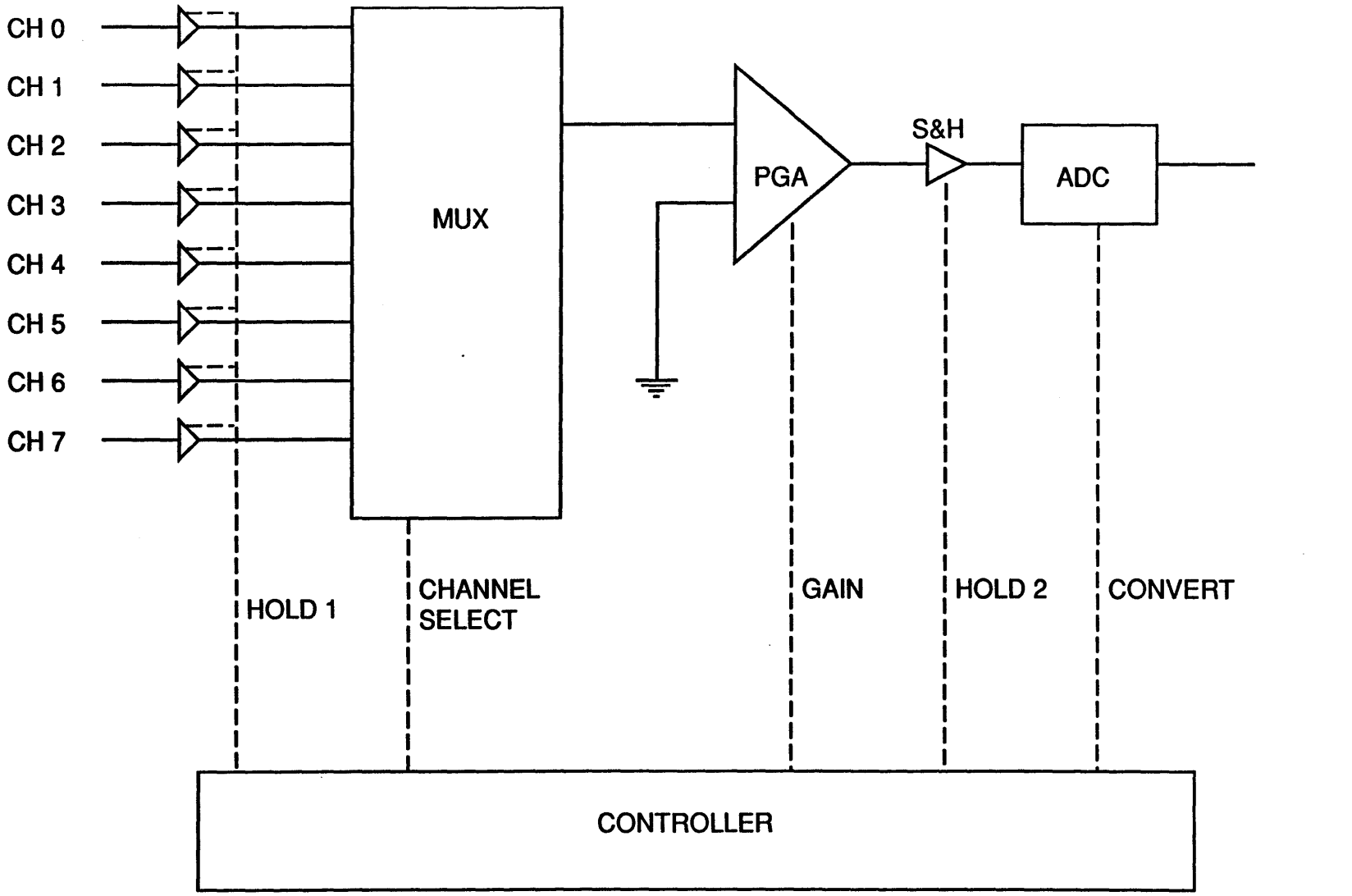


Figure 3.7.1-1. Analog Input Processing (Single-Ended)

the ADC Timer/Sequencer times out, or in response to an external trigger. Input gain is program controlled by a Programmable Gain Amplifier (PGA) from x1 to x16.

Channel pipelining is used to achieve the maximum possible scanning rate. The signal level of each channel is stored in a second (ADC) Sample-and-Hold Amplifier during each conversion, to allow the multiplexer and PGA to settle to the level of the next channel to be digitized.

3.7.2 Data Retrieval

A VMEbus memory read request causes the contents of the selected location to be latched into a memory data latch by the WR VME DATA strobe, after which the memory arbiter/sequencer is available for servicing the next request. ADC data is latched in this manner to prevent a delayed VMEbus data transfer from interfering with the necessary refresh of dynamic memory.

3.7.3 Loopback Testing

To accommodate loopback self-testing of the board, the INPUT MODE control lines from the ICR permit analog input Channels 03 and 07 to be replaced with the two analog output Channels 00 and 01.

3.8 ANALOG OUTPUTS

3.8.1 Digital-to-Analog Converters

The two analog outputs shown in Figure 3.5.1-1 are derived from a dual 12-bit Digital-to-Analog Converter (DAC). Data inputs to the converter are obtained from the 64-Kword analog output data buffers. Converter outputs are deglitched and buffered to permit driving 10 mA loads. The outputs are jumper-programmable for either unipolar or bipolar output voltage ranges, and can be commanded into either an on-line or off-line mode with the ANALOG OUTPUTS ON-LINE control line from the CSR. Both analog outputs are connected to the I/O connector in the on-line mode, and are disconnected in the off-line mode.

3.8.2 Analog Outputs Synchronization

Synchronization operations for the analog outputs are identical to those for the analog inputs. With the exception of the shared MASTER MODE control, analog output synchronization is independent of input synchronization. An output external sync event is a falling edge on EXT DA SYNC or CSR bit D11. These inputs are "OR-ed" together, so D11 must be kept low if EXT DA SYNC is used.

3.9 DIGITAL I/O PORTS

Two bi-directional digital I/O ports are provided at the front panel P5 connector (Figure 3.9-1). Each port consists of an octal bi-directional transceiver with tri-state outputs. The direction of each port is controlled by the associated DIRECTIONAL 0, 1 OUT line from the CSR. A port is configured as an output port if the associated control line is HIGH, or as an input port if the control line is LOW. The ports occupy two read/write byte-length registers in the short I/O space (Section 4).

3.10 POWER CONVERTER

Electrical power for the analog networks is supplied by a single DC-to-DC Converter which converts 5 VDC logic power from the VMEbus into isolated and regulated 15 VDC.

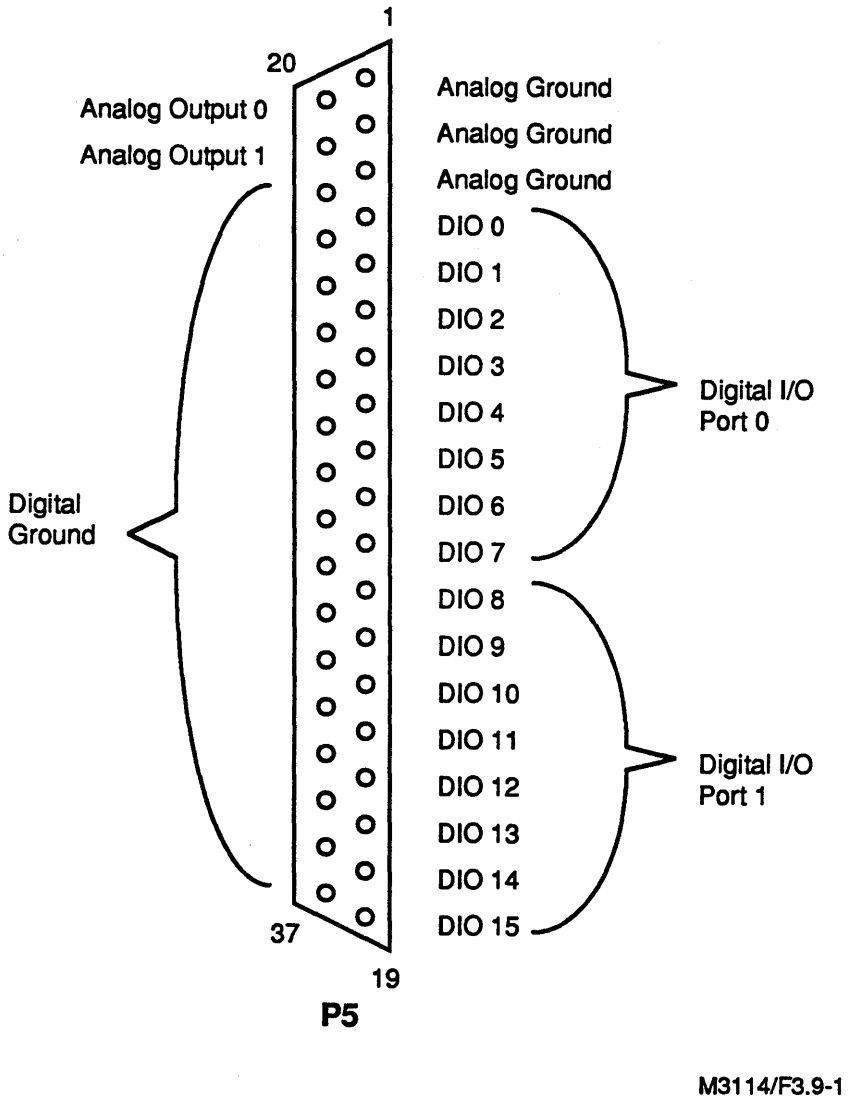


Figure 3.9-1. Digital I/O Ports and Analog Outputs

SECTION 4

PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-3114 BOARD

Control of the VMIVME-3114 Board takes place in the VMEbus short I/O space. All short I/O registers are listed in Table 4.1-1.

Four 64-Kword data buffers in the standard or extended address space contain the input data from the eight analog input channels, and the output data for the two analog output channels. VME access to the buffers is controlled by a control bit in the Control and Status Register (CSR), and is disabled when the board is reset. One input buffer and one output buffer are available simultaneously to the VMEbus. The CSR selects one input buffer and one output buffer for VME access (see Figure 4.1-1).

When enabled, the input/output buffers occupy 128 Kwords of contiguous address space, with the lower 64 Kwords representing one of the two analog input buffers, and the upper 64 Kwords representing one of the two analog output buffers. The buffers support both read and write data transfers for D00 through D11.

Analog input data is accumulated in the two analog input data buffers. Block size, scanning rate, synchronization, and all other control functions associated with the analog input data, are controlled and monitored by the short I/O registers. An interrupt can be programmed to occur when an input block is filled.

Analog output data is obtained by scanning the two analog output buffers, after the buffers are loaded from the VMEbus. Block size, scanning rate, synchronization, and all other control functions associated with the analog outputs, are controlled and monitored by the short I/O registers. An interrupt can be programmed to occur when the scanning of an output block is completed.

Two digital I/O ports also are controlled through the short I/O registers.

4.2 BOARD IDENTIFICATION REGISTER

The Board Identification Register (BID) contains the board identification code (000A 0000 HEX) for the VMIVME-3114 Board, and occupies two words within the short I/O space.

Table 4.1-1. VMIVME-3114 Short I/O Register Map

ADDRESS HEX	ADDRESS DEC	REGISTER FUNCTION	ACCESS MODE
00	00	BOARD IDENT (000A)	READ ONLY
02	02	BOARD IDENT (0000)	
04	04	CONTROL AND STATUS (CSR)	READ/WRITE
06	06	(Reserved)	---
08	08	SCAN STATUS (SSR), D00 to D07	READ ONLY
0A	10	DIGITAL I/O PORTS PORT 0 = D00 to D07 (byte at 0B HEX) PORT 1 = D08 to D15 (byte at 0A HEX)	READ/WRITE
0C	12	INPUT CONTROL (ICR)	READ/WRITE
0E	14	OUTPUT CONTROL (OCR), D00 to D07	READ/WRITE
10	16	INTERRUPT CONTROL, INPUT BUFFER	READ/WRITE
12	18	INTERRUPT CONTROL, OUTPUT BUFFER	READ/WRITE
14	20	(Reserved)	
16	22	(Reserved)	
18	24	INTERRUPT VECTOR, INPUT BUFFER	READ/WRITE
1A	26	INTERRUPT VECTOR, OUTPUT BUFFER	READ/WRITE
1C	28	(Reserved)	
1E	30	(Reserved)	

M3114/T4.1-1

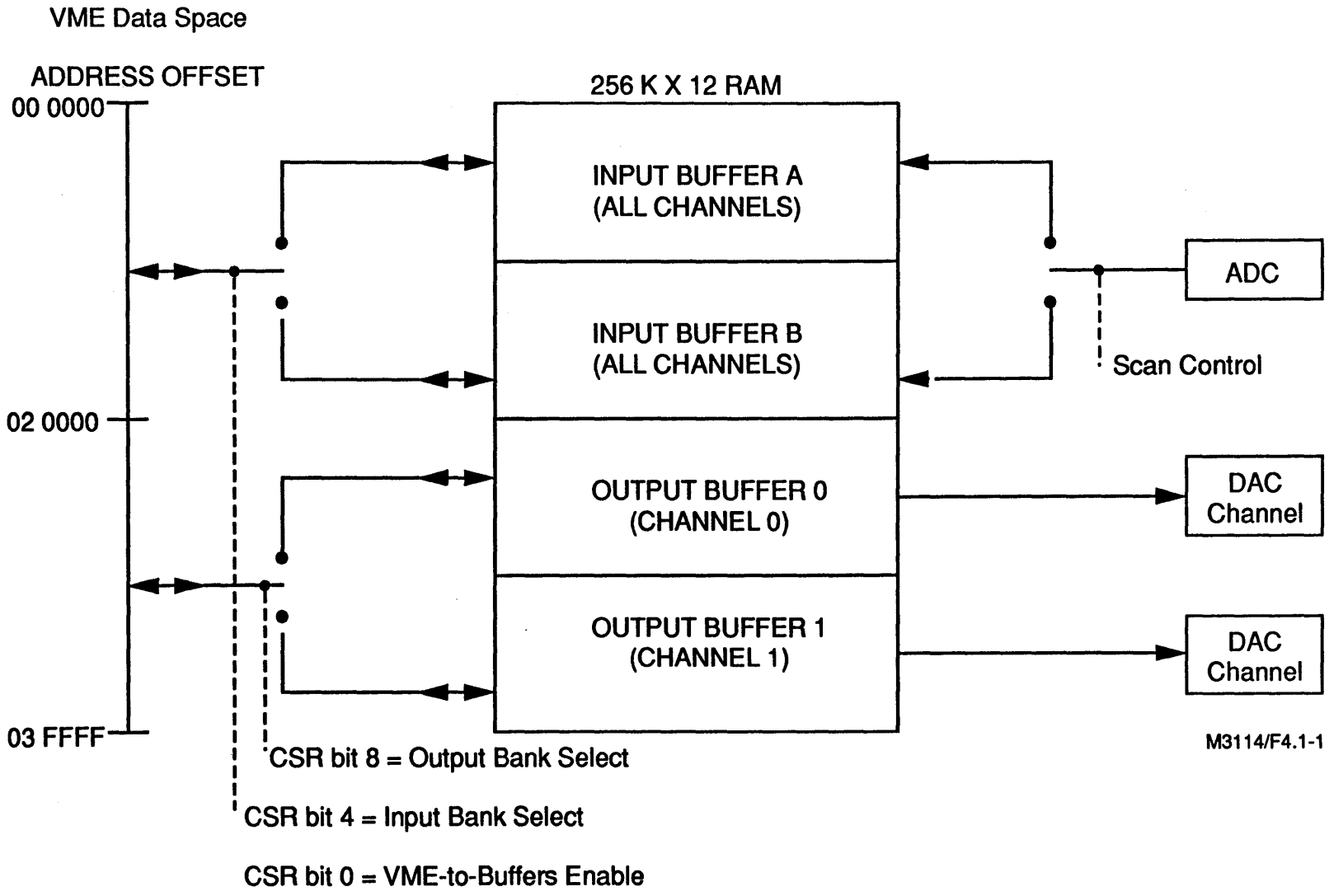


Figure 4.1-1. VMIVME-3114 Memory Buffers

4.3 BOARD ADDRESS AND ACCESS MODE

Programmable address jumpers permit the short I/O registers to be located on any 16-word boundary within the VME short I/O address space. Access mode may be programmed for supervisory, nonprivileged, or both.

Jumpers also are provided for locating the input/output data buffers on any 20000 (HEX) word boundary in either the standard or the extended VME address space. Selection of board address and access mode is described in Section 5.

4.4 CONTROL AND STATUS REGISTER (CSR)

CSR functions are summarized in Table 4.4-1. All Control Register bits are mapped directly to the Status Register. The CSR provides control and monitoring of the following board functions:

a. Synchronization modes
b. Buffer selection and control
c. Scanning modes
d. Analog outputs ON or OFF
e. Direction of digital I/O ports
f. Board self-test
g. Self-test LED
h. Board reset

4.5 ANALOG INPUT DATA BUFFERS

ADC data is accumulated in two data buffers, referred to as Buffer A and Buffer B. Input data accumulates initially in Buffer A until the Buffer A data block is filled. Accumulation then transfers to Buffer B. Channel data is contiguous, beginning with Channel 0 at location zero and proceeding consecutively through all active channels (4 or 8). The CSR directs VMEbus access to one of the two buffers. Location of the buffers in the VMEbus address space is controlled by address jumpers. The size of each buffer is fixed at 64-Kwords, but the size of the active data block within each buffer is programmable from two words to 64-Kwords.

4.5.1 Buffer Selection

VMEbus access to input Buffer B is selected if the CSR bit D04 is set. Buffer A is selected if D04 is cleared. D04 is cleared during reset.

LOGIC STATE CONVENTION

TO AVOID AMBIGUITIES IN REFERENCES TO LOGIC LEVELS, THIS DOCUMENT USES THE CONVENTION THAT A DATA BIT OR CONTROL LINE IS "SET" WHEN IT IS IN THE "ONE", OR HIGH STATE, AND IS "CLEARED" WHEN "ZERO" OR LOW.

Table 4.4-1. VMIVME-3114 Board Control and Status Register (CSR) Functions

D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
|----------byte 4----------|----------byte 5----------|
MSB CONTROL and STATUS REGISTER (CSR) DATA FORMAT LSB

CONTROL and STATUS BIT	NAME	FUNCTION
D00	ENABLE BUFFER ACCESS	VMEbus access to the data buffers is enabled if D00 is set, or is disabled if D00 is cleared.
D01	DISABLE OUT	Output scanning sequence is stopped (at the last used output levels) and reset if D01 is set, or is enabled if D01 is cleared.
D02	MASTER MODE	If D02 is set HIGH, the board is a Sync Master and can be used to clock other VMIVME-3114 Boards. If D02 is cleared, the board becomes a Sync Slave, and can respond to sync inputs from a Sync Master. Refer to the descriptions for D05 and D09, and to Section 4.7.
D03	SOFTWARE RESET	The board is RESET if D03 is set. D03 clears automatically after reset has been completed.
D04	SELECT INP BUFFER B	Input Buffer B is selected for VMEbus access if D04 is set; Input Buffer A is selected if D04 is cleared.
D05	INPUT SYNCHRONOUS	The synchronous input mode is selected if D05 is set. Asynchronous (independent) input operation is selected if D05 is cleared.
D06	INPUT SINGLE SCAN	If D06 is set, the input scanning sequence will halt when the buffer receiving converter data is filled. If D06 is cleared, the sequence will circulate continuously through both input buffers.
D07	INPUT SINGLE STEP	When Input Synchronous (bit D05) is set, this bit can be toggled to initiate a single frame of A/D conversions. Each high-to-low transition of D07 will cause a simultaneous sample and a conversion of each of the (4 or 8) input channels. D07 has no effect if D05 is cleared

M3114/T4.4-1/1

Table 4.4-1. VMIVME-3114 Board Control and Status Register (CSR) Functions (Concluded)

CONTROL and STATUS BIT	NAME	FUNCTION
D08	SELECT OUTPUT BUFFER 1	Buffer 1 is selected for VMEbus access if D08 is set; Buffer 0 is selected if D08 is cleared.
D09	OUTPUT SYNCHRONOUS	The synchronous output mode is selected if D09 is set. Asynchronous (independent) output operation is selected if D09 is cleared.
D10	OUTPUT SINGLE SCAN	If D10 is set, the output scanning sequence will halt at the end of the buffer which is providing output data. If D10 is cleared, the sequence will circulate continuously through both output buffers.
D11	OUTPUT SINGLE STEP	When OUTPUT SYNCHRONOUS (bit D09) is set, this bit can be toggled to initiate the next D/A conversion for each output. Each high-to-low transition of D11 will cause the outputs to be updated from the next locations in their buffers.
D12	DIRECTION 0 OUT	Digital PORT 0 is configured as an output port if D12 is set, or as an input port if D12 is cleared.
D13	DIRECTION 1 OUT	Digital PORT 1 is configured as an output port if D13 is set, or as an input port if D13 is cleared.
D14	ANALOG OUTPUTS ON	The analog outputs are connected to the I/O connector if D14 is set, or are disconnected if D14 is cleared.
D15	LED OFF	The "Fail" LED is OFF if D15 is set, or is ON if D15 is cleared.

M3114/T4.4-1/2

4.5.2 Location

The input buffers are located at the VMEbus address selected by programmable jumpers, as described in Section 5. The input buffers can be located on any 20000 (HEX) word boundary within the standard A24 or extended A32 address space.

4.5.3 Enabling

Access to the data buffers is enabled by setting CSR control bit D00 HIGH. D00 is cleared during a reset operation.

If the CSR bit D00 is cleared, VMEbus attempts to access data buffers are ignored. This feature allows multiple VMIVME-3114 Boards to share a common region in the VMEbus address space. It also serves to hide the buffer RAM from systems which search for active RAM during their power-up configuration.

4.5.4 Block Size

A data block is the active portion of a data buffer, and has the same base address as the buffer. Input data block size is controlled by the Input Control Register (ICR) shown in Table 4.5.4-1. ICR bits D00 to D03 adjust the size of the active analog input data block from two words to 64 Kwords in 15 equal binary steps. Only the active region is filled with data during a scan. All 64 Kwords may be reached by the VMEbus.

4.5.5 Data Format and Coding

Data from the ADC is stored in the input buffers in 12-bit right-justified format, as shown in Figure 4.5.5-1. Coding of the data is two's complement if the Two's COMPLEMENT jumper is installed, or is binary if the jumper is removed (refer to Section 5). The data coding selected by the Two's COMPLEMENT jumper also applies to the analog outputs.

4.5.6 Block Transfers

Block transfers are supported to a maximum of 128 words per transfer.

4.6 INPUT SCAN CONTROL

4.6.1 Single-Scan and Continuous Modes

CSR bit D06 selects the input single-scan operating mode when set, or the continuous mode when cleared. In the single-scan mode, digitizing ceases when Buffer A is filled, and will not resume until the scan address is reset by ICR bit D07 or by CSR bit D03. Buffer B is not used in single-scan mode.

Table 4.5.4-1. Input Control Register (ICR)

D00 to D03 .... INPUT BLOCK SIZE

D03	D02	D01	D00	DATA BLOCK SIZE (HEX)
0	0	0	0	2 WORDS (Note 1)
0	0	0	1	4 (Note 1)
0	0	1	0	8 (Note 1)
0	0	1	1	10
0	1	0	0	20
0	1	0	1	40
0	1	1	0	80
0	1	1	1	100
1	0	0	0	200
1	0	0	1	400
1	0	1	0	800
1	0	1	1	1000
1	1	0	0	2000
1	1	0	1	4000
1	1	1	0	8000
1	1	1	1	10000

D04 to D06 .... A/D CONVERSION RATE (TOTAL FOR ALL INPUT CHANNELS)

D06	D05	D04	CONVERSION RATE (CONV/SEC)
0	0	0	125.0 kHz
0	0	1	62.5 kHz
0	1	0	31.2 kHz
0	1	1	15.6 kHz
1	0	0	7.8 kHz
1	0	1	3.9 kHz
1	1	0	1.9 kHz
1	1	1	0.9 kHz

D07 .... DISABLE IN H — When this bit is set, input scanning is disabled (halted). When it is cleared, the scan will begin with the first location of buffer A.

D08 to D10 .... INPUT GAIN

D10	D09	D08	INPUT GAIN
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	1	1	x16

D11 to D12 .... INPUT TEST MODE

D12	D11	INPUT DATA CHAN 03	INPUT DATA CHAN 07
0	0	INPUT 03	INPUT 07 (Normal Operation)
0	1	OUTPUT 00	OUTPUT 01
1	0	OUTPUT 00	ANALOG RETURN
1	1	ANALOG RETURN	ANALOG RETURN

NOTE 1: If the block size specified is less than the channel count, channel count is truncated to block size. The default block size is 8 which allows all 8 channels to be stored.

NOTE 2: This table is for 8-channel mode. When 4 differential channels are used, Channel 3 will read the difference between the OUTPUT 0 and OUTPUT 1.

M3114/T4.5.4-1

ADC DATA FORMAT

```
MSB                                                                   LSB
 D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
| * | * | * | * | D | D | D | D | D | D | D | D | D | D | D | D |
```

*** = Zero (binary) or extended sign (two's complement).**

ADC CODING

UNIPOLAR RANGE	STRAIGHT BINARY		
INPUT	0 to +5 V	D15	D00
+FS-1 LSB	+4.9988 V	0000 1111 1111 1111	
+1/2 FS	+2.5000 V	0000 1000 0000 0000	
+1 LSB	+0.0012 V	0000 0000 0000 0001	

BIPOLAR RANGE	OFFSET BINARY		
INPUT	5 V	D15	D00
+FS-1 LSB	+4.9976 V	0000 1111 1111 1111	
+1/2 FS	+2.5000 V	0000 1100 0000 0000	
+1 LSB	+0.0024 V	0000 1000 0000 0001	
ZERO	0.0000 V	0000 1000 0000 0000	
-FS+1 LSB	-4.9976 V	0000 0000 0000 0001	
-FS	-5.0000 V	0000 0000 0000 0000	

BIPOLAR RANGE	TWO'S COMPLEMENT		
INPUT	5 V	D15	D00
+FS-1 LSB	+4.9976 V	0000 0111 1111 1111	
+1/2 FS	+2.5000 V	0000 0100 0000 0000	
+1 LSB	+0.0024 V	0000 0000 0000 0001	
ZERO	0.0000 V	0000 0000 0000 0000	
-1 LSB	-0.0024 V	1111 1111 1111 1111	
-FS+1 LSB	-4.9976 V	1111 1000 0000 0001	
-FS	-5.0000 V	1111 1000 0000 0000	

M3114/F.4.5.5-1

Figure 4.5.5-1. ADC Data Format and Coding

If continuous operation is selected, the accumulated data alternately fills each buffer, transferring to the opposite buffer as each buffer is filled. To prevent the overwriting of data in either buffer when the opposite buffer becomes filled, VMEbus transfer rates must exceed the conversion rate. In asynchronous operation, the A/D converter runs at the rate selected by ICR bits D4 to D6. For example, when these bits are all zeros, the converter runs at 125 kHz and each channel is converted at 31.25 kHz (4 channels) or 15.625 kHz (when 8 channels are configured). In synchronous operation, ICR bits D4 to D6 set the maximum conversion rate.

As each buffer is filled, the event can be determined either by polling the A/D SCAN A flag in the SSR, or by programming an interrupt to occur when either buffer becomes filled (refer to Section 4.9 "Bus Interrupter"). The AD SCAN A flag is set when the ADC is filling Buffer A, and is cleared when filling Buffer B.

4.6.2 A/D Conversion Rate

The maximum conversion rate for the ADC is selected by the ICR, which is shown in Table 4.5.4-1. ICR control bits D04 to D06 adjust the maximum conversion rate in seven equal binary steps. In the asynchronous or independent mode of operation, conversions occur automatically at the selected maximum rate. In the synchronous mode, sampling is initiated by an input sync event. Input sync events are identified in Table 4.6.2-1.

The maximum sampling rate or sync rate equals the conversion rate divided by the number of input channels, and has a maximum value of 31.25 kHz if the board is configured for four input channels, or 15.625 kHz for eight input channels. The number of channels is four for differential operation, or eight for single-ended operation. External sync rates may be a fraction of a percent higher than this, but if they are too high, then every other sync will be missed.

4.6.3 Scan Status Register (SSR) Monitored Functions

Functions monitored by the SSR include the status of the scanning sequence, and the states of configuration jumpers. Scan status monitored functions are described in Table 4.6.3-1. The SSR is a read only register.

4.7 INPUT SYNCHRONIZATION MODES

4.7.1 Synchronous Operation

Synchronous operation of analog inputs is selected by setting CSR bits D05 and D02 HIGH. In this mode, all input channels are sampled and digitized once for each input sync event. A sync event is a falling edge on either the EXT AD SYNC input or CSR bit D07. These inputs are OR-ed together, so bit D07 must be kept low when the external input is used. When the EXT AD SYNC input is not used, a built-in resistor pulls it low. If CSR bit D02 is set but CSR bit D05 is cleared, the input scan will sync with the M/S AD SYNC signal from another VMIVME-3114.

Table 4.6.2-1. Analog Input Synchronization Modes

CSR bits D05.D02		Mode	Controlling Sync Event	Is M/S AD SYNC driven?
0	0	Asynchronous (free running)	On-board rate generator	NO
0	1	Async. Master	On-board rate generator	YES
1	0	Slave	M/S AD SYNC input	NO
1	1	Ext. Sync Master	Falling edge on EXT DA SYNC input or CSR bit D07	YES

M3114/T4.6.2-1

Table 4.6.3-1. Scan Status Register (SSR)

SSR bit	NAME	DESCRIPTION
D00	AD SYNC RDY	The analog inputs are ready for the next sync event when this is HIGH.
D01	AD SCAN A	The results of the next A/D conversions will be sent to buffer A when this is HIGH, or to buffer B when this is LOW. Bit D01 also goes LOW when a single-scan input scan finishes.
D02	AD SCAN COMPLETE	This bit is set the first time an input scan has filled buffer A. It is cleared by a reset from ICR bit D07 or CSR bit D03.
D03	DA SYNC RDY	The analog outputs are ready for the next sync event when this is HIGH.
D04	-	Bit D04 is reserved.
D05	DA SCAN COMPLETE	This bit is set the first time the output scans reach the ends of their buffers. It is cleared by a reset from CSR bit D01 or CSR bit D03.
D06	STRAIGHT BINARY	The A/D and D/A converters are using straight binary and/or offset binary, as determined by jumper J1, when bit 6 is high. When this bit is LOW, the VMIVME-3114 is configured for two's complement data.
D07	DIFF INPUTS	HIGH indicates that four differential inputs are being scanned, instead of eight single-ended inputs.
D08...D15	-	These bits are reserved.

M3114/T4.6.3-1

The maximum sync event rate may not be more than the ICR's preset conversion rate, divided by the number of channels used. For instance, the ICR defaults to a conversion rate of 125 kHz. In this case, the sync event rate is limited to 15.625 kHz in 8-input (single-ended) mode or 31.25 kHz in 4-input (differential) mode.

4.7.2 Asynchronous (Independent) Operation

The asynchronous analog inputs operating mode is selected by clearing CSR bit D05. External sync inputs are ignored in this mode, and digitizing of the analog inputs occurs automatically at the selected conversion rate in the ICR. If CSR bit D02 is set, the VMIVME-3114 will drive M/S AD SYNC for other boards to sync to.

4.7.3 Multiboard Synchronization

Multiple VMIVME-3114 Boards can be configured to provide synchronized, simultaneous sampling of analog inputs. This feature is implemented by designating one of the boards as a master, and by designating the remaining boards as slaves. External cabling at the P2 or P5 connectors provides the necessary hardware interconnections for multiboard synchronization, the control signals for which are described in Sections 3 and 5. A single master can control as many as seven slaves.

Master/slave behavior is program-controlled by CSR bit D02 (MASTER MODE). A master may operate in any sync mode. It will retransmit its sync signals (both input and output) to the slaves. A slave will follow the input sync signal (M/S AD SYNC) if bit D05 of its CSR is set. It will run asynchronously if bit D05 is clear. CSR bit D02 also affects the OUTPUT master/slave behavior.

4.8 ANALOG OUTPUTS

The VMIVME-3114 Board provides two dynamic analog output channels, both of which use Digital-to-Analog Converters (DACs) to convert 12-bit digital values from scanned data buffers into sequences of analog voltage levels. The data buffers can be: scanned automatically, single-stepped, or synchronized to either an external sync signal or to another VMIVME-3114 Board. A self-test multiplexer permits the analog outputs to be routed to the analog input multiplexers for loopback self-testing.

The outputs are disabled on power-up or after a reset. They are enabled when CSR bit D14 is set.

4.8.1 Output Buffers

Two 64-Kword buffers are dedicated to the two analog output channels. Output 0 values are obtained from Output Buffer 0, and Output 1 values are obtained from Output Buffer 1. Like the analog input buffers, the active portions of the output buffers are referred to as blocks. The Output Control Register (OCR) determines their size. Both outputs are scanned at the same clocking rate, which also is controlled by the OCR. OCR functions are summarized in Table 4.8.1-1.

4.8.2 Output Scan Control

Scanning of the output buffers is controlled by CSR bits D08 to D11, and by the OCR. CSR output control functions are identical to the corresponding functions for the analog inputs, and are described in Table 4.4-1.

Block size and clocking rates are controlled by the OCR, as shown in Table 4.8.1-1. D00 to D03 control the block size from two words to 64 Kwords in 15 equal binary steps. D04 to D07 adjust the clocking rate from 3.8 Hz to 125 kHz, in 15 equal binary steps. D08 to D15 are not used.

4.8.3 Output Synchronization Modes

Synchronization modes for the analog outputs are identical to those described for the analog inputs. With the exception of CSR bit D02 (MASTER MODE), all output synchronization functions are independent of analog input activity. The maximum sync event rate for the outputs is 125 kHz. The possible input and output sync combinations are shown in Table 4.7.3-1. The output modes alone are shown in Table 4.8.3-1.

4.8.4 Self-Testing the VMIVME-3114 Board

The analog outputs can be monitored through the ADC to provide a closed loop self-test of the VMIVME-3114 Board. ICR control bits D11 and D12 select the self-test mode, as shown in Table 4.5.4-1. The self-test modes permit the analog outputs to be monitored instead of Analog Input Channels 03 and 07. All other control functions are unaffected, and the closed loop test configuration can be applied in both the on-line and off-line analog output modes.

4.9 BUS INTERRUPTER

Interrupts are available to inform a host CPU of progress in the analog input and output scans. There are two interrupt channels. Channel 0 is for the analog input scan. It can do interrupts when the input scan crosses from buffer A to B and vice-versa. Channel 1 is the analog output end-of-buffer interrupt.

Table 4.8.1-1. Output Control Register (OCR)

D00 to D03 .... OUTPUT BLOCK SIZE

D03	D02	D01	D00	DATA BLOCK SIZE (HEX)
0	0	0	0	2 WORDS
0	0	0	1	4
0	0	1	0	8
0	0	1	1	10
0	1	0	0	20
0	1	0	1	40
0	1	1	0	80
0	1	1	1	100
1	0	0	0	200
1	0	0	1	400
1	0	1	0	800
1	0	1	1	1000
1	1	0	0	2000
1	1	0	1	4000
1	1	1	0	8000
1	1	1	1	10000

D04 to D07 .... OUTPUT CLOCKING RATE

D07	D06	D05	D04	CLOCKING RATE (Samples per second, each output)
0	0	0	0	125,000 Hz
0	0	0	1	62,500 Hz
0	0	1	0	31,250 Hz
0	0	1	1	15,625 Hz
0	1	0	0	7,813 Hz
0	1	0	1	3,906 Hz
0	1	1	0	1,953 Hz
0	1	1	1	977 Hz
1	0	0	0	488 Hz
1	0	0	1	244 Hz
1	0	1	0	122 Hz
1	0	1	1	61.0 Hz
1	1	0	0	30.5 Hz
1	1	0	1	15.26 Hz
1	1	1	0	7.63 Hz
1	1	1	1	3.81 Hz

(D08 to D15 are not used).

M3114/T4.8.1-1

Table 4.8.3-1. Analog Output Synchronization Modes

CSR bits D09, D02	Mode	Controlling Sync Event	Is M/S DA SYNC Driven?
0 0	Asynchronous (free running)	On-board rate generator	NO
0 1	Async. Master	On-board rate generator	YES
1 0	Slave	M/S DA SYNC input	NO
1 1	Ext. Sync Master	Falling edge on EXT DA SYNC input or CSR bit D11	YES

M3114/T4.8.3-1

As shown in Table 4.1-1, each channel has a Control Register and a Vector Register. The Control Registers determine if an interrupt channel is enabled, and at what level the interrupt request will be made. All interrupts are disabled unless programmed. The Vector Registers hold the eight-bit vectors delivered to the host CPU during the interrupt acknowledge cycles. Vectors are also known as "status/IDs". The internal layout of these registers is shown in Table 4.9-1.

4.9.1 Interrupt Control Registers

The Interrupt Control Registers control the interrupt level, as well as enabling or disabling the interrupt. The ICRs are preset to 00 after a board reset or system reset. The exact functions of the ICRs' bits are shown in Table 4.9.1-1.

4.9.2 Interrupt Vector Registers

The contents of an Interrupt Vector Register are supplied as a byte (D00 through D07) on the data bus during an interrupt acknowledge cycle. The meaning of this byte is determined by the interrupt handler device. After a reset, the IVRs are preset to 0F HEX.

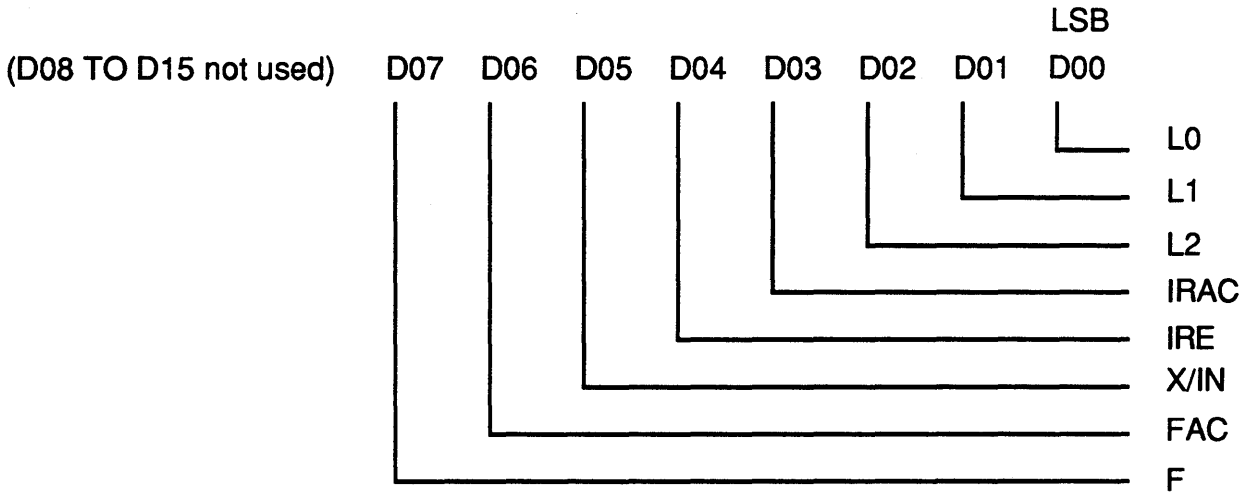
4.10 DIGITAL I/O PORTS

Two independent 8-bit digital I/O ports are controlled through the Digital I/O Ports Register. The lower byte (D00 to D07) of the register represents PORT 0, and the upper byte (D08 to D15) represents PORT 1. Logical sense (polarity) is preserved, and a "one" in the register represents a "one", or HIGH level, at the I/O port. Each port can be controlled independently as either an input or an output port by using byte-wide (D8) data transfers. Digital inputs are latched before reading.

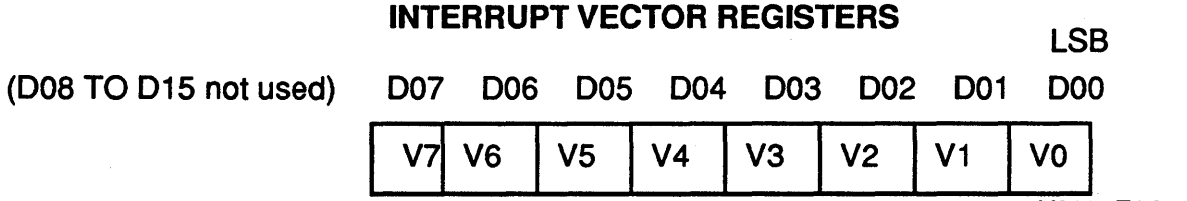
Directions of the digital ports are controlled by D12 (DIRECTION 0 OUT) and D13 (DIRECTION 1 OUT) in the CSR. Setting D12 or D13 configures the corresponding port as an output; clearing the bit configures the port as an input. Output ports, when read, return the last value written to them.

Table 4.9-1. Interrupt Registers Organization

INTERRUPT CONTROL REGISTERS



INTERRUPT VECTOR REGISTERS



M3114/T4.9-1

Table 4.9.1-1. Interrupt Control Register Functions

INTERRUPT LEVEL (L2, L1, L0, Bits D02, D01, D00):

Determines the level at which an interrupt will occur:

REGISTER BIT			
L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

INTERRUPT ENABLE (IRE, Bit D04):

When this bit is set HIGH, the bus interrupt is enabled; the interrupt is disabled if IRE is LOW.

INTERRUPT AUTO-CLEAR (IRAC, Bit D03):

If the IRAC bit is set HIGH, the interrupt-enable bit (IRE) is cleared during the interrupt acknowledge cycle which responds to the request. The IRE bit must then be set HIGH again to enable the next interrupt.

EXTERNAL/INTERNAL (X/IN, Bit D05):

This control bit MUST be cleared LOW at all times.

FLAG (F, Bit D07):

This control bit has no effect on the operation of the board, and is available for use by the controlling processor as a utility flag.

FLAG AUTO-CLEAR (FAC, Bit D06):

If "FAC" is set HIGH, the flag bit "F" is automatically cleared during an interrupt acknowledge cycle.

4.11 RESET CONFIGURATIONS

4.11.1 System and Power-On Reset

At initial application of power, or after a system reset operation, the VMIVME-3114 Board is configured as follows:

a. Buffer access .....Disabled
b. Data Buffers (VME).....Input Buffer A, Output Buffer 0
c. Buffer size, Analog In .....8 Words
d. Buffer size, Analog Out .....2 Words
e. Scanning rate .....Maximum
f. Scanning mode.....Continuous
g. Synchronization mode.....Asynchronous (nonmaster)
h. Self-test.....Disabled
i. Digital ports.....Input ports
j Analog outputs .....Off-line (disconnected)
k. LED indicator.....ON

4.11.2 Software Reset

A program controlled reset occurs when CSR bit D03 is set, and all power-on reset defaults are invoked. D03 clears automatically when reset has been completed.

4.12 APPLICATION EXAMPLE

4.12.1 Definition of Board Register Offsets

The example code ("x3114.c") is provided with a header file ("x3114.h") that demonstrates one method of defining Board Registers as offsets in a structure. This method allows the same structure to be used in accessing different boards by defining multiple pointers to this structure and initializing them to point to different boards. These pointer values are system and processor dependent and require knowledge of the user's particular system. The definitions stated here are for a single board CPU in a VMEbus chassis with a resident debug monitor. Figure 4.12.1-1 is the header file. Figure 4.12.1-2 is the C source code listing.

4.12.2 Definition of Board Buffer Offsets

The header file ("x3114.h") also defines the board buffers as a separate structure that consists of two arrays for analog inputs and outputs. The analog input buffer is defined as a two-dimensional array because the channel data is stored consecutively from Channel zero to Channel seven at the programmed scan rate and repeated to the programmed buffer size. Defining the buffer in this

```
/*  VMIVME-3114 ANALOG TO DIGITAL, DIGITAL TO ANALOG, AND DIO BOARD */

struct vmivme_3114_reg {
  unsigned  short   bid;        /* Board ID     (2 words)    */
  unsigned  short   bidx;       /*     2nd word is xxxx      */
  unsigned  short   csr;        /* Control Status Register   */
  unsigned  short   unused_1;   /* unused register address   */
  unsigned  short   ssr;        /* Scan    Status Register   */
  unsigned  char    port1;      /* Digital IO ports 1        */
  unsigned  char    port0;      /* Digital IO ports 0        */
  unsigned  short   icr;        /* Input  Control  Register  */
  unsigned  short   ocr;        /* Output Control  Register  */
  unsigned  short   ici;        /* Interrupt Control Input   */
  unsigned  short   ioc;        /* Interrupt Control Output  */
  unsigned  short   unused_2;   /* unused register address   */
  unsigned  short   unused_3;   /* unused register address   */
  unsigned  short   ivi;        /* Interrupt Vector  Input   */
  unsigned  short   ivo;        /* Interrupt Vector  Output  */
};

struct vmivme_3114_buf {
  unsigned short adc3114[0x2000][0x8];  /* adc buff is a 2D array */
  unsigned short dac3114[0x10000];      /* dac buff is a 1D array */
};

typedef struct vmivme_3114_reg Reg3114;    /* 3114 register types  */
typedef struct vmivme_3114_buf Buf3114;    /* 3114 ram buff types  */

/*  Board Control Register bit definitions and codes */

#define    BOARD_ID             0x000A      /* Board ID code (word) */

#define    FAIL_LED_OFF         0x8000      /* CSR control bits */
#define    ANALOG_OUTPUTS_ON    0x4000
#define    PORT1_DIR_OUT        0x2000
#define    PORT0_DIR_OUT        0x1000
#define    ADVANCE_OUTPUT_ADDR  0x0800
#define    OUTPUT_SINGLE_SCAN   0x0400
#define    OUTPUT_SYNCRONOUS    0x0200
#define    SEL_OUTPUT_BUFF_1    0x0100
#define    ADVANCE_INPUT_ADDR   0x0080
#define    INPUT_SINGLE_SCAN    0x0040
#define    INPUT_SYNCRONOUS     0x0020
#define    SEL_INPUT_BUFF_B     0x0010
#define    SOFTWARE_RESET       0x0008
#define    MASTER_MODE          0x0004
#define    DIS_OUTPUT_SCAN      0x0002
#define    ENABLE_BUFFERS       0x0001
```

M3114/F4.12.1-1/1

Figure 4.12.1-1. Program Example - 3114 Header File

```
#define    INPUTS_ARE_DIFF      0x0080      /* SSR status bits */
#define    BINARY_CODING        0x0040
#define    DAC_SCAN_COMPLETE    0x0020
#define    DAC_SCAN_BUFF_A      0x0010
#define    DAC_SYNC_ENABLED     0x0008
#define    ADC_SCAN_COMPLETE    0x0004
#define    ADC_SCAN_BUFF_A      0x0002
#define    ADC_SYNC_ENABLED     0x0001

#define    TEST_MODE_3          0x1800      /* ICR & OCR bit codes   */
#define    TEST_MODE_2          0x1000      /* not all bits apply to */
#define    TEST_MODE_1          0x0800      /* both ocr and icr regs */
#define    TEST_MODE_OFF        0x0000
#define    GAIN_16              0x0700
#define    GAIN_8               0x0300
#define    GAIN_4               0x0200
#define    GAIN_2               0x0100
#define    GAIN_1               0x0000
#define    SCAN_3               0x00F0
#define    SCAN_7               0x00E0
#define    SCAN_15              0x00D0
#define    SCAN_30              0x00C0
#define    SCAN_61              0x00B0
#define    SCAN_122             0x00A0
#define    SCAN_244             0x0090
#define    DIS_INPUT_SCAN       0x0080      /* <- ICR only */
#define    SCAN_488             0x0080
#define    SCAN_977             0x0070
#define    SCAN_1953            0x0060
#define    SCAN_3906            0x0050
#define    SCAN_7813            0x0040
#define    SCAN_15625           0x0030
#define    SCAN_31250           0x0020
#define    SCAN_62500           0x0010
#define    SCAN_125000          0x0000
#define    BUFF_64K             0x000F
#define    BUFF_32K             0x000E
#define    BUFF_16K             0x000D
#define    BUFF_8K              0x000C
#define    BUFF_4K              0x000B
#define    BUFF_2K              0x000A
#define    BUFF_1K              0x0009
#define    BUFF_512             0x0008
#define    BUFF_256             0x0007
#define    BUFF_128             0x0006
#define    BUFF_64              0x0005
#define    BUFF_32              0x0004
#define    BUFF_16              0x0003
#define    BUFF_8               0x0002
#define    BUFF_4               0x0001
#define    BUFF_2               0x0000
```

M3114/F4.12.1-1/2

Figure 4.12.1-1. Program Example - 3114 Header File (Continued)

```
#define    FLAG_BIT              0x80        /*  BIM control bits */
#define    FLAG_AUTO_CLEAR       0x40
#define    EXTERNAL_VECTOR       0x00        /* always 0 (see manual) */
#define    INTERRUPT_ENABLE      0x10
#define    INTR_AUTO_CLEAR       0x08
#define    REQUEST_LEVEL_7       0x07
#define    REQUEST_LEVEL_6       0x06
#define    REQUEST_LEVEL_5       0x05
#define    REQUEST_LEVEL_4       0x04
#define    REQUEST_LEVEL_3       0x03
#define    REQUEST_LEVEL_2       0x02
#define    REQUEST_LEVEL_1       0x01
#define    INTERRUPTS_OFF        0x00
```

M3114/F4.12.1-1/3

Figure 4.12.1-1. Program Example - 3114 Header File (Concluded)

```
/*
**  VMIVME-3114 application example:
**
**  > Set up AO channel 0 for full scale ramp output at 125khz.
**  > Set up AO channel 1 for +5 volt square wave at 125khz.
**  > set up DIO port 0 as an input port.
**  > set up DIO port 1 as an output port.
**  > set up AI to scan all channels at 125khz into 64k buffer.
**  > read input port, write input to output port, and display
**    digital data in and full buffer average of each analog
**    input channel to crt. Loop forever ...
*/

#include  <stdio.h>
#include  "x3114.h"


/*
**  These cpu dependent defines for short io and
**  standard VMEbus space are for a Force cpu-33.
*/

#define   VME_SHORT_IO    0xfbff0000
#define   VME_STANDARD    0xfb000000


/*
**  declare global board and buffer pointers to 3114
**
**    registers begin at offset zero in short io space
**    buffers begin at offset zero in standard space
*/

Reg3114 * board   = (( Reg3114 * )( VME_SHORT_IO + 0x00 ));
Buf3114 * buffer  = (( Buf3114 * )( VME_STANDARD + 0x00 ));


/*
**  declare global variables for example
*/

unsigned  char  dio;              /* dio data variable */

unsigned  short soft_csr,         /* memory image of CSR */
                soft_ssr,         /* memory image of SSR */
                average[ 8 ];     /* channel avg'ing array */

unsigned  int   sum,              /* averaging accumulator */
                loop,             /* general loop variable */
                chan;             /* adc chan ptr variable */
```

M3114/F4.12.1-2/1

Figure 4.12.1-2. Program Example - C Source Code

```
main()
{
  printf("\r\n\n");      /* cr,lf,lf */

  printf("VMIVME-3114 application example ... ");

  /*
  **  initialize board registers and misc var's
  */

  soft_csr = ( FAIL_LED_OFF | ANALOG_OUTPUTS_ON |
                      PORT1_DIR_OUT | ENABLE_BUFFERS );

  board->csr = ( SOFTWARE_RESET | DIS_OUTPUT_SCAN );
  board->csr = soft_csr;


  board->ocr = ( SCAN_125000 | BUFF_64K );

  board->icr = ( DIS_INPUT_SCAN );
  board->icr = ( SCAN_125000 | BUFF_64K );


  /*
  **  init and fill output buffer 1 for 0 to +5 square wave
  **
  **    assumes bipolar configuration of +-10v
  */

  board->csr = ( soft_csr | SEL_OUTPUT_BUFF_1 );

  for( loop = 0; loop < 0x10000; loop++ ) {
    if( loop & 0x1 )
      buffer->dac3114[ loop ] = 0xc00;      /* +5.000 */
    else
      buffer->dac3114[ loop ] = 0x800;      /*  0.000 */
  }

  /*
  **  init and fill output buffer 0 for full scale ramp
  **
  **    assumes bipolar configuration of +-10v
  */

  board->csr = soft_csr;

  for( loop = 0; loop < 0x10000; loop++ ) {
    buffer->dac3114[ loop ] = ( loop & 0xfff );
  }
```

M3114/F4.12.1-2/2

Figure 4.12.1-2. Program Example - C Source Code (Continued)

```
  /*
  **  setup crt with channel info to print data beneath
  */

  printf("\r\nDIN CH_0 CH_1 CH_2 CH_3 CH_4 CH_5 CH_6 CH_7 \r\n");

  for( ;; ) {     /* begin forever loop */

    /*
    **  read data from port 0 and write to port 1
    */

    dio = board->port0;
    board->port1 = dio;

    /*
    **  get average of all 8 channels from input buffer A or B
    */

    soft_ssr = board->ssr;
    if( soft_ssr & ADC_SCAN_BUFF_A ) {
      board->csr = ( soft_csr | SEL_INPUT_BUFF_B );
    }
    else {
      board->csr = ( soft_csr );
    }

    for( chan = 0; chan < 8; chan++ ) {
      for( loop = sum = 0;  loop < 0x2000; loop++ ) {
        sum += buffer->adc3114[ loop ][ chan ];
      }
      average[ chan ] = sum / 0x2000;
    }

    printf("\r%.2x  %.4X %.4X %.4X %.4X %.4X %.4X %.4X %.4X",
      dio, average[ 0 ], average[ 1 ], average[ 2 ], average[ 3 ],
           average[ 4 ], average[ 5 ], average[ 6 ], average[ 7 ] );

  } /* loop forever */

} /* end main */
```

M3114/F4.12.1-2/3

Figure 4.12.1-2. Program Example - C Source Code (Concluded)

manner allows the user to access blocks of eight channels or allows random access to multiple occurrences of a particular channel. The analog output buffer is a single-dimensional array that is fed in consecutive order to an analog output channel at the selected update (scan) rate.

4.12.3 Example Code Initialization

The example code ("x3114.c") initializes the VMIVME-3114 Board to the following modes of operation with the VMIVME-3114 in continuous asynchronous scan mode:

a. Analog output zero for full-scale ramp updating at 125 kHz
b. Analog output one for positive 5 V square wave updating at 125 kHz
c. Digital port zero as an input port and digital port one as an output port
d. Analog inputs to be scanned at 125 kHz into a 64 K word buffer

4.12.4 Example Code Execution Summary

The example code ("x3114.c") demonstrates the following events in a forever loop. It reads digital input port zero and writes the data to digital output port one, demonstrating both reading and writing the digital input-output ports. It does a read from the Board Status Register and a test on the status to determine if analog input data should be read from input buffer "A" or "B". (In continuous asynchronous mode both input buffers are filled by first filling "A", then "B", then back to "A", etc.) It also shows manipulating the Control and Status Register to access buffer "A" or "B". A loop then averages a buffer of values for display to the video terminal, demonstrating analog input buffer checking and accessing.

4.12.5 Example Code Details

The soft definition of the Control and Status Register (CSR) and Scan Status Register (SSR) allows bit manipulation of these registers. These registers are word-only hardware registers. The compiler used to compile the example generates true 68020 bit manipulations which are done on a byte boundary. The soft registers are in memory and may be read as a word, bytewise manipulated, then written back as a word to the VMIVME-3114 Board Register.

The soft definitions also allow setting a base value and including other values in particular lines of code. The example shows initializing the soft CSR to FAIL_LED_OFF, ANALOG_OUTPUTS_ON, PORT1_DIR_OUT, and ENABLE_BUFFERS from constant values from the header file. Then in later lines of code for the buffer "A" or "B" access, the soft CSR can be combined (using OR) with SEL_INPUT_BUFF_B for buffer "B" or used as is to get buffer "A". This is done without changing the value of the soft CSR which maintains the basic setup for the VMIVME-3114.

SECTION 5
CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURE

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

a. Verify that the sections pertaining to theory and programming, Sections 3 and 4, have been reviewed and applied to system requirements.

b. Review Section 5.4 and Table 5.4-1 to verify that all factory installed jumpers are in place. To modify the board configuration, refer to Section 5.4.

c. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to Section 5.6 for connector descriptions.

d. Calibration has been performed at the factory. If recalibration may be required, refer to Section 5.5.

After the checklist above has been completed, the board can be installed in a VMEbus system. DO NOT install or remove the board with power applied. This board may be installed in any slot position, except Slot 1 which is usually reserved for the master processing unit.

****
* CAUTION *
****

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

5.4 OPERATIONAL CONFIGURATION

Control of the board address and I/O access mode are determined by field replaceable jumpers. Other jumpers control input and output ranges, two's complement data, and single-ended versus differential inputs. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all jumpers are shown in Figure 5.4-1 and in Table 5.4-1.

5.4.1 Factory Installed Jumpers

Each VMIVME-3114 Board is configured at the factory with the specific jumper arrangement shown in Table 5.4-1. The factory configuration establishes the following functional baseline for the VMIVME-3114 Board, and ensures that all essential jumpers are installed.

a. Control and Status Registers are located at board address 0004 HEX (Table 4.1-1) in the short I/O space, with both supervisory and nonprivileged access allowed.

b. Data Buffers are located at address 00 0000 HEX, with standard (A24) supervisory or nonprivileged data access (Address modifier code = 3D or 39 HEX). Block transfers are allowed (A.M. codes 3F and 3B HEX).

c. Eight single-ended analog input channels referenced to RETURN pins of P3.

d. ±10 V ranges for analog inputs and outputs.

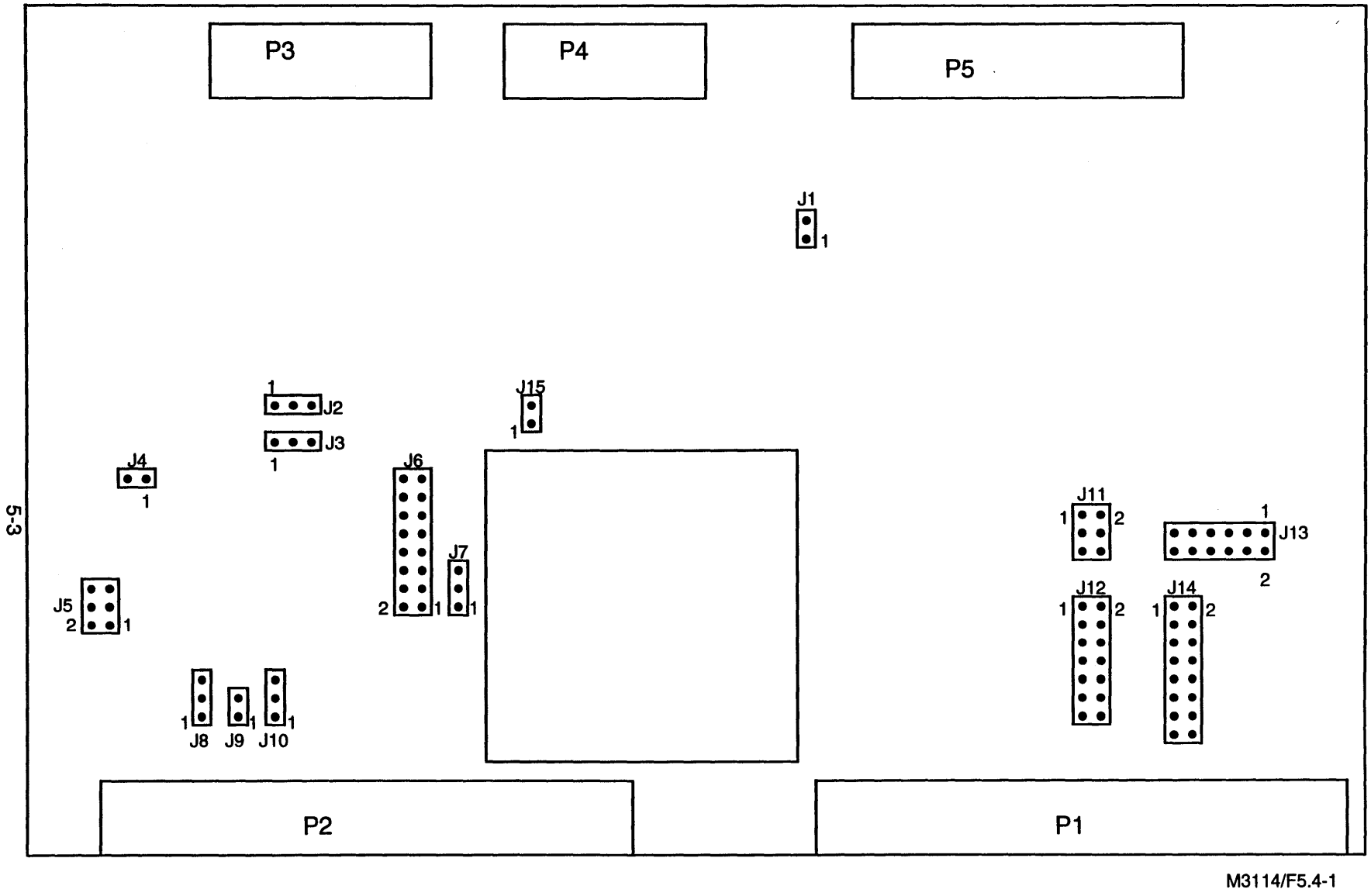


Figure 5.4-1. VMIVME-3114 Jumper Option Locations

Table 5.4-1. Programmable Jumper Functions

JUMPER IDENT	FUNCTION (Installed)	FACT CONFIG
J11-1,2	Short I/O Address Bit A05 = 0	Installed
J11-3,4	Short I/O Address Bit A06 = 0	Installed
J11-5,6	Short I/O Address Bit A07 = 0	Installed
J12-1,2	Short I/O Address Bit A08 = 0	Installed
J12-3,4	Short I/O Address Bit A09 = 0	Installed
J12-5,6	Short I/O Address Bit A10 = 0	Installed
J12-7,8	Short I/O Address Bit A11 = 0	Installed
J12-9,10	Short I/O Address Bit A12 = 0	Installed
J12-11,12	Short I/O Address Bit A13 = 0	Installed
J12-13,14	Short I/O Address Bit A14 = 0	Installed
J14-1,2	Short I/O Address Bit A15 = 0	Installed
J14-3,4	Short Nonpriv Access	Omitted (was installed)
J14-5,6	Short Superv or Nonpriv Access	Installed
J13-1,2	Buffer Address Bit A18 = 0	Installed
J13-3,4	Buffer Address Bit A19 = 0	Installed
J13-5,6	Buffer Address Bit A20 = 0	Installed
J13-7,8	Buffer Address Bit A21 = 0	Installed
J13-9,10	Buffer Address Bit A22 = 0	Installed
J13-11,12	Buffer Address Bit A23 = 0	Installed
J6-1,2	Buffer Address Bit A24 = 0	Installed
J6-3,4	Buffer Address Bit A25 = 0	Installed
J6-5,6	Buffer Address Bit A26 = 0	Installed
J6-7,8	Buffer Address Bit A27 = 0	Installed
J6-9,10	Buffer Address Bit A28 = 0	Installed
J6-11,12	Buffer Address Bit A29 = 0	Installed
J6-13,14	Buffer Address Bit A30 = 0	Installed
J6-15,16	Buffer Address Bit A31 = 0	Installed (was omitted)
J14-7,8	Buffer Standard Addressing*	Installed
J14-9,10	Allow Supervisory Block Transfers	Installed
J14-11,12	Allow Supervisory Data Transfers	Installed
J14-13,14	Allow Nonpriv. Block Transfers	Installed
J14-15,16	Allow Nonpriv. Data Transfers	Installed
J7-1,2	Buffer Standard Addressing*	Installed
J7-2,3	Buffer Extended Addressing*	Omitted
J1	Two's Complement Analog Input Data Coding	Omitted
J15	Single-ended Inputs	Installed
J4	Ext S.E. Input Returns Shorted to VME Ground	Omitted (was installed)
J5-1,2	Differential Inputs	Omitted

*J7 and J14 must select the same addressing mode. For example, remove the J14-7,8 shunt and put it over J7-2,3 for extended mode, and remove J7-1,2.

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Table 5.4-1. Programmable Jumper Functions (Concluded)

JUMPER IDENT.	FUNCTION (INSTALLED)	FACT. CONFIG.
J5-3,4	S.E. Reference Ext. Input Return (Note 1)	Installed
J5-5,6	S.E. Reference to VME Ground (Note 1)	Omitted
J8-2,3	Analog Inputs 20 V FSR (Note 2)	Installed
J8-1,2	Analog Inputs 5 V FSR	Omitted
J9	Analog Inputs 5 V or 10 V FSR	Omitted
J10-1,2	Analog Inputs Unipolar	Omitted
J10-2,3	Analog Inputs Bipolar	Installed
J2-1,2	Analog Outputs 5 V FSR (Note 3)	Omitted
J2-2,3	Analog Outputs 10 V FSR (Note 3)	Omitted
J3-1,2	Analog Outputs Unipolar	Omitted
J3-2,3	Analog Outputs Bipolar	Installed

NOTES:
1. EXT. S.E. Returns 940 Ω to VME ground if both J5-3,4 and J5-5,6 are in.
2. FSR = Full-Scale Range.
3. Omit J2 entirely for 20 V FSR.

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5.4.2 Board Location in Short I/O Space

All Control and Status Registers are located within the VME short I/O space (Refer to Sections 3 and 4). Jumper blocks J11, J12, and J14 permit the VMIVME-3114 Board to be located on any 16-word short I/O address boundary.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in jumper blocks J11, J12, and J14, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A05 has a weight of 32-byte locations. Short supervisory access is selected by installing jumper J14-3 and 4. Short nonprivileged access is selected by omitting the jumper. Installation of the jumper in the J14-5 and 6 position produces response to either short privileged or short nonprivileged access. For example, the typical jumper arrangement shown in Table 5.4.2-1 would produce a short I/O board address of 8F80 HEX, with short supervisory access.

Table 5.4.2-1. Typical Board Address Selection

JUMPERS J11,12,14 CONFIGURATION
for Short Supervisory Access
at Address 8F80 (HEX)

Position	Addr Bit	State (Note 1)
J11-1,2	A05	SHORTED
J11-3,4	A06	SHORTED
J11-5,6	A07	OPEN
J12-1,2	A08	OPEN
J12-3,4	A09	OPEN
J12-5,6	A10	OPEN
J12-7,8	A11	OPEN
J12-9,10	A12	SHORTED
J12-11,12	A13	SHORTED
J12-13,14	A14	SHORTED
J14-1,2	A15	OPEN
J14-3,4	AM2	OPEN
J14-5,6	AM2	OPEN (Note 2)

Notes:
1. SHORTED = "0", OPEN = "1"
2. Installing J14-5,6 produces response to either supervisory or nonprivileged access.

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5.4.3 Data Buffer Location

Jumper blocks J13 and J6 permit the data buffers to be located on any 20000 HEX word boundary within the VMEbus standard or extended address space. The buffer address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in jumper blocks J13 and J6, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A18 has a weight of 40000 HEX bytes.

Standard A24 addressing is selected by installing a jumper at J7-1,2; extended A32 addressing is selected by installing a jumper at J7-3,4. The buffer access mode, or address modifier code, can be controlled with jumper block J14. Any combination of the SUPERVISORY/NONPRIV. and block/single data accesses may be enabled. A24 and A32 addressing are mutually exclusive.

5.4.4 Data Coding

The coding of analog input data and analog output data is controlled with jumper J1. Two's complement coding is selected by installing jumper J1; binary or offset binary coding is selected by removing the jumper.

5.4.5 Analog Input Configuration

Analog inputs can be configured for either single-ended or differential operation with jumpers J15, J4, and J5, as shown in Table 5.4.6-1. In the single-ended configuration, all eight input channels are active and can be referred either to the VMIVME-3114 internal signal return, or to an external return for pseudo-differential operation.

For differential operation, input Channels 4 through 7 become the LOW (negative) references for input Channels 0 through 3, respectively.

5.4.6 Analog Input Range Selection

Analog inputs for the VMIVME-3114 Board can be jumper-programmed for any of the voltage ranges shown in Table 5.4.6-1.

5.4.7 Analog Output Range Selection

The analog output channels can be jumper-programmed for any of the voltage ranges shown in Table 5.4.6-1.

Table 5.4.6-1. Analog Input and Output Range Selection

ANALOG INPUT RANGE

INPUT RANGE	JUMPERS INSTALLED		
0 to +5 V	J8-1,2	J9	J10-1,2
0 to +10 V	(Omit J8)	J9	J10-1,2
±2.5 V	J8-1,2	J9	J10-2,3
±5 V	(Omit J8)	J9	J10-2,3
±10 V	J8-2,3		J10-2,3

ANALOG OUTPUT RANGE

OUTPUT RANGE	JUMPERS INSTALLED	
0 to +5 V	J2-1,2	J3-1,2
0 to +10 V	J2-2,3	J3-1,2
±2.5 V	J2-1,2	J3-2,3
±5 V	J2-2,3	J3-2,3
±10 V	(Omit J2)	J3-2,3

SINGLE-ENDED/DIFFERENTIAL COMBINATIONS

CONFIGURATION	JUMPERS INSTALLED		
Differential	J4*	J5-1,2	
Single-Ended Int. Gnd. Ref.	J4*	J5-5,6	J15
Single-Ended Ext. Gnd. Ref.		J5-3,4	J15

*J4 may be installed to ground the "return" pins of the P3 connector, through a 470 Ω , 1/8 Watt resistor.

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5.5 CALIBRATION

Before delivery from the factory, the VMIVME-3114 Board is fully calibrated and conforms to all specifications listed in Section 2. Should recalibration be required, refer to Sections 5.5.1 through 5.5.3, and perform the indicated calibration procedures in the order shown. The locations of all adjustments and test points are shown in Figure 5.5-1.

5.5.1 Equipment Required

a. Digital Voltmeter (DVM)	1.000 and 10.000 VDC ranges; 5 or more digits; 0.005 percent of reading measurement accuracy; 10 MΩ minimum input impedance.
b. Chassis	VMEbus backplane or equivalent, with J1 and J2 connectors, a CPU with a monitor or debug program, 5.0 VDC, power supply. One slot allocated for testing the VMIVME-3114 Board.
c. Extender board	VMEbus extender board.

CAUTION

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.5.2 Analog Outputs Calibration Procedure

a. Restore all program jumpers to the factory configuration, as described in Section 5.4. Locate the control registers and the data buffers at locations which are compatible with the VME operating system which will be used for the calibration. Remove the programming jumper from J1 (select offset binary coding).

b. Install the VMIVME-3114 Board on an extender board in the VMEbus chassis.

c. Apply power to the backplane. Allow a minimum warm-up interval of ten minutes before proceeding.

d. Connect the digital voltmeter between TP3 (+) and TP1 (-).

e. Write the following data to the indicated board relative short I/O addresses (indicated address and data values are hexadecimal):

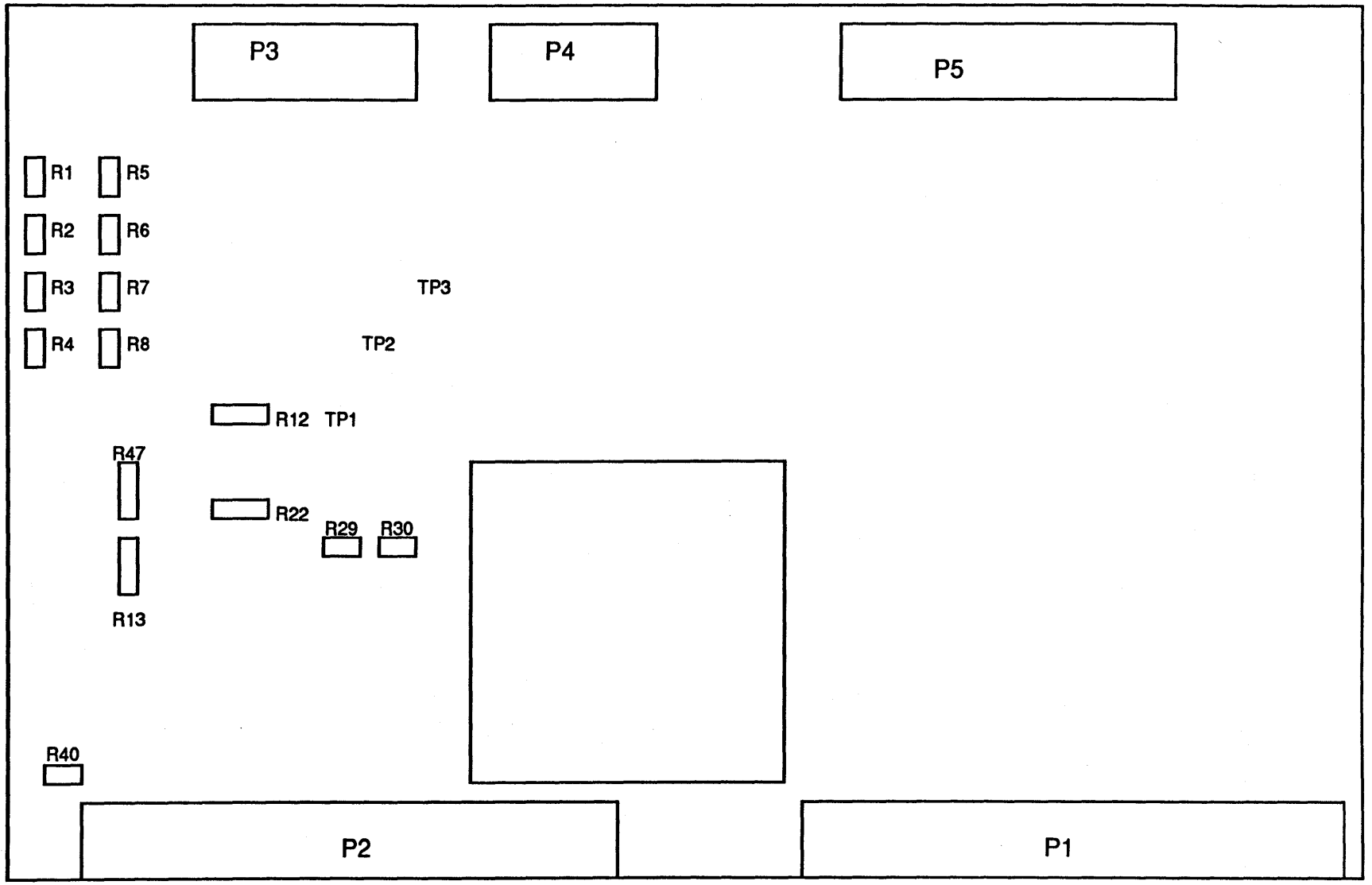

Figure 5.5-1. VMIVME-3114 Test Points and Adjustments

ADDRESS	DATA	REGISTER	MODE
0004	C001	CSR	Outputs enabled, continuous scanning, select buffer 0
000E	00F0	OCR	Minimum scan rate, minimum block size

f. Write the data value 0800 HEX (zero output) to the first four word locations in Analog Output Buffer 0.

g. Adjust potentiometer R12 for a digital voltmeter indication of 0.0000 VDC ±0.0005 VDC.

h. Write the data value 0FFF HEX (positive full scale) to the first four word locations in Analog Output Buffer 0.

i. Adjust potentiometer R47 for a digital voltmeter indication of +9.9951 VDC ±0.0010 VDC.

j. Write the data value 0000 HEX (negative full scale) to the first four word locations in Analog Output Buffers 0.

k. If the DVM does not indicate -10.0000 VDC ±0.0030 VDC, repeat steps f through j.

l. Move the positive (+) test lead of the DVM to TP2.

m. Write the data value C101 HEX to the CSR to select Channel 1.

n. Write the data value 0800 HEX (zero output) to the first four word locations in Analog Output Buffer 1.

o. Adjust potentiometer R22 for a digital voltmeter indication of 0.0000 VDC ±0.0005 VDC.

p. Write the data value 0FFF HEX (positive full scale) to the first four word locations in Analog Output Buffer 1.

q. Adjust potentiometer R13 for a digital voltmeter indication of +9.9951 VDC ±0.0010 VDC.

r. Write the data value 0000 HEX (negative full scale) to the first four word locations in Analog Output Buffer 1.

s. If the DVM does not indicate -10.0000 VDC ±0.0030 VDC, repeat steps n through r.

t. Calibration of the VMIVME-3114 analog outputs is completed. Remove the DVM test connections.

5.5.3 Analog Inputs Calibration Procedure

This procedure uses the analog output channels as references, so the outputs should have been recently calibrated in accordance with Section 5.5.2. It is useful but not necessary to have a routine which continuously displays the average for each input channel.

Allow the VMIVME-3114 to warm up for 10 minutes before calibrating. This procedure is for input and output ranges both set to ±10 V.

a. Remove the shunt (if any) from J1 to disable two's complement. Put a shunt on J4. Put a shunt on J5-3,4.

b. Write 00F0 HEX to the OCR (at offset 0E HEX).

c. Write C001 to the CSR (at offset 04).

d. Write 0FFE HEX to the first four locations of output buffer 0.

e. Write 170F to the ICR (at offset 0C HEX).

f. Adjust R30 to produce a reading of 0800 HEX on Channel 7.

g. Write 100F to the ICR (at offset 0C HEX).

h. Adjust R40 to produce a reading of 0FFE HEX on Channel 3.

i. Repeat steps e through h until no adjustment is necessary.

j. Write 000F to the ICR (at offset 0C HEX).

k. Short all of the input pins to RTN at the P3 connector.

l. Adjust the eight trim pots in the lower left corner of the board to produce readings of 0800 HEX for all eight channels.

m. Calibration is complete.

5.6 CONNECTOR DESCRIPTIONS

Electrical connections to the VMIVME-3114 Board are made through five connectors P1 through P5 (Figure 2.1-1). P1 and P2 are 96-pin DIN connectors, and have the pin configuration shown in Figure 5.6-1. P3, P4, and P5 are D-subminiature connectors, and have the pin configurations shown in Figure 5.6-2.

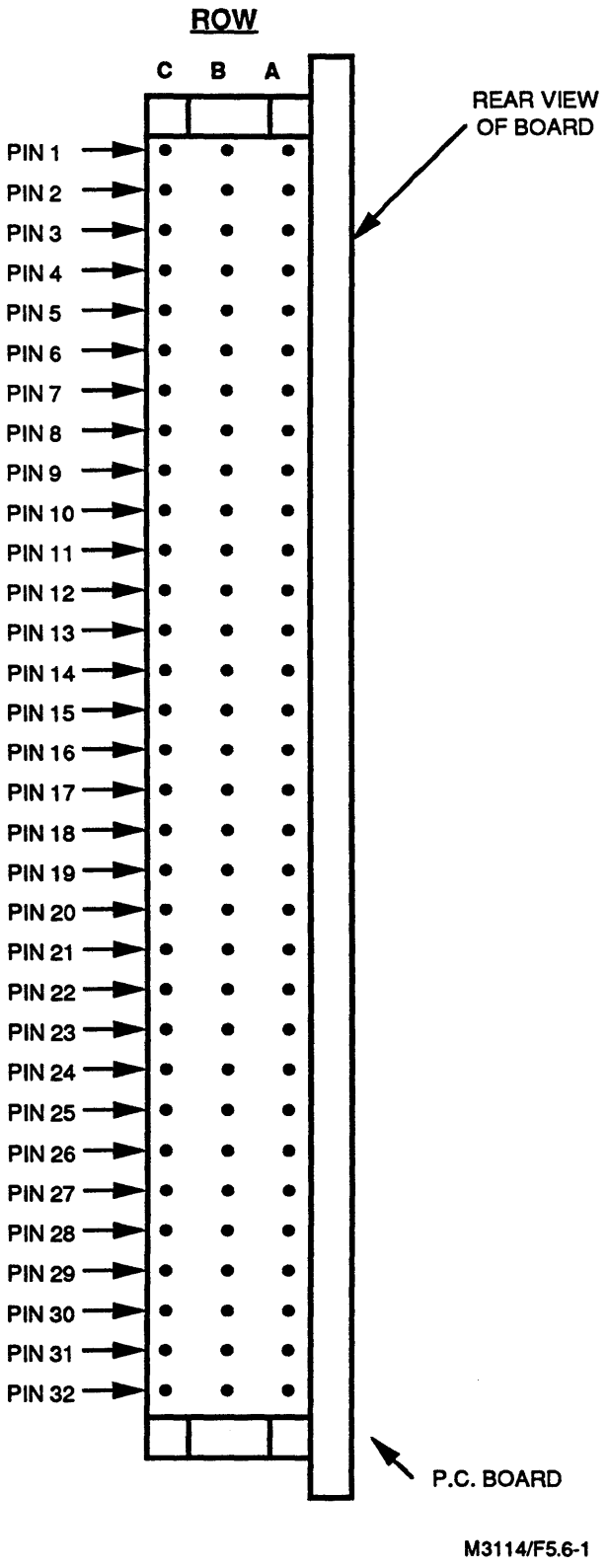

Figure 5.6-1. P1/P2 Connector - Pin Configurations

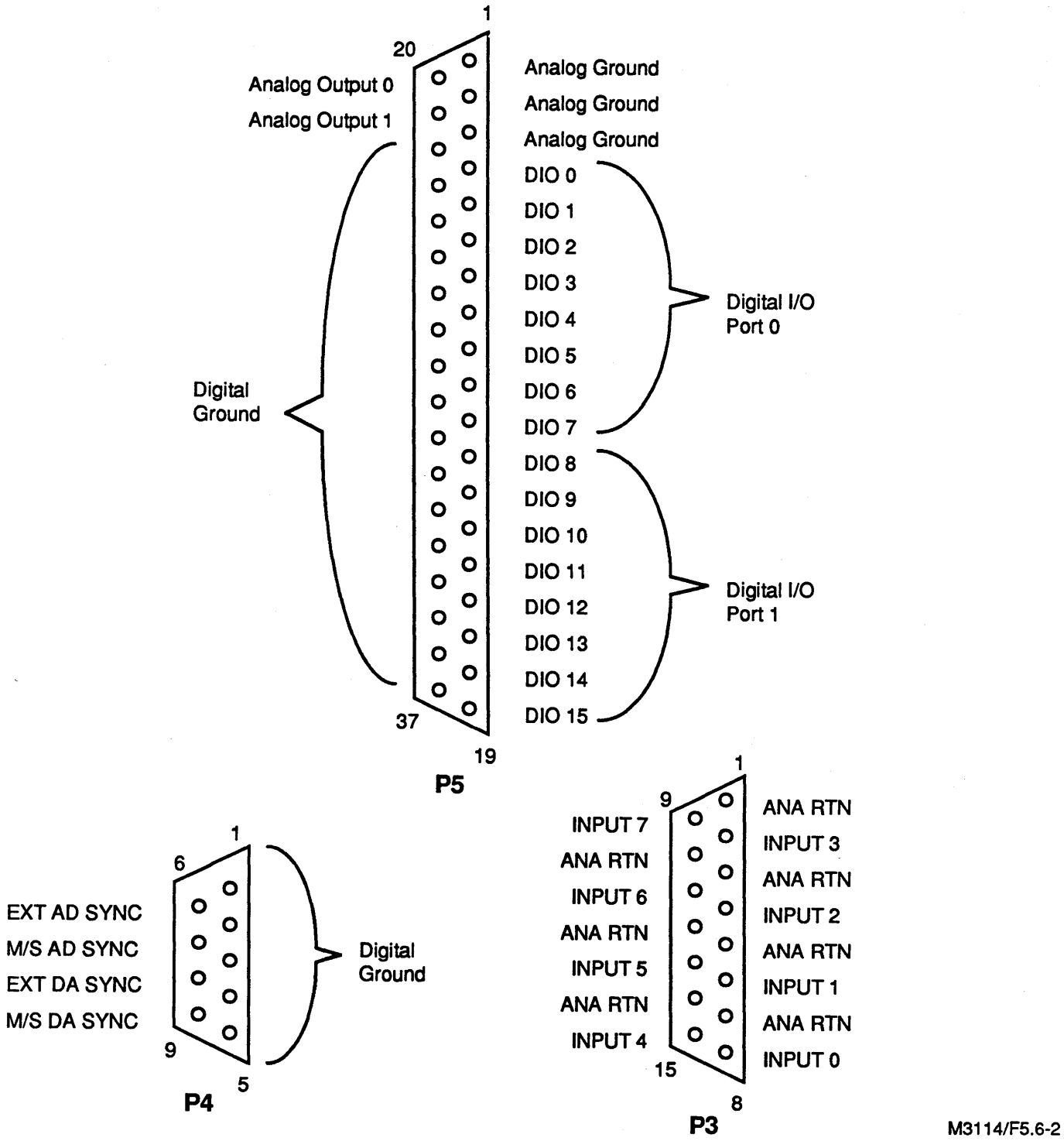

Figure 5.6-2. P3, P4, and P5 Connector Pin Configurations

P1 and P2 connect the board to the VMEbus backplane, and contain the address, data, and control lines necessary to control related VMEbus operations. P2 also provides the I/O pins necessary for external synchronization of the board. P2 user-pin assignments are listed in Table 5.6-1.

Analog inputs are connected to the VMIVME-3114 Board through a 15-pin D-subminiature connector P3 on the front panel. P3 pin assignments are listed in Table 5.6-2. Analog inputs can be jumper-configured as either 8 single-ended channels or four differential channels, as described in Section 5.4.

P5 is a 37-pin D-subminiature connector which provides I/O connections for two 8-bit digital ports and two analog output channels. P5 pin assignments are listed in Table 5.6-3.

External and master/slave synchronization I/O connections are available at the 9-pin D-subminiature connector P4, which is also connected internally to user-pins on the VMEbus backplane connector P2. Table 5.6-1 contains the pin assignments for P4. For external synchronization of any single board, connect the external TTL sync input to EXT AD SYNC for analog inputs, or to EXT DA SYNC for analog outputs. Make sure there is a DIGITAL GROUND connection between the input source and the VMIVME-3114. The board synchronizes on a HIGH-to-LOW transition of the external sync signal. Refer to Section 4 for synchronization programming instructions.

To synchronize multiple VMIVME-3114 Boards together, connect the M/S AD SYNC lines of all boards together for analog inputs, and the M/S DA SYNC lines of all boards together for analog outputs. The EXT AD SYNC and EXT DA SYNC inputs to the MASTER board can still be used to externally synchronize all boards simultaneously, or the MASTER can be programmed to run from its own clock.

Table 5.6-1. P2 User-Pin and P4 Signal Assignments

P2 USER-PIN SIGNAL ASSIGNMENTS

PIN	ROW A SIGNAL	ROW C SIGNAL
1	EXT AD SYNC	DIGITAL GND
2	M/S AD SYNC	DIGITAL GND
3	EXT DA SYNC	DIGITAL GND
4	M/S DA SYNC	DIGITAL GND
5	(NC)*	DIGITAL GND
6-32	(NC)	(NC)

* (NC) indicates no connection.

P4 SIGNAL ASSIGNMENTS

PIN	SIGNAL
1	DIGITAL GND
6	EXT AD SYNC
2	DIGITAL GND
7	M/S AD SYNC
3	DIGITAL GND
8	EXT DA SYNC
4	DIGITAL GND
9	M/S DA SYNC
5	DIGITAL GND

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Table 5.6-2. Analog Inputs Signal Assignments

P3 SIGNAL ASSIGNMENTS

PIN	S.E. SIGNAL	DIFF SIGNAL
8	ANA INPUT 0	ANA INPUT 0 HIGH (+)
7	ANA GND	ANA GND
6	ANA INPUT 1	ANA INPUT 1 HIGH (+)
5	ANA GND	ANA GND
4	ANA INPUT 2	ANA INPUT 2 HIGH (+)
3	ANA GND	ANA GND
2	ANA INPUT 3	ANA INPUT 3 HIGH (+)
1	ANA GND	ANA GND
15	ANA INPUT 4	ANA INPUT 0 LOW (-)
14	ANA GND	ANA GND
13	ANA INPUT 5	ANA INPUT 1 LOW (-)
12	ANA GND	ANA GND
11	ANA INPUT 6	AND INPUT 2 LOW (-)
10	ANA GND	ANA GND
9	ANA INPUT 7	ANA INPUT 3 LOW (-)

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Table 5.6-3. P5 Signal Pin Assignments

P5 SIGNAL ASSIGNMENTS PIN	SIGNAL
1	ANA GND
20	ANA OUT 00
2	ANA GND
21	ANA OUT 01
3	ANA GND
22	DIGITAL GND
4	PORT 0 D0
23	DIGITAL GND
5	PORT 0 D1
24	DIGITAL GND
6	PORT 0 D2
25	DIGITAL GND
7	PORT 0 D3
26	DIGITAL GND
8	PORT 0 D4
27	DIGITAL GND
9	PORT 0 D5
28	DIGITAL GND
10	PORT 0 D6
29	DIGITAL GND
11	PORT 0 D7
30	DIGITAL GND
12	PORT 1 D0
31	DIGITAL GND
13	PORT 1 D1
32	DIGITAL GND
14	PORT 1 D2
33	DIGITAL GND
15	PORT 1 D3
34	DIGITAL GND
16	PORT 1 D4
35	DIGITAL GND
17	PORT 1 D5
36	DIGITAL GND
18	PORT 1 D6
37	DIGITAL GND
19	PORT 1 D7

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SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The

defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

DOCUMENTATION EVALUATION FORM

VMIC welcomes your comments and suggestions.

Please return this form to:

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
(205) 880-0444
1-800-322-3616

Evaluation: Please rate the following areas on a scale of 1 to 5 (1 = Poor; 5 = Excellent).

DOCUMENT NO.: _____
REVISION DATE: _____

READABILITY	_____	ILLUSTRATIONS	_____
ORGANIZATION	_____	PROGRAMMING INFORMATION	_____
ACCURACY	_____	SPECIFICATIONS	_____
COMPLETENESS	_____	MAINTENANCE DIAGRAMS	_____

SPECIFIC PROBLEMS: **PAGE(s)**

( ) CLARIFICATION REQUIRED _____

( ) NOT ENOUGH INFORMATION GIVEN _____

( ) TYPOGRAPHICAL ERRORS _____

( ) TECHNICAL ERRORS (EXPLAIN): _____

_____

DOCUMENT USE: (check all that apply)

( ) HARDWARE	( ) SOFTWARE	( ) PRODUCT EVALUATION
( ) OPERATION	( ) MAINTENANCE	( ) TRAINING

ADDITIONAL COMMENTS: _____

_____

_____

_____

YOUR NAME: _____
TITLE: _____
COMPANY: _____
MAIL STOP: _____
STREET: _____
CITY, STATE, ZIP: _____
PHONE: _____

REVISIONS

REV.	DESCRIPTION	BY	DATE	APPR.
A	RELEASE PER ECO 91-0244	E.M.GREEN	10/23/91	M. SPANGLER
B	CHANGES PER ECO 91-0246	E.M.GREEN	10/23/91	M. SPANGLER
C	CHANGES PER ECO 91-0263	D. SMITH	10/23/91	M. SPANGLER
D	CHANGES PER ECO 91-0328	D. SMITH	12/20/91	M.C.L.
E	CHANGED PER ECO 92-0417	E.M. GREEN	10/15/92	T. Mauldy

INDEX

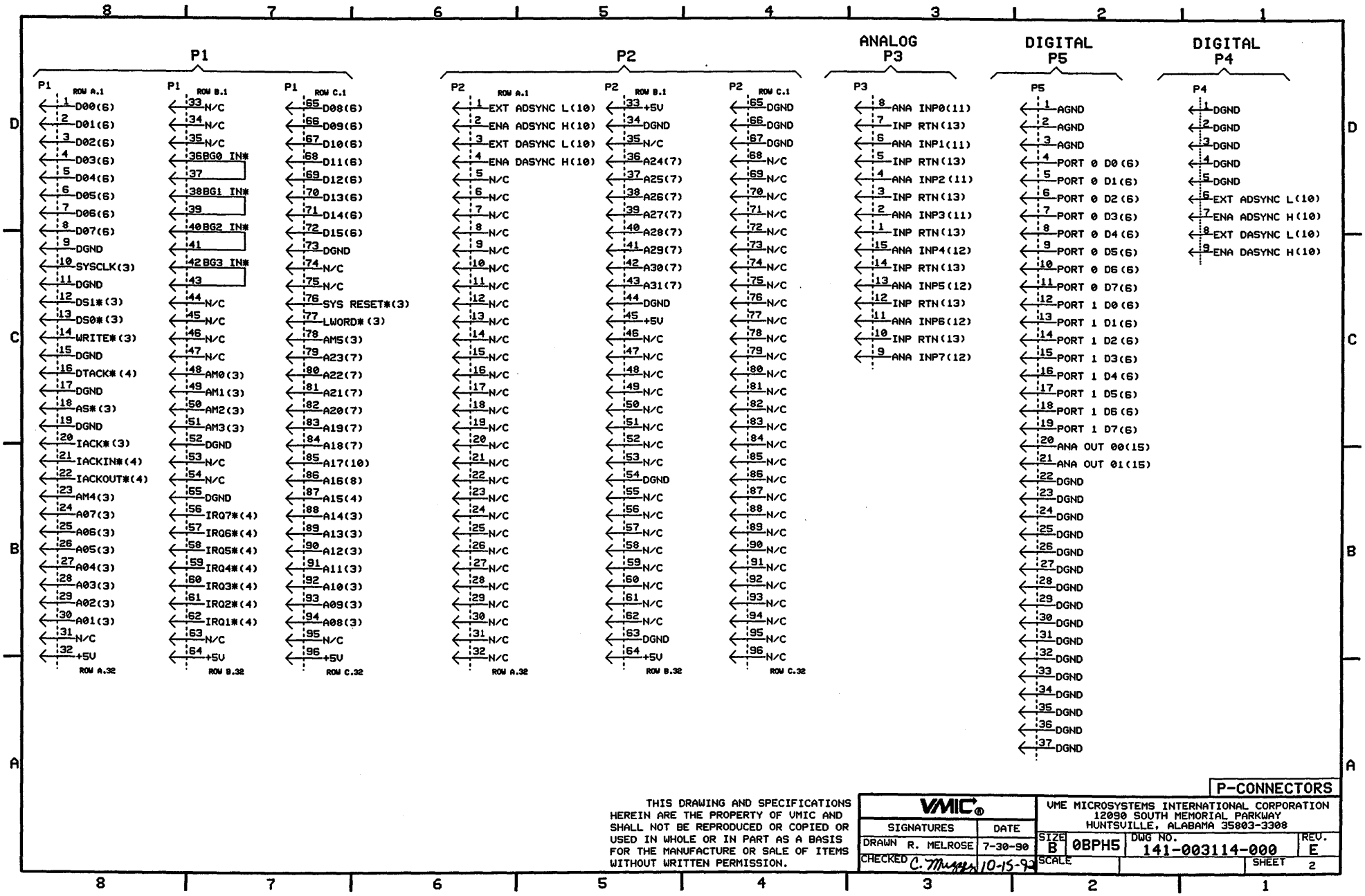
SIGNATURES		DATE
DRAWN	R. MELROSE	7-10-90
PROJ. ENG.	G. MEARES	1/10/91
ENG. MGR.	G. MEARES	1/10/91
PROD.	D. FOWLER	10/25/91
Q.A.	S. KEAGLE	10/28/91

COVER SHEET

VMIC®
12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803-3308
VME MICROSYSTEMS INTERNATIONAL CORPORATION

VMIVME-3114 SCHEMATIC

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 1

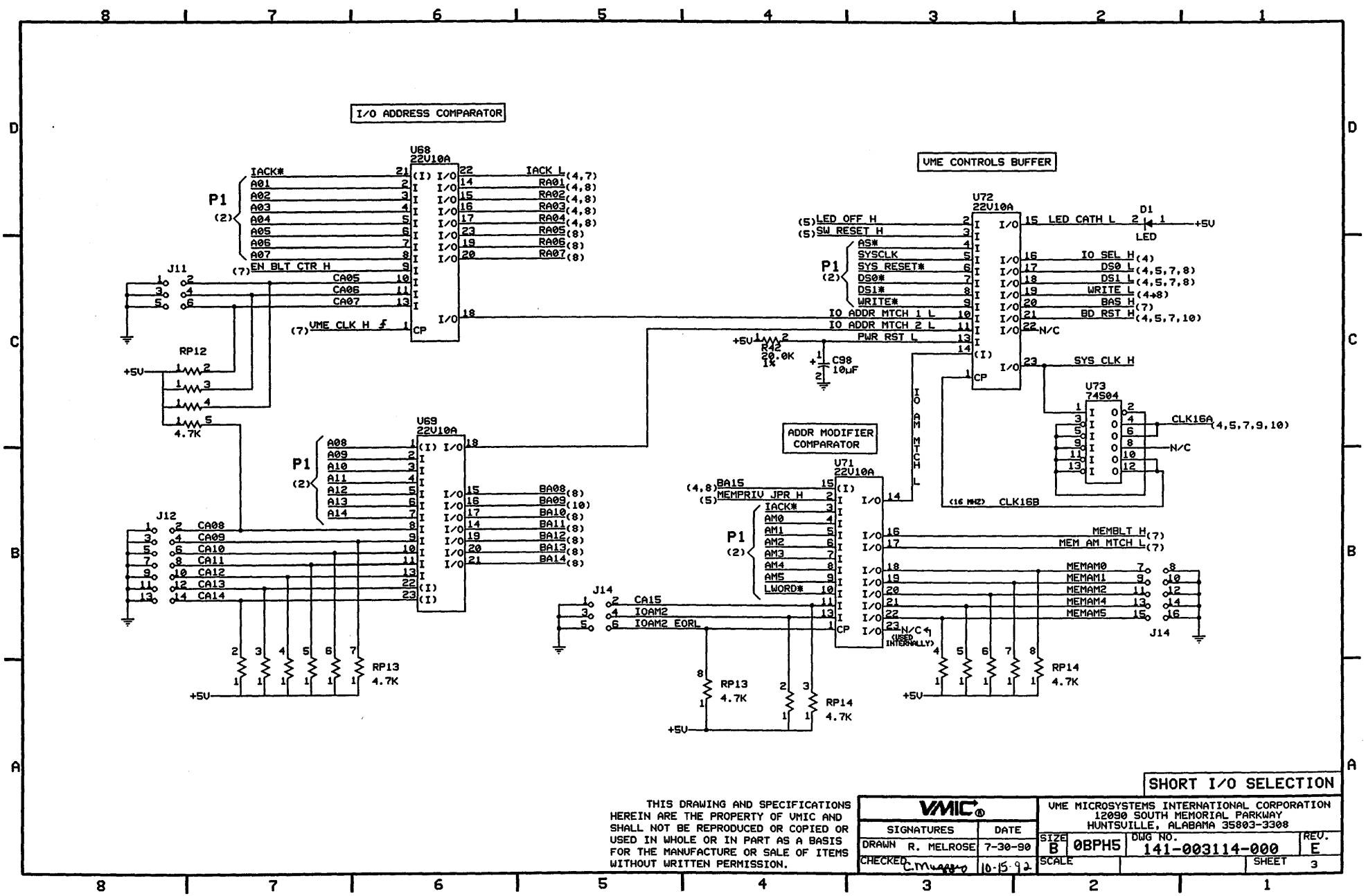


P-CONNECTORS

VMIC	
SIGNATURES	DATE
DRAWN R. MELROSE	7-30-90
CHECKED C. Mugge	10-15-90

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 2



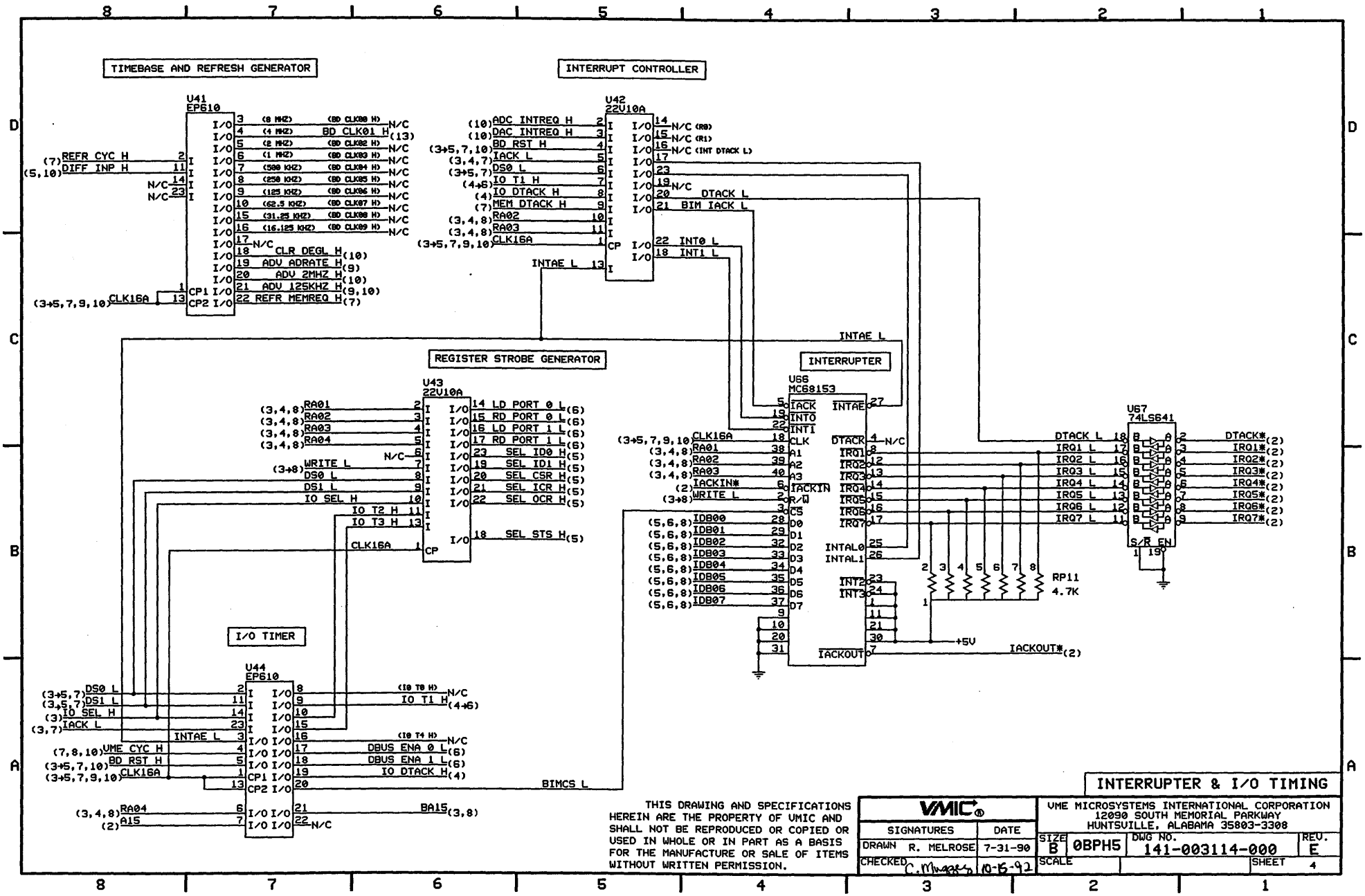
SHORT I/O SELECTION

VMIC	SIGNATURES	DATE
	DRAWN R. MELROSE	7-30-90
	CHECKED C.TYLER	10-15-92

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5	141-003114-000 E

SCALE | SHEET 3

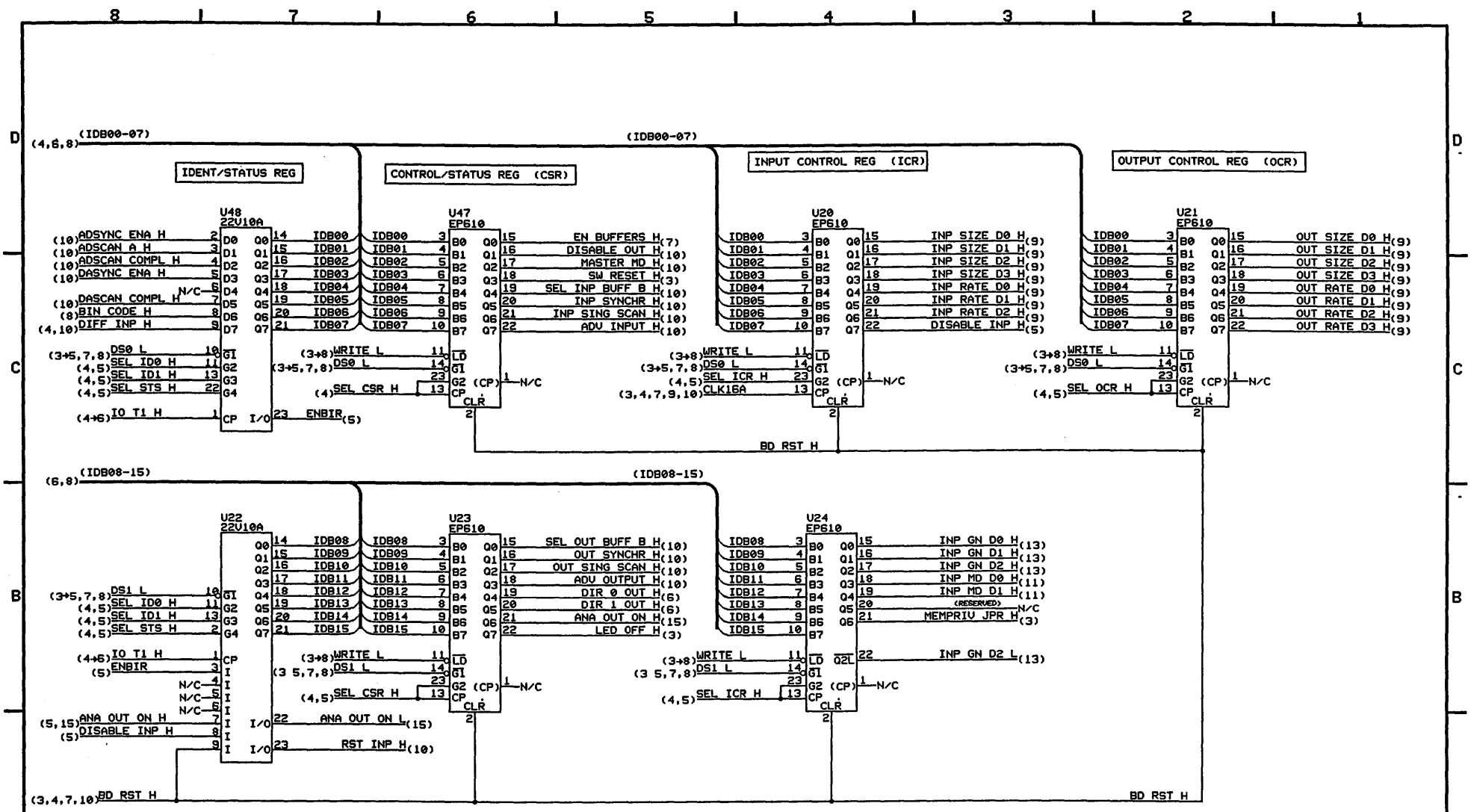


INTERRUPTER & I/O TIMING

SIGNATURES	DATE
DRAWN R. MELROSE	7-31-90
CHECKED C. Muggs	10-15-92

VMIC
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 4

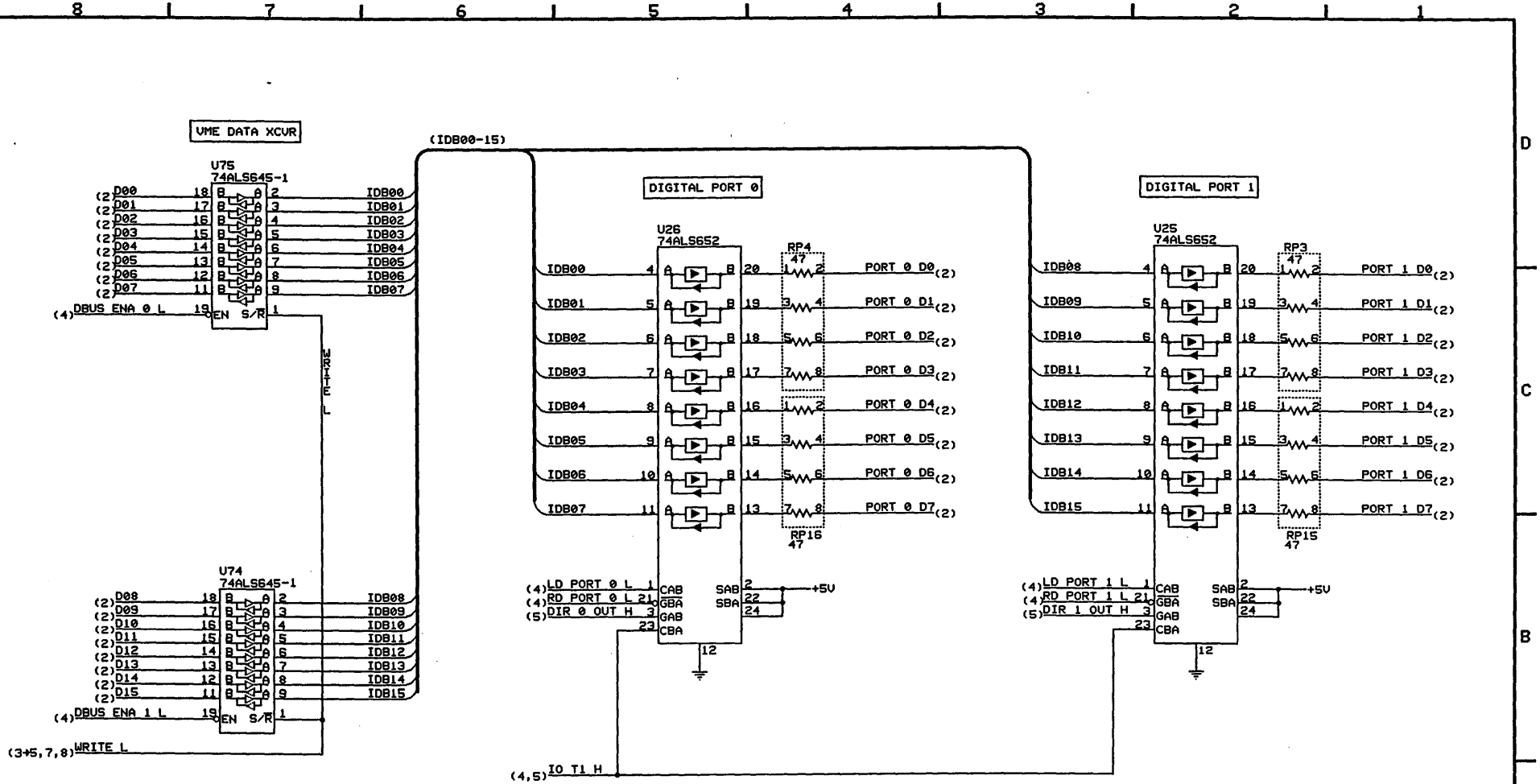


I/O CONTROL REGISTERS

SIGNATURES	DATE
DRAWN R. MELROSE	7-31-90
CHECKED C. Mussey	10-15-90

VMIC
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 5



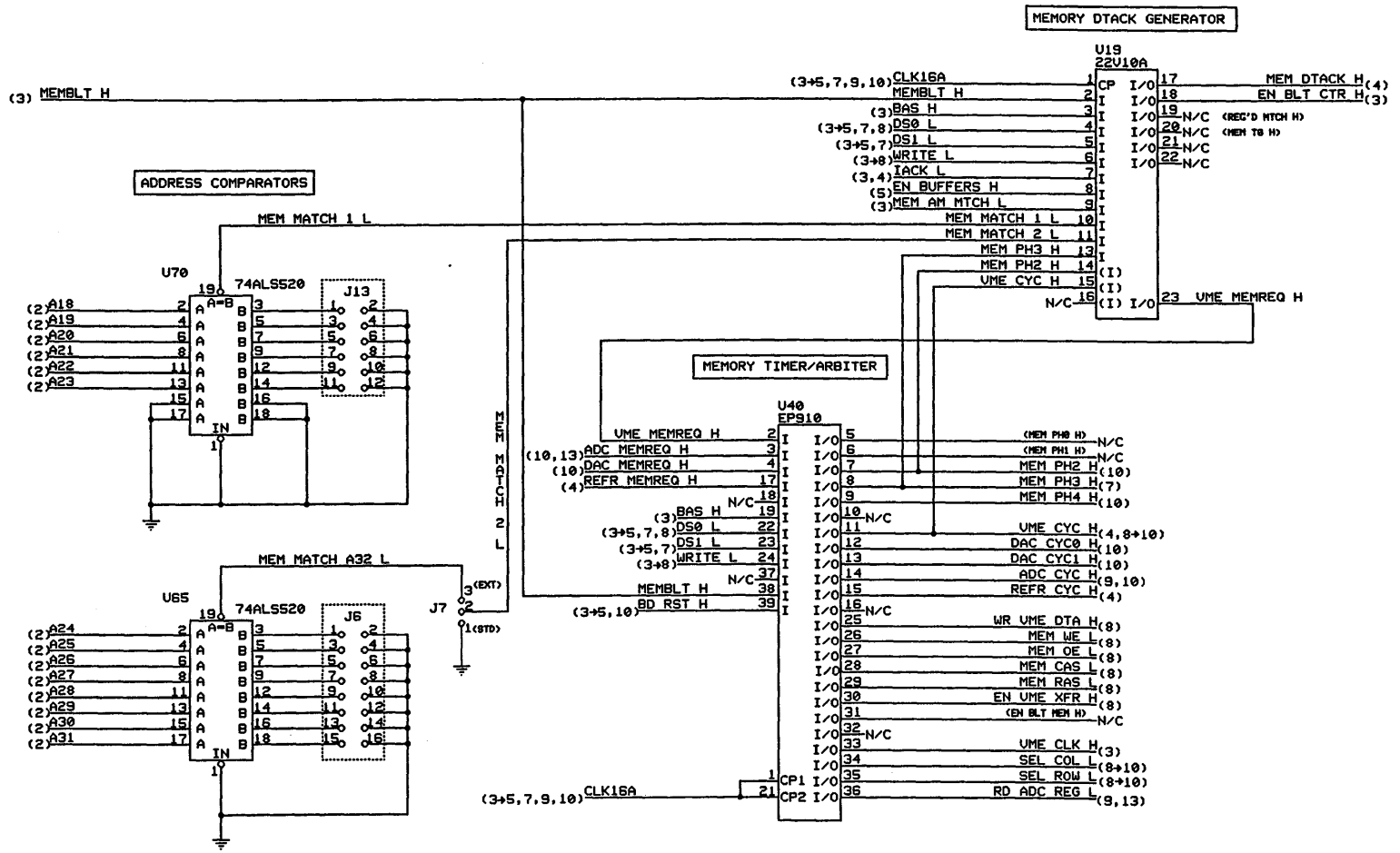
SIGNATURES	DATE
DRAWN R. MELROSE	7-31-90
CHECKED C. Murphy	10-15-90

VMIC®

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 6

DIGITAL PORTS



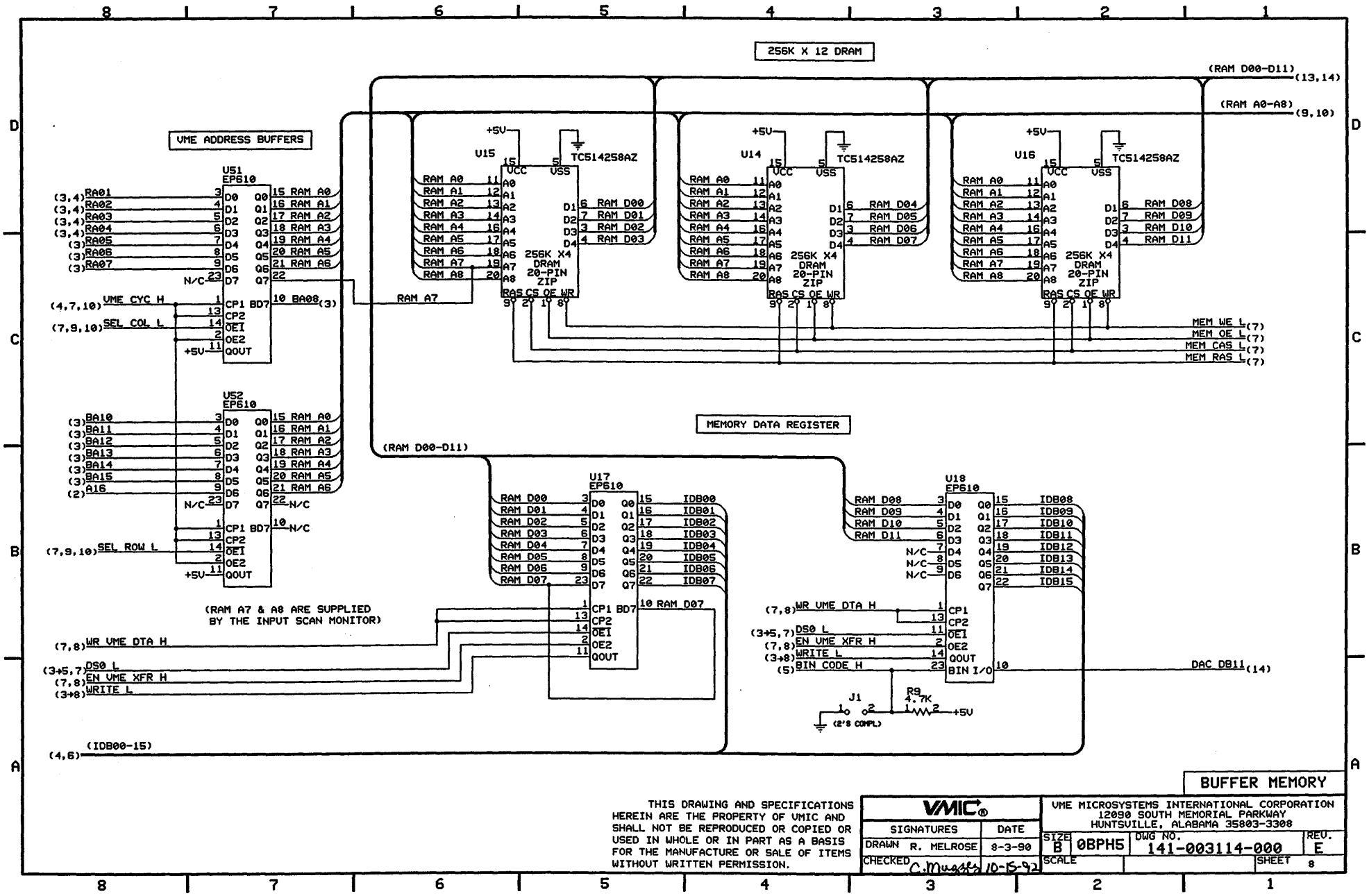
MEMORY TIMING & CONTROL

SIGNATURES	DATE
DRAWN R. MELROSE	8-3-90
CHECKED C. Musser	10-15-90

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E

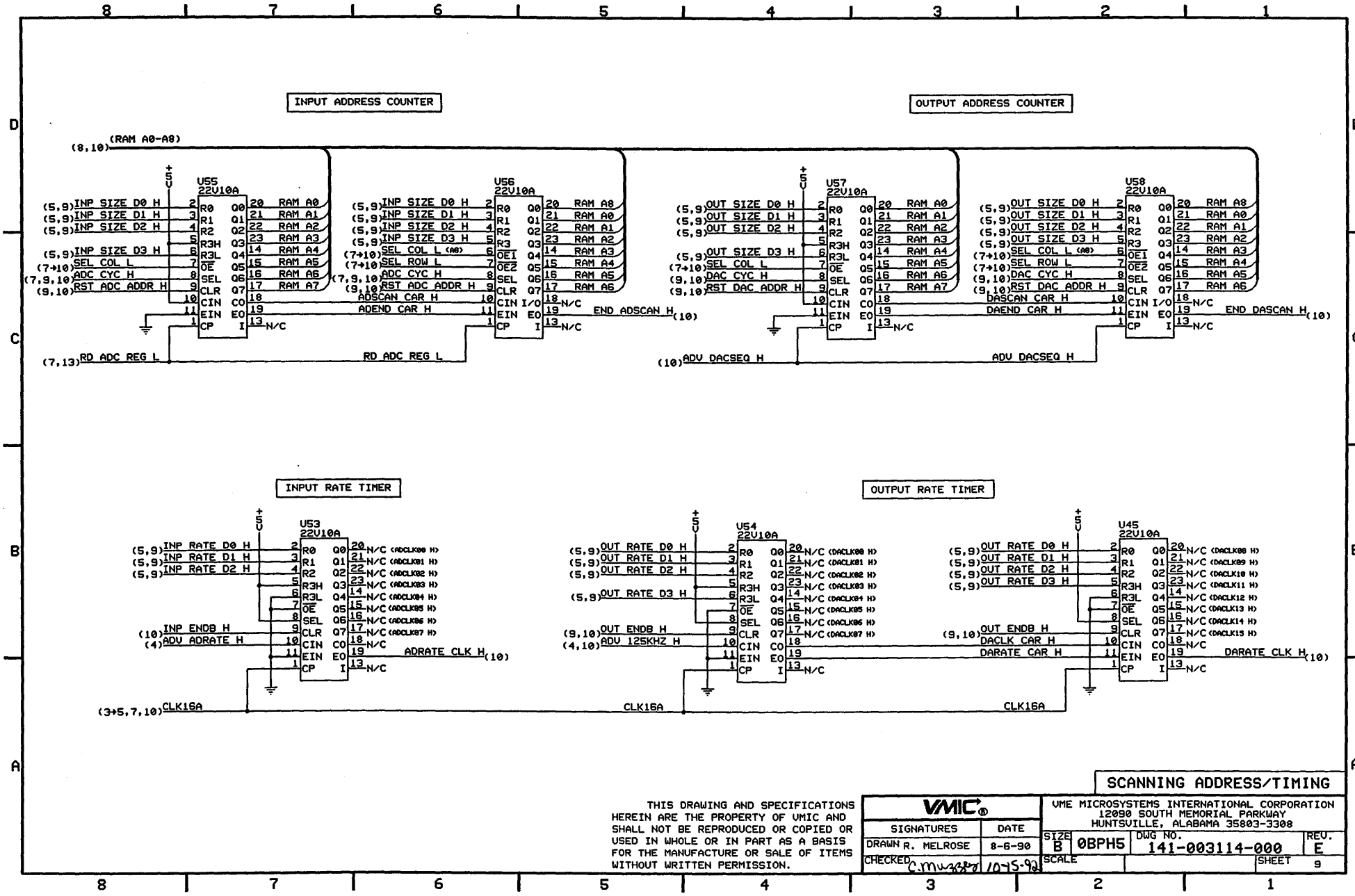
SCALE | SHEET 7



VMIC®	SIGNATURES	DATE
DRAWN	R. MELROSE	8-3-90
CHECKED	C. Muggli	10-15-92

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5	141-003114-000	E
SCALE		SHEET 8

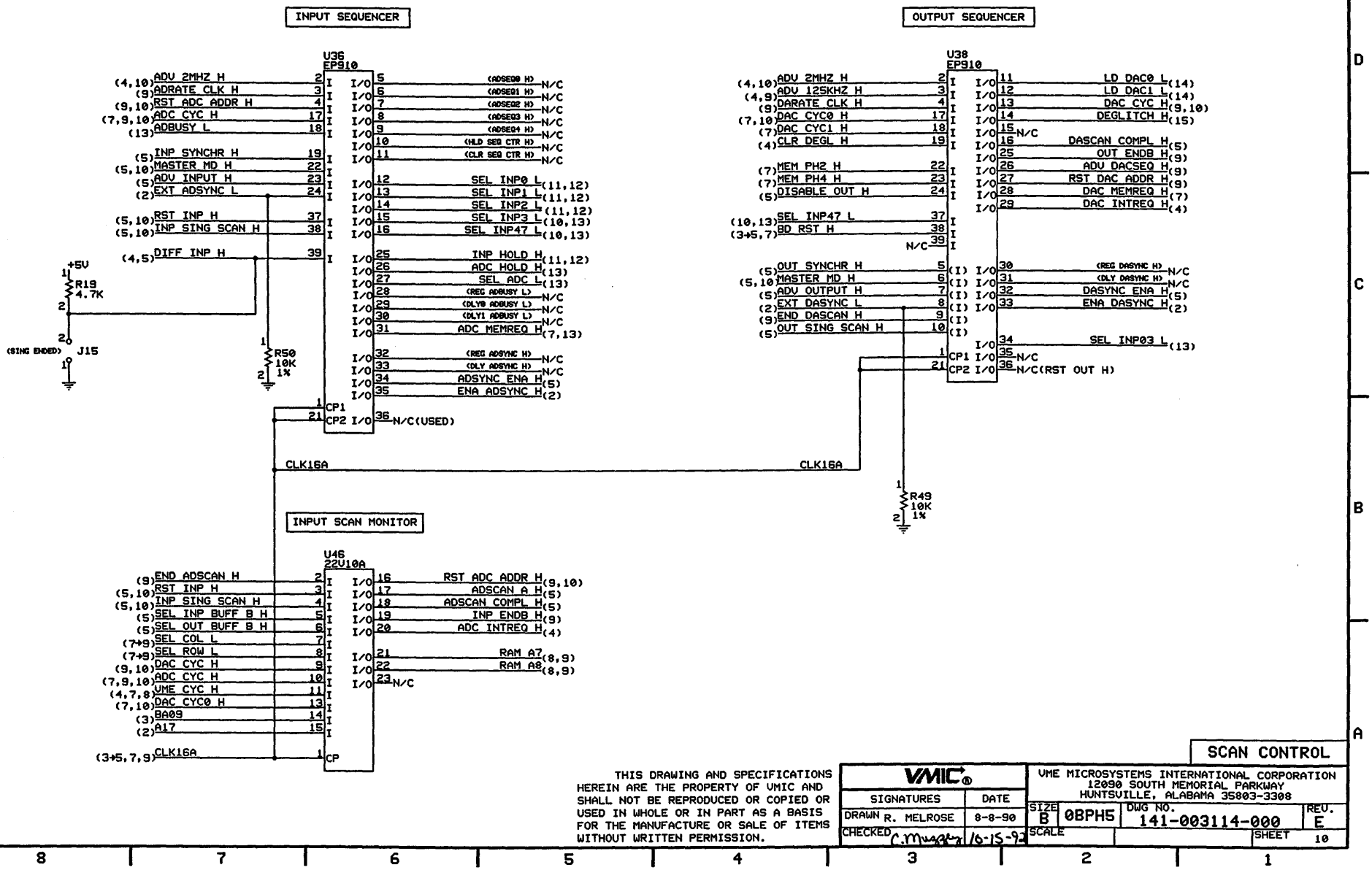


SCANNING ADDRESS/TIMING

SIGNATURES	DATE
DRAWN R. MELROSE	8-6-90
CHECKED C. Murphy	10-15-90

VMIC®
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 9



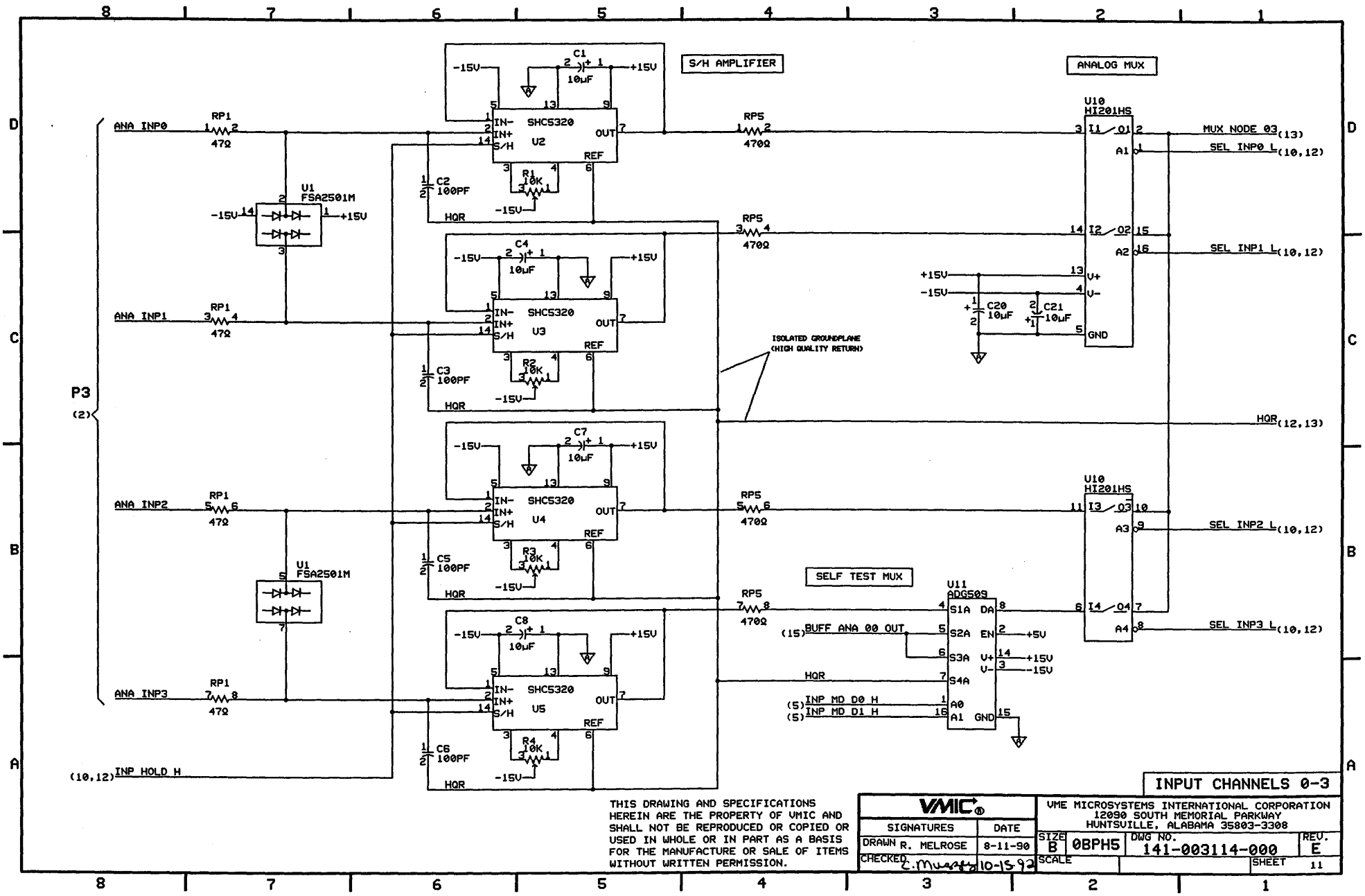
SCAN CONTROL

SIGNATURES	DATE
DRAWN R. MELROSE	8-8-90
CHECKED C. Murphy	10-15-92

VMIC®
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5	141-003114-000	E

SCALE | SHEET 10



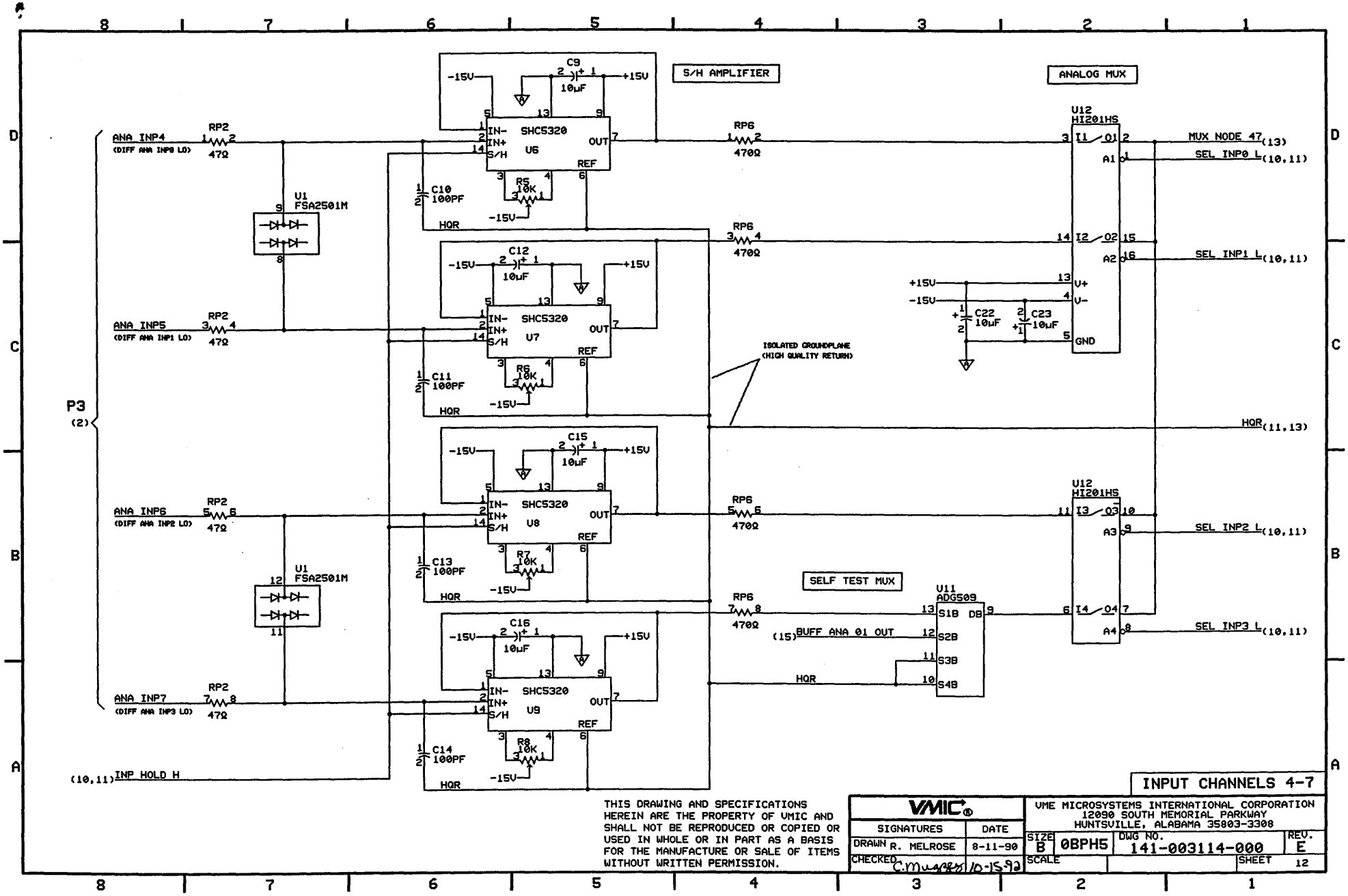
INPUT CHANNELS 0-3

SIGNATURES	DATE
DRAWN R. MELROSE	8-11-90
CHECKED C. Murphy	10-15-92

VMIC®

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 11



SIGNATURES	DATE
DRAWN R. MELROSE	8-11-90
CHECKED C. Mugeen	10-15-92

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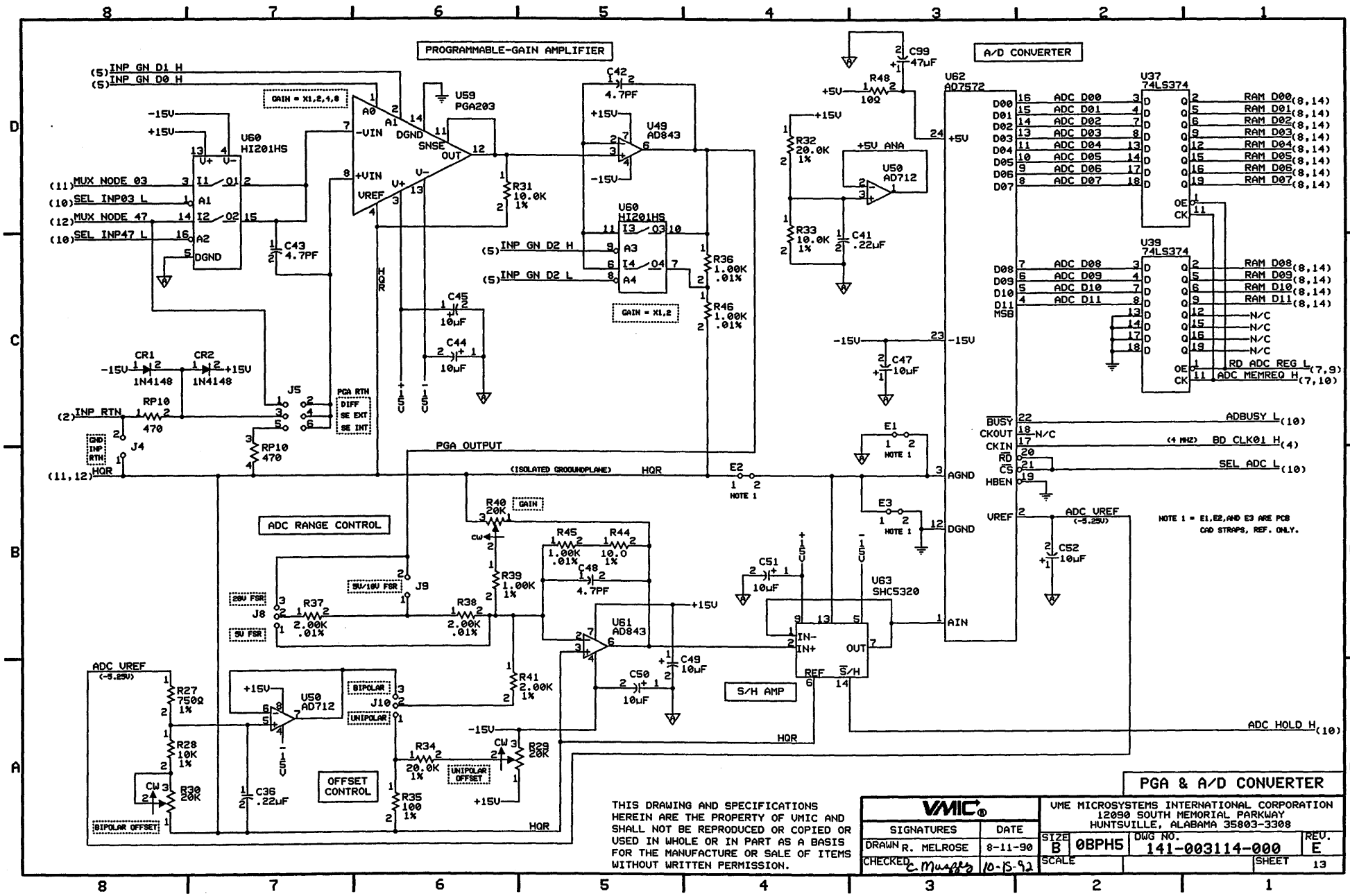
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 12


PROGRAMMABLE-GAIN AMPLIFIER
A/D CONVERTER
ADC RANGE CONTROL
S/H AMP
OFFSET CONTROL
PGA & A/D CONVERTER
U59 PGA203
U60 HI201HS
U49 AD843
U61 AD843
U62 AD7572
U63 SHC5320
U50 AD712
U37 74LS374
U39 74LS374
GAIN = X1,2,4,8
GAIN = X1,2
PGA OUTPUT
(ISOLATED GROUNDPLANE)
HQR
ADC VREF (-5.25V)
ADC HOLD H (10)
ADBUSY L (10)
SEL ADC L (10)
RD ADC REG L (7,9)
ADC MEMREQ H (7,10)
BD CLK01 H (4)
NOTE 1 = E1,E2,AND E3 ARE PCB CAD STRAPS, REF. ONLY.
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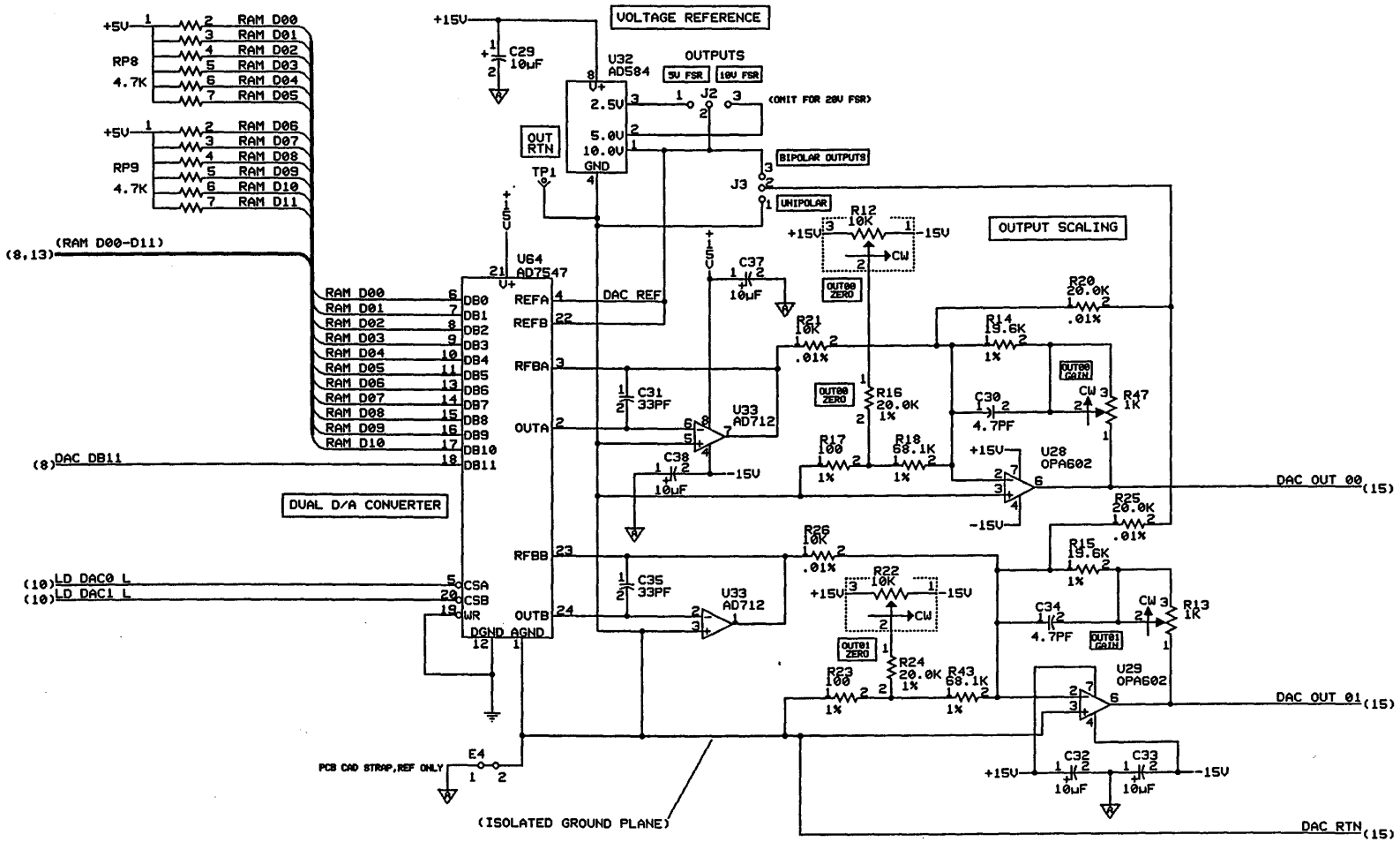
VMIC
SIGNATURES
DATE
DRAWN R. MELROSE 8-11-90
CHECKED C. Muggeo 10-15-92
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
SIZE B 0BPH5
DWG NO. 141-003114-000
REV. E
SCALE
SHEET 13

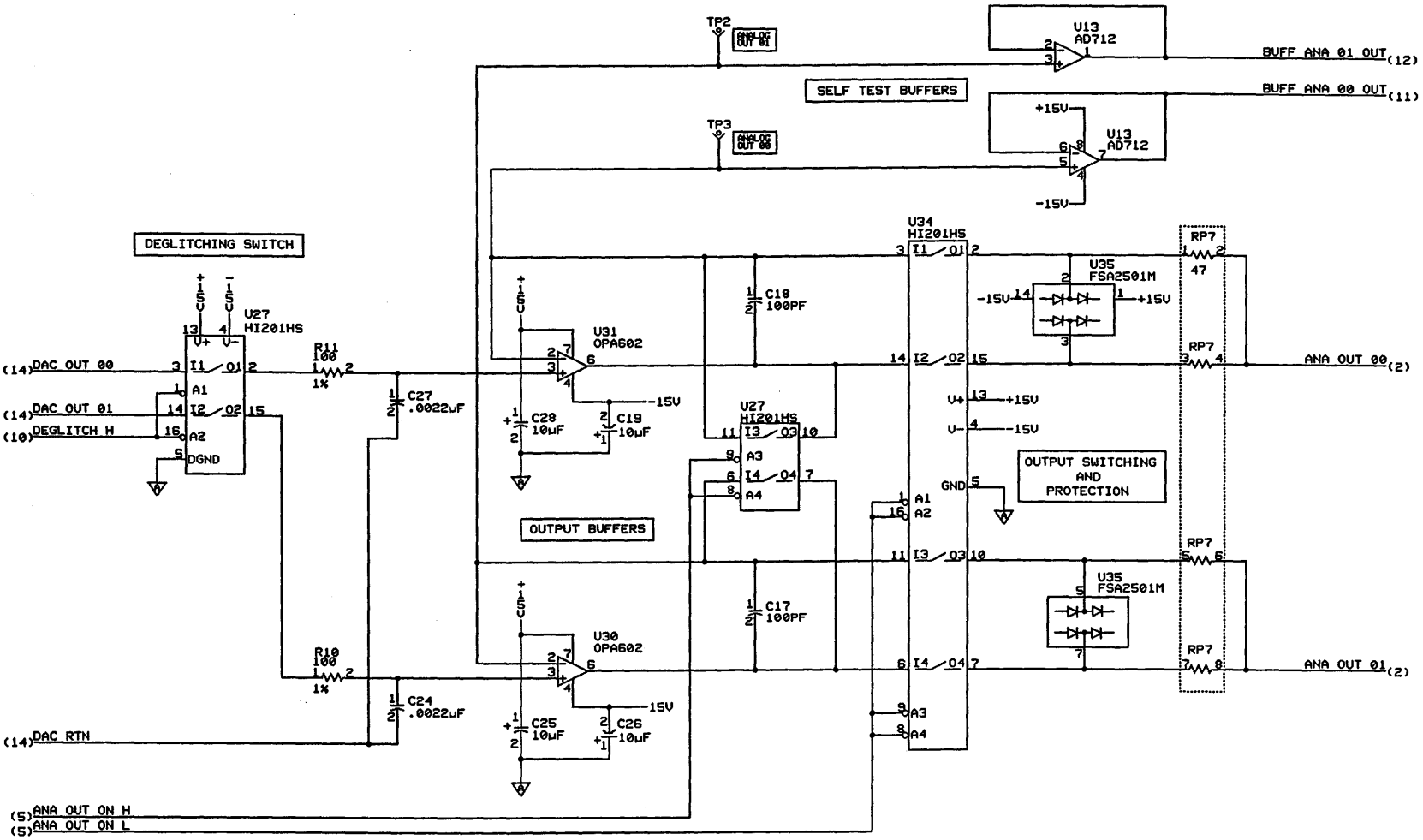


ANALOG OUT D/A CONVERSION

SIGNATURES	DATE
DRAWN R. MELROSE	8-10-20
CHECKED C. Mugglin	10-15-92

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 14



ANALOG OUTPUTS

SIGNATURES	DATE
DRAWN R. MELROSE	8-10-90
CHECKED C. Munsey	10-15-92

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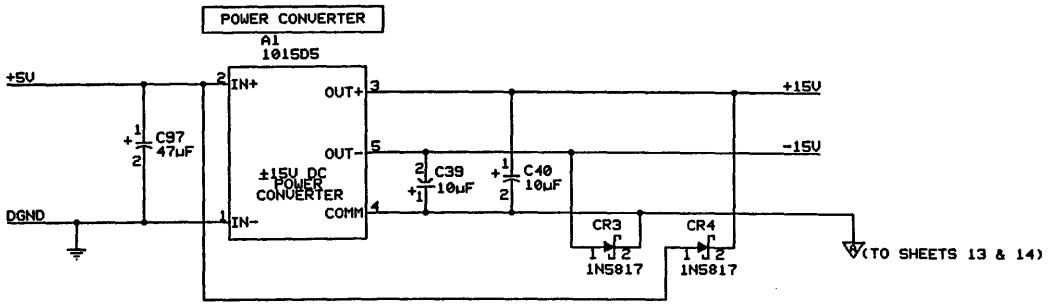
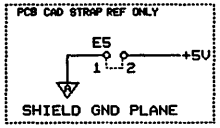
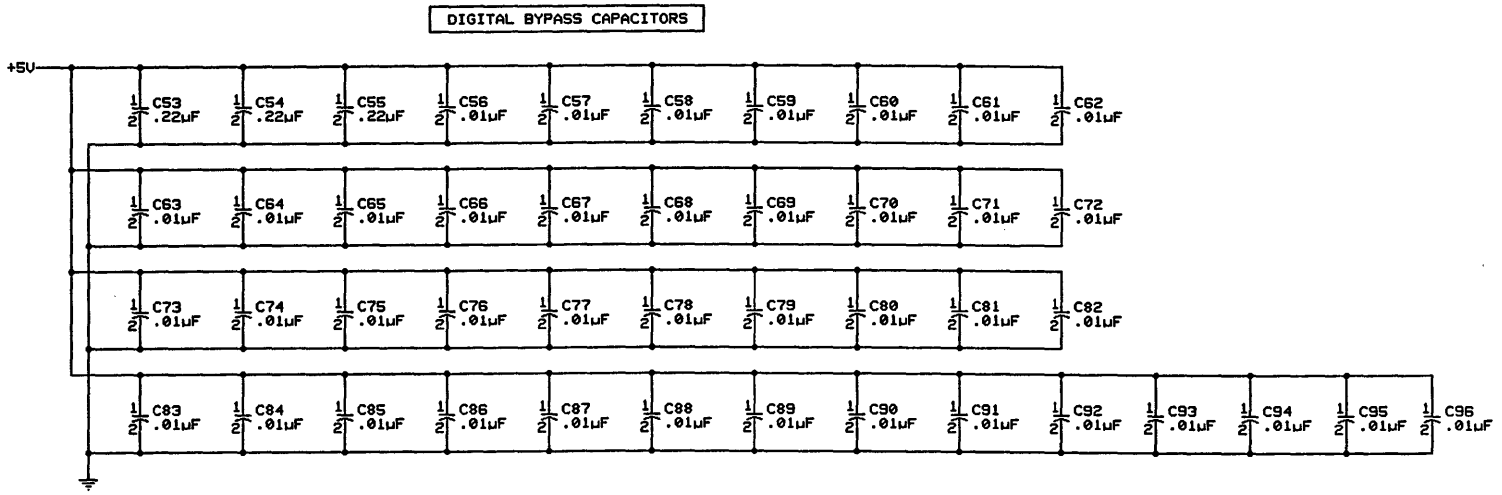
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E
SCALE		SHEET 15







POWER CONDITIONING

SIGNATURES	DATE
DRAWN R. MELROSE	8-10-90
CHECKED C. Murphy	10-15-92

VMIC
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-003114-000	E

SCALE

SHEET 16 OF 16

REVISIONS

132 REV.	332 REV.	DESCRIPTION	BY	DATE	APPR.
A	A	RELEASED PER ECO 91-0244	E. JORY	10/23/91	M. SPANGLER
B	B	CHANGES PER ECO 91-0246	E.M. GREEN	10/23/91	M. SPANGLER
C	C	CHANGES PER ECO 91-0263	D. SMITH	10/23/91	M. SPANGLER
D	D	CHANGES PER ECO 91-0328	E.M. GREEN	12/20/91	M.C.L.
E	E	ADDED REWORKS PER ECO 92-0074	E.M. GREEN	4/17/92	M.C.L.
F	E	CORRECTED DESCRIPTION PER ECO 92-0289	E.M. GREEN	8/17/92	D. FOWLER
G	E	CHANGED BIM PER ECO 92-0319	E.M. GREEN	9/15/92	A.J.
H	F	CHANGED PER ECO 92-0417	E.M. GREEN	10/15/92	T. Mccurdy

NOTES:

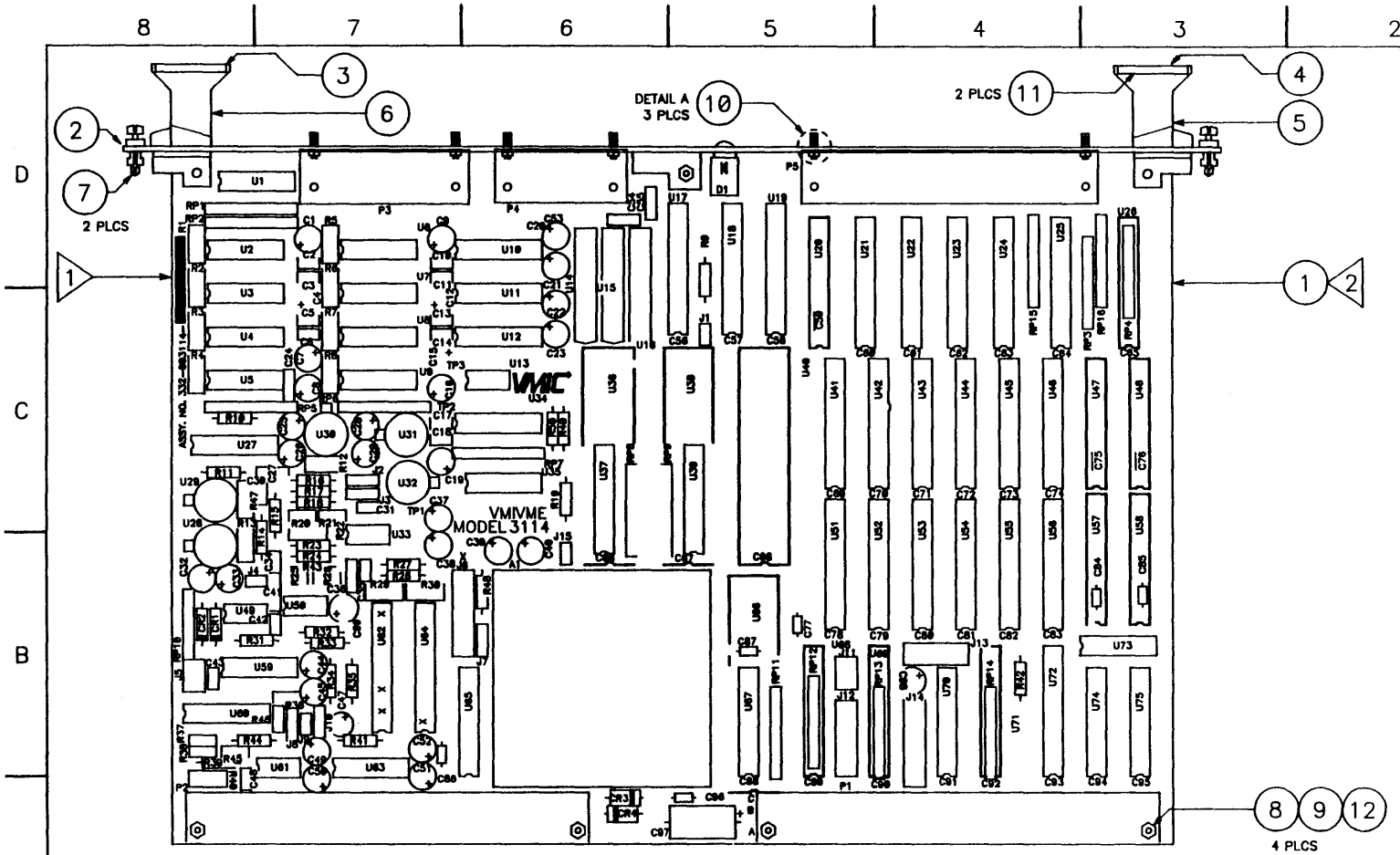
1. FOR SCHEMATIC DIAGRAM SEE 141-003114-000
2. FOR TEST PROCEDURE SEE 510-003114-000

APPROVALS	DATE
DRAWN E.M.GREEN	5/29/91
PROJ. ENG. E.D.D.	6/6/91
ENG. MGR. GEORGE MEARES	6/6/91
PROD. DENNIS FOWLER	10/28/91
Q.A. SHARON KEAGLE	10/28/91

VMIC®
12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803
VME MICROSYSTEMS INTERNATIONAL CORPORATION

ASSEMBLY DRAWING
VMIVME-3114

SIZE		DWG NO.	REV.
A	0BPH5	132-003114-000	H
SCALE			SHEET 1



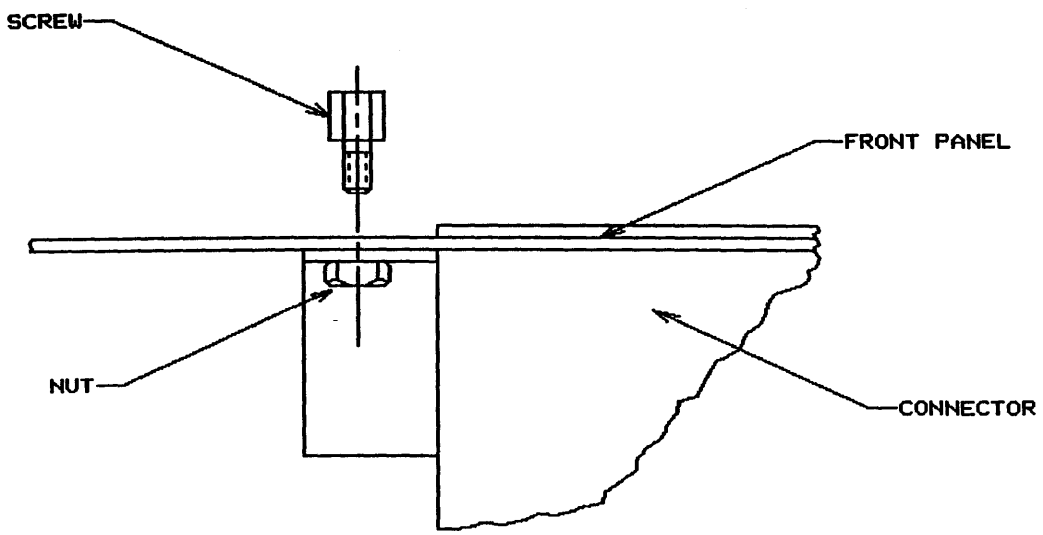
VMIC®	SIGNATURES	DATE
	DRAWN D. SMITH	12/19/90
	CHECKED C. Muggins	10-15-92

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG. NO.	REV.
B	OBPH5	132-003114-000	H
SCALE	NONE		SHEET 2

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H
MODEL NO. VMIVME-3114	SIGNATURES / DATE: DRAWN E. JORY 9/19/91; CHECKED C. Muggeo 10-15-92	CONTRACT NO.	SH 2A



DETAIL A

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	SH 3
VMIVME-3114	DRAWN E.M.GREEN	5/29/91		
	CHECKED C. Muzzey	10-15-92		

INSTRUCTIONS:

NOTES:

(1) A. ALL ASSEMBLED BOARDS SHALL BE IDENTIFIED WITH THE ASSEMBLED BOARD PART NUMBER. THIS NUMBER INCLUDES THE CURRENT REVISION LETTER LISTED IN THE 332-COLUMN OF THE REVISION TABLE (SEE SHEET 1). THE RESULTING PART SHALL BECOME A 332-003114-000(REV).

B. THE REVISION LETTER(S) OF THE ASSEMBLY DRAWING SHALL BE STAMPED IN THE DESIGNATED AREA.

C. REMOVE ANY EXISTING REVISION LETTER FROM THE 332 ASSEMBLED PART NUMBER.

D. REMOVABLE, NON-SMEARING INK SHALL BE USED TO STAMP REVISION LETTERS IN THE DESIGNATED AREA.

(2) SOLDER COMPOSITION COMPLIES WITH MIL-STD-2000.

PARTS LIST

VMIC® VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN E. JORY	9/19/91		SH 3A
	CHECKED C. Muggeo	10-15-92		

INSTRUCTIONS: REWORK

NOTES:

A. REWORK INSTRUCTIONS SHALL BE ACCOMPLISHED ON THE COPPER REVISION(S) INDICATED AND WILL BECOME A PART OF THE ASSEMBLED BOARD.

B. REWORK INSTRUCTION SYMBOLS

1. ■ PIN ONE DOT
2. ● DRILL HOLE
3. ✕ DISCONNECT TRACE
4. ---- TRACE ON INTERNAL LAYER
5. —— TRACE ON EXTERNAL LAYER

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

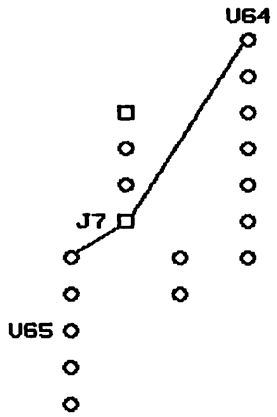
MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN E. JORY	9/19/91		SH 3B
	CHECKED C. Muggeo	10-15-92		

EFFECTIVITY: E.C.O. 91-0244
333-003114-000 REV. A

INSTRUCTIONS: REWORK

STEP 1

WIRE U65-10 TO J7-1 AND TO U64-12 ON THE SOLDER SIDE OF THE BOARD.



PARTS LIST

VMIC® VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN E.M. GREEN	9/23/91		SH 3C
	CHECKED C. Muggeo	10-15-92		

EFFECTIVITY: E.C.O. 91-0246
332-003114-000 REV. A

INSTRUCTIONS: REWORK

STEP 1
REMOVE U40. THIS IS A PAL LABELED 303-000537-000

STEP 2
REPLACE IT WITH A NEW PAL LABELED 303-000683-000

STEP 3
REMOVE U45. THIS IS A PAL LABELED 303-000522-000

STEP 4
REPLACE IT WITH A NEW PAL LABELED 303-000684-000

STEP 5
REMOVE U54. THIS IS A PAL LABELED 303-000532-000

STEP 6
REPLACE IT WITH A NEW PAL LABELED 303-000685-000

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN E.M. GREEN	9/23/91		SH 3D
	CHECKED C. Muggeo	10-15-92		

EFFECTIVITY: E.C.O. 91-0246
333-003114-000 REV. A

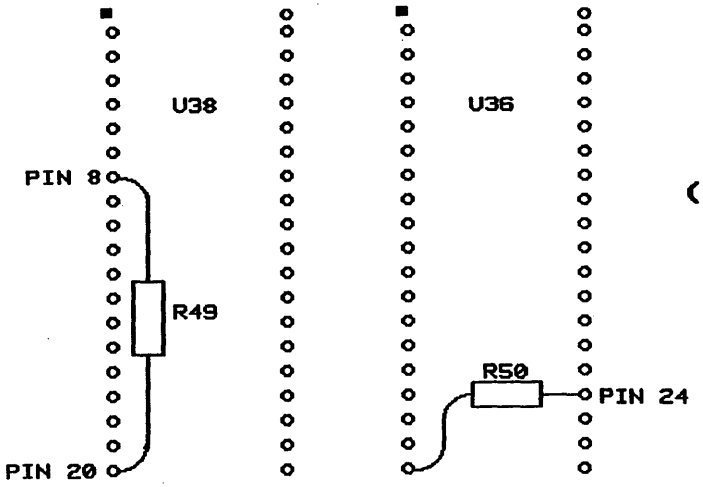
INSTRUCTIONS: REWORK

STEP 1

REMOVE U36 AND U38.

STEP 2

SOLDER RESISTORS R48 AND R49 TO THE ELEVATED SOCKET PINS AS SHOWN.



(COMPONENT SIDE)

STEP 3

REPLACE U36 AND U38.

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN D. SMITH	10/3/91		SH 3E
	CHECKED C. Muggeby	10-15-92		

EFFECTIVITY: E.C.O. 91-0263
332-003114-000 REV. A & B

INSTRUCTIONS: REWORK

STEP 1

IF U71 IS "3114U71A", PN 303-000544-000 THEN
REPLACE IT WITH "3114U71B" PN 303-000694-000.

EFFECTIVITY: E.C.O. 91-0328
333-003114-000 REV. A - D

INSTRUCTIONS: REWORK

STEP 1

WIRE U40 PIN 38 TO U71 PIN 16.

EFFECTIVITY: E.C.O. 92-0074
332-003114-000 REV. A - D

STEP 1

IF U18 IS "3114U18A", PN 303-000524-000 THEN REPLACE
IT WITH "3114U18B", PN 303-000799-000.

STEP 2

IF U36 IS "3114U36A", PN 303-000545-000 THEN REPLACE
IT WITH "3114U36B", PN 303-000800-000.

PARTS LIST

VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-003114-000	REV. LTR. H

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-3114	DRAWN E.M. GREEN	10/13/92		SH 3F
	CHECKED C. Mussey	10-15-92		

EFFECTIVITY: E.C.O. 92-0417
332-003114-000 REV. A - E

INSTRUCTIONS: REWORK

STEP 1

IF U19 IS "3114U19A", PN 303-000517-000 THEN
REPLACE IT WITH "3114U19B" PN 303-000905-000.

STEP 2

REMOVE C31 AND C35 FROM ASSEMBLED BOARD.

STEP 3

REPLACE EACH WITH ONE PART # 315-220000-330, WHICH IS
A 33pF, 10%, 200V, NPO CERAMIC MONOLYTHIC CAPACITOR.

END OF REWORK INSTRUCTIONS

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			1	1		333-003114-000	BOARD: PC, RAW, 8 LAYERS	
			1	2		324-000051-000	FRONT PANEL: ONE MIDDLE POS. 37, 9 & 15 PIN CUTOUT NO FAIL LED, EJECTOR CUTOUTS	
			1	3		324-000000-003	LOGO: ASSEMBLED - VMIC, SINGLE, EJECTOR HANDLES	
			1	4		324-003114-000	LOGO: ASSEMBELD - 3114, SINGLE	
			1	5		328-250508-000	HANDLE: TOP, FRONT PANEL WITH EJECTORS, GRAY	20817-328 (SCHROFF)
			1	6		328-250508-100	HANDLE: BOTTOM, FRONT PANEL WITH EJECTORS, GRAY	20817-327 (SCHROFF)
			1	7		328-250508-200	KIT: MOUNTING, FRONT PANEL WITH EJECTORS	21100-745 (SCHROFF)
			4	8	P1,2	328-250000-010	SCREW: METRIC, 2.5 X 10MM, SS	
			4	9	P1,2	328-250001-025	NUT: METRIC, 2.5MM, HEX, SS	
			3	10	P3-5	328-000002-001	SCREWLOCK: FEMALE, STANDARD FOR HDM,HDD,20 SERIES	205817-1 (AMP)
			A/R	11	REF. LOGOS	316-000001-000	LOCTITE: SUPER BONDER 430	
			A/R	12	REF. P1,2	316-000002-000	LOCTITE: SMALL SCREW THREADLOCKER 222	
			1	13	U19	303-000905-000	PROGRAMMED PAL: PAL A, FILE: 3114U19B.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	14	U22	303-000518-000	PROGRAMMED PAL: PAL B, FILE: 3114U22A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	15	U42	303-000519-000	PROGRAMMED PAL: PAL C, FILE: 3114U42A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	16	U43	303-000520-000	PROGRAMMED PAL: PAL D, FILE: 3114U43A.PLD, A PROGRAMMED 22V10A (331-300122-100)	

VMIC® PARTS LIST

VME MICROSYSTEMS INT'L CORP.

CODE OBPH5 | REV. H | DRAWING NUMBER 132-003114-000 | CHECKED C. Muzzey | DATE 10/15/92 | SH NO. 4

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			1	17	U17	303-000521-000	PROGRAMMED PAL: PAL E, FILE: 3114U17A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	18	U45	303-000684-000	PROGRAMMED PAL: PAL F, FILE: 3114U45B.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	19	U46	303-000523-000	PROGRAMMED PAL: PAL G, FILE: 3114U46A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	20	U18	303-000799-000	PROGRAMMED PAL: PAL H, FILE: 3114U18B.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	21	U48	303-000525-000	PROGRAMMED PAL: PAL I, FILE: 3114U48A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	22	U20	303-000526-000	PROGRAMMED PAL: PAL J, FILE: 3114U20A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	23	U21	303-000527-000	PROGRAMMED PAL: PAL K, FILE: 3114U21A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	24	U23	303-000528-000	PROGRAMMED PAL: PAL L, FILE: 3114U23A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	25	U53	303-000529-000	PROGRAMMED PAL: PAL M, FILE: 3114U53A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	26	U24	303-000530-000	PROGRAMMED PAL: PAL N, FILE: 3114U24A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	27	U41	303-000531-000	PROGRAMMED PAL: PAL O, FILE: 3114U41A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	28	U54	303-000685-000	3ROGRAMMED PAL: PAL P, FILE: 3114U54B.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	29	U44	303-000533-000	PROGRAMMED PAL: PAL Q, FILE: 3114U44A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	30	U47	303-000534-000	PROGRAMMED PAL: PAL R, FILE: 3114U47A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	

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VME MICROSYSTEMS INT'L CORP.

CODE OBPH5 | REV. H | DRAWING NUMBER 132-003114-000 | CHECKED C. Muggeo | DATE 10/15/92 | SH NO. 5

F0086-90

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			1	31	U51	303-000535-000	PROGRAMMED PAL: PAL S, FILE: 3114U51A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	32	U52	303-000536-000	PROGRAMMED PAL: PAL T, FILE: 3114U52A.PLD, A PROGRAMMED EP610-35 (331-300130-350)	
			1	33	U40	303-000683-000	PROGRAMMED PAL: PAL U, FILE: 3114U40B.PLD, A PROGRAMMED EP910-35 (331-300129-350)	
			1	34	U55	303-000538-000	PROGRAMMED PAL: PAL V, FILE: 3114U55A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	35	U56	303-000539-000	PROGRAMMED PAL: PAL W, FILE: 3114U56A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	36	U57	303-000540-000	PROGRAMMED PAL: PAL X, FILE: 3114U57A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	37	U58	303-000541-000	PROGRAMMED PAL: PAL Y, FILE: 3114U58A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	38	U68	303-000542-000	PROGRAMMED PAL: PAL Z, FILE: 3114U68A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	39	U69	303-000543-000	PROGRAMMED PAL: PAL AA, FILE: 3114U69A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	40	U71	303-000694-000	PROGRAMMED PAL: PAL BB, FILE: 3114U71B.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	41	U36	303-000800-000	PROGRAMMED PAL: PAL CC, FILE: 3114U36B.PLD, A PROGRAMMED EP910-35 (331-300129-350)	
			1	42	U38	303-000546-000	PROGRAMMED PAL: PAL DD, FILE: 3114U38A.PLD, A PROGRAMMED EP910-35 (331-300129-350)	
			1	43	U72	303-000547-000	PROGRAMMED PAL: PAL EE, FILE: 3114U72A.PLD, A PROGRAMMED 22V10A (331-300122-100)	
			1	44	U32	311-000017-005	AMP: OPERATIONAL, 40V INPUT, 10V, 7.5V, 5V AND 2V OUTPUTS, 600mW, TO-99 PACKAGE	AD584JH (ANALOG DEVICES)

VMIC® **PARTS LIST**

VME MICROSYSTEMS INT'L CORP.

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VMIC® **PARTS LIST**

VME MICROSYSTEMS INT'L CORP.

CODE	REV.	DRAWING NUMBER	CHECKED	SH NO.
OBPH5	H	132-003114-000	C. Muggeo	7
			DATE 10/15/92	

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			3	45	U13,33,50	311-000018-012	AMP: OPERATIONAL, +-18V, 500mW, 0 TO 70 DEGREES, PLASTIC DIP	AD712KN (ANALOG DEVICES)
			2	46	U49,61	311-000025-010	AMP: OPERATIONAL, 34MHz, CBFET, FAST SETTLING, 0 TO 70 DEGREES, PLASTIC DIP	AD843JN (ANALOG DEVICES)
			1	47	U59	311-000033-100	AMP: INSTRUMENTATION, 1,2,4,8 GAINS, +-18V, 750mW, +-(1 + 20/G), 0 TO 70 DEGREES	PGA203KP (BURR BROWN)
			41	48	C56-96	315-005002-104	CAP: .1uF, .300 LEAD SPACE, 10%, 50V, X7R, CERAMIC MOLDED	CW80C104KM (PHILLIPS)
			31	49	C1,4,7-9,12,15,16,19 C20-23,25,26,28,29, C32,33,37-40,44,45, C47,49-52,98	315-102001-106	CAP: 10uF, .100 LEAD SPACE, 20%, 25V, TANTALUM	T35(0,1)E106M025AS (KEMET)
			2	50	C24,27	315-210001-222	CAP: .0022uF, .200 LEAD SPACE, 20%, 100V, X7R, CERAMIC MONOLYTHIC	C317C222M1R5CA (KEMET)
			5	51	C36,41,53-55	315-205001-224	CAP: .22uF, .200 LEAD SPACE, 20%, 50V, Z5U, CERAMIC MONOLYTHIC	C32(2,3)C224M5U5CA (KEMET)
			10	52	C2,3,5,6,10,11,13,14 C17,18	315-220000-101	CAP: 100PF, .100 LEAD SPACE, 10%, 200V, NPO, CERAMIC MONOLYTHIC	C3(15,20)C101K2G5CA (KEMET)
			5	53	C30,34,42,43,48	315-220003-479	CAP: 4.7PF, .100 LEAD SPACE,.5pF, 200V, NPO, CERAMIC MONOLYTHIC	C3(15,20)C479D2G5CA (KEMET)
			1	54	C97	315-902000-476	CAP: 47uF, AXIAL, 20%, 35V, ALUMINUM ELECTROLYTIC	ECEB1VU470 (PANASONIC)
			10	55	U26,68,69,71	321-000007-002	SOCKET: IC, BREAKAWAY STRIP, 10 CONTACTS, TIN/GOLD	3852010-02 (MUPAC)
			26	56	J1-4,7-10,15 TP1-3	321-000016-011	TERMINAL: PC BOARD, SINGLE ROW, .025 THICK, GOLD PLATED, ONE POST	92983401-01 (PANDUIT)
			35	57	J5,6,11-14	321-000017-011	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, ONE POST	92983402-01 (PANDUIT)

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			1	58	P4	321-000040-111	CONNECTOR: PLUG, 9 PIN, METAL-SHELL, RIGHT-ANGLE, THREADED INSERTS, BOARDLOCKS, .318 MOUNT	747840-3 (AMP)
			1	59	P3	321-000040-211	CONNECTOR: PLUG, 15 PIN, METAL-SHELL, RIGHT-ANGLE, THREADED INSERTS, BOARDLOCKS, .318 MOUNT	747841-3 (AMP)
			1	60	P5	321-000040-411	CONNECTOR: PLUG, 37 PIN, METAL-SHELL, RIGHT-ANGLE, THREADED INSERTS, BOARDLOCKS, .318 MOUNT	747843-3 (AMP)
			1	61	P1	321-000054-001	CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C	913215 (ERNI)
			1	62	P2	321-000054-002	CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C	913216 (ERNI)
			27	63	U17-24,41-48,51-58, U62,64,72	321-001324-001	SOCKET: DIP, 24 PIN, .300 ROW	ICA-324-SGT (SAMTEC)
			4	64	U36,38,40,66	321-001640-081	SOCKET: DIP, 40 PIN, .600 ROW, ELEVATED	ICA-640-EGT (SAMTEC)
			1	65	U62	323-250031-000	CONVERTER: ANALOG TO DIGITAL, 3uS CONVERSION TIME, 45ppm SCALE, +-1LSB ACCURACY	MAX162C(C,I)NG (MAXIM)
			1	66	U73	331-300404-700	IC: DIGITAL, HEX INVERTER, PLASTIC DIP	SN74S04N (TI)
			2	67	U37,39	331-304374-600	IC: DIGITAL, OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP THREE-STATE, PLASTIC DIP	SN74LS374N (TI)
			2	68	U65,70	331-304520-100	IC: DIGITAL, 8 BIT IDENTITY COMPARATOR, PLASTIC DIP	SN74ALS520N (TI)
			1	69	U67	331-304641-610	IC: DIGITAL, OCTAL BUS TRANSCEIVER, OPEN COLLECTOR PLASTIC DIP	SN74LS641-1N (TI)
			2	70	U74,75	331-304645-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74ALS645A-1N (TI)
			2	71	U25,26	331-304652-110	IC: DIGITAL, OCTAL BUS TRANSCIEVER/REGISTER, PLASTIC DIP	SN74ALS652-1P (TI)

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F0086-90

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			5	72	U10,12,27,34,60	331-309006-002	IC: INTERFACE, 36V, DIGITAL & ANALOG INPUT, PLASTIC DIP	HI3-201HS-5 (HARRIS)
			1	73	U11	331-309011-202	IC: INTERFACE, 44V, DIFFERENTIAL 4 CHANNEL, +-2V ANALOG SIGNAL, 0 TO 75 DEGREES, PLASTIC DIP	HI3-0509-5 (HARRIS)
			9	74	U2-9,63	331-309029-000	IC: LINEAR, SAMPLE/HOLD AMPLIFIER, 0 TO 75 DEGREES CERAMIC DIP	SHC5320KH (BURR BROWN)
			1	75	U66	331-309099-000	IC: INTERFACE, CMOS VMEBUS INTERRUPTER MODULE, PLASTIC DIP	MX68C153 (MACRONIX)
			1	76	U64	331-309054-000	IC: INTERFACE, +-1LSB ACCURACY, +-6LSB GAIN ERROR, 0 TO 75 DEGREES, PLASTIC DIP	AD7547JN (ANALOG DEVICE)
			3	77	U14-16	331-309074-303	IC: MEMORY, DRAM, 5V, 330mW OPERATING POWER, PLASTIC ZIP	MCM514258AZ10 (MOTOROLA)
			1	78	D1	337-000002-211	DIODE: LED, RED, 5V, 12mA, CURRENT-LIMITING RESISTOR, RIGHT ANGLE PCB MOUNT	5302H1-5V (IDI)
			2	79	U1,35	337-000004-001	DIODE: ARRAY, MONOLYTHIC, 60V, 500mA, 14 PIN DIP	FSA2501(M/P) (FAIRCHILD)
			1	80	A1	340-000007-105	CONVERTER: DC/DC, 5V INPUT, +-15V OUTPUT, 60% EFFICIENCY	1015D5 (CDI)
			2	81	R9,19	347-000000-472	RESISTOR: 4.7K OHM, 1/4W, 5%, CARBON FILM	
			1	82	R44	347-000004-100	RESISTOR: 10.0 OHM, 1/4W, 1%, METAL FILM	
			5	83	R10,11,17,23,35	347-000005-100	RESISTOR: 100 OHM, 1/4W, 1%, METAL FILM	
			1	84	R39	347-000006-100	RESISTOR: 1.00K OHM, 1/4W, 1%, METAL FILM	
			5	85	R28,31,33,49,50	347-000007-100	RESISTOR: 10.0K OHM, 1/4W, 1%, METAL FILM	
			2	86	R14,15	347-000007-196	RESISTOR: 19.6K OHM, 1/4W, 1%, METAL FILM	

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VME MICROSYSTEMS INT'L CORP.

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OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			5	87	R16,24,32,34,42	347-000007-200	RESISTOR: 20.0K OHM, 1/4W, 1%, METAL FILM	
			2	88	R18,43	347-000007-681	RESISTOR: 68.1K OHM, 1/4W, 1%, METAL FILM	
			6	89	RP8,9,11-14	347-001001-472	SIP: 4.7K OHM, BUSSED, 8 PIN, LOW PROFILE	4608X-101-472 (BOURNS)
			7	90	RP1-4,7,15,16	347-001004-470	SIP: 47 OHM, ISOLATED, 8 PIN, LOW PROFILE	4608X-102-470 (BOURNS)
			2	91	RP5,6	347-001004-471	SIP: 470 OHM, ISOLATED, 8 PIN, LOW PROFILE	4608X-102-471 (BOURNS)
			1	92	RP10	347-001003-471	SIP: 470 OHM, ISOLATED, 6 PIN, LOW PROFILE	4606X-102-471 (BOURNS)
			3	93	R36,45,46	347-001200-102	RESISTOR: PRECISION, 1K OHM, .01%	S102K1K0000.01% (VISHAY)
			2	94	R21,26	347-001200-103	RESISTOR: PRECISION, 10K OHM, .01%	S102K10K000.01% (VISHAY)
			1	95	R41	347-000006-200	RESISTOR: 2.00K OHM, 1/4W, 1%, METAL FILM	
			2	96	R37,38	347-001200-202	RESISTOR: PRECISION, 2K OHM, .01%	S102K2K0000.01% (VISHAY)
			2	97	R20,25	347-001200-203	RESISTOR: PRECISION, 20K OHM, .01%	S102K20K000.01% (VISHAY)
			2	98	R13,47	347-500001-102	POT: TRIMMER, 1K OHM, VARIABLE, TOP ADJUSTMENT	3290W-1-102 (BOURNS)
			10	99	R1-8,12,22	347-500001-103	POT: TRIMMER, 10K OHM, VARIABLE, TOP ADJUSTMENT	3290W-1-103 (BOURNS)
			3	100	R29,30,40	347-500001-203	POT: TRIMMER, 20K OHM, VARIABLE, TOP ADJUSTMENT	3290W-1-203 (BOURNS)
			2	101	CR1,2	348-104148-000	DIODE: SWITCHING, HIGH CONDUCTANCE, ULTRA FAST, DO-35 OUTLINE	1N4148 (AMPEREX)
			2	102	CR3,4	348-105817-000	RECTIFIER: SILICON, 1 AMP, 20 VOLT, SCHOTTKY BARRIER, AXIAL	1N5817
			1	103	C99	315-101000-476	CAP: 47uF, .200 LEAD SPACE, 10%, 10V, TANTALUM	T35(2,3,6)H476K010AS (KEMET)

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VME MICROSYSTEMS INT'L CORP.

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VME MICROSYSTEMS INT'L CORP.

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OBPH5	H	132-003114-000	C. Muggeo DATE 10/15/92	11

OPT. A	OPT. B	OPT. C	QUANTITY	ITEM #	REFERENCE DESIGNATOR	PART NO.	NOMENCLATURE OR DESCRIPTION	MANUFACTURER'S PART NO.
			1	104	R48	347-000000-100	RESISTOR: 10 OHM, 1/4W, 5%, CARBON FILM	
			1	105	R27	347-000005-750	RESISTOR: 750 OHM, 1/4W, 1%, METAL FILM	
			4	106	U28-31	311-000009-017	AMP: OPERATIONAL, +-18VDC, +-100uV INPUT VOLTAGE, TO-99 PACKAGE	OPA602CM (BURR BROWN)
			2	107	C31,35	315-220000-330	CAP: 33PF, .100 LEAD SPACE, 10%, 200V, NPO, CERAMIC MONOLYTHIC	C3(15,20)C330K2G5CA (KEMET)