RECHENRAUM
620 f

REAL-TIME CLOCK

an option for the
Varian Data Machines 620/f
Computer System

Specifications Subject to Change Without Notice

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FOREWORD

The 620/f Real-Time Clock Manual defines and explains the logical, electrical, and mechanical parameters that control the interface between a Varian Data Machines 620/f computer and the real-time clock option.

The six sections of the manual:

- Introduce the real-time clock in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware with drawings, parts lists, and wire lists

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SECTION 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

The *Model 620/f-13 Real-Time Clock (RTC)* is a mainframe option for the Varian Data Machines 620/f computer system. The RTC provides flexible time orientation that can be used for time-of-day accumulation and as an interval timer. Known periods of time are generated by the RTC for program-sequencing. The RTC includes a free-running counter that can be read under program control.

A single circuit card contains the entire RTC. If the power failure/restart (PF/R) option is also used in the computer system, it is located on the same card. The RTC plugs into the central processing unit (CPU) tray of the computer.

The RTC periodically interrupts the main program to initiate subroutines that accomplish the desired real-time functions. The RTC generates two types of interrupts: increment (variable-interval) and overflow. The first is a time-base signal that increments a specific memory address when recognized by the computer. The second interrupt occurs when the incremented memory address reaches a count of 040001.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers and numbers with a leading zero are octal.

1.2 FUNCTIONAL DESCRIPTION

The RTC is functionally divided into seven sections: instruction decode and control logic, free-running counter, divide-by-110 logic, input timing source, variable interval logic, memory overflow detect logic, and interrupt control logic (figure 1-1).

1.2.1 Instruction Decode and Control Logic

This section decodes the internal I/O (AB) bus signals to detect the RTC device address (047) and instructions from the computer. It generates control signals to enable data transfers, assert interrupt addresses on the AB bus, enable or inhibit interrupts, and initialize the RTC.

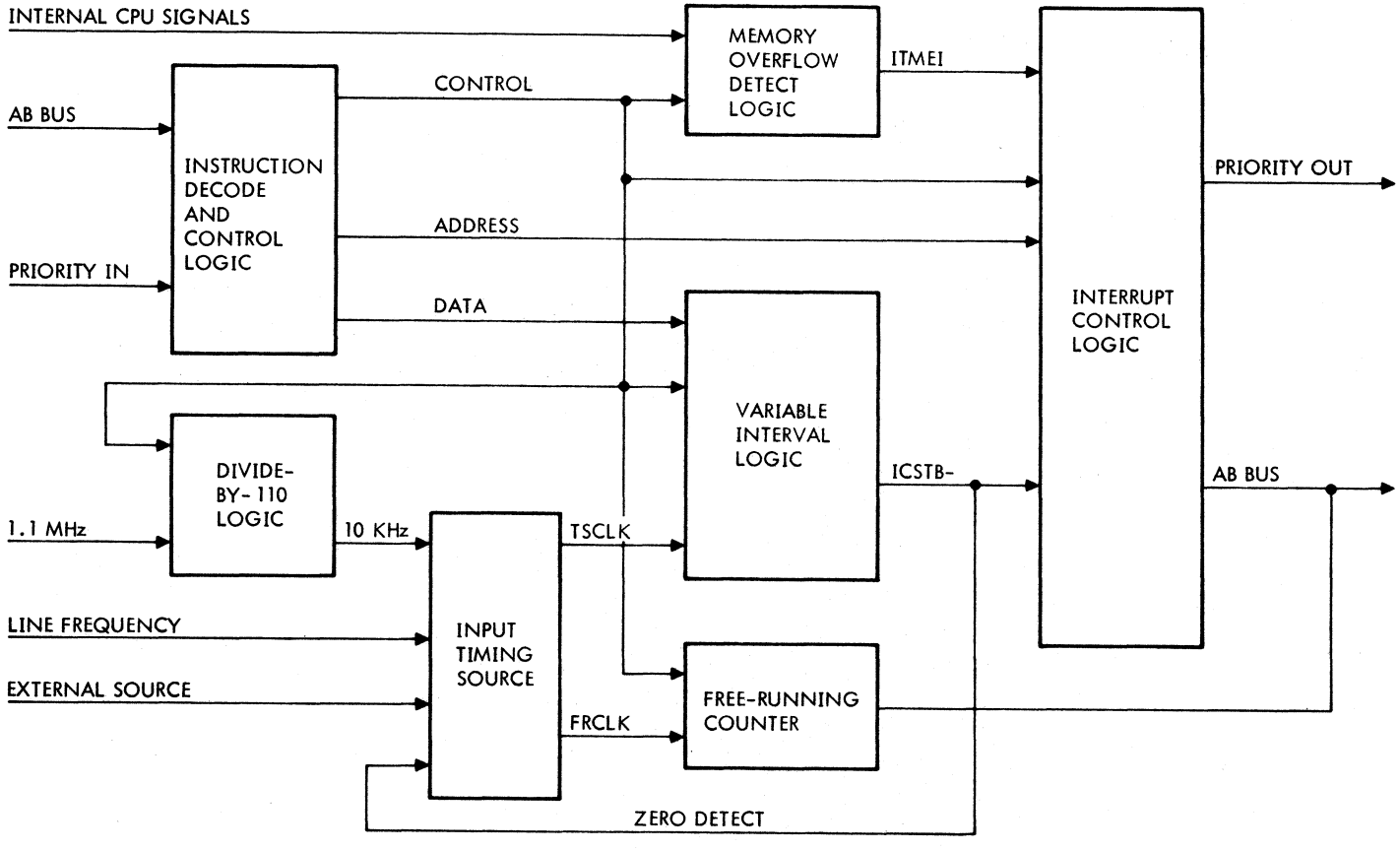

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Figure 1-1. Real-Time Clock Block Diagram

1.2.2 Free-Running Counter

The 16-bit free-running counter (FRC) is continually updated and can be read under program control. The user-selected clock for the FRC can be the 50- or 60-Hz line frequency, a user-supplied external source, the 10-kHz clock, or the variable-interval interrupt rate (section 1.2.5). Unless otherwise specified, the FRC is factory-adjusted for the line frequency source.

1.2.3 Divide-by-110 Logic

This section receives the 1.1-MHz square wave clock signal from the CPU and divides it by 110 to derive a 10-kHz signal. This establishes the variable-interval interrupt rate (section 1.2.5).

1.2.4 Input Timing Source

This section is a frequency-selector circuit that provides the 10-kHz, line frequency, or user-supplied external timing source for use in the variable interval logic and the FRC.

The divide-by-110 logic supplies the 10-kHz clock; the 50- or 60-Hz line frequency is a 24V ac output from the CPU power supply; and the user-supplied external timing source requires minimum up- and down-times of 5 microseconds each.

1.2.5 Variable Interval Logic

This section consists of a 12-bit select register, variable interval counter, and zero detect logic. It generates the variable interval interrupt (VII) rate at which the VII address is incremented.

The VII rate is preset at the factory at 1 kHz, using the following formula:

$$\text{VII rate} = \text{frequency source/selected count}$$

where the frequency source is the 10-kHz signal from the divide-by-110 logic and the selected count is 10. The selected count can be changed under program control and can range from 1 to 4,095.

Memory addresses 044 and 045 are reserved for the VII.

1.2.6 Memory Overflow Detect Logic

This section generates an interrupt request when it detects a count of 040001 in the incremented VII interrupt address (045). Memory addresses 046 and 047 are reserved for the memory overflow interrupt (MOI). The addresses normally contain a Jump and Mark (JMPM) to a suitable interrupt-processing subroutine, but can hold any suitable instruction.

1.2.7 Interrupt Control Logic

This section controls the generation of interrupt requests to the CPU. It stores the occurrence of VII and MOI requests until the interrupts are serviced by the computer. When both types of interrupts are present, the CPU services the VII first.

1.3 SPECIFICATIONS

The physical, electrical, and operating specifications of the RTC are listed in table 1-1.

Table 1-1. Real-Time Clock Specifications

Parameter	Description
Organization	Contains instruction and decode logic, divide-by-110 logic, free-running counter, input timing source, variable-interval logic, memory overflow detect logic, and interrupt control logic.
Priority Assignment	Normally third-highest with respect to DMA/ interrupt priority assignment (exceeded only by the memory protection and power failure/ restart options)

Table 1-1. Real-Time Clock Specifications *(continued)*

Parameter	Description
I/O Capability	Seven external control and eight transfer instructions
Operating Modes	Variable-interval interrupt, memory overflow interrupt, interval accumulation, time-of-day accumulation, and event accumulation
Timing Options	Three hardware-selected timing sources for the variable-interval interrupt and three hardware-selected timing sources for the free-running counter
Timing Sources:	
10-kHz	± 0.1 percent, squarewave; variable interrupt range, 100 microseconds to 409.5 milliseconds (in 100-microsecond increments)
Line Frequency	24V rms, sine wave; variable interrupt range (nominal), 16.7 milliseconds to 68.3 seconds at 60 Hz (in 16.7-millisecond increments) and 20.0 milliseconds to 81.9 seconds at 50 Hz (in 20.0-millisecond increments)
External (User-Supplied)	5.0 microseconds minimum positive and minimum negative duration
FRC Capacity	0177777
Logic Levels:	
I/O	Negative Logic True: -0.5 to +0.5V dc False: +2.4 to +5.0V dc
Internal	Positive Logic True: +2.4 to +5.0V dc False: -0.5 to +0.5V dc

Table 1-1. Real-Time Clock Specifications *(continued)*

Parameter	Description
Size	One 3-by-15-inch (7.7 x 38.1 cm) wired-socket card; shares card with optional PF/R
Interconnection	Plugs into the 620/f CPU motherboard
Input Power	+5V dc ± 5 percent at 2.0 amperes
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

It is recommended that Varian Data Machines Customer Service engineers install the RTC. Logic diagrams, assembly drawings, and wiring information are provided at the time of purchase.

2.1 PHYSICAL DESCRIPTION

The RTC is on a 3-by-15-inch (7.7 x 38.1 cm) wired-socket card (part number 44P0483-001). If the system includes the Model 620/f-14 Power Failure/Restart (PF/R) option, this circuit card is shared with the PF/R. Circuit elements are integrated circuits and discrete components (figure 2-1). All connections to the RTC are made through the 190-terminal card-edge connector, which mates with the corresponding connector in the CPU tray.

2.2 SYSTEM LAYOUT AND PLANNING

The RTC circuit card is located in card slot 14 of the CPU tray. The card slots in the CPU tray, which is mounted in the mainframe, are numbered 1 throuth 14 from rear to front when you face the front panel. Figure 2-2 shows the RTC mounted in the CPU tray.

2.3 SYSTEM INTERCONNECTION

The RTC circuit card is inserted into its designated card slot when the CPU tray is extended out the front of the mainframe and held by an extender assembly bolted to the front of the mainframe.

Insert the card into the mounting guides of slot 14 with the component side of the card toward the backplane connectors.

Apply moderate pressure to seat the card-edge connectors firmly into the mating connectors on the CPU tray. To prevent damage to the connectors or to the nylon guides, ensure that even pressure is applied across the top of the card during insertion.

The card has ejector handles for unseating it from its mating connectors. To remove a card, lift the inside edge of the ejector handles; then lift the card from the slot.

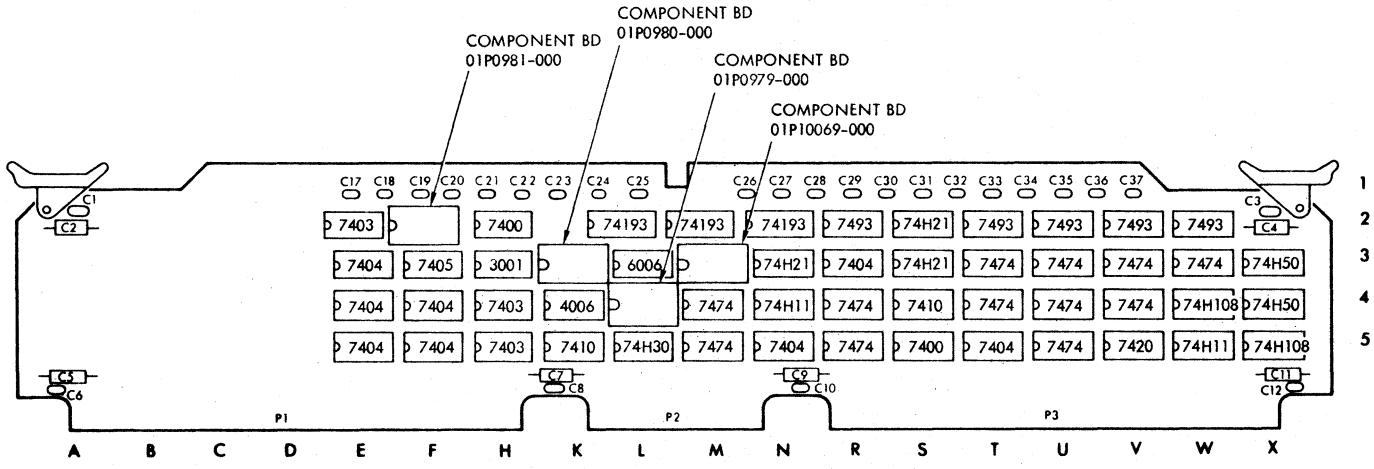

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Figure 2-1. RTC Component Layout Assembly

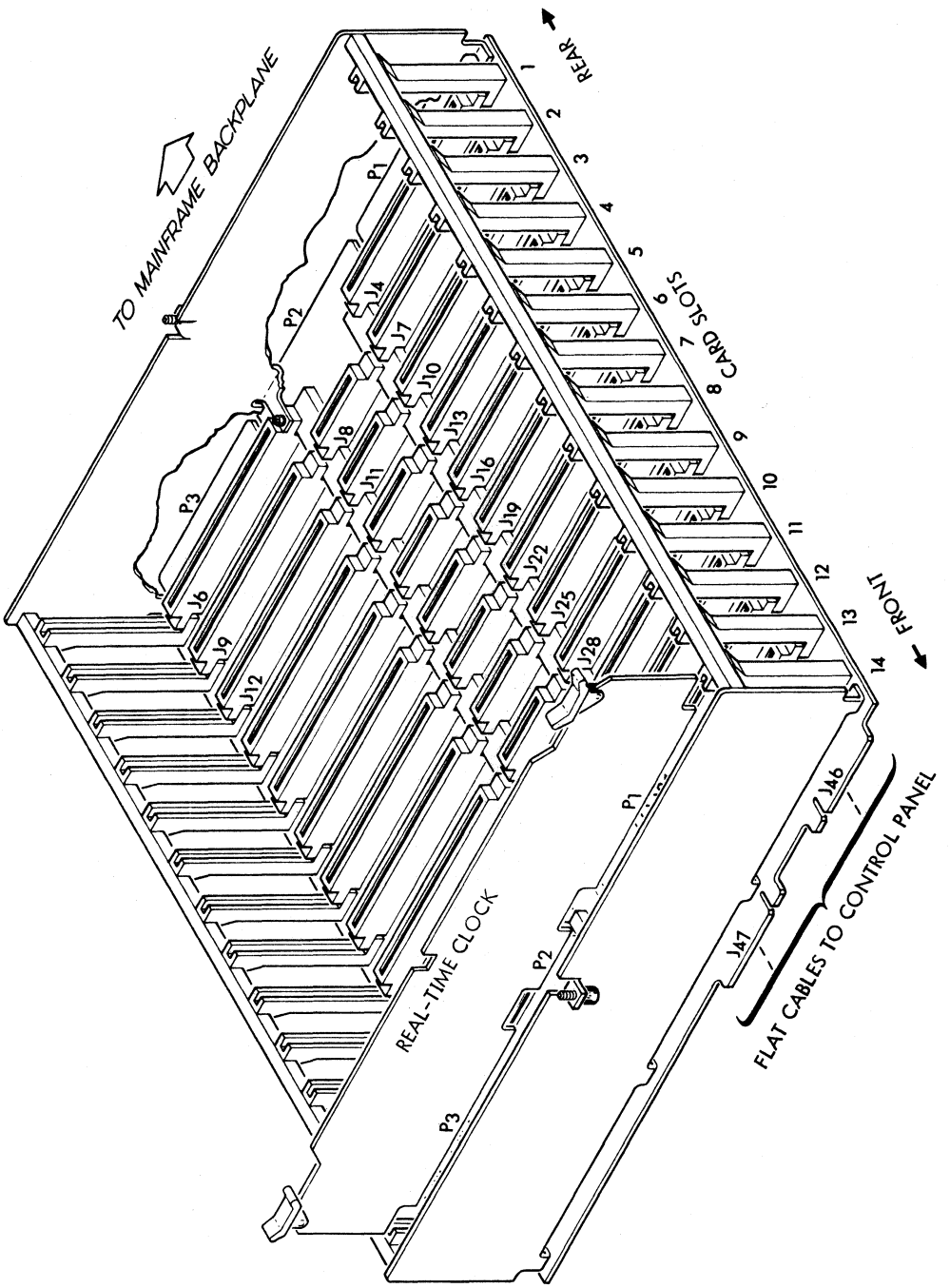

Figure 2-2. RTC Card Location

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SECTION 2
INSTALLATION

2.4 SIGNAL INTERFACES

The RTC interfaces with the computer via the control lines listed in table 2-1. A circuit-card connector pin number follows each signal mnemonic. For definitions of the mnemonics, refer to section 4.8.

Table 2-1. RTC Interface Signals

Signal	Pin Number	Signal	Pin Number
Input			
AB00-C	P1-75	ETR-	P1-54
AB01-C	P1-74	FRYX-C	P1-46
AB02-C	P1-73	INR	P1-57
AB03-C	P1-72	IUAX-C	P1-47
AB04-C	P1-71	IUCX-C	P1-48
AB05-C	P1-70	LFRTC+	P1-53
AB06-C	P1-69	LFRTC-	P1-52
AB07-C	P1-68	OF1	P1-58
AB08-C	P1-67	PRM2X-I	P1-51
AB09-C	P1-66	R14	P1-56
AB10-C	P1-65	SYRT-C	P1-59
AB11-C	P1-64	1.1 MHZ	P1-76
Output			
AB12-C	P1-63	IURX-C	P1-49
AB15-C	P1-60	PRN2X-I	P1-50

2.5 TIMING SOURCE SELECTION

Figure 2-3 illustrates timing source selection wiring for the FRC and the variable interval logic. Optional sources are represented by dashed lines.

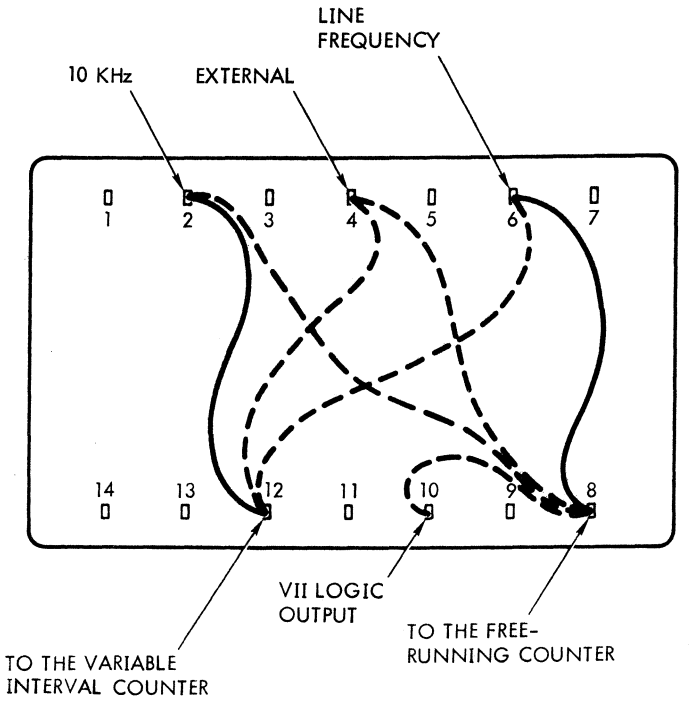

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Figure 2-3. Timing Source Selection Wiring

SECTION 3
OPERATION

There are no operating controls or indicators on the RTC circuit card. Data and control are under CPU program control (refer to section 4.9).

SECTION 4
THEORY OF OPERATION

The following subsections describe the seven functional sections of the RTC: the instruction decode and control logic, free-running counter, divide-by-110 logic, input timing source, variable interval logic, memory overflow detect logic, and interrupt control logic. Table 4-1 lists the RTC functions in relation to the timing and ranges of the variable interval interrupt (VII) and the free-running counter (FRC).

In the following descriptions, numbers in parentheses indicate the location of circuit components on the logic diagrams (section 6). The first number locates the sheet; the following letter and number indicate the area on that sheet. RTC mnemonics are listed in section 4.8.

Table 4-1. Major RTC Functions

Function	Variable-Interval Interrupt Source	Range	Free-Running Counter Source	Range
High-rate interval interrupt and interrupt accumulation	10 kHz	100 microsec to 409.5 msec in 100-microsec increments	VII rate	6.5 sec to 7.46 hr depending on interrupt rate
High-rate interval interrupt and event accumulation	10 kHz	Same as above	External	Up to 65,536 events
High-rate interval interrupt and time-of-day accumulation	10 kHz	Same as above	Line frequency	Up to 18.2 min
High-rate interval interrupt and high-rate interval accumulation	10 kHz	Same as above	10 kHz	6.5 sec in 100-microsec increments
Low-rate interrupt and interrupt accumulation	Line frequency	16.7 msec to 68.3 sec in 16.7-msec increments	VII rate	18.2 min to 51.8 days depending on interrupt rate

SECTION 4
THEORY OF OPERATION

Table 4-1. Major RTC Functions *(continued)*

Function	Variable-Interval Interrupt Source	Range	Free-Running Counter Source	Range
Low-rate interrupt and event accumulation	Line frequency	Same as above	External	Up to 65,536 events
Low-rate interrupt and time-of-day accumulation	Line frequency	Same as above	Line frequency	Up to 18.2 min
Low-rate interrupt and time-of-day accumulation	Line frequency	Same as above	10 kHz	6.5 sec in 100-microsec increments
Event count interrupt and interrupt accumulation	External	One to 4,095 events	VII rate	65,536 to 268 million events depending on interrupt rate
Event count interrupt and event accumulation	External	Same as above	External	Up to 65,536 events
Event count interrupt and time-of-day accumulation	External	Same as above	Line frequency	Up to 18.2 min
Event count interrupt and time-of-day accumulation	External	Same as above	10 kHz	6.5 sec in 100-microsec increments

4.1 INSTRUCTION DECODE AND CONTROL LOGIC

The instruction decode and control logic consists of receivers and drivers, flip-flops, inverters, logic gates, and an instruction decoder. These logic components decode instructions from the CPU and generate the control signals to enable data transfers, mask or unmask interrupts, and initialize or clear the RTC.

The 16-bit bidirectional internal I/O (AB) bus interfaces (sheet 2) the RTC and the CPU (AB00-C through AB15-C). Instructions or data are accepted by the receivers and data are transmitted by the drivers. ITAB01, ITAB02, and ITAB05 assert the RTC interrupt addresses on the AB bus.

The instruction decoder (3G2) is a 3-to-8-line decoder. It decodes DCB06, DCB07, and DCB08 into one of eight states, DC00- through DC07-. These signals enable or disable logic functions in the RTC circuits. The instruction decoder is enabled by FRYX-C, DCB11, and DCDA47.

Memory overflow enable flip-flop DCMOE (3E1) activates the memory overflow detect logic. DCMOE is preset by DC01- to enable the RTC. The memory overflow detect logic is disabled by clearing the flip-flop with DC02-, DC03-, DC04-, or SYRT-C. The same logic deciphering is true for the set and reset conditions of variable interrupt enable flip-flop DCVIE (3D1). This signal activates the interrupt control logic (sheet 8).

Data transfer in and transfer out instructions, with DCFRY and DCDA47, are decoded by DCDI (3C4) and DCDO (3C3), respectively. DCDI presets flip-flop DCDTI, indicating that FRC data are to be transferred to the CPU. DCDO presets flip-flop DCDTO, indicating that the RTC is accepting select register data from the CPU. DCDTI and DCDTO are clocked by DCDRY- and DCRST-.

The RTC device address is DCDA47 (3D4). The states of AB00 through AB05 are decoded by a NAND gate and inverter in the presence of the interrupt acknowledgement signal to generate DCDA47.

Computer signals (3G4) IUCX, IUAX, FRYX, and DRYX are inverted and generated to various functional circuits. DCPRM (3E4) is a priority signal from a higher-priority device. It is the inversion of PRM2X-. DCRST (3F4) is a system reset or initialize RTC signal and is generated to various functional circuits.

SECTION 4
THEORY OF OPERATION

4.2 FREE-RUNNING COUNTER

The FRC (sheet 7) consists of 16-bit binary flip-flops and can be read under program control. One application of the FRC is to indicate to the CPU elapsed time. By subtracting a previous count from the current count, the CPU can determine the number of events in a given period of time, time of day, and large quantities of elapsed time. The FRC is controlled by flip-flop FRCL (7H2) and gating circuits.

FRCL is clocked by FRCLK (7H4). The output of FRCL is the conditioned clock input to the 16-bit FRC flip-flops. The direct clock input sets FRCL, thereby clocking the FRC. FREN (7H3) presets FRCL. This gate prevents FRCLK- from clearing FRCL during a data transfer in (DCDTI-).

DC00- (7G3) is output by the instruction decode logic. It goes to ground during an EXC 047 instruction, clearing the FRC. DC00- goes to the FRC as well as to the reset input of FRCL. When an EXC 047 instruction is executed, FRCL is initialized high and other FRC flip-flops, to zero. This provides a point of reference for the program in computing elapsed time and time of day. The FRC outputs (FRC00-15) are routed to the AB bus.

4.3 DIVIDE-BY-110 LOGIC

The divide-by-110 logic (top half of sheet 4) counts down the CPU 1.1-MHz clock to 10 kHz. TR10K (4E2) is input to the input timing source; it is the 10-kHz signal used as a possible input to the variable interval logic.

The divide-by-110 counter consists of flip-flops and gating logic. The first six flip-flops are decoded so that the maximum count is 54. The decode is accomplished by TSCNT5 (4F2); its output is generated to TSR54 (4E3) when the count number is 55. Note that TSCNT5 is coupled to the D input of TSR54, which is set by the following clock pulse (TSCP-) (4E4). TSR54 serves two purposes. Its output, TSR54-, is directed back to clear and recycle the previous six-stage counter. TSR54- (4D3) also toggles TR10K (4E2), generating the 10-kHz input to the input timing source. The divide-by-110 counter can be reset by DC06-, DCDTO-, or DCRST- (4D2). These signals are control signals derived from the instruction decode and control logic.

4.4 INPUT TIMING SOURCE

The input timing source consists of the line frequency and external buffer circuits (lower half of sheet 4). The outputs of these two circuits are routed to a frequency-selector connection. TR10K from the divide-by-110 logic is also routed to this connection.

The frequency-selector connection selects the 10 kHz output of the divide-by-110 logic 50- or 60-Hz line frequency, external source, or VII rate for timing RTC functions. TSCLK (4C1) can be connected either to the 10 kHz, external source, or line frequency and FRCLK (4B1) can be connected to either the line frequency, external source, or the VII rate.

The external source circuit consists of a pair of inverters (4B4) that buffer the external timing source going into the frequency-selector connection. The line frequency circuit (4C2, 4C3, and 4C4) filters out noise and shapes a pulse going to the frequency connection. The line frequency is 24V ac rms.

4.5 VARIABLE INTERVAL LOGIC

The variable interval logic provides the VII rate to the CPU to increment memory address 045. In the interrupt control logic, the VII rate generates the interrupt request (IURX-C) signal.

The variable interval logic can be divided into two subfunctional circuits.

The first circuit consists of a 12-bit select register (sheet 5) that can be programmed via the instruction and control logic. The 12-bit select register consists of 12 D-type flip-flops loaded (DCB00 through DCB11) with a binary number proportional to the desired time interval. This binary number is routed to the D inputs of the flip-flops. All 12 flip-flops are clocked by DCDTO (5B3, 5D3, and 5G3), indicating a data transfer out is in process. The flip-flop outputs are transferred to the 12-bit up counter (sheet 6). The 12-bit register can be cleared by DCRST (5B2, 5D2, and 5G2).

The second circuit consists of logic gates, flip-flops, and a 12-bit up counter (sheet 6). ICR00- through ICR11- (6E2, 6E3, and 6E4) are transferred into the 12-bit up counter by ICLD- (6G2) for increment processing. ICLD- is derived by flip-flops ICKK- (6G3) and ICLFF (6G2). ICLD- is generated by ICCTI (6C1), indicating an all-ones minus one condition being decoded. The loading of the up counter is synchronized with TSCLK (6G4) so that the up counter does not attempt to load and increment at the same time.

Also, under logic control utilizing ICKK- and ICLFF, the 12-bit up counter is incremented to zero by ICCLK (6F2). Note that, if the 12-bit select register is set to zero, the up counter reacts as if the count were 4,096. When the up counter reaches zero, it is again loaded and incremented. The VII continues to occur at a rate determined by the frequency source and the 12-bit select register, until changed under program control. ICSTB- (6F4), derived from ICCTI and TSCLK, is then routed at the VII rate to the interrupt control logic for interrupt processing.

4.6 MEMORY OVERFLOW DETECT LOGIC

The memory overflow detect logic (top half of sheet 8) interrupts the CPU, when the contents of memory address 045 overflow. Prior to incrementation, the contents of the memory address specified by the INR instruction in address 044 (typically address 045) are placed in the R register of the CPU and the RTC memory overflow detect logic checks the 15th bit during the execution of an Increment Memory and Replace (INR) instruction and CPU operand fetch time (OF1). If this bit is set, indicating a count of 040001 or more, the RTC records an overflow interrupt for processing by the CPU. This processing uses storage addresses 046 and 047, which usually contain a Jump and Mark (JMPM) instruction but can hold any suitable instruction.

The memory overflow detect logic contains gates and flip-flops for generating the MOI request (ITMFI) signal (8F1). Flip-flop ITEMT (8G3) is clocked by OF1 (8G4) and set by ITED- (8H4), indicating that the VII is in process and that the memory overflow condition is inhibited. Flip-flop ITMFL (8F2) is clocked by ITPIP (8F3) and set by ITMDS- (8F3), indicating memory overflow. The detecting of memory overflow is further scrutinized by ITMFS (8F2). This signal indicates that memory overflow exists and the VII request is not pending. Flip-flop ITMFI (8F1) is set if it is enabled by DCMOE, ITMFS, and ITVII-. The output of ITMFI is the MOI request that is transferred to the interrupt control logic to generate IURX-C. When the CPU has acknowledged the MOI request, ITMFL (8F2) is reset by ITRST-, and ITMFI (8F1) is reset by DCRST-, synchronized with IUCX-C.

4.7 INTERRUPT CONTROL LOGIC

The interrupt control logic consists of gates and flip-flops for generating IURX-C and addresses, and ensuring RTC priority.

The interrupt process is initiated by ICSTB- (8E4) setting ITVIL (8D3). Every time the up counter cycles, ICSTB- sets ITVIL, indicating a VII is in process. ITVII (8D2) is then set, generating the VII request when the VII is enabled and the MOI is not in process. ITVIL and ITVII can be cleared by SYRT-C, when the CPU is transferring data out, or when the VII up counter is initialized. Priority output signal PRN2X- (8D1) is generated to lower-priority I/O devices to indicate that the RTC has interrupt priority.

IURX-C is generated to the CPU by ITMFI or ITVII, along with DCPRM. ITINT- (8C3) low indicates that the interrupt request flip-flop is set and no higher-priority interrupt request is active. Either a VII or MOI request signal can then request the CPU to execute an instruction.

The interrupt addresses are ORed with the output of the FRC and the interrupt request logic. When ITAB01 (8A3), ITAB02 (8C2), and ITAB05 (8B2) are high, the interrupt addresses (either 044 and 045 or 046 and 047) are asserted at the AB bus, indicating an RTC interrupt is being processed. When an interrupt is being processed, data are not transferred in and, when the FRC is being read, the interrupt addresses are inhibited.

4.8 MNEMONICS

The mnemonics used in the RTC are listed alphabetically in table 4-2. The source column lists the location of the signal's source on RTC logic diagram 91C0259; the first number is the drawing sheet number and the following letter and number, the location coordinates (refer to section 6). Each signal's function is briefly described.

Table 4-2. RTC Mnemonic Definitions

Mnemonic	Source	Description
AB00-C to AB15-C	2	Bidirectional internal I/O (AB) bus data lines
B10	3G3	Inverted source of AB10-C to the computer
DCB00-14	2	AB bus data lines to the RTC
DCDA47	3D3	Device address from the AB bus

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DCDI	3C4	Data input command from the AB bus
DCDRY	3G4	Indicates data are on the AB bus
DCDTI	3C3	Data transfer in flip-flop; indicates the free-running counter value is being transferred to the AB bus
DCDTIA	3B3	Same as DCDTI
DCDTO	3C2	Data transfer out flip-flop; indicates the interval select register count is being transferred from the AB bus
DCDA47-	3D4	Device address decoded from the AB bus
DCEN	3G2	Indicates an external control instruction is on the AB bus
DCFRY	3G4	Indicates the device address and function to be performed are on the AB bus
DCIUA	3G4	Interrupt acknowledgement
DCIUC	3H4	1.1-MHz squarewave from the computer
DCMEN-	3E1	Set MOI mask; clears DCMOE
DCMOE	3F1	MOI enable flip-flop
DCPRM	3E4	Priority-in input; indicates whether a higher-priority device has requested an interrupt
DCRST	3F4	Device reset; indicates a system reset or an initialize RTC instruction has been issued

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DCVCR-	3E1	Reset VII mask; sets the VII enable flip-flop
DCVEN-	3C1	Set VII mask; clears DCVIE
DCVIE	3D1	VII enable flip-flop
DC01-07	3G1, 3H1	Clear FRC; decoded from the AB bus
DRYX-C	3G4	Indicates data are on the AB bus
ETR	4B4	External timing source
FRCL	7H2	FRC clock
FRCLK	4B1	Input to the FRC from the frequency-selector circuit; produces FRCL
FRC00 to FRC15	7	FRC outputs
FREN	7H3	Enables FRC clock flip-flop; set by the negative-going edge of FRCLK
FRRST	7G3	Reset FRC
FRYX-C	3G4	Indicates the device address and instruction are on the AB bus
GNDXY	3, 6, 7	Ground source
ICCLK	6F2	Interval counter clock

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
ICCTA ICCTB ICCTC	6C3 6D2	Outputs generated by each stage of the interval counter; produce ICCT1
ICCT1	6C1	Interval counter output; set when the count is 4,095
ICC00 to ICC11	6D2, 6D3, 6D4	Outputs of the interval counter
ICDOA ICDOB ICDOC	5A3, 5D3, 5G3	Interval select register clock; indicates count set data are on the AB bus
ICKK	6F3	Flip-flop output following the interval counter clock source
ICKR	6G3	Preset input to the ICKK flip-flop
ICLD-	6G1	Loads the interval counter with the contents of the interval select register
ICLFF	6G2	Generated when the interval counter value is 4,095 or when ITRST- is active; produces ICLD-
ICR	6G4	With ICKK, produces ICKR; generated by a zero level on TSCLK or ITRST-
ICRSA ICRSB ICRSC	5B2, 5E2, 5G2	Initialize interval select register to 012

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
ICR00 to ICR11	5	Interval select register outputs
ICSTB-	6F4	VII rate; goes to the interrupt control logic to generate a VII request
INR	8F4	Indicates an INR instruction is being executed
INT	8B2	Indicates an interrupt is to be processed and that request line IURX-C can be set; produced by ITINT and DCIVA
ITAB01 ITAB02 ITAB05	8B1, 8C2 8B3	Signals indicating interrupt addresses in memory when requesting an interrupt, and FRC0x when reading the FRC
ITEDS-	8H4	Enables a memory overflow check produced when a VII is processed
ITEMT	8G3	Enables memory overflow check gate; set by ITEDS-
ITFIP	8F3	Generated by FRYX-C, IUAX-C, and PRMX-C during interrupt processing
ITINT	8C2	Indicates the interrupt request flip-flop is set and no higher-priority line is active
ITIVI	8E3	Sets the VII request flip-flop
ITMDS-	8G3	Memory overflow indication

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
ITMFI	8F1	MOI request flip-flop output
ITMFI	8F1	Indicates the MOI request flip-flop is set and no higher-priority interrupt line is active
ITMFII	8F1	Sets the MOI request flip-flop
ITMFL	8F2	Set output of MOI request flip-flop; reset by ITFIP
ITMFS	8F2	Indicates that memory has overflowed, but a VII request is not pending
ITRST-	8D4	Reset; active during data output, system reset, and RTC and interval counter initialization
ITVII	8D2	VII request flip-flop output
ITVIL	8D3	Flip-flop set by a VII and reset by ITFIP
ITOF1	8G3	Indicates CPU state 1 is active
IUAX-C	3G4	Interrupt acknowledgement from the computer
IUCX-C	3H4	1.1-MHz clock from the computer
IURX-C	8C2	Interrupt request to the computer
LFRTC	4C4	24V ac output from the computer power supply

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
LFRTC1,2	4C3	Intermediate stage outputs of the Schmidt trigger circuitry
OF1	8G4	CPU state 1
PRM2X-I	3E4	Priority-in input from a higher-priority controller
PRN2X-I	8D1	Priority-out output to a lower-priority controller
R14	8F4	Indicates that bit 14 of the R register is set
SYRT-C	3F4	System reset
TR10K	4F2	10-kHz output of the divide-by-110 logic
TSCLK	4C1	Variable interval logic clock
TSCLR	4D3	Resets the divide-by-110 logic
TSCNT5	4F2	Flip-flop set when the divide-by-110 count is 53
TSCP	4G4	1.1-MHz clock input to the divide-by-110 logic
TSETS	4B3	External timing source input to the variable interval logic and the FRC
TSLFA TSLFB	4C3	Intermediate stage outputs of the Schmidt trigger circuitry

Table 4-2. RTC Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
TSLFS	4C2	60-Hz line frequency source input to the variable interval logic and the FRC
TSRST-	4D2	Resets the divide-by-110 logic
TSR01, 04, 16, 32, 54	4E2, 4E3, 4H2, 4H3	Intermediate outputs of the divide-by-110 logic
TSR8	4H2	Intermediate stage output of the divide-by-110 logic
W1001,2	6E3, 6E4	Carry outputs of the interval counter
1.1MHZ	4H4	1.1-MHz clock to the divide-by-110 logic

4.9 PROGRAMMING

4.9.1 Considerations

The user writes the RTC service routines. The RTC device address is 047. Interrupt addresses 044 and 045 process variable interval (increment) interrupts, and addresses 046 and 047 process overflow interrupts.

If the memory overflow interrupt is used, 044 is loaded with an INR instruction and 045 is incremented. Normally a JMPM to a suitable processing subroutine is loaded in 046 and 047. However, if the overflow interrupt capability is not used, 044 and 045 contain the JMPM.

4.9.2 Restrictions

In a system including the priority memory access (PMA), two-word I/O instructions OME and IME (section 4.9.3) cannot be used for communication with the RTC. Intervening PMA cycles can lock the variable interval logic indefinitely (OME), or the FRC count can be lost (IME).

The RTC service routine must conclude with enabling instructions for other internal computer options (e.g., the priority interrupt module) whose interrupt requests have been inhibited.

4.9.3 Description of Instructions

The RTC responds to the seven external control (EXC) and eight transfer instructions listed in table 4-3.

Table 4-3. RTC Instructions

Mnemonic	Code	Description
External Control		
EXC 047	0100047	Clear FRC; the FRC cannot otherwise be reset
EXC 0147	0100147	Enable RTC interrupts; pending RTC interrupts are immediately processed
EXC 0247	0100247	Inhibit memory overflow interrupts; inhibits only overflow interrupts
EXC 0347	0100347	Enable variable interval interrupts; inhibits overflow interrupts

Table 4-3. RTC Instructions *(continued)*

Mnemonic	Code	Description
EXC 0447	0100447	Initialize RTC; inhibits all interrupts and resets the interrupt control logic and divide-by-110 logic
EXC 0647	0100647	Initialize variable interval counter; loads the contents of the interval select register in the interval counter and resets the divide-by-110 logic
EXC 0747	0100747	Inhibit variable interval interrupt
Transfer		
OAR 047	0103147	Output A register to interval select register
OBR 047	0103247	Output B register to interval select register
OME 047*	0103047	Output memory to interval select register

NOTE

The above instructions load the 12-bit interval select register with the selected count, reset the divide-by-110 logic and the MOI requests in the interrupt control logic, and load the variable interval counter with the new count.

Table 4-3. RTC Instructions *(continued)*

Mnemonic	Code	Description
INA 047	0102147	Input FRC contents to A register
INB 047	0102247	Input FRC contents to B register
IME 047*	0102047	Input FRC contents to memory
CIA 047	0102547	Clear and input FRC contents to A register
CIB 047	0102647	Clear and input FRC contents to B register

* Cannot be executed in a system that includes the PMA.

4.9.4 Sample Program

Table 4-4 shows a typical service routine for the RTC.

Table 4-4. Typical Service Routine

```
                    ***RTC INITIALIZATION CODING***

                SET INTV = 1000 (interrupts to occur once each second)
                SET INSC = 10 (variable interval interrupts, 1 per million)

                EQU     1000
                ORG     044             INITIALIZE ADDRESSES 044-047
                INR     * + 1
PERIOD          DATA    040001-INTV
                JMPM    TIMUP
```

Table 4-4. Typical Service Routine *(continued)*

Mnemonic		Code	Description
		INITIALIZE RTC	
	ORG	0500	
INSK	DATA	INSC	INTERVAL SELECT COUNT
BEGIN	EXC	0447	INITIALIZE RTC
	EXC	047	CLEAR FRC
	LDA	INSK	
	OAR	047	OUTPUT INT SEL COUNT
	EXC	0147	ENABLE RTC
		(USER'S PROGRAM)	
		INTERRUPT PROCESSOR	
	ORG	01000	
TIMUP	ENTR	0	PROGRAM COUNTER STORED
	EXC	0247	INHIBIT MOI
	STA	SAVEA	SAVE A REGISTER CONTENTS
	LDAI	040001-INTV	REINITIALIZE RTC COUNTER
	STA	PERIOD	
		(Other instructions can be inserted here)	
	LDAI	0	RESTORE A REG
SAVEA	BES	0	
	EXC	0147	ENABLE MOI
	JMP*	TIMUP	RETURN TO INTERRUPT
	END		

SECTION 5
MAINTENANCE

RTC maintenance consists of running the RTC test program, troubleshooting, and making repairs, if required. The RTC test program (part number 98A0105-001), described in the 620 test programs manual (document number 98 A 9908 960), in conjunction with the 620/f maintenance manual (document number 98 A 9908 050), help isolate an error condition. Troubleshooting is facilitated by familiarization with the operation of the RTC and use of the logic diagram (section 6).

5.1 EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the RTC.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM265 Extender Card, part number 44P0437

d. CPU Extender Cables

e. Card Puller, Titchener type 1731

5.2 TEST PROGRAM

The RTC test program is an integral part of the MAINTAIN II test program system. It is provided as part of the regular troubleshooting package for the 620/f computer.

RTC operation should be periodically checked with the RTC test program, under the control of the test executive program (part number 92A0107-001). The variable interval and memory overflow interrupts and the free-running counter are software-timed and tested. Malfunctions are reported in the form of error messages and/or codes.

The RTC test program is described in detail in the 620 test programs manual (document number 98 A 9908 960).

SECTION 5
MAINTENANCE

5.3 TROUBLESHOOTING

With the computer turned off and the control panel opened on its hinges, disconnect the CPU tray from the motherboard. Extend the CPU tray out the front and connect an extender cable between CPU tray connectors P1, P2, and P3 and backplane connectors J8, J9, and J10. Firmly attach the CPU tray to a bracket mounted on the front of the mainframe.

After removing the card retainer bar, install the RTC card (DM265) on an extender card (part number 44P0437).

The computer can then be turned on to begin troubleshooting.

5.3.1 Input Power

Verify +5V dc ± 5 percent and common (ground) at the following locations:

+5V dc	Common
P1-75	P1-1
P1-78	P1-2
P1-79	P1-3
P1-80	P1-4
P3-1	P3-77
P3-2	P3-78
P3-3	P3-79
P3-4	P3-80

5.3.2 Divide-by-110 Logic

Verify 1.1 MHz ± 0.1 percent squarewave input at P1-76, and 10-kHz ± 0.1 percent squarewave output at M3, pin 2.

5.3.3 Schmitt-Trigger Circuit

Verify 24V rms, 50- or 60-Hz ± 5 percent sinewave input at P1-53; common at P1-52; and 50- or 60-Hz ± 5 percent squarewave output at M3, pin 6. Check that the output signal follows the input signal.

5.3.4 External Timing Source

If the user-supplied external timing source (M3, pin 4) is jumpered to either pin 8 (free-running counter) or pin 12 (variable interval counter) of M3:

a. Apply + 5 ± 0.5V dc to P1-55. Measure + 5 ± 0.5V dc at M3, pin 4.

b. Apply 0.0 ± 0.5V dc to P1-55. Measure 0.0 ± 0.5V dc at M3, pin 4.

5.4 REFERENCE DOCUMENTS

In addition to this manual, the documents listed below are useful aids to understanding and maintaining the RTC.

a. 620/f Reference Handbook (98 A 9908 001)

b. 620/f Maintenance Manual (98 A 9908 050)

c. 620 Test Programs Manual (98 A 9908 960)

d. DM256 Assembly Drawing (44D0483-001)

e. DM256 Logic Diagram (91C0259)

f. DM256 Wire List (95W0721)

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains logic schematics and parts information for the RTC.

2 1

REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
A		PRODUCTION RELEASE EN 5106	[illegible]	12/14/70

NOTES: (UNLESS OTHERWISE SPECIFIED)

REFERENCE DESIGNATIONS	
LAST USED	NOT USED

REFERENCE DRAWINGS	
44D0483	ASSEMBLY
44P0483	PARTS LIST
95W0722	WIRE LIST

DR	[illegible]	12/4/70
CHK		
DSGN		
ENGR	[illegible]	12/14/70
APPD	[illegible]	12/14/70
APPD	[illegible]	12/14/70

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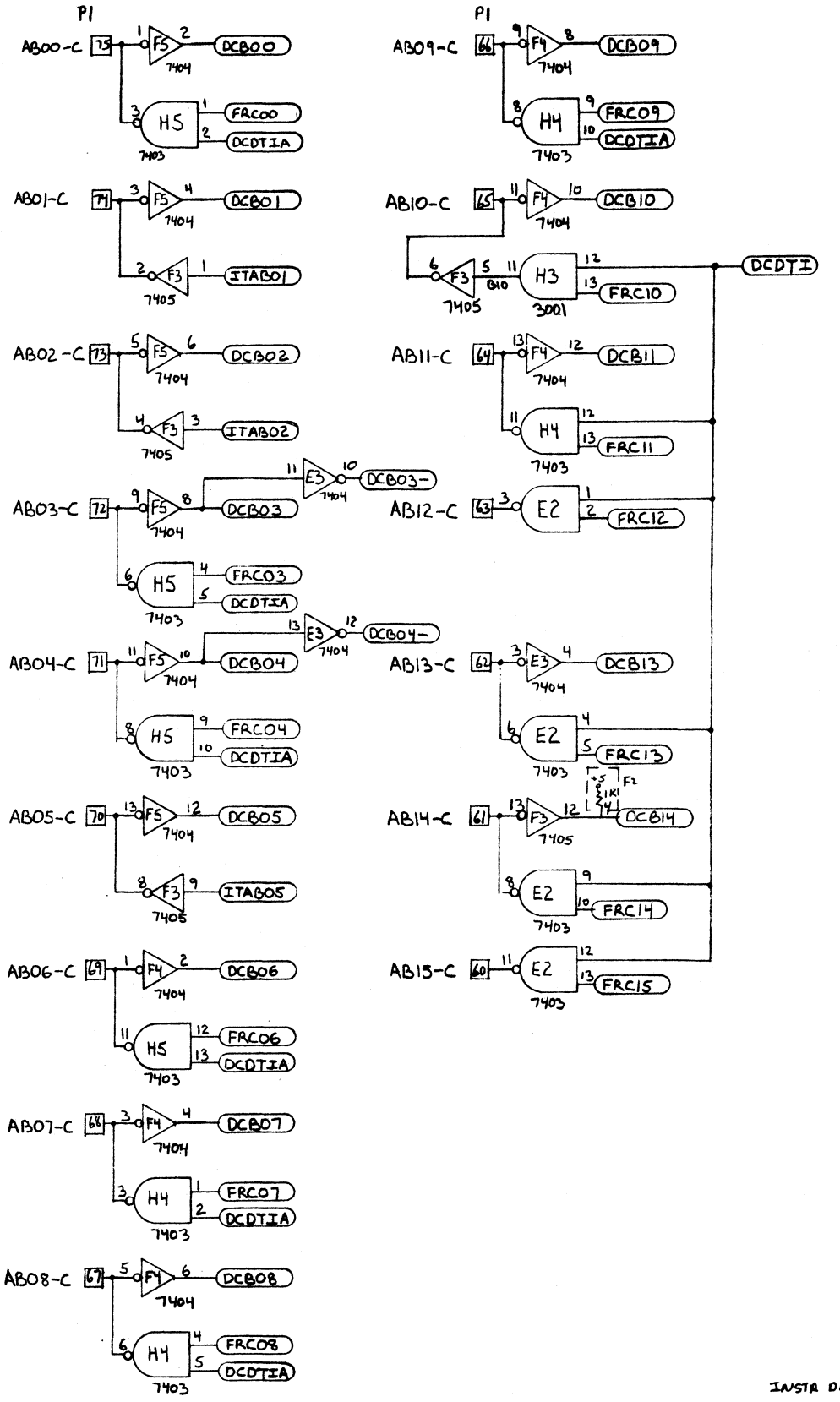
TITLE
LOGIC DIAGRAM-REAL TIME CLOCK

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0259	A

SCALE ——— SHEET 1 OF 8

3/70 DIETERICH-POST CLEARPRINT 1000H-6



INSTR DECODE AND CONTROL LOGIC

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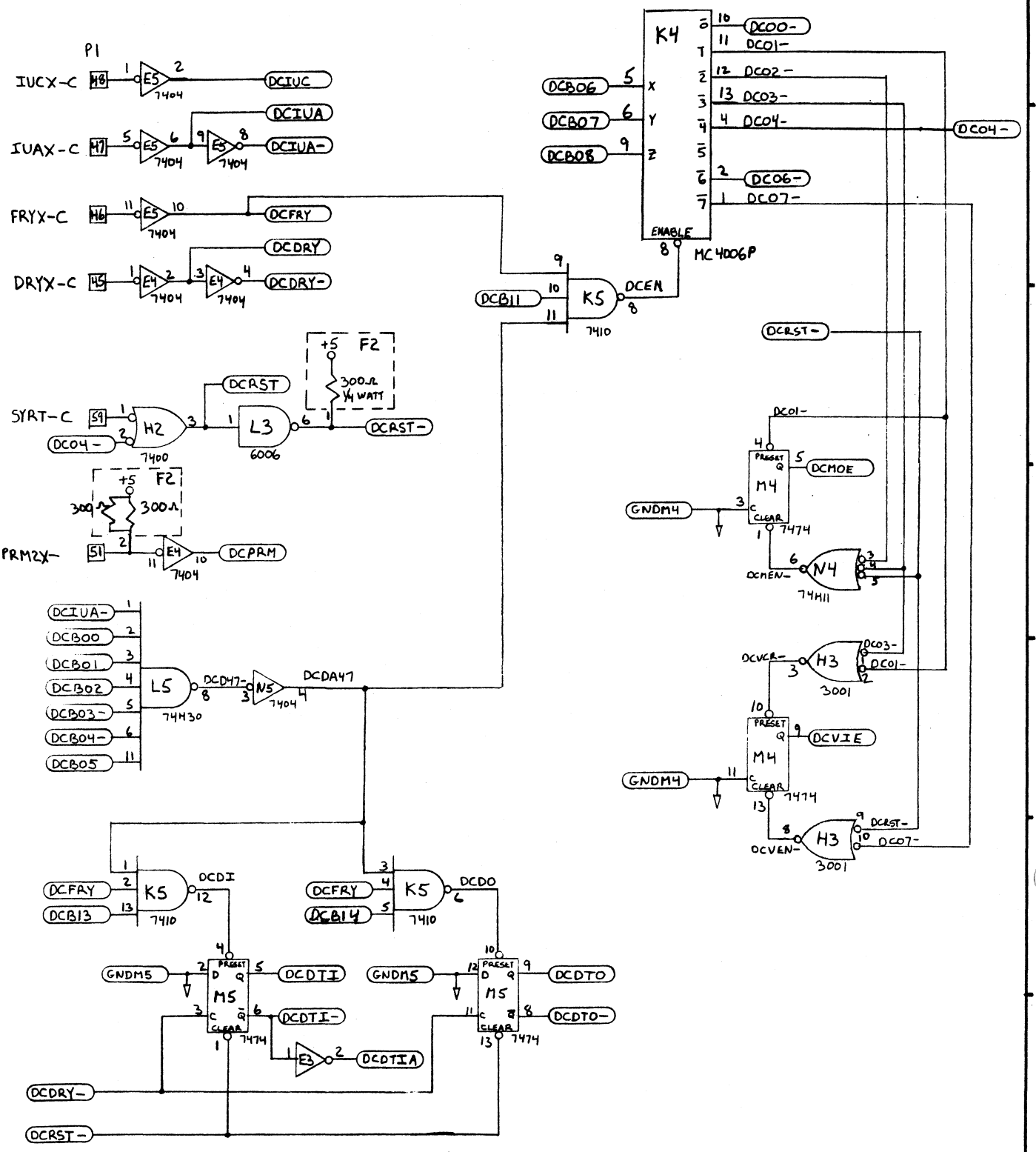
SCALE	J.F. Buddy	SHEET 2 OF 8	



INSTR DECODE AND CONTROL LOGIC

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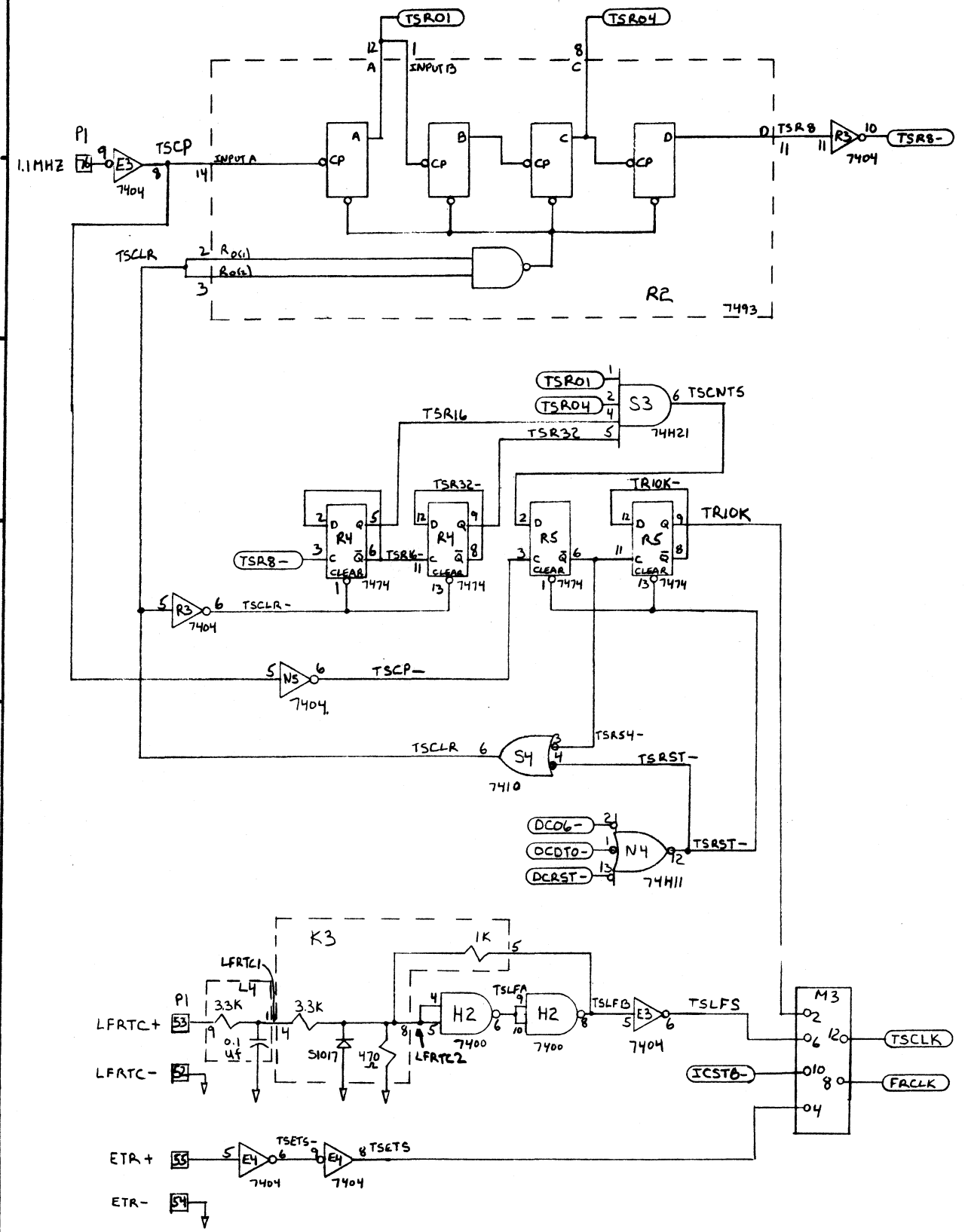
SCALE		SHEET 3 OF 8	

1/70 DIETZGEN-POST CLEARPRINT 300SH-8



DIVIDE BY 110 AND TIMING SOURCE INPUT CIRCUITS

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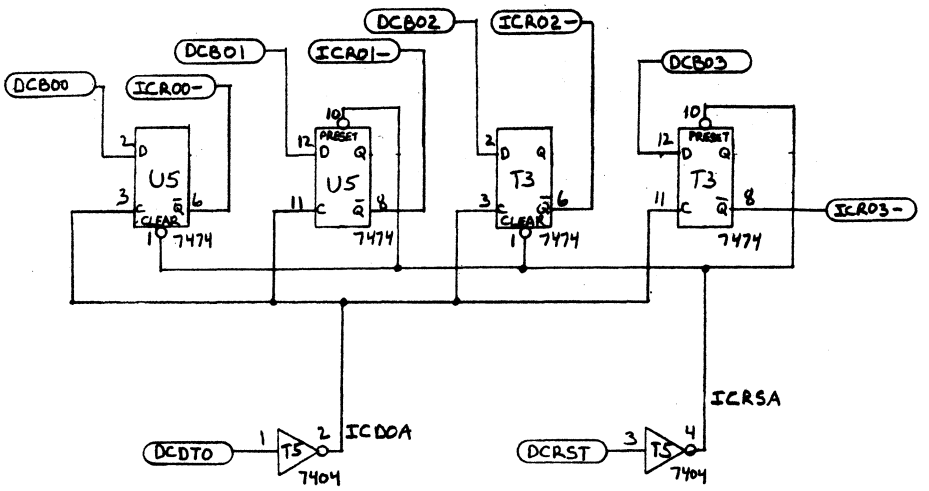
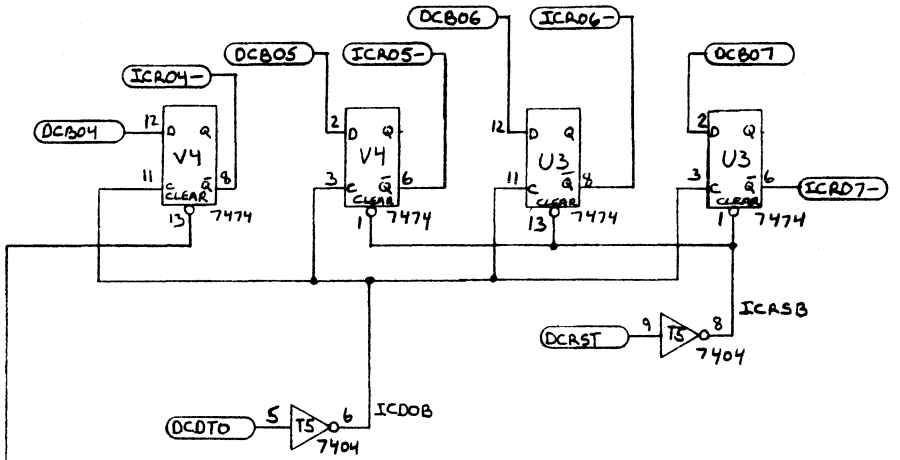
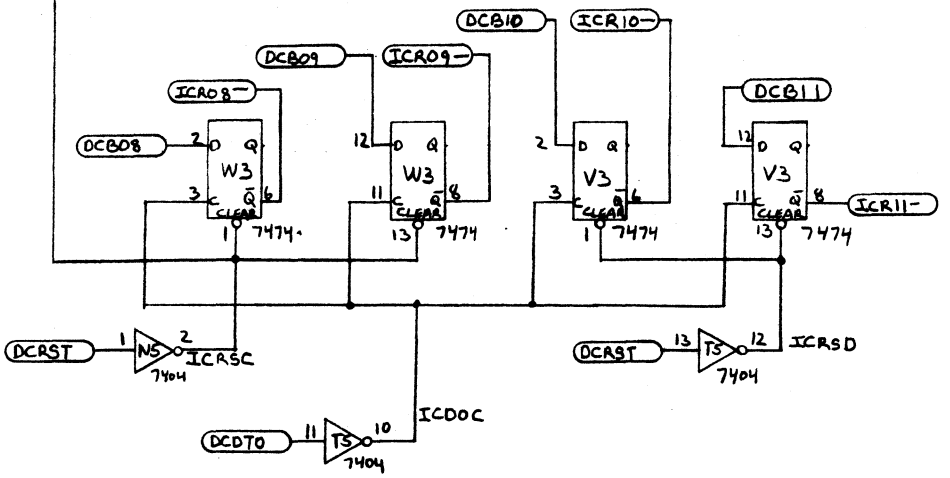
SCALE		SHEET 4 OF 8	

1/70 DIETRICH-FOST CLEARPRINT







VARIABLE INTERVAL LOGIC

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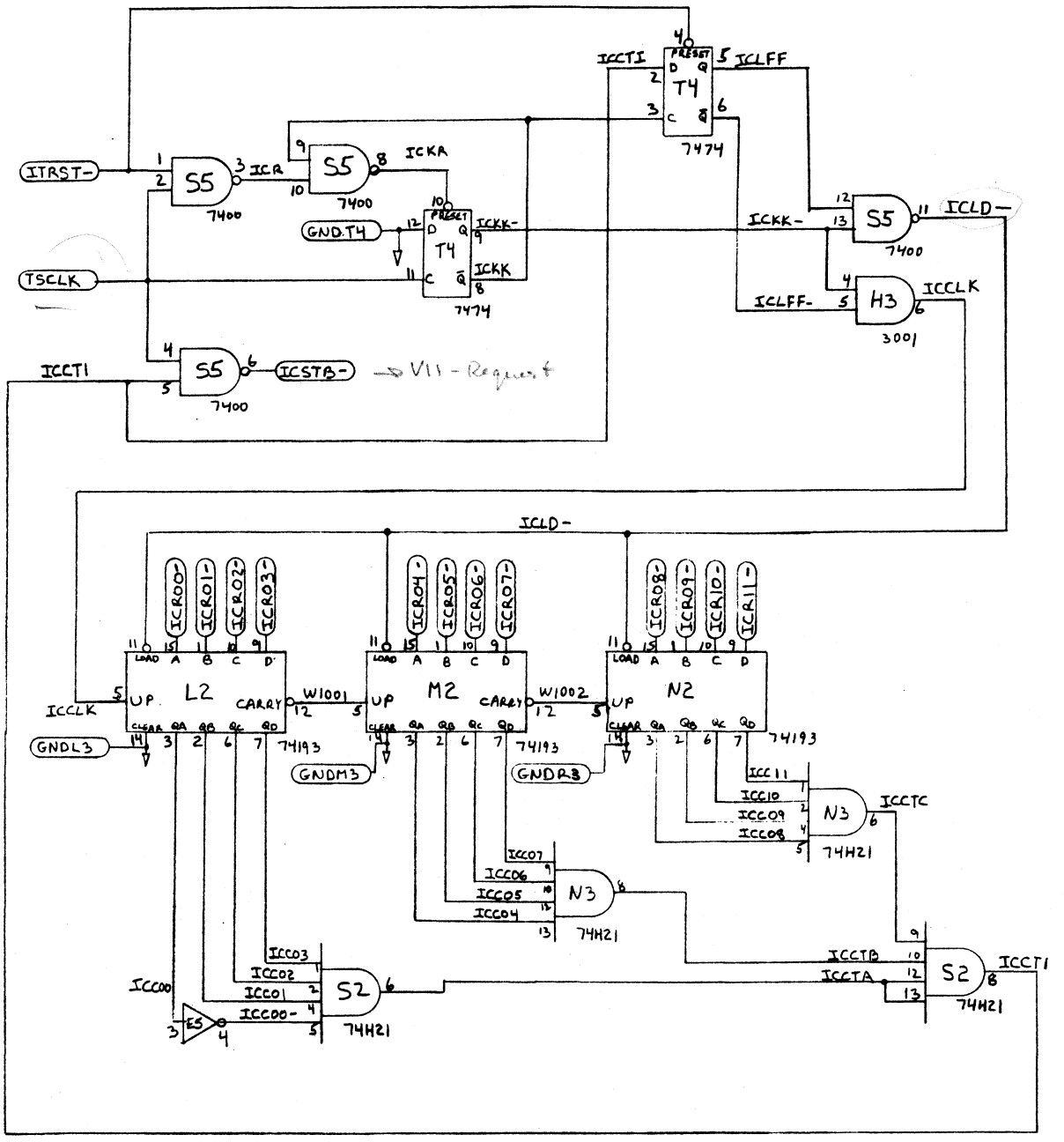
SCALE		SHEET 5 OF 8	



VARIABLE INTERVAL LOGIC

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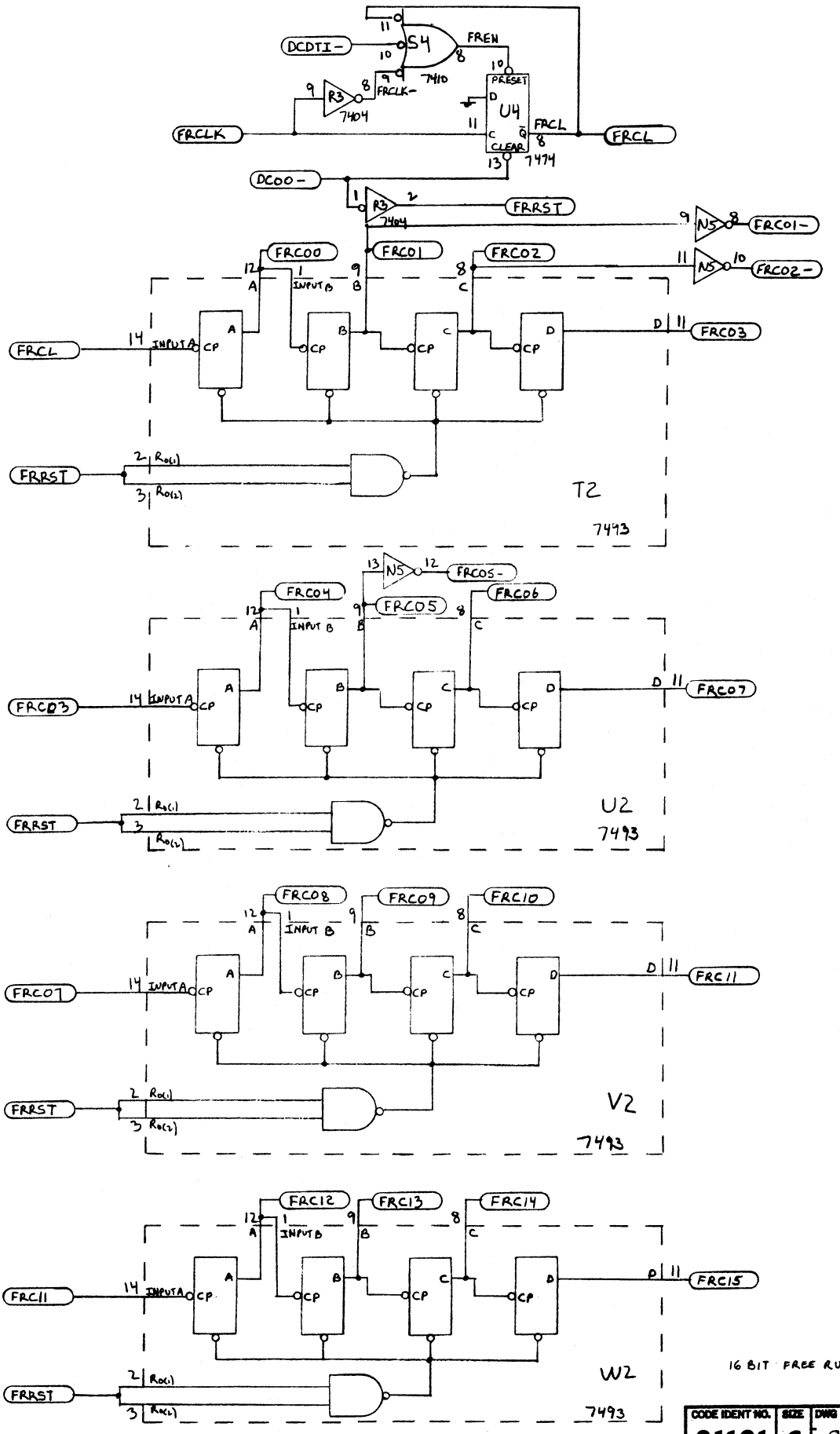

16 BIT FREE RUNNING COUNTER

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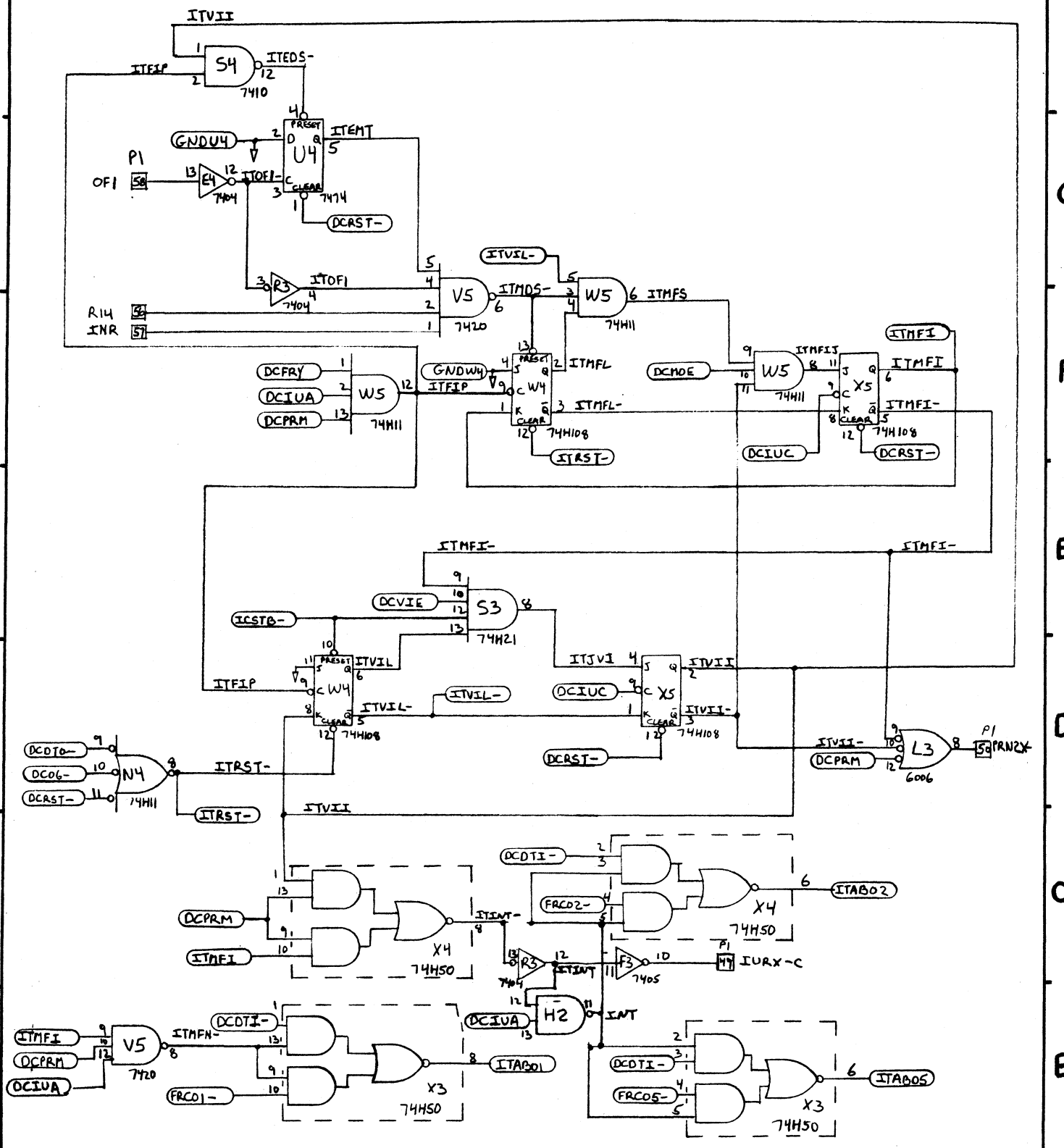

INTERRUPT CONTROL LOGIC AND MEMORY OVERFLOW DETECT

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21101	C	91C0259	A
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DWG. NO. 44P0483

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				REF	REF	REF	–	44D0483C	ASSEMBLY		
				REF	–	REF	–	91C0260C	LOGIC DIAGRAM		
				REF	–	REF	–	95W0722D	WIRE LIST		
				REF	–	REF	–	98A0579A	TEST SPEC		
				REF	REF	–	–	91B0259A	LOGIC DIAGRAM		
				REF	REF	–	–	95W0721C	WIRE LIST		
				REF	REF	–	–	98A0578A	TEST SPEC		
				1	1	1	1	40D0457-000B	BOARD DETAIL		
				1	–	1	2	49A0019-000	I.C. SN74H40N		
				2	–	2	3	49A0020-000	I.C. SN74H72N		
				1	–	1	4	49A0023-000	I.C. SN74H04N		
				1	–	1	5	49A0524-000	I.C. U6E960129		
				1	–	1	6	49A0039-000	I.C. SN74H00N		
				1	–	1	7	49A0082-001	I.C. SN74H74N		
				3	2	1	8	49A0007-000	I.C. SN7400N		
				4	3	1	9	49A0081-001	I.C. SN7403N		
				3	1	2	10	49A0104-000	I.C. MC3001P		

NEXT ASSY 01A0950 | MODEL NO | APPD A. Whittemore

TITLE: PARTS LIST
PFR/RTC ASSEMBLY

REV	X1	X2	A	B	C	D	–	E	F	G	–
EN NO			5106	5167	5244	5269		5343	5347	5365	5377
DATE	11-2-70		12/11/70	4/26/71	4/26/71	4/26/71		4/26/71	4/26/71	4/26/71	4/26/71
DR	GRL		JZ	GR	GR	GR		GR	GR	GR	GR
CHK	AW										

DWG NO 44P0483 | REV G

SHEET 1 OF 3

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QUANTITY REQ'D PER DASH NO							PARTS LIST			CODE IDENT: 21101	
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				2	2	-	12	49A0005-000	I.C. SN7410N		
				1	1	-	13	49A0006-000	I.C. SN7420N		
				1	1	-	14	49A0010-000	I.C. SN6006N		
				12	12	-	15	49A0012-000	I.C. SN7474N		
				2	2	-	16	49A0022-000	I.C. SN74H11N		
				8	8	-	17	49A0040-000	I.C. SN7404N		
				1	1	-	18	49A0060-000	I.C. SN74H30N		
				1	1	-	19	49A0086-000	I.C MC4006P		
				3	3	-	20	49A0091-001	I.C. SN74193N		
				2	2	-	21	49A0093-001	I.C. SN74H50N		
				3	3	-	22	49A0094-001	I.C. SN74H21N		
				2	2	-	23	49A0099-000	I.C. SN74H108N		
				5	5	-	24	49A0112-000	I.C. SN7493N		
				1	-	1	25	01P0936-000	COMPONENT BD.		
				1	-	1	26	01P0937-000	COMPONENT BD.		
				1	-	1	27	01P0938-000	COMPONENT BD.		
				1	1	-	28	01P0979-000	COMPONENT BD.		
				1	1	-	29	01P0980-000	COMPONENT BD.		
				1	1	-	30	01P0981-000	COMPONENT BD.		
				1	1	-	31	01P1069-000	COMPONENT BD.		

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QUANTITY REQ'D PER DASH NO							PARTS LIST			CODE IDENT: 21101	
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				3	3	-	33	58A0060-001	CONNECTOR, 16 PIN		
				1	1	1	34	16S1057-057	CARD HANDLE		
				1	1	1	35	16S1057-070	CARD HANDLE		
				31	25	6	36	71A0009-003	CAPACITOR, 0.1 uf	C1, 3, 6, 8, 10, 12 THRU 37	
				6	4	2	37	71N0200-225	CAPACITOR, 2.2 uf	C2, 4, 5, 7, 9, 11	
				174	174	174	38	58C0170-000	WIRE WRAP POST		
				0	0	0	39	53A0333-040	WIRE, YELLOW	30 AWG	
				1	-	1	40	49A0061-000	IC. SN74H05N		

NOTES:

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SHEET 3 OF 3

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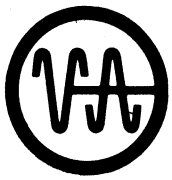

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