Texas Instruments

EXPLORER™

68020-BASED PROCESSOR

GENERAL DESCRIPTION

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, can cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computer device pursuant to Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference; in which case, the user at the user's own expense will be required to take whatever measures necessary to correct the interference.

WARNING: High voltages are present inside the chassis of this equipment. Only qualified service personnel who are familiar with the dangers of high voltages are permitted to open the chassis of this equipment to the service access position.

MANUAL REVISION HISTORY

CONTENTS

Paragraph	Title	Page

ABOUT THIS MANUAL

Purpose

This document provides a general description of the Texas Instruments (TI) 68020-based processor. The information in this document is intended for use by system designers, value-added resellers (VARs), maintenance personnel, system users, and operators.

Contents

This manual is divided into the following three sections:

Section 1: General Information — Provides a general overview of the processor's features and specifications; includes a list of reference documents for the processor.

Section 2: Installation and Operation — Provides detailed information on installation and operation of the processor.

Section 3: Processor Description — Provides a brief general description of the major components in the processor.
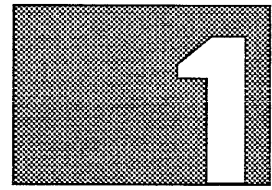
GENERAL INFORMATION

Introduction

1.1 This section provides general information on the 68020-based processor board (Figure 1-1) used in the Explorer LX system. This information is organized under the following topics:

- Features

- Specifications

- Reference documents

The 68020-based processor board uses the 68020 32-bit microprocessor. The processor operates on the NuBus and supports limited input/output through the system maintenance terminal (SMT) port.

The 68020-based processor expands the scope of the Explorer artificial intelligence workstation by integrating numeric-computation programs written in C, Fortran, COBOL, or Pascal with symbolic processing and artificial intelligence application programs written in Lisp and provided by the existing Explorer processor.

Features

1.2 The 68020-based processor has the following key features:

- Virtual memory for sharing system operations, addressable to 4 gigabytes

- Three main buses for addresses and data

- 68020 microprocessor for system operation and control, operating at 16.7 MHz

- 68881 floating-point coprocessor for floating point calculations operating at 16.7 MHz

- 68851 paged-memory management unit (PMMU) for memory control

- 16-kilobyte cache memory for logical address, data, and instructions

- Main memory for software operations; 2 megabytes of error-correcting on-board memory with an optional 2 megabytes of memory on a piggyback board

- Interrupt control chip (ICC) for handling board and bus interrupts

- Three timers for real-time clock, interval timing, and time accounting

- Nonvolatile RAM (NVRAM) for system configuration support

- ROM for board information and self-test

Figure 1-1 68020-Based Processor Board

add-on memory mounting holes, 6 places

ICC with interval timer

lithium battery

board info ROM

RTC timer

time accounting timer

NVRAM

self-test ROM, 4 places

68881 coprocessor

68020 microprocessor

68851 PMMU

cache memory

2 MB memory

bus connectors, 3 places

power failure warning switch
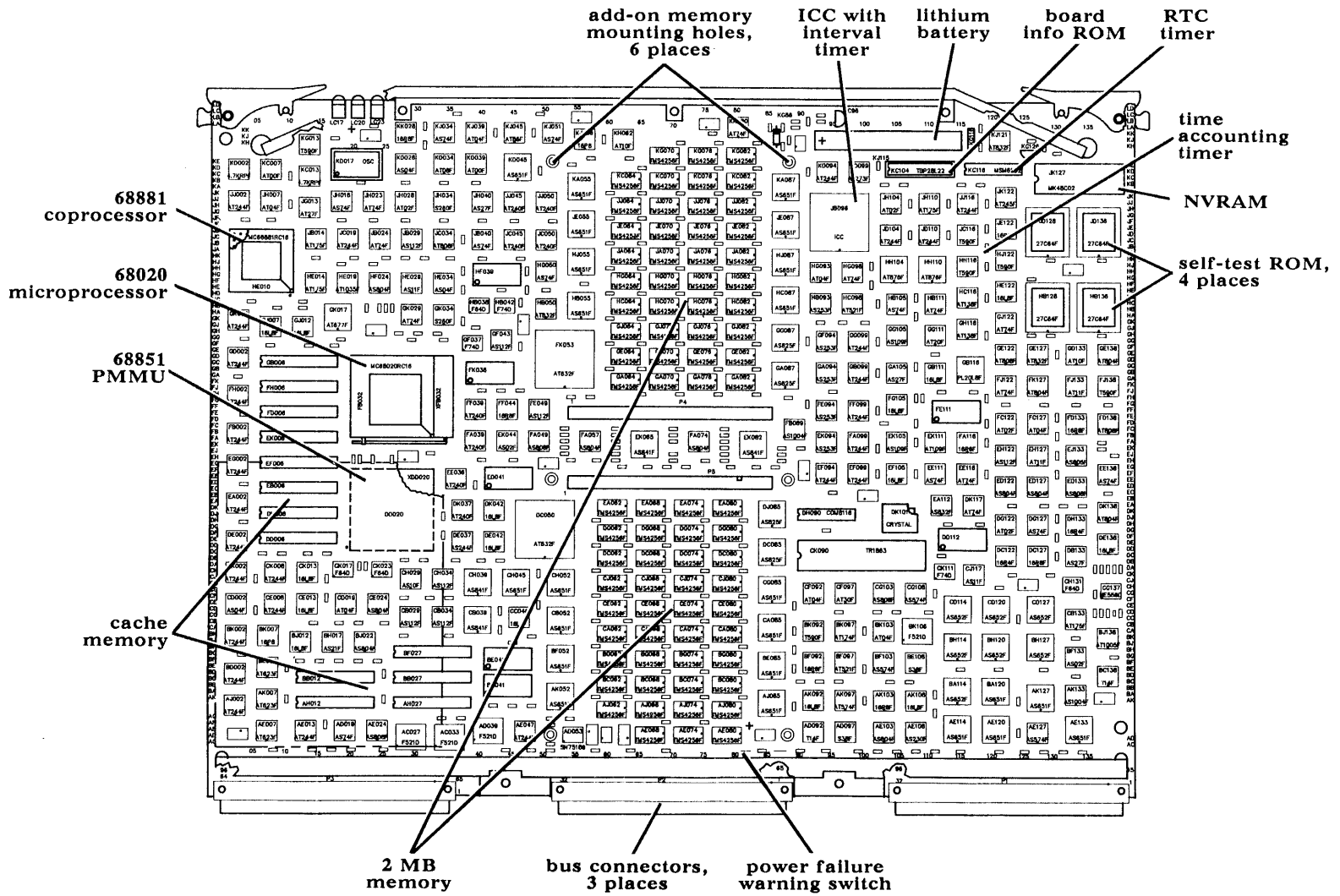
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Specifications   1.3 Table 1-1 lists the environmental and power specifications for the 68020-based processor.

Table 1-1 68020-Based Processor Specifications

Item	Type	Specifications
Temperature	Operating	5° to 45° C
	Nonoperating	−40° to 65° C
Relative Humidity	Operating	8% to 80% (noncondensing) Maximum wet bulb temperature 27° C
	Nonoperating	5% to 95% (noncondensing) Maximum wet bulb temperature 35° C
Shock	Operating	15 g (3 axes, 1/2 sine, 6 ms)
	Nonoperating	20 g (3 axes, square wave, 55 in/s velocity change)
Vibration	Operating	0.0118 in. (5-20 Hz), 0.25 g (20-250 Hz) (3 axes, sine, sweep rate 1 octave/minute)
	Nonoperating	0.0276 in. (5-20 Hz), 0.5 g (20-250 Hz) (3 axes, sine, sweep rate 1 octave/minute, 15-minute dwell at resonant points)
Altitude	Operating	−1000 to 6,500 ft.
	Nonoperating	−1000 to 10,000 ft.
Power		+5 volts main, 16.30 amperes, 81.50 watts +12 volts, 0.04 amperes, 0.48 watts −12 volts, 0.0 amperes, 0.0 watts Total power consumption, 81.98 watts

**Reference
Documents**

1.4 The following reference documents provide additional technical information on the 68020-based processor:

- *Specification System 1500 Processor*, TI part number 2535864-0001 (and references therein)

- *S1500 Processor Assembly,* TI part number 2535860-0001

- *S1500 Processor Logic Diagram,* TI part number 2535862-0001

- *Explorer 7-Slot System Installation*, TI part number 2243140-0001

- *Explorer 7-Slot System Enclosure*, TI part number 2243143-0001

- *Explorer System Field Maintenance*, TI part number 2243141-0001

- *Explorer NuBus Peripheral Interface General Description*, TI part number 2243146-0001

- *Explorer LX System Installation Guide*, TI part number 2537227-0001

INSTALLATION AND OPERATION
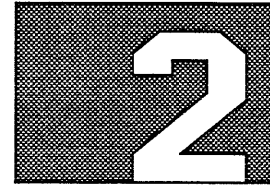
Introduction

2.1 This section is divided into the following major headings:

- Installation

- Operation

Installation

2.2 The discussion of the installation of the 68020-based processor provides information on the following topics:

- Unpacking

- Installing the processor board

- Installing memory expansion

- Installing the software protection adapter

Unpacking 2.2.1 The processor board (Figure 1-1) may be shipped installed in the system enclosure. Depending on your system configuration and options, however, you may have to install the board. You also may need to install the board when upgrading your system.

CAUTION: All system boards, options, adapters, and peripherals contain components that are sensitive to static electricity. When handling any of these items, protect against static electricity by using wrist grounding straps, grounded working mats, and antistatic bags for moving or storing the items.

If your board is not already installed, locate the board packing container. If any packing instructions are attached to the exterior of the packing container, follow those instructions. If not, perform the following steps:

1. Open the packing container and carefully remove the packing material; then remove the processor board with its static-protective bag in place.

    When working with the processor board, you must be careful not to short-circuit the real-time clock battery. The battery is located behind the stiffener, at the upper front corner of the processor board.

WARNING: Each processor board contains a lithium battery. Lithium batteries can explode if the positive and negative terminals are shorted together. DO NOT place the processor board on a conductive surface. The outside surfaces of all antistatic shipping bags are conductive; do not place the processor on an antistatic shipping bag.

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2. Remove the static-protective bag from the processor board.

Installing the Processor Board

2.2.2 The address of the processor is determined by the slot ID of the slot that the processor board occupies. Use of the board with Explorer I requires that the power failure warning switch at board location A-080 (Figure 1-1) be set to open (up) or that the jumper be cut on boards with a wire jumper. When the memory expansion board is installed, accessing this switch is difficult.

NOTE: The inner, metal front door and the rear door of the system enclosure must be closed for the system to be operational.

All system boards including the processor board are installed in the same general manner. Complete the following procedures each time you install a processor board:

WARNING: To eliminate the possibility of electrical shock during option or upgrade installation, you must isolate the system enclosure from all potential energy sources. To isolate the system enclosure:

1. Power off the system enclosure and all peripherals.

2. Disconnect the power cable from the wall outlet of all local peripherals connected to the system enclosure.

3. Disconnect all interface cables between the system enclosure and all remote peripherals at the remote peripheral interface.

4. Unplug the system enclosure power cable from the wall outlet.

Once you have performed the four steps shown in the previous warning, perform the following steps:

1. Open the outer and inner front system enclosure doors.

2. Install the upgrade board in the selected slot (slot 1 is preferred for the 68020-based processor board). When installing a board, make note of the slot number so that the adapters can be installed in the corresponding slot of the backplane.

NOTE: Refer to the *Explorer LX System Installation Guide*, TI part number 2537227-0001, for further instructions on slot locations in multiprocessor installations.

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   a. Orient the board with the LEDs to the bottom and the components facing right.

   b. Slide the board into the selected slot, and make sure it is seated into the three backplane connectors.

   c. Press the top and bottom ejector tabs so that the board is locked into the card cage.

3. Close the rear and the two front system enclosure doors.

CAUTION: Only trained service personnel are to remove and install the power supply board. Hazardous components are located behind the power supply cover. Do not attempt to service the power supply. Refer power supply problems to your TI customer representative or other TI authorized service personnel.

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4. Reconnect the system enclosure power cable to the wall outlet.

5. Reconnect all interface cables between the system enclosure and the remote peripherals.

6. Reconnect the power cable to the wall outlet of all local peripherals connected to the system enclosure.

7. Power on the peripherals and then the system enclosure. If the system enclosure does not power on, turn the power off and check to see that the front inner door and rear enclosure door are closed.


NOTE: Refer to the *Explorer System Field Maintenance* supplement, TI part number 2537183-0001, for information on removing and installing the power supply board.

Installing Memory Expansion

2.2.3 Each 68020-based processor board contains 2 megabytes of on-board memory and can support an additional 2 megabytes of add-on memory with the memory expansion board (Figures 2-1 and 2-2).

The connectors located at the center of the expansion board mate with the two sets of pins located near the center of the processor board. The processor has six mounting holes, and the expansion board has six mounting standoffs. Note that the center sets of holes and standoffs are offset to ensure that the expansion board can be mounted in only one orientation.

Figure 2-1 Memory Expansion Board
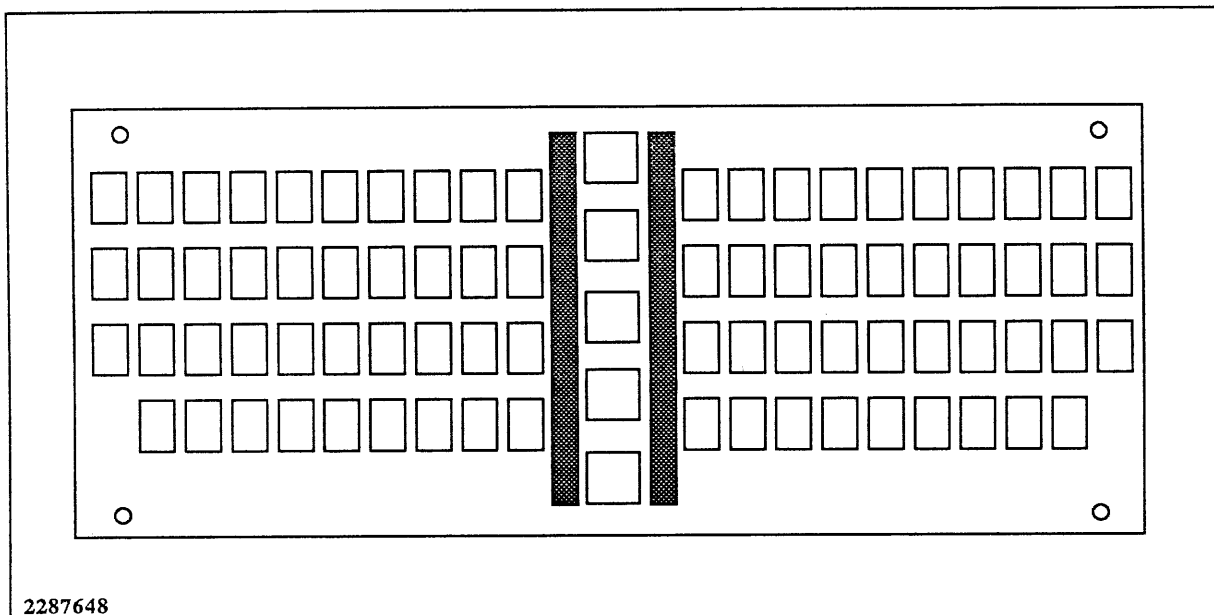
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When working with the processor board, you must be careful not to short-circuit the real-time clock battery. The battery is located behind the stiffener, at the upper front corner of the processor board.

WARNING: Each processor board contains a lithium battery. Lithium batteries can explode if the positive and negative terminals are shorted together. DO NOT place the processor board on a conductive surface. The outside surfaces of all antistatic shipping bags are conductive; do not place the processor on an antistatic shipping bag.

Complete the following procedures each time you perform the memory expansion installation:

WARNING: To eliminate the possibility of electrical shock during option or upgrade installation, you must isolate the system enclosure from all potential energy sources. To isolate the system enclosure:

1. Power off the system enclosure and all peripherals.

2. Disconnect the power cable from the wall outlet of all local peripherals connected to the system enclosure.

3. Disconnect all interface cables between the system enclosure and all remote peripherals at the remote peripheral interface.

4. Unplug the system enclosure power cable from the wall outlet.

To mount the expansion board on the processor board, follow these steps:

1. Remove the processor board from the system enclosure or its static-protective shipping bag, and place it on an antistatic surface. If the board is being installed in an Explorer I system, check the power failure warning switch at board location A-080 (Figure 1-1), and set the switch to open (up) or cut the jumper on boards with a wire jumper. When the memory expansion board is installed, accessing this switch is difficult.

2. Position the expansion board over the processor board so that all six of the mounting holes and mounting studs are aligned.

3. Press the expansion board connectors onto the processor board mounting pins. Check to make sure that no pins were bent during the mounting of the expansion board. If a pin is bent, follow these steps:

    a. Carefully lift the memory expansion board from the processor board.

    b. With a pair of longnose pliers, carefully straighten the bent pin.

    c. Try again to install the memory expansion board.

4. Install the six screws and washers that hold the expansion board to the processor board. With a small screwdriver, tighten the screws firmly; do not over-tighten.

When you complete this procedure, reinstall the upgraded processor board in the enclosure card cage, as described in paragraph 2.2.2, Installing the Processor Board.

**Installing
the Software
Protection Adapter**

2.2.4 The software protection adapter (SPA) protects your software from unauthorized use; system users must know the correct password to access system software. Each system enclosure has only one SPA.

For a system with one processor board, the SPA attaches on the backplane at P2 of the slot containing the processor board. The system boots from the processor board in the lowest numbered slot. The slots are numbered 0 through 6 from right to left as you face the rear of the system enclosure.

Each SPA has an ID number located on the SPA board protective cover. Record the SPA ID number and the sales order number from the SPA label. You will need these numbers along with your customer number when obtaining your system login code from Texas Instruments Incorporated.

To install the SPA, follow these steps:

1. Power off the system enclosure and peripherals. Remove the ac power cord from the system enclosure.

2. Open the rear door of the enclosure and follow the instruction that applies to your system:

   ■ If your system contains only one 68020-based processor board, locate P2 of the slot containing that board.

   ■ If your system contains more than one 68020-based processor board, locate P2 of the lowest numbered slot containing a 68020-based processor board.

3. Position the SPA so that the shield faces toward the left, the 96-pin connector faces toward the backplane, and the two 18-pin cable ports are at the top rear of the SPA.

4. Slide the SPA into the mounting rails until it is seated in the backplane P2 connector.

5. Close the rear enclosure door securely.

6. Reinstall the ac power cable, and power on the peripherals and the system enclosure.

7. If the system enclosure does not power on, turn the power off and check to see that the front inner door and rear enclosure door are closed.

Operation

2.3 The discussion of the operation of the 68020-based processor provides information on the following topics:

■ Processor

■ Software protection adapter (SPA)

■ Diagnostic port

■ System boot

Processor **2.3.1** In the Explorer LX system, the 68020-based processor is the system test boot master (STBM). It uses the Explorer monitor and keyboard instead of a separate system maintenance terminal for display and user input. The SPA must be installed on P2 of the slot containing the STBM processor. Figure 2-2 shows the 68020 processor board with optional memory and SPA.

The processor board has three LEDs that represent self-test failure, uncorrectable memory error, and correctable memory error. These LEDs, which can be viewed through the openings in the inner front system enclosure door, indicate the status of the board.

For additional information on the the 68020-based processor, refer to the *Specification System 1500 Processor*, TI part number 2535864-0001.

Figure 2-2 **68020-Based Processor With Optional Memory and SPA**

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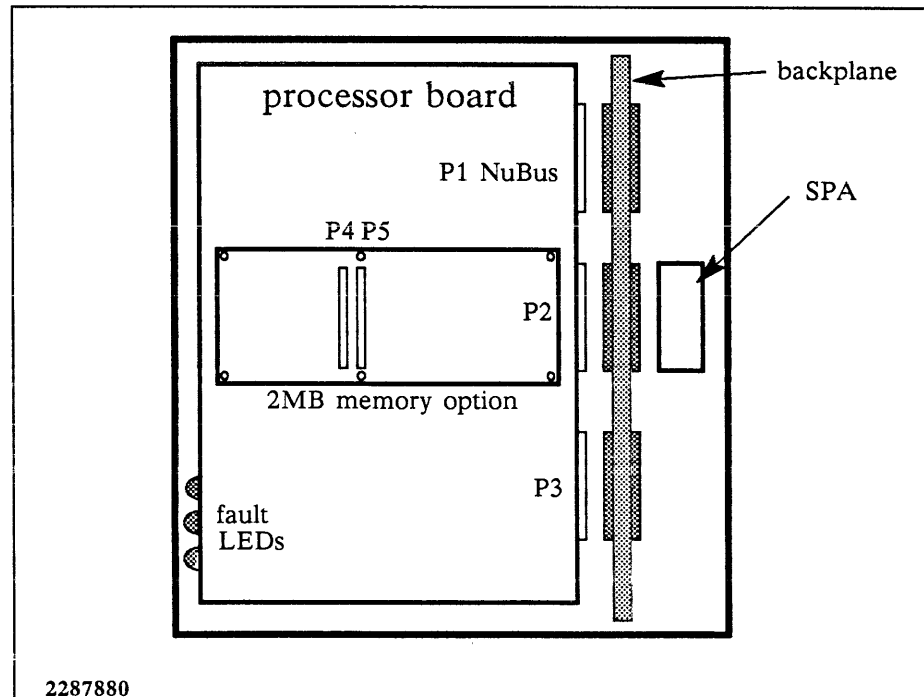
**Software
Protection Adapter**

2.3.2 The software protection adapter (SPA) shown in Figure 2-3 protects the TI System V software on the system from unauthorized use. Only one SPA is used per system. The SPA mounts on the P2 connector of the backplane slot containing the 68020-based processor board.

Affixed to the metal cover of the SPA is a label that contains the identification number of the SPA. Each SPA has a unique ID. The ID code of the SPA must match the password that is in the boot software.

Figure 2-3

Software Protection Adapter

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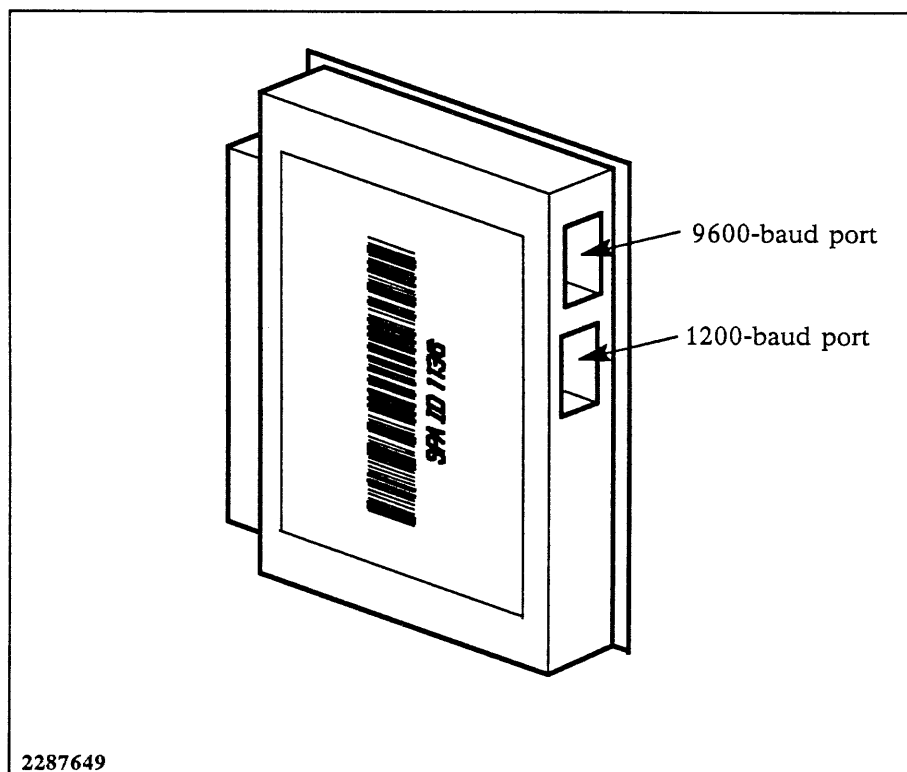
Diagnostic Port

2.3.3 The processor diagnostic port (9600-baud or 1200-baud port) is not used in the Explorer LX system.

System Boot 2.3.4 The system begins the boot process with the activation of the ac power switch on the front of the system enclosure. The initial portion of the system boot, before software is loaded from the primary disk to system memory, uses the 68020-based processor as follows:

■ STBM — One processor board becomes the STBM. In systems using more than one processor board, the default STBM is the processor in the lowest numbered slot (the leftmost one when you face the system enclosure) that passes self-test. The STBM takes initial control of the system and executes the interface test of each of the boards in the system. Information from the tests is passed from the STBM over the NuBus to the Lisp processor, to the systems interface board, and to the Explorer LX monitor. For Explorer LX, the 68020-based processor in slot 1 is the STBM unless it fails self-test.

During the initial booting of the system, the following process takes place:

■ Power on — Power is applied to the system enclosure power supply, which in turn supplies power to the system boards and cooling fan.

■ Self-tests — Each processor board runs an initial self-test that is resident in ROM on each board. The Explorer LX monitor displays the results of the self-tests that run on the STBM processor.

■ Interface test — The STBM processor automatically controls and displays on the system LX monitor the status of each of the installed system boards.

For a more thorough treatment of the Explorer LX 68020-based processor operation, system boot, self-tests, interface test, and diagnostics,refer to the *Explorer LX System Installation* manual, TI part number 2537227-0001.
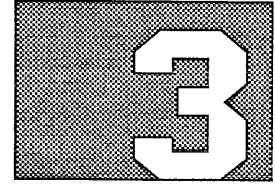
PROCESSOR DESCRIPTION

Introduction

3.1 The single board processor uses the 68020 32-bit microprocessor. It operates on the NuBus and supports limited input/output through the system maintenance terminal (SMT) port, which is not used in LX systems. This section describes the key features of the 68020-based processor (Figure 3-1), as listed in Section 2 of this manual. This section also describes the functions of the software protection adapter (SPA).

Features

3.2 The paragraphs that follow discuss the main features of the 68020-based processor.

Virtual Memory

3.2.1 Virtual memory in the system is accomplished with the use of paged-memory management. User programs can be written as if the program has the full 32-bit logical address range (4 gigabytes) available when a smaller amount of physical memory is actually present in the system.

The user program is divided into fixed-size segments called pages. Only the pages in current use reside in main memory. The remaining pages reside in mass storage. As needed, pages are transferred to and from the mass storage devices on page boundaries for use by the system.

Bus Structure

3.2.2 The 68020-based processor contains three main buses: NuBus, the physical bus, and the logical bus. The NuBus has 32-bit bidirectional data and addresses multiplexed on a single set of bus lines. The physical and logical buses each are 32-bit bidirectional data and address buses.

Physical bus ownership is determined by arbitration between the NuBus interface and the processor (through the paged-memory management unit (PMMU) and memory controller).

A special 64-bit-wide data bus runs from the main memory to the cache memory and the NuBus. This bus permits the transfer of double-wide, 64-bit data words.

Figure 3-1   68020-Based Processor Block Diagram

68020 processor board

data bus

| 16KB cache hit = no wait |
| 68020 16.7 MHz |
| 68881 FPU |
| 68851 PMMU |

logical address

| NVRAM |
| 112 event controller |
| 3 timers |
| configuraton |
| diagnostic |

physical address bus

| 2MB memory |
| 2MB option memory |

byte swap logic

NuBus interface

| test port | software protection/ diagnostic port | NuBus |
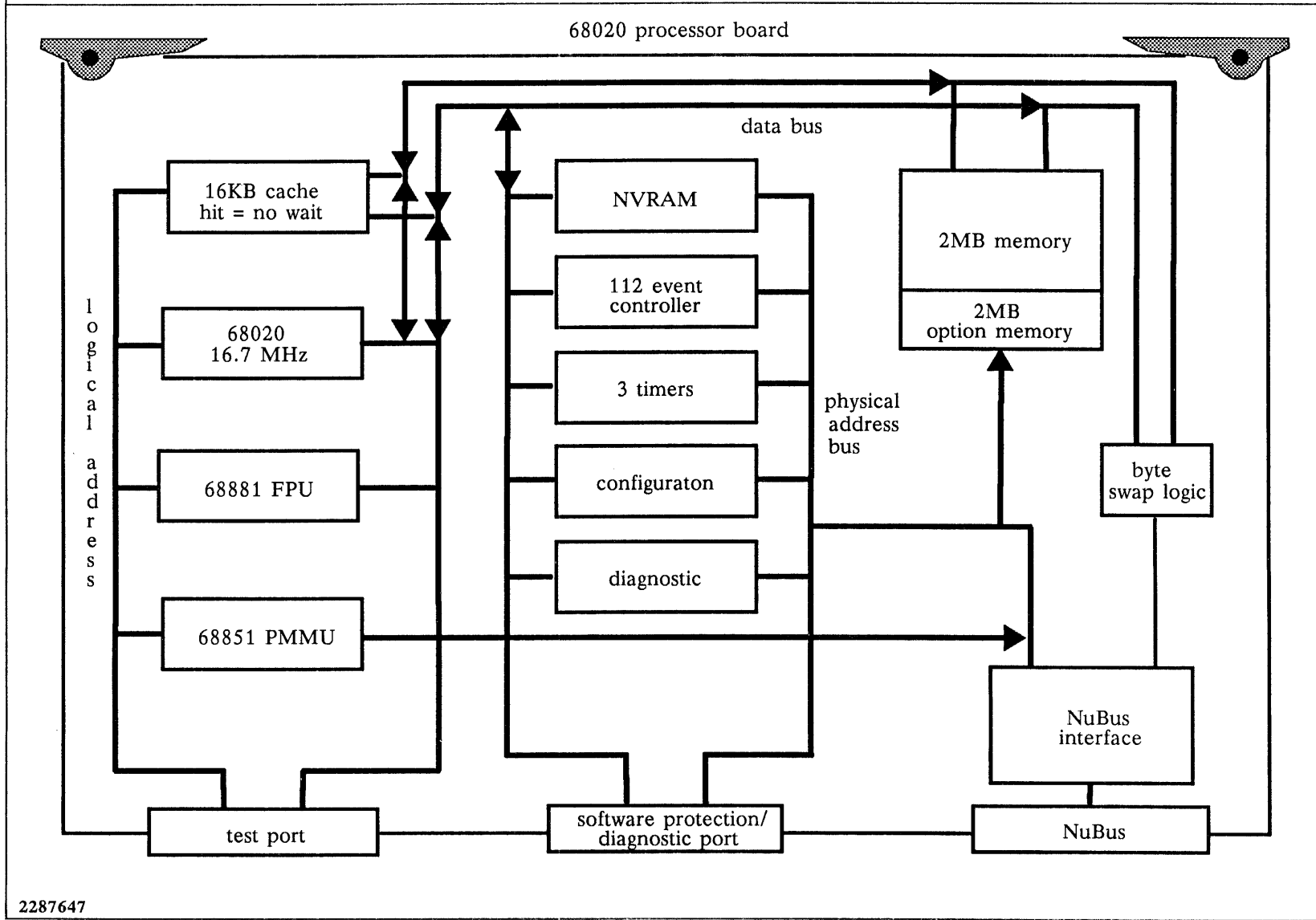
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Microprocessor **3.2.3** The 68020 microprocessor used on the 68020-based processor board has separate, nonmultiplexed, 32-bit address and data buses. The dynamic bus sizing of the 68020 microprocessor eliminates hardware restrictions on data alignment of any byte boundary. Other features of the 68020 microprocessor are as follows:

■ Virtual memory/machine support

■ Sixteen 32-bit general purpose data and address registers

■ Two 32-bit supervisor stack pointers

■ 32-bit program counter

■ Five special-purpose control registers

■ 4-gigabyte slot space

■ Eighteen addressing modes

■ Memory-mapped input/output (I/O)

■ Coprocessor interface

■ High-performance on-chip instruction cache

■ Operations on these seven data types:

    ■ Byte integer (8 bits)

    ■ Word integer (16 bits)

    ■ Longword integer (32 bits)

    ■ Single-precision binary real number (32 bits)

    ■ Double-precision binary real number (64 bits)

    ■ Extended-precision binary real number (80 bits)

    ■ Decimal real number string in packed BCD format (3-digit exponent and 17-decimal mantissa — for example, 123.12345678912345678)

For detailed information on the 68020 microprocessor, refer to the Motorola *MC68020 32-Bit Microprocessor User's Manual.*

Coprocessor

3.2.4 The 68020-based processor board also contains the 68881 floating-point coprocessor. The high-performance coprocessor interfaces with the 68020 microprocessor and the virtual-machine architecture. The coprocessor provides these features:

■ Eight 80-bit floating-point data registers

■ One 32-bit control register

■ One 32-bit status register

■ One 32-bit instruction register

■ Operations on seven data types (listed in the previous paragraph, Microprocessor)

Memory Management

3.2.5 The 68851 PMMU allows an unbroken linear address space as large as the address bus permits. The PMMU provides an address translation from logical memory addresses to physical memory addresses. Features of the PMMU are as follows:

■ Logical-to-physical address translation

■ Subdivision of physical memory into pages of different lengths depending on need and utilizing replacement algorithms

■ On-chip cache for recently used pages

■ Translation cache that holds entries for simultaneous access by eight user tasks, by supervisor registers, and by direct memory.

The operating instruction set for the PMMU is an extension of the 68020 instruction set. For additional information on the 68851 PMMU, refer to the Motorola *MC68000 Family Paged-Memory Management Unit Design Specification - Revision 5*.

Cache Memory

3.2.6 The 68020-based processor has two levels of cache memory available: a small instruction cache internal to the 68020 microprocessor and the processor board cache memory. The internal cache is dedicated to instructions only, with a capacity of 64 longword instructions. Processor board cache memory is available for both data and instruction storage and has a capacity of 16 kilobytes.

Main Memory

3.2.7 The 68020-based processor board main memory is 2-megabyte dynamic random-access memory (DRAM) with error checking and single-bit error correction.

Data storage and retrieval takes place in two identical arrays. Each array consists of 39 DRAM chips, 32 for memory data and 7 for error-correction-check bit storage. The even array stores or retrieves even longwords (memory data), and the odd array stores or retrieves odd longwords.

Interrupt Control Chip

3.2.8 The interrupt control chip (ICC) on the 68020-based processor board controls interrupts generated by the processor board in the system power supply, by the diagnostic port, and by other NuBus logic boards. The ICC is a semicustom 68-pin gate array that provides interrupt and NuBus event services for the 68020 processor. Features of the ICC are as follows:

■ Complete 68020 interrupt protocol

  ▪ Prioritized interrupt code output

  ▪ Vector assigned to each interrupt

■ Four external interrupt requests with programmable priority

■ Two nonmaskable external interrupt requests, hardwired to the highest priority level

■ 112 event locations for external NuBus-initiated interrupts

■ Program option to clear event bits

■ On-board programmable interval timer (PI/T)

■ Interrupt vector error detection

■ Sixteen 8-bit registers for programming, control, and status checking

■ Three-state interrupt vector output and register data I/O lines

Timers

3.2.9 The 68020-based processor board has three separate timer functions. All timer functions are interfaced to the processor board physical bus for access and control. The processor on-board timers are as follows:

■ Real-time clock (RTC) — The RTC provides real-time clock/calendar functions for the system. A lithium battery provides power to the RTC during chassis power-down periods.

■ Interval timer — The interval timer function is provided by the PI/T section of the ICC. The primary function of the interval timer is to interrupt the system operating software to allow the scheduler software to run. Intervals from 10 microseconds to 2.55 seconds can be programmed for the interval timer with resolutions of 10 microseconds, 100 microseconds, 1 millisecond, and 10 milliseconds.

■ Accounting timer — The system software checks the accounting, free-running timer to obtain the length of time a task has been running. This timer is intended for on-board use by the 68020, not for remote operations over the NuBus.

NVRAM and ROM

3.2.10 The 68020-based processor board uses nonvolatile random-access memory (NVRAM) and read-only memory (ROM) to store semipermanent and permanent data used in different types of board operations. The types of NVRAM and ROM are as follows:

■ NVRAM and backup battery — The 68020-based processor board provides 2048 bytes of NVRAM, which is addressable from the NuBus. The NVRAM shares the on-board battery backup and battery monitor circuit with the RTC. With a fully charged battery, NVRAM and RTC data will be retained for a minimum of one year after ac power has been removed from the system enclosure, unless the battery is shorted.

Data stored in the NVRAM is used in the system boot, system tests, power shutdown recovery, and crash analysis and recovery.

When the supply voltage decays to below 4.75 volts, the NVRAM switches to write-protect mode and issues a power-fail signal, putting the RTC in power-down mode. When supply voltage decays below 3 volts, the NVRAM switches to battery power. When the supply voltage recovers and exceeds 4.75 volts, the NVRAM returns to normal operation.

A monitor circuit checks the battery voltage. If the battery voltage falls below 2.4 volts, the warning message Warning Low Battery call for service is displayed.

■ Configuration ROM — Each 68020-based processor board has a configuration ROM. The configuration ROM contains permanent board data used for system booting, auto configuration, interboard communications, and self-testing. The processor board ROM contains the board serial number, cyclic-redundancy-check (CRC) signature, configuration ROM size, vendor ID, board type, board part number, and revision level. The ROM also contains address offsets to the configuration and flag registers.

■ Self-test ROM — The erasable programmable read-only memory (EPROM) devices that make up the processor's self-test ROM are connected to form 8,192 32-bit words. During power-up, the self-test ROM is activated to test the processor board circuitry.

SPA

3.3 The paragraphs that follow discuss the functions of the SPA.

Software Protection

3.3.1 The SPA provides, in a sealed (potted) unit, protection from unauthorized uses of the system software by requiring the use of a password unique to each individual SPA. If the SPA is replaced, a new password must be obtained and entered before access to the software can be made.

Interface Connection

3.3.2 The SPA provides two ports, each with a different speed, for supporting different SMT applications. One port supports a local terminal that is configured to run at 9600 baud. The other port can support a local terminal configured for 1200 baud, but its main function is to support a 1200-baud modem, allowing the system to be remotely booted over a telephone network. Only one port can be used at a time. This feature is not used in Explorer LX systems.

68020-Based Processor General Description
Documentation Questionnaire

Manual title_____

Manual part no._____ Date_____

What are your comments about this manual?

_____

_____

_____

What other TI software/manuals do you use?

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