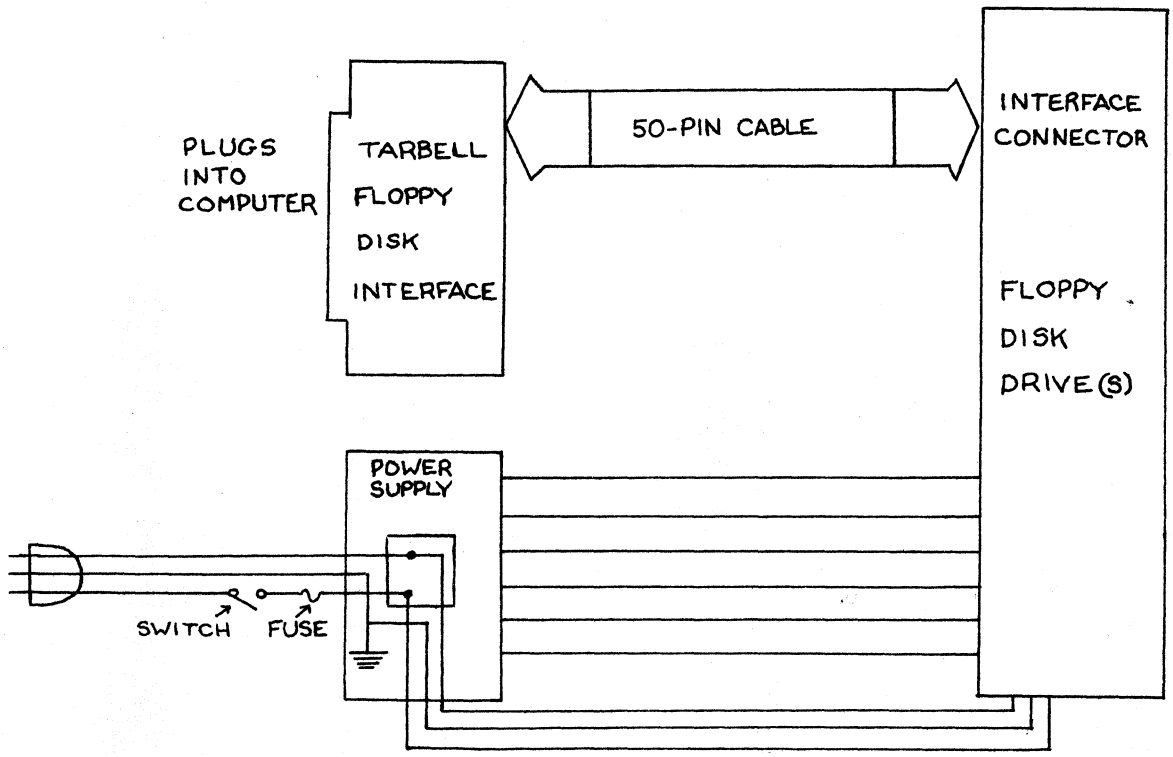
The Tarbell Floppy Disk Interface



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The Tarbell Floppy Disk Interface is a programmed-data-transfer (not DMA) device. It plugs into your IMSAI or ALTAIR* computer, and is designed to work with a variety of standard-size floppy disk drives. It includes a 32-byte ROM bootstrap program, which is automatically enabled when the computer RESET button is pushed, and which switches itself out after the bootstrap has run. In this way, no part of your memory needs to be dedicated to Read-Only-Memory (ROM). The interface runs at the standard speed of 250,000 bits per second, and the normal formatted capacity per diskette is 243 kilobytes. Places for two connectors are provided on the board. One 50-pin header connector and a cable with the mating connector are provided with the interface kit. There are four extra IC slots to allow you to do your own thing, and the connector pins come out to jumper pads, so you can adapt to different drives. The manual has the connections detailed for popular drives. An on-board dip-switch is used to select the device address, disable the bootstrap, and write-protect. Circuitry is included to run up to four drives, and eight can be accessed by using the spare IC slots.

The Tarbell Floppy Disk Interface and other related items can be bought in pieces, so that it's not necessary to make a single large outlay of cash. Because of this policy, the 6-month warranty will be limited to only those items traceable to Tarbell Electronics. Notice that we will be offering the CP/M floppy disk operating system, which is described on another page. An owner's manual for the interface is included with the kit or the bare board, and is also available separately.

Floppy Disk Interface Kit	190.00
CP/M Operating System (on disk)	70.00
CP/M System Manual Set (6)	25.00
BASIC-E Compiler Manual	5.00
Innovex Model 410 Floppy Disk Drive	575.00
Power Supply for Innovex 410	75.00
GSI 110 Floppy Disk Drive	525.00
Floppy Disk Interface Manual	5.00
Bare Floppy Disk Interface Board	40.00
Kit with all parts except 1771	125.00
Western Digital 1771 FDC IC	80.00
Assembled Floppy Disk Interface	265.00
PerSci 270 Dual Floppy Disk Drive	1130.00
Power Supply for PerSci 270	125.00
Blank Formatted Diskette	10.00
BASIC-E Source Listing (PL/M)	9.00
Additional Charge for Special Cable	10.00
Package of IC Sockets (35)	10.00

NOTE: These prices are preliminary, and are subject to change without notice. There are no discounts for complete systems; just add the prices together to find the total for your purchase.

Since Tarbell Electronics does not wish to get into the business of selling complete systems, we encourage you to buy your system, including the floppy disk drive, from your local dealer. If you add up the prices of the first six items, however, you can see that a complete floppy disk system including software and hardware can be had for less than a thousand dollars. Note that the Tarbell Floppy Disk Interface is not designed to work with double-density or mini-floppys, although it will work with multiple and double-sided drives. The drives that it has worked with so far include the Shugart 800/801, the Innovex 410, the Innovex 220 (modified by a jumper change), the GSI 110, the CDC 803, and the PerSci 270.

The first deliveries were made July 2, 1977. Delivery from the factory is 3-4 weeks after receiving your order, and individuals must send cash in advance. For faster delivery, check with your local dealer.

* ALTAIR is a trademark/tradename of MITS, Inc.

OPERATING INSTRUCTIONS

One nice thing about using a floppy disk is that the operation of the hardware is fairly simple:

1. Turn on computer power.
2. Turn on disk power.
3. Put a diskette into the drive and close the door.
4. Press the reset button on the computer.
5. Press the run button on the computer.

At this time, the hardware bootstrap routine automatically reads in the first sector of track zero, and runs it. This 128 byte module contains a more sophisticated loader which brings in the main operating system and runs it. Therefore, you should see the header that the operating system prints when it first comes up. In CP/M, this is something like "CPM V1.3". From this point on, you need to refer to your manual on CP/M (or whatever operating system you're using).

When you're all done, the shut-down procedure is as follows:

1. Open the disk drive door and remove the diskette.
2. Turn off the power to the disk drive.
3. Turn off the computer power.

GENERAL NOTES ABOUT USING YOUR DISK SYSTEM

1. In general, floppy disk drives are a very reliable method of storing data if nothing else goes wrong in the computer. As with any external medium, however, there will be some errors. These are normally detected by the interface and the software. The manual on your disk drive should have some figures as to the reliability of your particular unit. As a rule, you can expect the Tarbell floppy disk interface and your floppy disk drive to work for many days at a time without an error.

2. On the other hand, remember that your floppy disk interface is an on-line device; that is, the computer can write onto it any time, unless the write-protect is on. This has its advantages, but it also means that the disk is always subject to wipe-out,

******** IMPORTANT CAUTIONS ********

1. All RAM boards used in this disk operating system must have no wait states.

2. Take extreme care in handling the FD1771B-01 integrated circuit. Being a MOS device, it is liable to destruction from static charge induced by excessive handling--and it's expensive.

3. Before removing or installing the floppy disk interface board or any board in your computer, turn off the power and wait for at least ten seconds to let the capacitors discharge.

4. Before turning the computer power or the disk power on or off, be sure that the disk door is open, and preferably that the diskette is removed--so any transiets won't wipe out the disk.

5. Always turn on the computer power before the disk power, and turn off the disk power before the computer power.

THEORY OF OPERATION

The internal operation of a floppy disk system is probably the most complicated part of a micro-computer system. The hardware and software interact very closely. For best understanding, you should be familiar with both the 8080 machine/assembly language, and the common logic operations. Some understanding of the S-100 bus is also desirable. Remember to take into account any differences in your system's I/O setup as you follow the circuit.

Since the Tarbell Floppy Disk Interface is designed around the Western Digital 1771 Floppy Disk Integrated Circuit, it would be helpful to skim over the data sheets (reproduced in the appendix with the manufacturer's permission). The main thing is to get a feeling for what the 1771 does in order to get a perspective of how it fits into the circuit.

> ABOUT READING THE SCHEMATIC: note that lines of most drives are true when low--that is, a low voltage is a logic one. Active low lines have an asterisk following their name (e.g., RDY*). The convention of this schematic is that a darkened dot is a possible connection to a floppy disk drive; an open circle is a pad for a possible jumper wire; a little square with a number in it is a pin on the 100-pin S-100 bus; and a line with none of these, but a name close to it, is a connection to another line with the same name.

To see what we need in the interface, let's see what it must connect to on each side. On the computer side, we have two simple instructions: input a byte (IN), and output a byte (OUT).

On the side of the floppy disk, we have many different things to be concerned with. First, the data lines going to and from the floppy drive are serial (one bit at a time). Thus we must have some way to convert parallel computer data to serial data on the drive side.

Next, the drive has several control lines. These are lines that tell the drive what to do. For example, there are two lines to tell the drive to move the head in or out. There's another line that tells the drive to engage the head against the disk surface (normally the head is not in contact to reduce wear on the disk and on the head). Another control line is usually used to reset the drive electronics and return the head back to the zero (outside) track. There's a set

destroying some or all of the information on it. All it takes is a software error, power-line glitch or a temporary hardware malfunction to lose many hours, days, and even weeks of work if you only have that single copy.

It is therefore desirable to keep frequent back-ups of your files. This can be done by copying files to another diskette or to cassette. In this way, only the information entered since the last backup can be destroyed.

3. When first using any operating system, including CPM, run it in the write-protected mode for a little bit. Then make a back-up copy as soon as possible.

4. Note that CP/M always loads a program for execution at 100 hex. If it is desired to run a program at zero, such as basic, it must first be loaded at 100 hex and then moved down.

5. When the bootstrap switch (7) is on, a reset will gate the bootstrap program onto the bus. Even programs that run in other parts of the memory may be adversely affected if you attempt to run them before the bootstrap is disabled. Although the bootstrap is normally disabled automatically, there may be times when you want to disable it manually. This can be done by putting front panel data switch 5 to the up position and doing an examine, or by turning off dip-switch 7.

6, There is a difference in the reliability of different manufacturer's diskette media. We at Tarbell Electronics have not yet decided which ones are the best. Ask your friends who know. Try several kinds. You will find that you get more errors on some than on others.

7. Diskettes are usually initialized by the manufacturer in some way. IBM format dictates a certain sequence of information about track number, sector number, fill characters, etc. on each track. The proper format for IBM compatibility is shown in the 1771 data sheet.

of lines on some drives to select one drive out of several on a "daisy-chain" bus.

Still other lines tell the drive whether to read or write, and to write with how much current. All of these control lines need to be driven by the interface, normally at high-current TTL levels.

There are also a set of status lines which originate in the drive and come back to the interface. These lines tell the interface what is going on in the drive.

There is usually a ready line, set true when the drive is up to speed and a disk is in place. The index line has a pulse on it that indicates when the index hole in the diskette passes by the opening made for it. This is used by the interface to determine which sector is which on the track.

Some drives have a way to detect a notch cut out of the diskette holder, which indicates that disk is not to be written upon (write protected). There is usually a line going back to the interface to indicate this condition, so the controller can feed the information back to a program, and so the interface won't try to write to the disk. Another line indicates when the head is at track zero. Some drives have a write-fault flip-flop, which is set by an attempt to write when it was not possible. The output of this flip-flop is sometimes a status line.

You may begin to see now one reason why the floppy disk system is complicated: there are a lot of status and control lines to keep up with.

DEVICE-SELECTION (BOARD ADDRESSING)

The first task of the interface is to recognize when the program sets the hardware for a read or a write operation to the disk. Selection circuitry is used to recognize 5 of the 256 possible I/O addresses. In this way, the floppy disk interface will respond only to the I/O instructions given to it, and not to those intended for other interfaces. The components associated with this process are located in the lower part of the schematic, slightly to right of the middle. These are dip-switch S-1 (5 positions used here), DM8131 U25 (a 6-bit comparator), 74LS32 OR gates U27, a 3-input NAND gate from 74LS10 U43, plus a few inverters.

The comparator checks for a match between the 5 high bits of the device address (lines A3, A4, A5, A6, and A7) and the bit pattern set on the dip switch. If the five lines (B1-B5) on the left each have the same logic level as the ones on the right (T1-T5), then the

comparator output at pin 9 goes low, indicating the disk interface is being selected. For any other combination, pin 9 goes high, and the instruction on the bus if left for some other interface.

Since the lower three address bits (A0, lA1 and A2) can be any one of eight combinations, eight I/O ports out of the possible 256 are selected for use with the disk interface. Which set of eight depends on the upper five bits selected by the dip-switch.

From now on, let's assume that the upper five bits match--that is, an input or output instruction has been put on the bus with the correct address for the disk interface, so that the comparator output goes low). Note that this output goes up to an input on each of two OR gates (these gates are drawn as AND gates, to indicate that because of the inverted input signals, the AND function is being performed--ie. when both inputs of a gate are low, the output of the gate is low. On the top one of these two gates, pin 4 is connected to address line A2. So when A2 is low (and we've already said pin 5 is low), the gate's output at pin 6 is also low (active). This line is called CS*, for chip-select-not, and is connected to the 1771 chip-select line. This line, then, will be active anytime there is a transfer to be made between the computer and the 1771.

A similar decoding scheme sets each of the other individual operations. The table below shows how the address decoding scheme is set up, and the lines that are active for each situation.

A2	A1	A0	FUNCTION OUT	FUNCTION IN	LINE ACTIVE
0	0	0	Command to 1771	Status from 1771	CS*
0	0	1	Track to 1771	Track from 1771	CS*
0	1	0	Sector to 1771	Sector from 1771	CS*
0	1	1	Data to 1771	Data from 1771	CS*
1	0	0	decoded by U56	see table below	U43-6,U27-8
1	0	1	Not used	Not used	
1	1	0	Not used	Not used	
1	1	1	Not used	Not used	

Notice that no further decoding of address bits A0 and A1 is required to perform the first four functions in the table. That's because these functions are decoded inside the 1771. Notice also that U-55 pin 4 is fed by U3-3, which is true when PDBIN is high and SINP* is low (both true). This indicates to the 1771 that an input (1771-to-computer) operation is taking place. U55-2 is fed by U43-6, which is true when an output (computer-to-1771) transfer is taking place; PWR* and SOUT are both true.

If A2, A1 and A0 are 1, 0 and 0 respectively, and the other five I/O address bits match the setting of

switch S1, gates U44, U43, U27 and U25 (all in lower right) pull line IO* down. This line, along with an active low signal from U43 (when SOUT and PWR* inverted are true) enables U56 (a 3-to-8 line decoder). This is the fifth state given in the table above. Enabling U56 allows it to pull one of its output lines low in accordance to the state of the three least-significant data-out lines, D0, D1, and D2 which are the inputs to the decoder. Only the top three of the available 8 outputs are used: Y5, Y6, and Y7. This actually decodes the bottom three combinations of D0, D1, and D2, since these lines are active low (inverted). The table below shows what these combinations are used for:

D2	D1	D0	Y	U56-	FUNCTION DESCRIPTION
0	0	0	7	7	Pad E-32, can be used to pulse RST* line
0	0	1	6	9	Inverted, then to E-14 for SO* line
0	1	0	5	10	Strobes data bits 4,5,6,7 into latch U40

BUFFERS

Once the board has been selected and the operation decoded, the actual data transfers are done by a series of buffers.

The buffers in this interface have three main purposes: 1) To protect the expensive LSI chip (1771 IC) from voltage transients on external lines; 2) To provide sufficient drive current for the lines that need it; 3) To provide multiplexing (switching) of two data paths. The signal that comes out of a buffer is either the same signal that went in or simply the inverted form of what went in.

Looking in the lower left corner of the schematic, we see a row of 12 buffers. All the data inputs for these buffers come from the disk drives(s), and all the outputs go someplace in the interface. The line on the top of each buffer is the control line. When this line is low, the buffer is active--that is, the output equals the input for that buffer. When the control line is high, the output for that buffer is floating in an open state so it does not affect any connecting circuits. Notice that every other buffer is hooked to the same control line, and that there are two main control lines. One control line activates the buffers that have signals from drive number 0, the other control line activates the buffers that have signals from drive number 1. Thus the buffers are acting as a 12-line to 6-line multiplexer. This multiplexing operation is only necessary if there is more than one drive, and the drives do not have multiplexers built in (most late-model drives do).

Also notice the 120 ohm resistors on the inputs of these buffers. They have two purposes. One is to

match the normal low line impedance so that ringing caused by reflections will be minimized. The other is to make it difficult for external noise to provide enough current to cause a false signal on the line. The six outputs of these buffer pairs will be called by their signal name, while their inputs are named by the signal line plus the number of the drive (i.e., RDY, RDY0, and RDY1).

Next move your eye on the schematic up and slightly to the right. There is a row of five 7438 2-input NAND high- current open-collector gates. These are used as buffers in this interface. Their main advantage is that they are capable of supplying the high current required by the floppy drive(s). They also can double as NAND gates. As set by the jumpers, they are used to send the appropriate signals from the 1771 to the various disk control lines (see the 1771 data sheet and your drive's manual for a full explanation of the various lines). If both inputs to these gates are a logic high, the output is low. To the right, in the middle of the schematic, are seven more of these 7438 buffers. These too go to the drive(s).

About two thirds of the way to the right near the top of the schematic, there are two rows of 8 buffer/inverters each. These buffers link the computer input and output data busses to the 1771 data bus. The inputs to the left row of buffers come from the S-100 bus. The control lines for all these buffers are connected together. When this control line is low, the data on the output data bus is inverted and gated onto the 1771 data bus. The gates on the right hand side do the reverse: when their control line is low, the data on the 1771 data bus is gated onto the computer's input data bus.

The last set of buffers is on the far right-hand side of the schematic, and is a row of nine non-inverting buffers. Their purpose is to suspend the usual CPU control of the data bus and gate the proper control signals onto the S-100 status lines to put the bootstrap in operation. When their common control line is low, whatever is on their inputs is gated to their outputs. Once the bootstrap is completed, U43, U34, and U37 relinquish control back to the bus.

Bootstrap is initiated by NOR gate U28 (lower right) receiving Power On Clear (also generated by RESET) from the computer, which sets flip-flop U34 (upper right). The not-Q output, if passed by S1 position 5, is the bootstrap signal. This gates those nine buffers, and is used along with a signal from U37 (upper right) to activate U27 (middle) during the read cycle, thus reading from the 82S123 memory but writing through the bus to regular RAM.

TIMING CIRCUITS, SEPERATOR, AND PROCESSOR HOLD

At the lower right of the schematic, U1, U2, U17, U33, U34, U35, and U36 form the clock and data seperator, which operates on the raw data which comes in on the line wich runs across the very bottom of the schematic. The actual clock oscillator circuit (also lower right) is composed of two sectons of U17 plus the 4MHz crystal Y1. Grounding pin 25 of the 1771 (XTDS*) disables the internal seperator.

On the bottom middle, the INTRQ and DRQ signals from the 1771 are used to control the run or wait state of the CPU through gates U30 and U57 and bus signals PRDY or XRDY. These circuits allow the 1771 to temporarily suspend execution of the next CPU instruction until an internal process has been completed.

HEAD-LOAD CIRCUIT

The 1771 checks for head-load by looking at the HLT line 10 milliseconds after the HLD line is activated. U41 and U57, in the upper-left corner of the schematic, sample the HLD line and generate the proper delay to allow for the physical head-load time of the drive before passing the signal on to the HLT input of the 1771.

STEP-IN AND STEP-OUT CIRCUIT

The 1771 signals your drive to step the head in or out by providing a short pulse from the step output and a DIRC output which is high for stepping in and low for stepping out. These signals must be reformatted for many drives, and they must be buffered. The circuitry at U59, U51 and U61, all in the upper left side, perform these tasks.

Most drives require a longer step pulse than is output at pin 15 of the 1771, so one-shot U51 is used to stretch the pulse out. For drives which require a step signal and the same polarity direction signal, like the Innovex 410, the other signals are simply buffered and then routed to the drives by the appropriate jumpers. For drives like the CDC BR803A, which require a step-in and step-out line, the jumpers are set to make these circuits decode those signals from the DIRC and step lines.

A few drives require step signals faster than those generated by the 1771. The line into pin 1 of buffer U59 can be driven directly by the computer, and can therefore be pulsed at a much faster rate. However,

in this case, the program must keep track of the number of pulses that this line puts out, plus observing any timing constraints.

WRITE DATA, WRITE GATE, TRACK GREATER THAN 43

The write data, write gate, and track greater-than-43 signals control the write-to-disk functions. The circuits to control these signals are just above the middle left.

The write-data line contains the actual data mixed with a clock signal. From pin 31 of the 1771, it goes through buffer U57, and line driver U62, and then out through the jumpers to the disk. The TG43 line which tells the drive to reduce the head current while writing on the physically smaller tracks is set high when the track number is higher than 43. From the 1771 pin 29, it goes to U35, where it can be inverted for drives which require the opposite polarity, and then through driver U62 and the jumpers out to the disk.

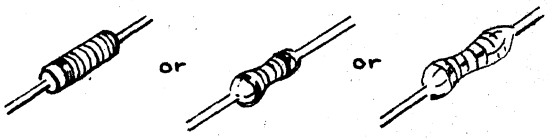
The write-gate signal tells the drive that it is time to start a write operation. It comes out of the 1771 pin 30, is buffered by U57, and NANDed with the write protect signal at U62, where it goes to the jumper pads and the disk. The write gate signal can only go active (low) when switch position 6 of DIP-switch S1 is off, providing a logic 1 to pin 5 of U62. This switch allows you to prevent any write operation to the disk, regardless of any deliberate or accidental commands in the program. When this switch is not in the protect position, any time the write-gate is driven high from pin 30 of the 1771, the disk will be overwritten.

POWER SUPPLY (VOLTAGE REGULATOR) SECTION

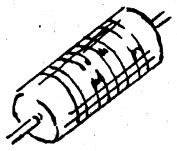
The interface requires +5 Volts, +12 Volts, and -5 Volts. These are provided by on-board regulators driven from the unregulated DC voltages of the S-100 bus.

A 7805 (LM309) regulator supplies the +5 Volts. To make it run a little cooler, a 15 Ohm 2 watt resistor has been placed in parallel to bypass some of the current while still allowing the regulator to control the voltage.

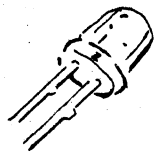
The +12 Volt DC is regulated by a 12 Volt zener and 120 ohm resistor, since this supply must only provide a small amount of current. The -5 Volt supply is a similar zener-resistor pair.



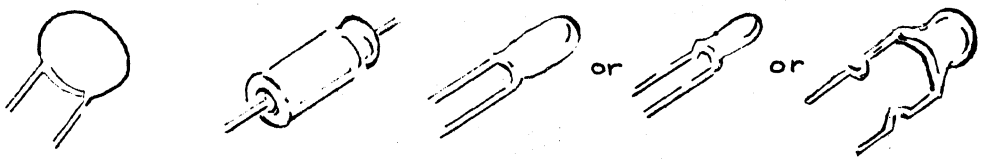
¼ W resistors



2 W resistor



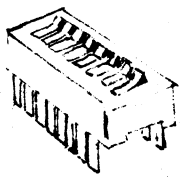
LED



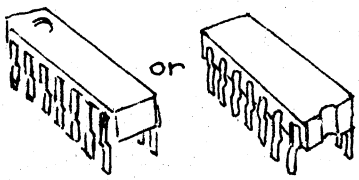
disc capacitor

electrolytic capacitor

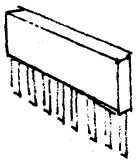
mylar capacitors

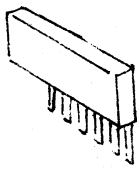


DIP switch



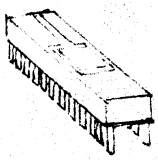
integrated circuits



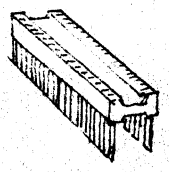


resistor networks

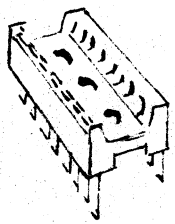
crystal



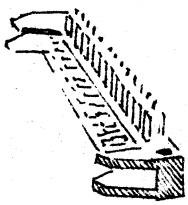
1771



40-pin socket



16-pin socket



50-pin header

PARTS LIST - JULY 28, 1977

QTY	PART NØ.	REF. NUMBERS	DESCRIPTIØN
4	74LS367	U18,19,24,30	HEX BUFFER
3	8T97	U52,53,57	HEX BUFFER
1	82S123	U23	32-BYTE PRØM
2	74LS32	U27,29	QUAD 2-INPUT ØR GATE
1	DM8131	U25	6-BIT DIGITAL CØMPARITØR
1	74LS10	U43	TRIPLE 3-INPUT NAND GATE
3	74LS04	U17,44,59	HEX INVERTER
3	74LS08	U28,36,63	QUAD 2-INPUT AND GATE
2	74LS00	U3,45	QUAD 2-INPUT NAND GATE
3	74LS368	U20,21,22	HEX TRI-STATE INVERTER
1	74LS74	U34	DUAL TYPE-D FLIP-FLØP
3	74LS175	U33,37,40	QUAD LATCH
1	74LS86	U35	QUAD EXCLUSIVE-ØR GATE
2	74LS161	U1,2	4-BIT BINARY CØUNTER
2	74LS123	U41,51	DUAL RETRIGGERABLE 1-SHØT
3	7438	U42,61,62	QUAD 2-INPUT NAND BUFFER Ø/C
1	74LS138	U56	3-8 LINE DECØDER
1	7805UC	U65	5-VØLT REGULATØR
1	FD1771B-01	U55	FLØPPY DISK CØNTRØLLER
4	4.7K-1/4W	R14,16,20,30	4.7 KØHM 1/4 WATT RESISTØR
2	10K-1/4W	R21,22	10 KØHM 1/4 WATT RESISTØR
14	120-1/2W	R1-12,19,24	120 ØHM 1/2 WATT RESISTØR
1	330-1/4W		330 ØHM 1/4 WATT RESISTØR (FØR TESTS)
1	15K-1/4W	R13	15 KØHM 1/4 WATT RESISTØR
1	510-1/4W	R15	510 ØHM 1/4 WATT RESISTØR
2	33K-1/4W	R17,18	33 KØHM 1/4 WATT RESISTØR
1	470-1/2W	R23	470 ØHM 1/2 WATT RESISTØR
1	15-2W	R27	15 ØHM 2-WATT RESISTØR
2	1K-1/4W	R28,33	1 KØHM 1/4 WATT RESISTØR
1	2.2K-1/4W	R29	2.2 KØHM 1/4 WATT RESISTØR
1	1K-RES-NW	Z1	1 KØHM RESISTØR NETWØRK - 8 PIN
1	4.7K-RES-NW	Z2	4.7 KØHM RESISTØR NETWØRK - 6 PIN
15	.1MFD	C6,8,9,10,11-21	.1 MFD 10-VØLT CAPACITØR
1	33MFD	C2	33 MFD 10% CAPACITØR
1	4.7MFD	C5	4.7 MFD 10% CAPACITØR
1	390PF	C22	390 PF CAPACITØR
1	1000PF	C4	1000 PF (.001 MFD) 10% CAPACITØR
2	22MFD	C1,C3	22 MFD 25-VØLT CAPACITØR
1	1N751A	VR1	5.1-VØLT 1/2 WATT ZENER
1	1N4742A	VR2	12-VØLT 1 WATT ZENER
1	LED		LIGHT-EMITTING-DIØDE (FØR TESTS)
1	CY3A	Y1	4 MHZ CRYSTAL
1		U26(S1)	7-PØSITIØN DIP-SWITCH
1	362-BA	HS1	HEAT SINK
1			#6 SCREW, NUT, WASHER (FØR HEAT SINK)
2			#2 SCREW, NUT, WASHER (FØR HEADER)
1	1011		PRINTED CIRCUIT BØARD
1			50-CØNDUCTØR CABLE & 1 CØNNECTØR
1	3433-1002		50-PIN HEADER CØNNECTØR
1			16-PIN DIP SØCKET
1			40-PIN DIP SØCKET

ASSEMBLY

The assembly of the disc interface consists of a series of small steps, each one of which should be checked before proceeding to the next one. You should have a computer mainframe of the IMSAI or ALTAIR type available.

You may elect, of course, to disregard the detailed instructions, and just mount the components as shown in the assembly drawing, plug the board in, and hope for the best. If you do take this route, please at least check the voltages that go to the 1771 chip before this last part is installed (+5, -5, +12).

NOTES:

1) When the instructions say "Install board in mainframe in test configuration", make sure mainframe power has been off for at least 10 seconds, then install the board in any slot. No other interface board or memory board should be in the mainframe unless specified in the instructions. At the end of the test, turn off mainframe power and wait at least 10 seconds before removing the disk interface board.

2) "Locate and install" means find the indicated parts, mount each one as shown on the circuit board diagram, and solder them in place.

****

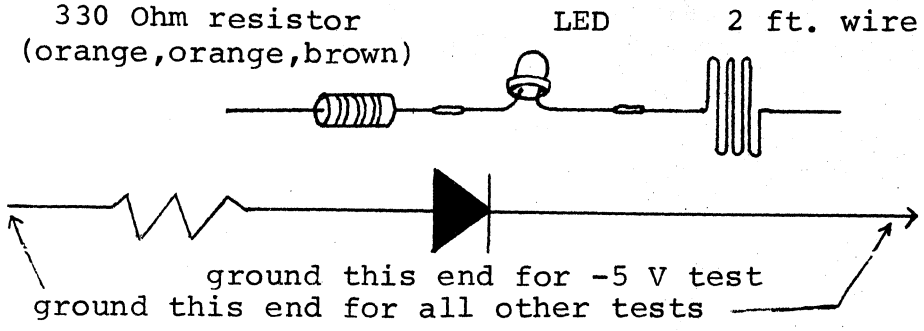
1. Inspection

( ) Check the printed circuit board carefully for flaws. Look especially closely for any shorts between traces which might later be covered under a socket or IC

( ) Check contents of kit against parts list. If any parts are missing, contact Tarbell Electronics for prompt correction. If you have any extra parts, be sure and note this too, so they won't confuse you later on.

2. Construct LED (Light-Emitting-Diode) Tester

( ) Find the 330 ohm resistor (orange, orange, brown) and the LED. As shown in the diagram, solder the LED anode (usually the anode is marked in red, or the cathode is a wider lead) to the resistor. Connect the LED cathode to a two-foot length of scrap flexible insulated wire (18-24 gauge is best). Strip about 1/4 in from the end of the wire. This assembly will be referred to as the "LED probe".



3. Install 40-pin socket

( ) Find the 40-pin socket. Using the parts layout diagram, orient the socket so the notch indicating pin 1 faces the top of the card and pin 1 fits in the square pad.
( ) Insert the socket, and carefully check that every pin is showing through on the solder side of the board.
( ) Hold the socket in firmly and solder all pins.

4. -5 Volt regulator

( ) Locate and install the following components:
  ( ) R23--470 ohm 1/2 watt resistor (yellow, violet, brown)
  ( ) VR1--5.1 volt zener diode (marked 1N751); make sure polarity band is at left
  ( ) C9--.1 MFD 10-volt disc ceramic capacitor.

Test--Install board in mainframe in the test configuration.

( ) Temporarily connect the resistor end of the LED probe to a circuit ground. Touch the end of the wire from the probe to the left end of R23, which connects to the -16 volt bus. Notice the relative brightness of the LED.
( ) Move the wire to the right end of R23. The glow should be considerably less but not extinct.
( ) If you have a voltmeter or oscilloscope, check that voltage at the right end of R23 is -5.1 within 10%.

5. +5 Volt regulator

( ) Find the parts for the 5-volt regulator: ( ) 7805 or LM309 3-pin IC; ( ) regulator heat sink; ( ) #6-32 mounting screw, and matching nut and washer;
( ) Using the assembly diagram, position the regulator at U65. Insert the leads through the appropriate holes.
( ) With the heat sink in place between the regulator and the board, bend the regulator pins over and fasten the regulator body against the heat sink with the screw and washer on the solder side of the board and the nut on the parts side. Solder the regulator in.
( ) Install a 22 mfd. capacitor at C1 observing polarity shown on diagram.
( ) Install the other 22 mfd. capacitor at C3, again observing polarity.

Test--Install the board in the computer mainframe in the test configuration.

( ) Connect the wire lead end of the LED probe to a good circuit ground. This end will remain connected for the rest of the assembly process. Touch the resistor end of the probe to the bottom lead of the +5 volt regulator (U65). Note the relative brightness.
( ) Move the probe to the middle lead of the regulator. The light should go out altogether--if not, this pin is not properly grounded.
( ) Move the probe to the top lead of the regulator. The LED should glow with slightly less brightness than at the bottom lead.
( ) The top lead should measure +5 volts within 10% using a voltmeter or oscilloscope.

6. +12 Volt regulator

( ) Locate and install the following parts:
  ( ) R24--120 ohm 1/2 W carbon resistor (brown, red, brown)
  ( ) VR2--12-volt 1 W zener diode (marked 1N4742); be sure to place the polarity band of VR2 at right, as shown on the asssembly diagram
  ( ) C10--.1MFD 10-volt disc ceramic capacitor.

Test--Install the board in the test configuration.

( ) Place the tip of the LED probe on the left end of R24. Notice the brightness.
( ) Touch the probe to the right end of R24. Check that the glow is less, but still quite visible.
( ) If you have an oscilloscope or voltmeter, the voltage at the left end of R24 should be +12 volts within 10%.

NOTE--Do not proceed until you are confident the foregoing circuits are working properly. If not, they might damage the 1771 IC or other expensive chips.

7. Primary address circuit

( ) Locate and install the following parts:
  ( ) U24--74LS367 hex buffer IC.
  ( ) U25--DM8131 6-bit comparator IC.
( ) Install the 4.7K 6-pin in line resistor network at Z2 with the dot in square pad.
( ) Install switch S1 (7 position DIP switch) in the upper 14 holes at U26--this will leave two empty holes at bottom.

Test--Install board in test configuration.

( ) Set all switch positions off;
( ) Using the computer's front panel switches, examine location F8 (hex).
( ) Using the LED probe, check that pin 9 of IC 25 is in the low-state (out).
( ) Check that the LED goes on if any of the address switch positions (S1 1 to 5) on the board are changed.

( ) Reset the switches, and check that the LED goes on if any other location smaller than F8 is examined.

8. Secondary Address Gate Circuitry

( ) Locate and install the following components:
  ( ) U28--74LS08 quad 2-input and gate IC
  ( ) U30--74LS367 hex buffer IC
  ( ) U57--8T97 hex buffer IC
  ( ) R20--4.7K ohms 1/4 watt resistor (yellow, violet, red)
  ( ) R16--4.7K ohms 1/4 watt resistor (yellow, violet, red)
  ( ) R14--4.7K ohms 1/4 watt resistor (yellow, violet, red)
  ( ) R15--510 ohm 1/4 watt resistor (green, brown, brown)
  ( ) C8--.1MFD 10 volt disc ceramic capacitor
  ( ) R28--1K ohm 1/4 watt resistor (brown, black, red)
  ( ) R33--1K ohm 1/4 watt resistor (brown, black, red)

Test--Install board in test configuration.

( ) Connect probe to U28 pin 8. Push reset switch on computer. Pin 8 should go low (LED out).
( ) Push the external clear switch on computer. Pin 8 should go low.

9. Command Logic decoding gates

( ) Locate and install the following components:
  ( ) U27--74LS32 quad 2-input OR gate IC.
  ( ) U43--74LS10 triple 3-input NAND gate IC.
  ( ) U44--74LS04 hex invertor IC.

Test--Install the board in the test configuration.

( ) Set all switch positions to off. This sets the base address to F8 (hex).
( ) Use the LED probe to look at U27 pin 6 and U27 pin 8 for high (LED on) or low (LED off) states as follows--examine each location shown in the address table below, and check that U27 pin 6 and 8 shows the indicated state:

FUNCTION	ADDRESS	U27 PIN 6	U27 PIN 8
Status/Command Port	F8	Low	High
Track Command	F9	Low	High
Sector Command	FA	Low	High
Data Port	FB	Low	High
Wait/Control Port	FC	High	Low
Unused	FD	High	High
"	FE	High	High
"	FF	High	High

10. Read-write-control decoding gates.

( ) Locate and install the following components:
  ( ) U3--74LS00 quad 2-input NAND gate IC.
  ( ) U22--74LS368 hex invertor/buffer IC.
  ( ) U29--74LS32 quad 2-input OR gate IC.

Test--Install board in test configuration.

( ) Install a memory card addressed at location 0. Using the computer's front panel switches, load this data:

ADDRESS	DATA
0000	DB
0001	F8
0002	C3
0003	00
0004	00

( ) Connect probe to U29 pin 11. Examine location 0 and single step. When the input light on your front panel comes on, U29 pin 11 should go low.

( ) Install (with power off) a memory card addressed at 0. Using the computer front panel switches, deposit D3 (hex) at location 0. Examine location 0. Attach probe to U43 pin 6.

( ) Check that the probe indicates a high state. Single step computer usings ts front panel switch. When the front panel "OUT" light goes on, U43 pin 6 should go low.

11. Bus Control

( ) Locate and install the following components:
  ( ) R29--2.2K ohm 1/4 watt resistor (red, red, red).
  ( ) U34--74LS74 dual type flip flop IC.
  ( ) U18--74LS367 hex buffer IC.
  ( ) U19--74LS367 hex buffer IC.
  ( ) U20--74LS368 hex invertor/buffer IC.
  ( ) U21--74LS368 hex invertor/buffer IC.
  ( ) U17--74LS04 hex invertor IC.
  ( ) U37--74LS175 quad latch IC.

Test--Install board in test configuration.

( ) Set switch position 7 off. Turn power on and hit the reset switch. Front panel lights "MEMR", "M1" and "WO" should be on.

( ) Set switch 7 to on. Front panel lights "WO" and "WAIT" should be on. All data lights should also be on.

12. Oscillator section

( ) Locate and install the following components:
  ( ) C6--.1 microfarad capacitor.
  ( ) U33--74LS175 quad latch IC.
  ( ) Z1--1K ohm in line 8-pin resistor network.
  ( ) Install the 4 MHz crystal at Y1. If your crystal has mounting holes in the side of the case, thread a small piece of wire through the holes in the crystal case and solder to the board at each end to hold the crystal down.

Test--Install the board in the test configuration.

( ) If possible, use an oscilloscope to look at pin 6 of U17. You should see a 4 MHz square wave.

( ) If no scope is available, use the LED probe. First, touch the probe to U17 pin 14. Note the LED intensity. Now, touch the probe to pin 6, U17. The LED should still glow but less intensely. If the LED is as bright as at pin 14, or is not on, then the oscillator is not working.
( ) Using the probe, check that U33 pin 10 also shows a glow between the intensity at U17 pin 14 and nothing.

13. Install rest of clock/data separator.

( ) Locate and install the following components:
  ( ) U35--74LS86 quad exclusive OR gate IC
  ( ) U1--74LS161 binary counter IC
  ( ) U2--74LS161 binary counter IC

There is no test for this section.

14. Data I/O buffers and status/control

( ) Locate and install the following components:
  ( ) U23--16 pin IC socket for 82S123 PROM
  ( ) U36--74LS08 quad 2-input AND gate IC
  ( ) Install the 82S123 programmable read-only memory IC in the socket at U23.

Test--Install the board in the test configuration.

( ) Set switch position 7 to off. Hit the reset button on computer. All data lights should be on.
( ) Move switch position 7 to on. Data bus should now be DB (hex).
( ) Using the examine switch, check the next 31 bytes against the bootstrap program--
0000: DB FC AF 6F 67 3C D3 FA 3E 8C D3 F8 DB FC B7 F2
0010: 19 OO DB FB 77 23 C3 OC OC DB F8 B7 CA 7D OO 76

15. Install remaining components.

( ) Install the thirteen 120 ohm 1/2 watt resistors at the following locations:
( ) R1, ( ) R2, ( ) R3, ( ) R4, ( ) R5, ( ) R6, ( ) R7,
( ) R8, ( ) R9, ( ) R10, ( ) R11, ( ) R12, ( ) R13.
( ) Install the eleven .1 MFD disc ceramic capacitors at the following locations:
( ) C11, ( ) C12, ( ) C13, ( ) C14, ( ) C15, ( ) C16,
( ) C17, ( ) C18, ( ) C19, ( ) C20, ( ) C21.
( ) Install the following components:
  ( ) U52--8T97 hex buffer IC.
  ( ) U53--8T97 hex buffer IC.
  ( ) U45--74LS00 quad 2-input NAND gate IC
  ( ) R27--15 ohm 2 watt resistor (brown, green, black)
  ( ) R21--10K 1/4 watt resistor (brown, black, orange)
  ( ) R22--10K 1/4 watt resistor (brown, black, orange)

( ) U59--74LS04 hex inverter IC
( ) U41--74LS123 dual one-shot IC
( ) R18--33K 1/4 watt resistor (orange, orange, orange)
( ) C5--4.7 MFD 10% capacitor
( ) U51--74LS123 dual one-shot
( ) R17--33K 1/4 watt resistor (orange, orange, orange)
( ) C4--1000 pF capacitor
( ) R13--15K 1/4 watt resistor (brown, green, orange)
( ) C2--33MFD capacitor
( ) R30--4.7K ohm 1/4 watt resistor (yellow, violet, red)
( ) U61--7438 quad 2-input NAND buffer IC
( ) U62--7438 quad 2-input NAND buffer IC
( ) U63--74LS08 quad 2-input NAND gate IC
( ) U40--74LS175 quad latch IC
( ) U56--74LS138 3-8 line decoder IC
( ) U42--7438 quad 2-input NAND buffer IC
( ) C22--390 pF disk ceramic capacitor

16. 50-Pin connector

( ) Mount the 50-pin connector from the component side of the board. Check that all the pins show through on the solder side.
( ) Using the number 2 screws from the rear side of the board and the nuts on the component side, screw the connector down tight.
( ) Solder each one of the 50 connector pins on the solder side. Make sure that none have been overlooked.

* * * * *

You should now be all out of components, except for the cable and the 1771 IC. If you have components left over, use the parts list and the assembly diagram to make sure that a proper part has been installed at each position. If so, you may just have some extra parts.

Check to see that the following slots on the board are not used:

( ) U46, ( ) U47, ( ) U48, ( ) U58, ( ) U64--spare IC slots
( ) R34 and ( ) C24--for the spare one-shot
( ) C7 not used.

USING THE JUMPER PADS

The system of jumper pads on the Tarbell floppy disk interface is designed to allow maximum flexibility in matching the interface to your floppy disk drive requirements. There are also four spare IC slots that may be used in conjunction with the jumper pads to implement special circuits.

We have worked out the jumper positions for some of the popular drives, and will be doing some more. If you work out your own jumper set-up for a drive that is not listed, or if you find something wrong with the set-ups we have, please write to us and let us know what you did.

If you want to set up your own drive configurations, the functions of the jumper pads are as follows:

NOTES:

1. Some drives (see individual listings) require a connector on the end of the 50-line ribbon cable which can only be installed using a special tool. Tarbell Electronics has the connectors and the tool, and can install one on your cable for $10.

2. At the board end of the cable, the connector pins are numbered alternatedly from 1 to 50, going from left to right. All the odd-numbered ones are grounded. The signal leads are thus J2, J4, etc.

3. When installing the power supply, use fairly heavy wire, and twist each power line with a ground line. Before plugging in the drive, check the voltages on each pin of the connector with a voltmeter.

4. Also, it is a good idea to do a continuity check on each of the interconnections between board and drive before you fire your drive up the first time. Look especially for inadvertently-switched lines.

E1,E3 Inputs to 7438 gate which drives S0* line to floppy drive. Must both be high to make S0* line active (low).

E5,E7 Inputs to 7438 gate which drives SI* line to floppy drive. Must both be high to make SI* line active (low).

E8,E9 Both come from the output of a 12 microsecond one-shot which is triggered by the 1771 step output. These are active high. The repetition rate of these pulses is dependent upon bits 0 and 1 of a type 1 command to the 1771 as shown in the data.

E10,11 These pads are both connected to the pull-up line #2, which has a 1K pull-up resistor to +5 volts.

E12 This active low line is an inverted version of the DIRC step direction line which comes out of the 1771. This line is low for step-in and high for step-out.

E13 This line is just the inverted version of E12; that is, it is low for step-out and high for step-in.

E14 This line will produce a positive-going pulse for one computer clock time, when an out instruction is given to port XXXXX100 (X's are selected by DIP-switch) and the data sent out from register A in the 8080 has the lower bits 001 (MSB first). This line is used to pulse the S0* line at a higher rate than the 1771 can do directly. This may be necessary when using a floppy disk drive with a high step rate, such as the PERSCI drives.

E15-E27 Interface to disk lines: See pin function page for details.

E28 This line is active high when an OUT instruction is given to port XXXXX100 as above, only the data is UU00U010. (U means that the corresponding bit has no effect on this line). This line may be used to activate the HLD3 line through E38.

E29 This line controls which set of lines is selected that come from the floppy disk drive. When E29 is low, the line names ending in a zero (RDY0, INDX0, etc.) are selected; these are marked R1,R3,R5,R7,R9, and R11 on the top right hand side of the board. When E29 is high, the line names ending in a one are selected; these are marked R2,R4,R6,R8,R10, and R12 on the board.

E30 This pad is connected directly to ground, and may be used to always select drive 0, when connected to E29 above.

E31 This is connected to the least significant bit (Bit 4) of the latch, and may be used to select drive 0 or 1 under software control, when connected to E29 above. This line is set according to bit 4 of the output instruction when the lower bits are 010, and the address is XXXXX100.

E32 This is a pulsed active low line, similar in operation to that of E14, except the low data bits need to be 000. When connected to E34, it may be used to pulse the RST* line.

E33 This line is connected to the latch bit 3 inverted. It may be used to make RST* stay high or low, when hooked to E34.

E34 This is hooked to an input of a NAND gate, the other of which is the internal master reset line. When either of these lines goes low, the RST* line is activated. The RST* line can be used either as a reset line for the floppy drive, or it can be used for a third drive-select line in systems incorporating binary select.

E35 The active high output line of the spare one-shot in U41.

E36 The negative-going trigger input of the spare one-shot in U41.

U37 The positive-going trigger input of the spare one-shot in U41.

E38,E39 These are the two inputs to the 7438 buffer gate that activates the HLD3 line going to the drive. If E38 is hooked to E28, and E39 is hooked to E53, then HLD3 is treated the same way as HLD0, HLD1,

and HLD2. These four lines can then be used to select four drives in a radial-select fashion. As an alternative, E39 may be connected to pull-up E40, and E38 can be connected to E52 (latch Q2*) or E42 (latch Q1*) and used for another disk control line.

E40 Connected to pull-up line #3, 1K to +5 volts.

E41 An input to a 1-4 decoder, normally connected to E52.

E42 Connected to latch bit 1 inverted.

E43 Goes directly to the ready line (an input) on the 1771. The 1771 will not perform a read or write operation without this line being active high. Connect to E44 if your drive has a ready line, and to E45 if it doesn't.

E44 Comes from the selected disk drive's ready line, after which it is inverted to make it in proper phase for E43.

E45 Is the output of a one-shot which is triggered by the selected drive's INDX (index) line. This can be used as a ready line, in case your particular drive doesn't have one. The one-shot, being of the retriggerable type, stays high as soon as the index pulses come close enough together to indicate that the disk is turning properly.

E46 This line comes from pin 3 of the computer bus, which is called XRDY.

E47 This line comes from pin 72 of the computer bus, which is called PRDY.

E48 This line is used to stall the machine in the wait state for operations that must respond quickly, such as read and write. It should be connected to E47 on IMSAI computers, and to E46 on ALTAIR computers--at least on the ones we've seen. If you want to double-check your machine, look at the schematic of the front panel on your computer. Either pin 3 (E46) or pin 72 (E47) will be connected to the output of a gate. Connect E48 to the other one.

E49 When E49 is connected to E50 (ground), TG43* going to drive is active low when TG43 coming from 1771 is active high. If the drive requires TG43* to be the opposite polarity, don't install this jumper.

E50 Ground for possible connection to E49.

E51 HLD (head-load) line buffered from 1771 pin 28. This line is active (high) when the 1771 decides that the head should be loaded against the disk. See the 1771 data sheet for further detail on the operation of this line.

E52 Latch bit 2 inverted, usually connected to E41.

E53 Common input on 7438 buffer gates which drive HLD lines to disk; is usually connect to either E51 or E40.

E54 Latch bit 2 non-inverted; may be connected to E55..

E55 Input to gate which drives E23. Connected to E54 or E51.

NOTE: Be sure to hook up E48; either to E46 or E47. See details above.

JUMPER SET-UP FOR CDC BR803A

( ) Make a one-one connection from the 50-pin connector(s) on the top of the PC board, through the 50-pin ribbon cable(s), to the connector(s) for your drive(s), except for pins 41 and 42. Since there are no pins 51 and 52 on the cable, pins 41 and 42 of the cable should be connected to pins 51 and 52 on the drive connector.

( ) See the general jumper set-up instructions for information about:

1) pin numbering at J1;
2) power supply connections;
3) pre-operation checks;
4) whether to hook E48 to E46 or E47.

Following are the jumpers to install for a 1 or 2-drive system:

	PAD	NAME	TO	NAME
( )	R11	RDAT0*	J1-20	Read data (composite) drive 0
( )	R12	RDAT1*	J2-20	Read data (composite) drive 1
( )	E19	HLD0*	J1-26	Head load drive 0
( )	E20	HLD1*	J2-26	Head load drive 1
( )	R7	TR00*	J1-28	Track 00 Drive 0
( )	R8	TR01*	J2-28	Track 00 Drive 1
( )	R3	INDX0*	J1-32	Index drive 0
( )	R4	INDX1*	J2-32	Index drive 1
( )	E18	TG43*	J1-36	Low current drive 0
( )	E18	TG43*	J2-36	Low current drive 1
( )	R9	WRFLT0*	J1-40	Write fault drive 0
( )	R10	WRFLT1*	J2-40	Write fault drive 1
( )	E22	SO*	J1-44	Step out Drive 0
( )	E22	SO*	J2-44	Step out drive 1
( )	E21	SI*	J1-46	Step in drive 0
( )	E21	SI*	J2-46	Step in drive 1
( )	E16	WG*	J1-48	Write enable drive 0
( )	E16	WG*	J2-48	Write enable drive 1
( )	E15	WD*	J1-50	Write data drive 0
( )	E15	WD*	J2-50	Write data drive 1
( )	E26	RST*	J1-42	Write fault reset drive 0
( )	E26	RST*	J2-42	Write fault reset drive 1
( )	E13		E5	High for step-in.
( )	E12		E1	High for step-out.
( )	E9		E3	High for any step.
( )	E8		E7	High for any step.
( )	E49		E50	TG43* goes low for low current.
( )	E43		E45	There is no ready line on this drive.
( )	E31		E29	Use the input multiplexer.
( )	E32		E34	Software write-fault reset.
( )	E52		E41	Maybe more drives someday.
( )	E51		E53	Head-load hook-up.

POWER HOOK-UP (BR803A)

+5 Volts DC - pins 2&4 on both drives.
-5 Volts DC - pin 6 on both drives.
+24 Volts DC - pins 12&14 on both drives.

JUMPER SET-UP FOR INNOVEX 210/220

( ) Make a one-one connection from J1, the 50-pin connector on the left hand side of the PC board, through the 50-pin ribbon cable, to the connector for your drive. If you have more than one drive, the cable can be connected to all of them (daisy chained). All but the last drive in the chain should have their terminating resistors removed. The 4 select lines should be wired one to a drive.

See the general jumper set-up instructions for information about:

1) the special connector at the drive end:
2) pin numbering at J1
3) power connections
4) pre-operation checks
5) where to install jumper at E48

Following are the jumpers to install:

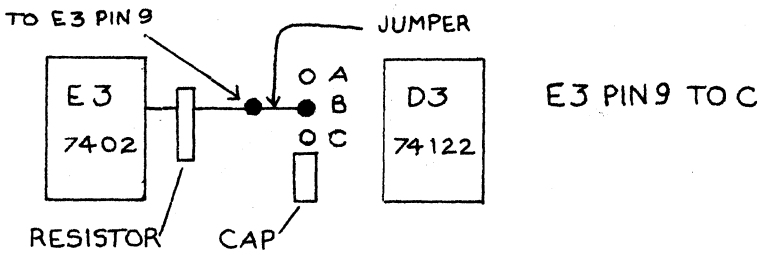
	PAD	NAME	TO	NAME
( )	E18	TG43	J1-L21	Current select
( )	E19	HLD0	J1-L18	Head load
( )	E23	INDX0	J1-L5	Index
( )	R1	RDY0	J1-L8	Ready
( )	E19	HLD0	J1-L13	Drive select 0
( )	E20	HLD1	J1-L13	Drive select 1
( )	E17	HLD2	J1-L13	Drive select 2
( )	E25	HLD3	J1-L13	Drive select 3
( )	E22	SO*	J1-L15	Direction
( )	E21	SI*	J1-L6	Step
( )	E15	WD*	J1-L10	Write data
( )	E16	WG*	J1-L7	Write gate
( )	R7	TR00*	J1-L12	Track zero
( )	R5	WRPT0*	J1-L16	Write protect
( )	R11	RDAT0*	J1-L17	Raw data
( )	E1		E13	
( )	E3		E11	
( )	E5		E10	
( )	E7		E9	
( )	E29		E30	
( )	E43		E44	
( )	E38		E28	
( )	E51		E55	
( )	E53		E40	

DC POWER CONNECTIONS TO DRIVE		AC POWER CONNECTIONS TO DRIVE	
( ) +24 VOLTS DC	R2,L2	( ) 117 VOLTS AC	PO4-3
( ) 24 VOLT RETURN	R3,L3	( ) FRAME GROUND	PO4-2
( ) -5 VOLTS DC	R20,L20	( ) 117 VOLTS AC	PO4-1
( ) +5 VOLTS DC	R11,L11		
( ) LOGIC GROUND	R1,L1,R22,L22		

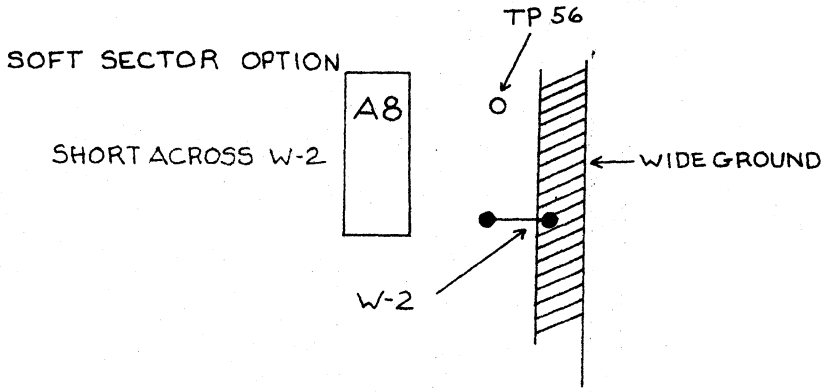
NOTE: Don't confuse the R numbers directly above with resistor numbers on the interface board. These R's are drive connector pins.

RAW DATA OPTION

JUMPER AREA



SOFT SECTOR OPTION



JUMPER SET-UP FOR INNOVEX 410

( ) Make a one-one connection from the 50-pin connector on the left hand side of the PC Board, through the 50-pin ribbon cable, to the connector for your drive(s).

( ) If you have more than one drive, they should all be connected in parallel (daisy-chain). See further instructions below.

See the general jumper set-up instructions for information about:

1) the special connector at the drive end
2) pin numbering at J1
3) power supply connections
4) pre-operation checks
5) where to connect the jumper at E48

Following are the jumpers to install for a 1 or 2-drive system:

	PAD	NAME	TO	NAME	
( )	E18	TG43	J1-2	Current select	
( )	E23	DS0*	J1-18	Head-load	
( )	R3	INDX0	J1-20	Index	
( )	R1	RDY0	J1-22	Ready	
( )	E19	HLD0*	J1-26	Drive Select 0	
( )	E20	HLD1*	J1-28	Drive Select 1	
( )	E17	HLD2*	J1-30	Drive Select 2	
( )	E25	HLD3*	J1-32	Drive Select 3	
( )	E22	SO*	J1-34	Direction	
( )	E21	SI*	J1-36	Step	
( )	E15	WD*	J1-38	Write data	
( )	E16	WG*	J1-40	Write gate	
( )	R7	TR00*	J1-42	Track zero	
( )	R5	WRPT0*	J1-44	Write protect	
( )	R11	RDAT0*	J1-46	Raw data	
( )	E1		E13		
( )	E3		E11		
( )	E5		E10		
( )	E7		E8		
( )	E29		E30		
( )	E39		E40		
( )	E28		E38	For HLD3	
( )	E41		E52	For full decoder	
( )	E51		E55	For head-load	
( )	E43		E44		
( )	E53		E40		

If more than one drive is used, each drive should have its select jumper changed (on the drive) so that each drive uses a different select line. Also only the last drive in the daisy chain should have the terminating resistors left in. Those on all other drives should be removed.

DC Power Requirements

Pin 1	+24 Volts DC
Pin 2	+24 Volt return
Pin 3	-5 Volt return
Pin 4	-5 Volts DC
Pin 5	+5 Volts DC
Pin 6	+5 Volts return

AC Power Requirements

Pin 1	110 Volts AC
Pin 2	Frame ground
Pin 3	110 Volts return

JUMPER SET-UP FOR GSI 110

( ) Make a one-one connection from the 50-pin connector on the left hand side of the PC board, through the 50-pin ribbon cable, to the connector for your drive.

If you have more than one drive, they should all be connected in parallel (daisy-chain), except for the select line--the jumper inside each drive which sets the select should be changed to a different line. The terminating resistors should be removed from all drives except for the last drive in the daisy chain.

See the general jumper set-up section for information about:

1) the special connector at the drive end
2) pin numbering at J1
3) power supply connetctions;
4) pre-operation checks
5) where to connect E48

Following are the jumpers to install for a 1 or 2 drive system:

	PAD	NAME	TO	NAME	
( )	E18	TG43	J1-16	Current select	
( )	E23	DS0*	J1-18	Head load	
( )	R3	INDX0	J1-20	Index	
( )	R1	RDY0	J1-22	Ready	
( )	E19	HLD0*	J1-26	Drive select 0	
( )	E20	HLD1*	J1-28	Drive select 1	
( )	E17	HLD2*	J1-30	Drive select 2	
( )	E25	HLD3	J1-32	Drive select 3	
( )	E22	SO*	J1-34	Direction	
( )	E21	SI*	J1-36	Step	
( )	E15	WD*	J1-38	Write data	
( )	E16	WG*	J1-40	Write gate	
( )	R7	TR00*	J1-42	Track zero	
( )	R5	WRPT0*	J1-44	Write protect	
( )	R11	RDAT0*	J1-46	Raw data	
( )	R1		E13		
( )	R3		E11		
( )	R5		E10		
( )	R7		E8		
( )	E29		E30		
( )	E39		E40		
( )	E28		E38	for HLD3	
( )	E41		E52	for full decoder	
( )	E49		E50	current select polarity	
( )	E51		E55	for head load	
( )	E43		E44		
( )	E53		E40		

DC POWER REQUIREMENTS

Pin 1	+24 Volts DC
Pin 2	+24 Volt return
Pin 3	-5 Volt return
Pin 4	-5 Volts DC
Pin 5	+5 Volts DC
Pin 6	+5 Volts return

AC POWER REQUIREMENTS

Pin 1	110 Volts AC
Pin 2	Frame ground
Pin 3	110 Volt return

JUMPER SET-UP FØR PERSCI 270

ØN THE BØARD, THE CØNNECTØR PINS ARE NUMBER ALTERNATLY FRØM 1 TØ 50, FRØM LEFT TØ RIGHT, AND ALL THE ØDD ØNES ARE GRØUNDED. THUS, FRØM LEFT TØ RIGHT, THE J1 AND J2 CØNNECTØR PADS ARE NUMBERED 2,4,6...50.

FØLLØWING ARE THE JUMPERS TØ INSTALL:

PAD	NAME	CØNN. TØ	NAME
E19	HLD0*	J1-18	DRIVE SELECT 2 LEFT
E20	HLD1*	J1-4	DRIVE SELECT 2 RIGHT
R3	INDX0*	J1-20	INDEX 0
R4	INDX1*	J1-8	INDEX 1
R1	RDY0*	J1-22	READY 0
R2	RDY1*	J1-6	READY 1
E23	DS0*	J1-28	DRIVE SELECT 1 RIGHT
E24	DS1*	J1-2	
E25	HLD3*	J1-26	DRIVE SELECT 1 LEFT
E26	RST*	J1-12	RESTØRE
E27	SCMP*	J1-10	SEEK CØMPLETE
E22	S0*	J1-34	DIRECTIØN SELECT
E21	SI*	J1-36	STEP
E15	WD*	J1-38	WRITE DATA
E16	WG*	J1-40	WRITE GATE
R7	TR00*	J1-42	TRACK ZERØ
R8	TR01*	J1-42	TRACK ZERØ (REMØVE ØR DISCØNNECT RESISTØR R8)
R5	WRPT0*	J1-44	WRITE PRØTECT 0
R6	WRPT1*	J1-30	WRITE PRØTECT 1
R11	RDAT0*	J1-46	READ DATA
R12	RDAT1*	J1-46	READ DATA (REMØVE ØR DICØNNECT RESISTØR R12)
	GND	J1-24	SPINDLE MØTØR ENABLE

E1	E13	MAKE DIRECTIØN SELECT = 1771 DIRC
E3	E11	PULL-UP FØR U61 PIN 12
E5	E10	PULL-UP FØR U61 PIN 10
E7	E8	MAKE PERSCI STEP = 1771 STEP STRETCHED
E29	E31	USE ØN-BØARD MULTIPLEXER FØR 2 DRIVES
E33	E34	USE BIT 3 ØF LATCH FØR PERSCI RESTØRE LINE
E39	E40	PULL UP FØR U42 PIN 10
E41	E40	PULL-UP E41 S0 HLD0 AND HLD1 ALTERNATE.
E52	E38	USE Q2* ØF LATCH TØ ACTIVATE DRIVE SELECT 1 LEFT
E43	E44	CØNNECT READY LINES FRØM PERSCI TØ 1771 READY
E51	E53	CØNNECT DRIVERS TØ HEAD-LØAD LINE.
E54	E55	USE DSØ ON BIT 2 OF LATCH.

THE PØWER SUPPLY CØNNECTIØNS ARE AS FØLLØWS:

PIN NØ.	SIGNAL	NØTES
1	CHASSIS GND	SHØULD BE HØØKED TØ HØUSE GRØUND (3RD PRØNG)
2	+5V DC	CØNNECT TØ +5 VØLTS ØN CP206 PØWER SUPPLY
3	+5V UNREG	CØNNECT TØ SMALL 5 VØLT SUPPLY
4	KEY	PLUGGED UP TØ MAKE SURE CØNNECTØR IN RIGHT
5	+24V DC	CØNNECT TØ +24 VØLTS ØN CP206 PØWER SUPPLY
6	GND	CØNNECT TØ ØTHER GRØUNDS INCLUDING CHASSIS GND
7	GND	SAME
8	GND	SAME
9	GND	SAME
10	-5V DC	CØNNECT TØ -5 VØLTS ØN CP206 PØWER SUPPLY

WHEN INSTALLING THE PØWER CABLE, USE FAIRLY HEAVY WIRE, AND TWIST EACH PØWER LINE WITH A GRØUND LINE. BEFØRE PLUGGING INTØ THE DRIVE, CHECK THE VØLTAGES ØN EACH PIN ØF THE CØNNECTØR WITH A VØLTMETER.

WHEN INSTALLING THE 50-PIN CABLE, MAKE SURE THAT PIN 1 ØN THE INTERFACE END MATCHES UP WITH PIN 1 ØN THE PERSCI END. NUMBERS ARE MARKED ØN EACH ØF THE BØARDS.

ADDITIØNAL PERSCI 277/270 NØTES

CØNVERSIØN ØF PER SCI 277 TØ 270 CØNFIGURATIØN

THE PER SCI 277 DRIVE SELECT LINES ARE THE SAME AS THE HEAD-LØAD LINES. A DISK HAS TØ BE SELECTED, HØWEVER, TØ RECEIVE A READY SIGNAL FRØM IT. THUS, A HEAD HAS TØ BE LØADED BEFØRE IT IS PØSSIBLE TØ DETERMINE WHETHER A DISK IS READY. WE FEEL THAT THE 270 CØNFIGURATIØN IS BETTER, WHICH SEPERATES THE SELECT AND HEAD LØAD FUNCTIØNS. FØLLØWING IS THE CHANGES TØ MAKE ØN A MØDEL 277 DRIVE TØ CHANGE IT TØ THE 270:

REMØVE THESE JUMPERS:

J-Z
K-L
N-P
S-T
U-V
AP-AR

ADD THE FØLLØWING JUMPERS:

D-E
F-G
H-J
M-P
R-S

ALSØ ADD A .1 MFD CAPACITØR AT C36.

USE ØF PERSCI WITH CP/M SØFTWARE

THE STANDARD VERSIØN ØF CP/M WHICH TARBELL ELECTRØNICS DISTRIBUTES HAS AN I/Ø SECTIØN (CBIØS) WRITTEN BY TARBELL ELECTRØNICS FØR ØUR INTERFACE. THIS VERSIØN ASSUMES THAT THE DRIVES HAVE SEPERATE STEPPER MØTØRS. THIS MØDULE MUST BE MØDIFIED FØR A DUAL-DRIVE SUCH AS THE PERSCI 270, WHERE THE HEADS MØVE TØGETHER. THERE ARE TWØ DAD D INSTRUCTIØNS (19 HEX) IN THE RØUTINE CALLED SELDSK. THESE TWØ INSTRUCTIØNS SHØULD BE REPLACED WITH A NØP (00 HEX) FØR EACH.

THE PRESENT VERSIØN ØF CBIØS SUPPØRTS ØNLY THE 10 MS STEP RATE. FASTER VERSIØNS WILL BE AVAILABLE AT A LATER DATE.

JUMPER SET-UP FOR SHUGART SA800

( ) Make a one-one connection from the 50-pin connector on the left hand side of the PC board, through the 50-pin ribbon cable, to the connector for your drive(s). If you have more than one drive, they should all be connected in parallel (daisy-chain), except for the select line--set the jumpers on the drives to connect each one to a seperate select line. Remove the terminating resistors on all drives except for the last one in the chain.

See the general jumper set-up instructions for information about:

1) the special connector at the drive end
2) pin numbering at J1
3) power supply connections
4) pre-operation checks

Following are the jumpers to install for a one or two drive system:

	PAD	NAME	TO	NAME
( )	E23	DS0*	J1-18	Head load
( )	R3	INDX0	J1-20	Index
( )	R1	RDY0	J1-22	Ready
( )	E19	HLD0*	J1-26	Drive select 0
( )	E20	HLD1*	J1-28	Drive select 1
( )	E17	HLD2*	J1-30	Drive select 2
( )	E25	HLD3*	J1-32	Drive select 3
( )	E22	SO*	J1-34	Direction
( )	E21	SI*	J1-36	Step
( )	E15	WD*	J1-38	Write data
( )	E16	WG*	J1-40	Write gate
( )	R7	TR00*	J1-42	Track zero
( )	R5	WRPT0*	J1-44	Write protect
( )	R11	RDAT0*	J1-46	Raw data
( )	E1		E13	
( )	E3		E11	
( )	E5		E10	
( )	E7		E8	
( )	E29		E30	
( )	E39		E40	
( )	E28		E38	for HLD3
( )	E41		E52	for full decoder
( )	E51		E55	for head-load
( )	E43		E44	
( )	**E53**		**E40**	

DC POWER REQUIREMENTS

Pin 1	+24 volts DC
Pin 2	+24 volt return
Pin 3	-5 volt return
Pin 4	-5 volts DC
Pin 5	+5 volts DC
Pin 6	+5 volts return

AC POWER REQUIREMENTS

Pin 1	110 volts AC
Pin 2	frame ground
Pin 3	110 volts return

VISUAL INSPECTION

It is always a good idea to give the board a thorough visual inspection before using it in your system. If you haven't yet done so, now is the time to thoroughly clean the board. Scrape with a sharp point between lines and pins that are close together to remove microscopic conductive particles. The board may work fine, but if you don't clean it, it is possible for conductance of these particles to build up over a period of time. After the scraping operation, alcohol may be used to wash the solder side of the board. If the edge connector looks dirty or tarnished, a pencil eraser can be used to clean it. Look for solder bridges, components not in right, jumper wires touching, anything that looks wrong. Many times it is easy to spot something that would cost you many hours or days of work later on.

On the component side, look for loose pieces of wire, solder, and other particles. Just about anything can conduct and cause a problem sometime. If you use sockets for the other IC's, make sure that none of them have pins turned under. This is not easy to spot, and has caused considerable loss of time, money, and energy in the past. Look at each pin very closely.

On the solder side, look for joints which are not shiny. If you find any, resolder them. Wiggle jumpers on the top of the board and watch the bottom to make sure the connections are soldered solidly.

INSTALLING THE 1771

If you have a voltmeter or other measuring device, you might want to check the voltages on the 40 pin IC socket before mounting the 1771B.

TEST:	PIN 1	-5 VOLTS
	PIN 20	GROUND
	PIN 21	+5 VOLTS
	PIN 40	+12 VOLTS

Find the Pin 1 position (upper left) of the socket at U55. To reduce the probability of damage due to static discharge, touch the 1771 leads as little as possible, avoid wearing synthetic clothing, and avoid carpet that tends to build up static charge (you know--when you touch things they spark).

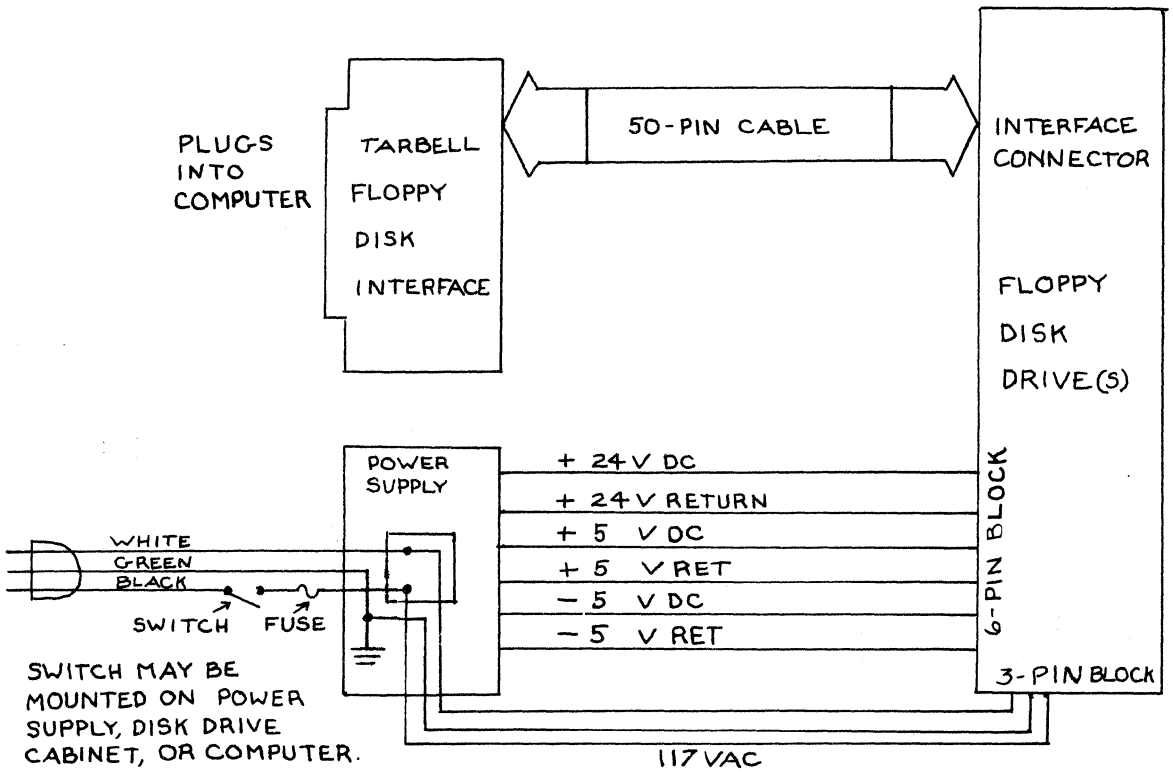
Lay the 1771 carefully on top of the socket. Check thoroughly that all pins line up with the socket holes. Apply even pressure to both ends and middle of the package, and push down until it is firmly seated.

INTERCONNECTING DRIVE, INTERFACE, AND POWER SUPPLY

Now is a good time to concern yourself with the installation and maintenance manual that hopefully came with your floppy disk drive. First check the power supply requirements and select a suitable unit (If you need help, Tarbell Electronics will be glad to select a power supply to fit your needs).

Most of the recently manufactured drives have a six pin Molex connector for the electronics board. A three pin connector is often used for the AC connections (if any). Connect this AC up first. Check carefully and make sure you're right before you plug it in.

The diagram below shows the normal hook-ups:



OPERATIONAL TESTS

CAUTION---For the following system tests set switch position 6 to on and position 7 to off.

- Do not set write inhibit switch off until you are sure you are ready to write onto the disk.

- Do not use your CP/M diskette for these preliminary tests.

System configuration:
Floppy disk interface card with drive and power supply connected; Computer mainframe; front panel; CPU; power supply; with 16K bytes minimum memory (no wait states) addressed continuously from 0000 hex to 3FFF hex.

The console input/output interface is assumed to have the characteristics defined below. If not, it will be necessary to change port numbers and status bits in this procedure to work with your set-up.

Input status	port 00	Ready=bit 0 low
Input data	port 01	
Output status	port 00	Ready=bit 7 low
Output data	port 01	

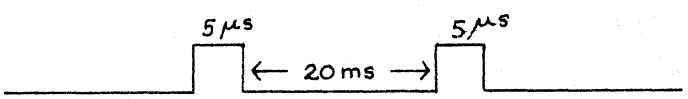
MASTER RESET TEST

( ) With all power off, move the head out about half way by turning the shaft of the stepper motor.

( ) Turn on computer power, then turn on drive power. Press system reset. The head should move to track 0 (outside) and stop.

If the stepper chatters in the home position, then the track 0 flag did not go low, or if it did, the 1771 pin 31 did not see it. If the head goes toward track 76, then reverse jumper E3 from E12 to E13.

If the head does not step at all check U55 pin 15 and U51 and associated timing components R17, C4. If you have a scope then U55 should put out a string of pulses like those shown below:



( ) Push RESET on your computer. U55 pin 19 should go low (LED out, if you use the LED probe).

STEP IN/OUT TEST

( ) Load the following program at location 0000 hex (switch position 7 should be off):

***CAUTION--Do not press run for these tests or you will run the head into the limits.

```
ADDRESS  MACHINE CODE  ASSEMBLY CODE     COMMENTS
  0000   3E 43         START MVI A,43H   Load step in
  0002   D3 F8                OUT OF8H   Issue step in
  0004   C3 00 00              JMP START  Do it again
```

( ) Single step through the above program. Immediately before the C3, the head will move out one track. Step through this about 5 times.

( ) Examine at 0001 hex. (Do not press reset) Replace the step in (43) with step out (63 hex).

( ) Examine at 0000 hex. Single step again but this time the head should step toward track 00 (outside track).

We can now do these things: reset, step in, step out. These commands (plus seek) comprise the type 1 commands, and do not require diskette or diskette loading, or door closed.

SEEK TEST

( ) Deposit following program:

```
0000  DB FF      START:  IN   SNSW    ;Read sense switches.
0002  D3 FB              OUT  DDATA   ;Track # to data reg.
0004  3E 13              MVI  A,13H   ;Load seek command.
0006  D3 F8              OUT  DCOM    ;Issue seek command.
0008  C3 00 00           JMP  START   ;Do it again.
```

( ) Turn drive power on, mount disk, close door.
( ) Examine at zero. Again, do not press RESET button as this would run the boot.
( ) Set sense switches to 05 hex and single step through the program. The drive should go to track 5--of course you can't tell exactly which track it's going to, but keeping in mind that the tracks are numbered from 0 (outside) to 76 (inside), you should be able to tell if there is a drastic difference from what it should be.
( ) You can put the run switch on now, and enter various combinations, but don't enter a combination into the sense switches any higher than 3F hex.

This concludes testing of the type 1 commands.

TYPE 2 COMMANDS

These commands are read a sector and write a sector. But before we read or write, we need to know if we can load the head.

( ) Put this program into memory at the addresses shown :

```
0000 3E 8C      START:  MVI A,8CH    ;Load read command.
0002 D3 F8              OUT DCOM     ;Issue read command.
0004 C3 00 00           JMP START    ;Do it again.
```

For these commands we need the ready line low from the drive. Ready is defined within the drive, usually as all these conditions : a diskette is mounted, the door is closed, the disk is up to speed.

( ) With the disk running and loaded, single step the program above. After the second instruction, the head should load. When the head loads it will be only for a very short time--if the read request is not re-issued after two revolutions of the disk, it will unload. You can tell when the head loads, because there will be a definite click. If your drive is open, you may also see the solenoid activate.

READ A SECTOR

This routine is a modified version of the boot program.

( ) Address a RAM board at the location called RAMADDR in the program and load the following program at location 00:

```
00FC =          WAIT    EQU 0FCH
00F8 =          DCOM    EQU 0F8H
00FB =          DDATA   EQU 0FBH
00F8 =          STAT    EQU 0F8H
00FA =          SECT    EQU 0FAH
C000 =          RAMADD  EQU 0C000H ;CAN BE ANY RAM ADDRESS
                ;
0000 DBFC       BEGIN   IN WAIT      ;WAIT FOR HOME
0002 2100C0             LXI H,RAMADD;START LOCATION IN RAM
0005 3E01               MVI A,01H    ;LOAD SECTOR NUMBER
0007 D3FA               OUT SECT     ;LOAD SECTOR REGISTER
0009 3E8C               MVI A,8CH    ;GET READ COMMAND
000B D3F8               OUT DCOM     ;ISSUE READ COMMAND
000D DBFC       RLOOP   IN WAIT      ;WAIT FOR DRQ OR INTRQ
000F B7                 ORA A        ;SET FLAGS
0010 F21A00             JP RDONE     ;DONE IF INTRQ
0013 DBFB               IN DDATA      ;READ A BYTE
0015 77                 MOV M,A      ;MOVE IT TO RAM
0016 23                 INX H        ;BUMP RAM ADDRESS
0017 C30D00             JMP RLOOP    ;GO BACK FOR MORE
001A DBF8       RDONE   IN STAT      ;READ STATUS WORD
001C B7                 ORA A        ;SET FLAGS
001D 322200             STA $+5      ;SAVE STAT WORD
0020 76                 HLT          ;STOP
```

( ) Clear 10 to 20 bytes at the start of RAMADD so you can check to see if any data was entered.

( ) Mount a fresh diskette and run the above program. The RAMADD and next 127 bytes should contain the data fill byte; IBM uses E5 (hex), but other manufacturers may use something different.

If the RAM did not load then examine the location of the status word (F8 hex) and check the bits against the 1771 Status Bits For Type II and III Commands (page 12 of the 1771 data sheet) to see if this explains the problem.

WRITE A SECTOR

The purpose of this routine is to write one sector and halt.

( ) Select a location in memory for RAMADD and load it with a recognizable data pattern.

( ) Load the following program at location 0:

```
00FC =          WAIT    EQU 0FCH
00F8 =          STAT    EQU 0F8H
00F8 =          DCOM    EQU 0F8H
00FB =          DDATA   EQU 0FBH
00FA =          SECT    EQU 0FAH
C000 =          RAMADD  EQU 0C000H
                ;
0000 DBFC               IN WAIT         ;WAIT FOR HOME
0002 2100C0             LXI H,RAMADD    ;SET ADDRESS POINTER
0005 3E01               MVI A,01        ;LOAD SECTOR NUMBER
0007 D3FA               OUT SECT        ;OUTPUT TO CONTROLLER
0009 3EAC               MVI A,0ACH      ;LOAD SECTOR WRITE COMMAND
000B D3F8               OUT DCOM        ;OUTPUT TO COMMAND REGISTER
000D DBFC       WLOOP   IN WAIT         ;WAIT FOR INTRQ OR DRQ
000F B7                 ORA A           ;SET FLAGS
0010 F21A00             JP DONE         ;JUMP WHEN INTRQ
0013 7E                 MOV A,M         ;LOAD DATA FROM RAM
0014 D3FB               OUT DDATA       ;WRITE ON DISK
0016 23                 INX H           ;BUMP RAM POINTER
0017 C30D00             JMP WLOOP       ;GET MORE
001A DBF8       DONE    IN STAT         ;READ STAT
001C E6FD               ANI 0FDH        ;MASK NON ERR BITS
001E 322200             STA $+4         ;SAVE STAT WORD
0021 76                 HLT
```

( ) Run the program. Clear the 128 bytes starting at RAMADD and run the read one sector program given previously. Check that the data is restored.

If the write is not successful, check the status bits against the table after writing and before reading.

THE BOOTSTRAP

HARD BØØTSTRAP PRØGRAM (ØN 82S123 PRØM)

```
ADDR MACH CØDE   LABEL   ASY LANGUAGE      CØMMENTS
0000   DB FC     BØØT:    IN    WAIT       ;WAIT FØR HØME.
0002   AF                 XRA   A          ;CØMPLETE.
0003   6F                 MØV   L,A        ;SET L=0.
0004   67                 MØV   H,A        ;H&L=0.
0005   3C                 INR   A          ;SET A=1.
0006   D3 FA              ØUT   SECT       ;SECTØR = 1.
0008   3E 8C              MVI   A,8CH      ;READ SECTØR.
000A   D3 F8              ØUT   DCØM
000C   DB FC     RLØØP:   IN    WAIT       ;WAIT FØR DRQ ØR INTRQ.
000E   B7                 ØRA   A          ;SET FLAGS.
000F   F2 19 00           JP    RDØNE      ;DØNE IF INTRQ.
0012   DB FB              IN    DDATA      ;READ A BYTE ØF DATA.
0014   77                 MØV   M,A        ;PUT INTØ MEMØRY.
0015   23                 INX   H          ;INCREMENT PØINTER.
0016   C3 0C 00           JMP   RLØØP      ;DØ IT AGAIN.
0019   DB F8     RDØNE:   IN    DSTAT      ;READ DISK STATUS.
001B   B7                 ØRA   A          ;SET FLAGS.
001C   CA 7D 00           JZ    07DH       ;IF ZERØ, GØ TØ SBØØT.
001F   76                 HLT              ;DISK ERRØR, SØ HALT.
                 WAIT:    EQU   0FCH
                 SECT:    EQU   0FAH
                 DCØM:    EQU   0F8H
                 DDATA:   EQU   0FBH
                 DSTAT:   EQU   0F8H
```

This program will be executed whenever the bootstrap enable switch (S1 position 5) is on and RESET is pushed. Its purpose is to read the first sector of track 0 into memory starting at 0000 hex, and then execute it. If an error is detected, the program puts the computer in the halt state--you may try again by pressing RESET, or stop your computer by pressing RESET and STOP at the same time. If you do not wish to use this PROM bootstrap, a similar program may be run elsewhere in memory (with addresses relocated), as long as the memory it runs in has no wait states and is above C0FF hex.

Locating a program at address 0 to read from the disk into memory at zero would normally be impossible since the programwould be overwritten by the sector loaded, thus destroying the bootstrap before it was finished. The special hardware tricks played on the board make

this possible by controlling the bus to write into main memory while reading from the PROM bootstrap.

Note that the upper five bits of I/O instructions are always high, to match the standard setting of the dip switch. If the dip switch were set for a different device address, the upper five bits on all the I/O commands would have to be adjusted accordingly, and you would have to change the 82S123 PROM.

The first instruction is "IN WAIT" (port FC). This instruction tells the interface board to force a hardware wait until either the DRQ or INTRQ outputs of the 1771 go true--these signals tell the computer (program) that the interface is ready to do something. In this case, we're waiting for INTRQ to go true, which tells us that the head is in the "home" position (track 0).

"XRA A" makes register A zero, and "MOV L,A" and "MOV H,A" make registers H and L zero. The "INR A" makes reg A=1. Now when we do the "OUT SECT", this is a type 1 command to the sector register in the 1771 (see the data sheets), and sets this register to 1 (for sector 1). With the "MVI A,8CH", we set reg A up for a read operation (type 2). Bits 7,6,5 are 100 as shown in the command summary. Bit 4 is 0 because we want a single record. Bit 3 is 1 for IBM format. Bit 2 is 1 to make the head load at the beginning of the read operation. We then do an output "OUT DCOM" to make it all happen.

The next "IN WAIT" is used to wait for each data byte, and it also retrieves the status which indicates end of operation. "ORA A" sets the flags so we can tell whether to jump out of the loop. If the most significant bit is 0, the interface is indicating that it was the INTRQ that caused the end of the wait. If 1, it was the DRQ, indicating some data is ready to process. IN DDATA" actually reads the data from the 1771 data register into the 8080 register A. "MOV M,A" of course transfers the data to memory. "INX H" increments the memory data pointer register. "JMP RLOOP" transfers control back to the beginning of the loop to do it again.

When the INTRQ goes true, indicating an end of the read operation or an error, a transfer to "RDONE" is made. There, the "IN DSTAT" reads the disk status from the 1771 status register. The meaning of each

WRITING DRIVER ROUTINES

Most driver routines will follow a similar form as the bootstrap program. The first step, then, is to familiarize yourself with that program.

Then, consult the 1771 data sheet. Note the various options, and decide what you want done--read or write, track #, etc.

Next, combine these with the sample driver routines in the next section. While the interior hardware of the interface may be complex, the software need not be at all. Make sure you load the proper registers, issue commands, and check for results.

SAMPLE DRIVER ROUTINES

The easiest way to write your driver routines at first is to splice together blocks of existing, working programs. The following routines should serve as a good starting point--but remember to make any necessary changes to correspond to your system's peculiarities.

To move head to home (track 0):

```
HØME:   MVI   A,0D0H      ;CLEAR ANY PENDING CØMMAND.
        ØUT   DCØM
HØME1:  IN    DSTAT       ;READ INTERFACE STATUS.
        RRC               ;LØØK AT LEAST SIG. BIT.
        JC    HØME1       ;WAIT FØR NØT BUSY.
        MVI   A,3         ;GET BITS FØR HØME CØMMAND.
        ØUT   DCØM        ;ISSUE HØME CØMMAND.
        IN    WAIT        ;WAIT FØR INTRQ (END ØF ØP.).
        ØRA   A           ;SET FLAGS.
        MVI   A,1         ;SET UP ERRØR INDICATØR.
        JM    ERRØR       ;ERRØR IF DRQ INSTEAD ØF INTRQ.
        IN    DSTAT       ;READ DISK INTERFACE STATUS.
        MØV   E,A         ;SAVE IN REGISTER E.
        ANI   4           ;LØØK AT BIT 2.
        JZ    HERR        ;ERRØR IF NØT AT TRACK 0.
        MØV   A,E         ;GET STATUS BACK.
        ANI   91H         ;MASK NØN-ERRØR BITS.
        RET               ;RETURN IF NØ ERRØR.
HERR:   MVI   A,1         ;SET HARDWARE ERRØR.
        ØRA   A           ;SET FLAGS.
        RET               ;RETURN FRØM HØME RØUTINE.
```

To select one disk out of four:

```
SELECT: MØV   A,C        ;GET DISK NUMBER FRØM REGISTER C.
        ANI   3          ;LØØK ØNLY AT 2 LEAST SIG. BITS.
        RAL              ;MØVE INTØ BITS 4&5.
        RAL
        RAL
        RAL
        ØRI   2          ;GET CØDE TØ SET LATCH.
        ØUT   DEXT       ;SEND TØ EXTENDED CØMMAND PØRT.

        ØUT   DDATA      ;WRITE CØNTENTS ØF REG A ØNTØ DISK.

        IN    DDATA      ;READ A BYTE FRØM DISK INTØ REGISTER A.
```

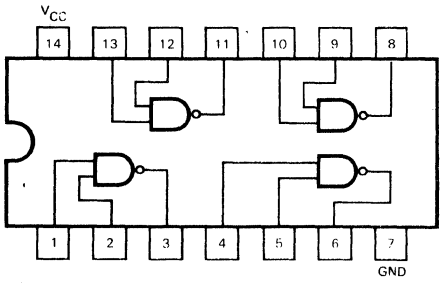
CMA

```
DCØM:   EQU   ØF8H       ;DISK 1771 CØMMAND PØRT.
DSTAT:  EQU   ØF8H       ;DISK 1771 STATUS PØRT.
TRACK:  EQU   ØF9H       ;DISK 1771 TRACK PØRT.
SECTP:  EQU   ØFAH       ;DISK 1771 SECTØR PØRT.
DDATA:  EQU   ØFBH       ;DISK 1771 DATA PØRT.
WAIT:   EQU   ØFCH       ;DISK WAIT CØMMAND.
DEXT:   EQU   ØFCH       ;DISK EXTENDED CØMMAND PØRT.
```

READ A SECTOR, WRITE A SECTOR

Full listings for these progams are given under the Operational Tests Section. Also, see the 1771 manual for the various format and control options for these operations.

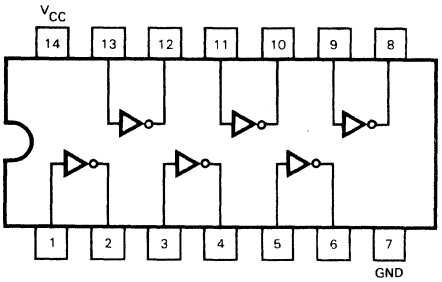
QUAD 2-INPUT NAND GATE



74LS00)

INPUTS			OUT
1	2		3
0	0		1
0	1		1
1	0		1
1	1		0

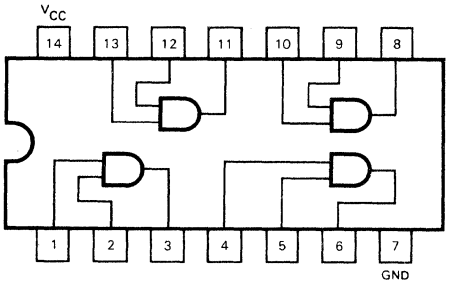
HEX INVERTER



9LS04 (54LS/74LS04)

IN		OUT
1		2
0		1
1		0

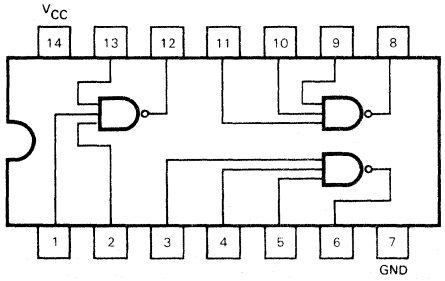
QUAD 2-INPUT AND GATE



9LS08 (54LS/74LS08)

INPUTS			OUT
1	2		3
0	0		0
0	1		0
1	0		0
1	1		1

TRIPLE 3-INPUT NAND GATE



9LS10 (54LS/74LS10)

INPUTS				OUT
3	4	5		6
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		0

7438 quad 2-input NAND buffer (open collector)

general description

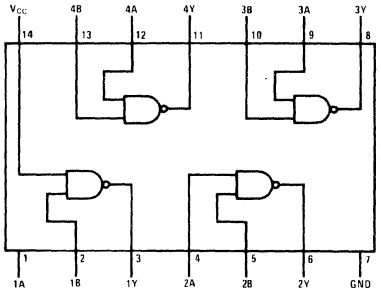
These are quad two-input NAND buffers. The DM5437/DM7437 has a normal TTL "Darlington" output configuration whereas the DM5438/DM7438 has an open-collector. Aside from the output, the circuitry is identical.

features

- Series 54/74 TTL and DTL compatible
- Input clamping diodes
- Typical noise immunity 1V
- Fan Out 30

schematic and connection diagrams

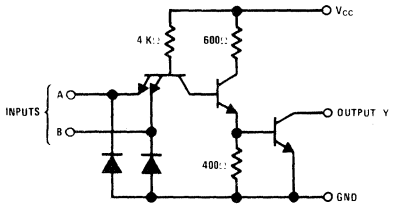
Dual-In-Line and Flat Package



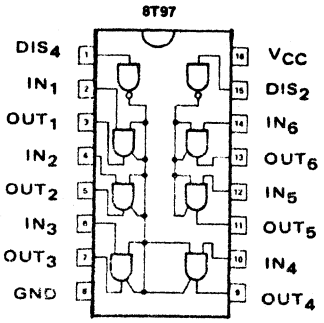
TOP VIEW †

POSITIVE LOGIC: $Y = \overline{AB}$

DM5438/DM7438



8T97 HEX TRI-STATE INVERTERS



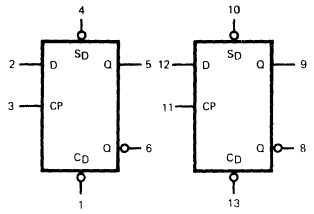
INPUTS		OUTPUT
DIS	IN	OUT
H	X	Hi-Z
L	H	H
L	L	L

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION – The 9LS74 (54LS/74LS74) dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

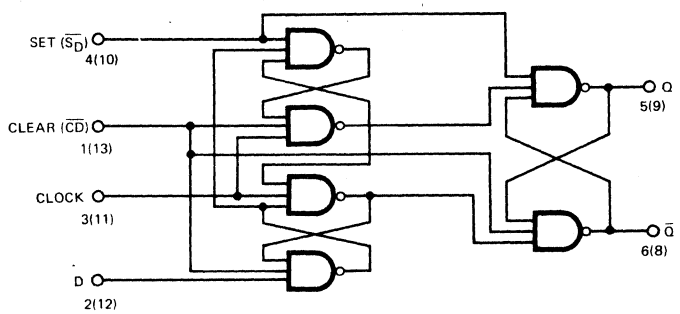
Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM (EACH FLIP-FLOP)



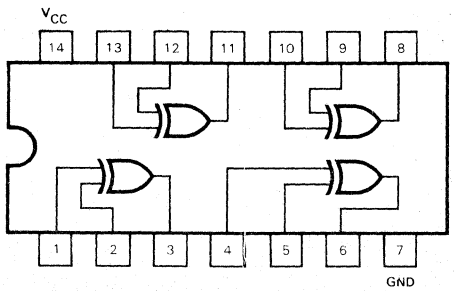
MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S_D}$	$\overline{C_D}$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S_D}$ and $\overline{C_D}$ are LOW, but the output states are unpredictable if $\overline{S_D}$ and $\overline{C_D}$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

SN74LS123
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- **Functionally and Mechanically Identical to SN54122/SN74122 and SN54123/SN74123**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Low Power Dissipation:**
  'LS122 . . . 30 mW Typical
  'LS123 . . . 60 mW Typical

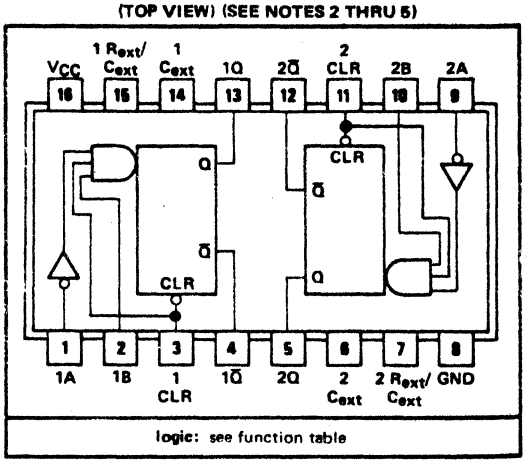
'LS123 FUNCTION TABLE (SEE NOTE 1)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

description

The 'LS122 and 'LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.

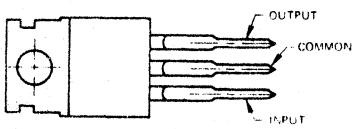
(TOP VIEW) (SEE NOTES 2 THRU 5)



logic: see function table

NOTES:
1. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).
2. To use the internal timing resistor of 'LS122, connect R_{int} to V_{CC}.
3. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
4. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
5. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

CONNECTION DIAGRAMS
TO-220 PLASTIC POWER PACKAGE
(TOP VIEW)



7805

- OUTPUT CURRENT IN EXCESS OF 1 AMP
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION
- AVAILABLE IN THE PLASTIC TO-220 AND THE METAL TO-3 PACKAGE

ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit) TO-3 Package	300°C
(Soldering, 10 second time limit) TO-220 Package	230°C

74LS138

FUNCTIONAL DESCRIPTION – The 9LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The 9LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 9LS138s and one inverter. (See Figure a.)

The 9LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

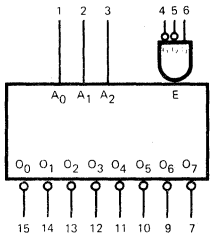
TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

DESCRIPTION – The LSTTL/MSI 9LS138 (54LS/74LS138) is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 9LS138 devices or to a 1-of-32 decoder using four 9LS138s and one inverter. The 9LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **TYPICAL POWER DISSIPATION OF 32 mW**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



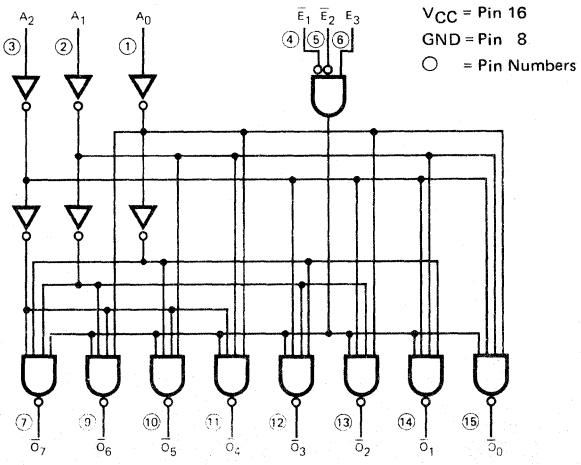
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1$, $\overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

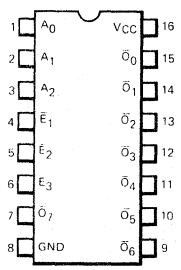
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

74LS175

QUAD D FLIP-FLOP

DESCRIPTION — The LSTTL/MSI 9LS175 (54LS/74LS175) is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The 9LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

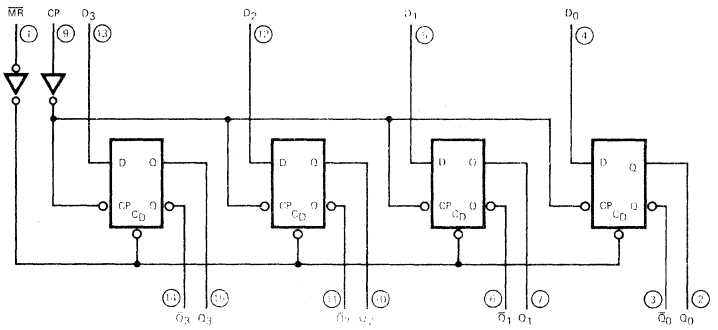
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 14 ns**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

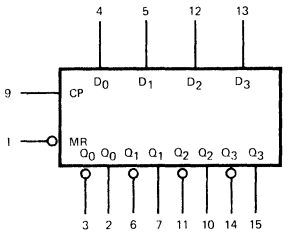
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC DIAGRAM



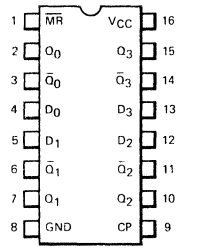
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DM8131 6-bit unified bus comparator

general description

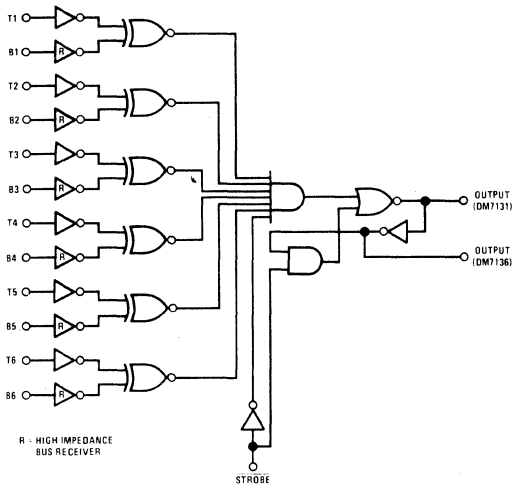
The DM7131/DM8131, DM7136/DM8136 compare two binary words of two-to-six-bits in length and indicates matching bit-for-bit of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high impedance receivers driven by a terminated data bus. These bus inputs include 1V typical hysteresis which provides 1.8V noise immunity. The DM7131/DM8131 has active pull up output and goes to the low state upon comparison. The DM7136/DM8136 has open-collector output which goes to high state upon comparison and is expandable to n bits by collector-ORing. Both devices have an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level without affecting the state of output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

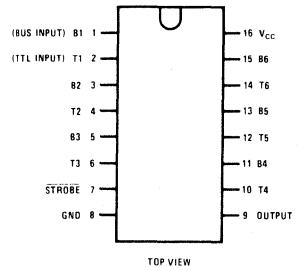
features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.8V typ
- High fan out
- Input clamping diodes
- Output compatible with TTL circuits
- Output latch provision

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

82S123 256-BIT BIPOLAR TRI-STATE PROGRAMMABLE ROM

DESCRIPTION

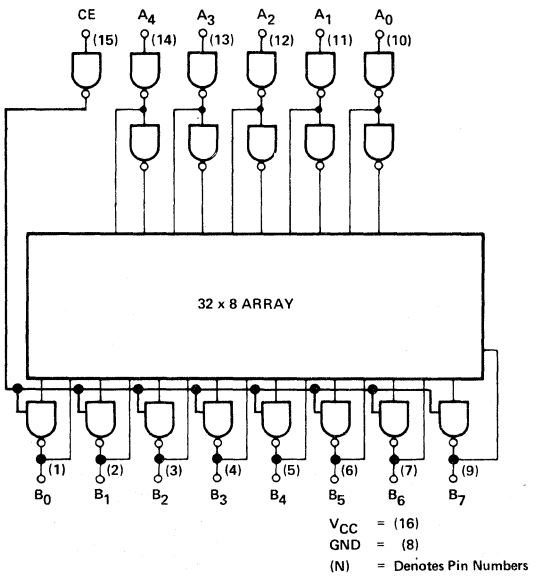
The 82S23 (open Collector Outputs) and the 82S123 (Tristate Outputs) are Bipolar 256 Bit Read Only Memories organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. A chip enable line is provided and the outputs are bare collector or Tristate to allow for memory expansion capability.

The 82S23 and 82S123 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35 nS.

FEATURES

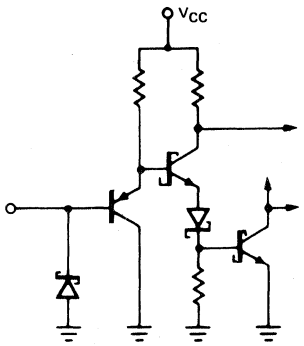
- PNP INPUTS
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- A CHIP ENABLE LINE
- OPEN COLLECTOR OR TRISTATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- BOARD PROGRAMMABLE

LOGIC DIAGRAM

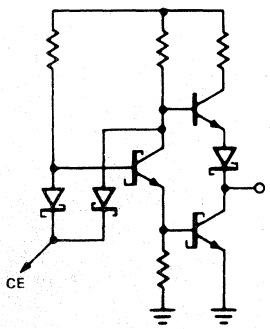


INPUT/OUTPUT SCHEMATIC DIAGRAMS

INPUT SCHEMATIC



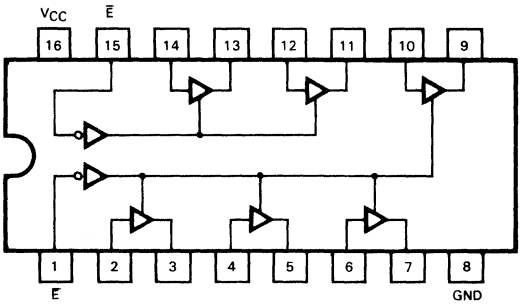
OUTPUT SCHEMATIC



82S123

74LS367

HEX 3-STATE BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS

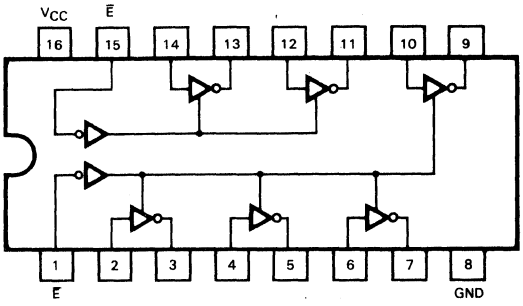


TRUTH TABLE

INPUTS		OUTPUT
Ē	D	
L	L	L
L	H	H
H	X	(Z)

74LS368

HEX 3-STATE INVERTER BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

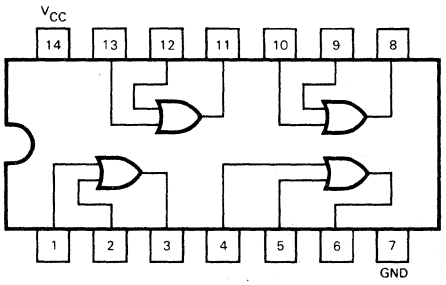
INPUTS		OUTPUT
Ē	D	
L	L	H
L	H	L
H	X	(Z)

DESCRIPTION — The 9LS365/366/367/368 are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

When the Output Enable Input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

74LS32

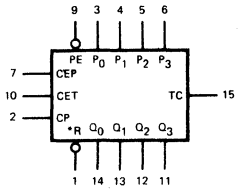
QUAD 2-INPUT OR GATE



INPUTS		OUT
1	2	3
0	0	0
0	1	1
1	0	1
1	1	1

74LS161

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

DESCRIPTION – The 9LS160/161/162/163 are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The 9LS160 and 9LS162 count modulo 10 (BCD). The 9LS161 and 9LS163 count modulo 16 (binary.)

The 9LS160 and 9LS161 have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The 9LS162 and 9LS163 have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	9LS160	9LS161
Synchronous Reset	9LS162	9LS163

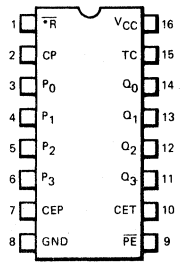
- **SYNCHRONOUS COUNTING AND LOADING**
- **TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION**
- **TERMINAL COUNT FULLY DECODED**
- **EDGE-TRIGGERED OPERATION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.6 U.L.	0.3 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.6 U.L.	0.3 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.6 U.L.	0.3 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

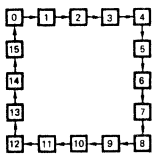
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commerical (XC) Temperature Ranges.

CONNECTION DIAGRAMS
DIP (TOP VIEW)



STATE DIAGRAM

9LS161 • 9LS163



LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for 9LS160 & 9LS162 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for 9LS161 & 9LS163 = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP+ (rising clock edge)
Reset = $\overline{MR}$ (9LS160 & 9LS161)
Reset = $\overline{SR}$ • CP+ (rising clock edge)
(9LS162 & 9LS163)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

WESTERN DIGITAL
MOS/LSI

FD1771 A/B - 01

DATA SHEET

FLOPPY DISK FORMATTER/CONTROLLER

MAR 77

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accomodates the interface signals from most drive manufactures. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

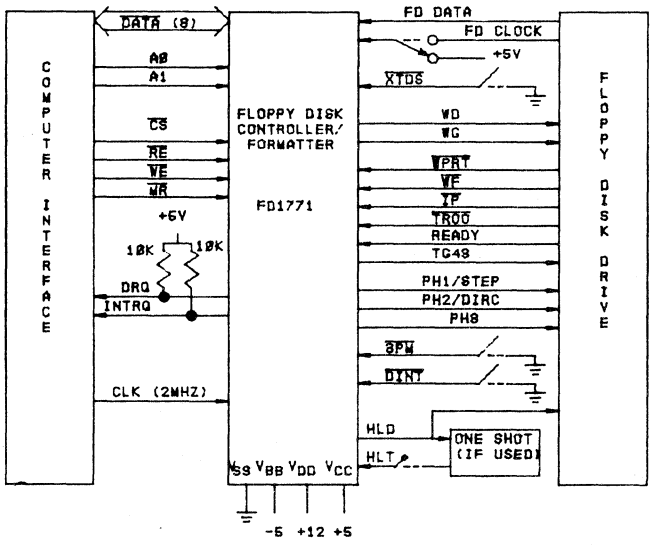
The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS

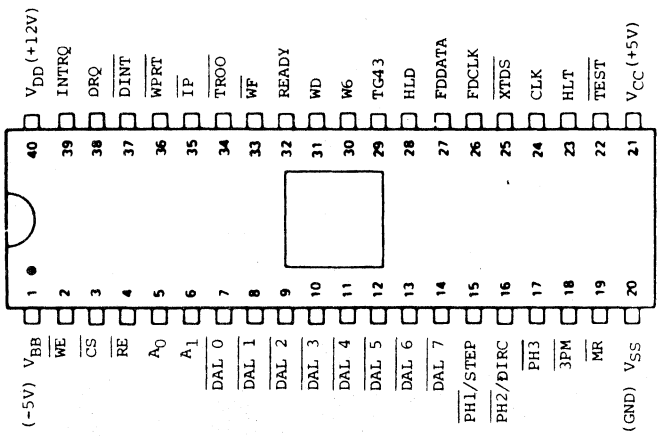
- o FLOPPY DISK DRIVE INTERFACE
- o SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- o NEW MINI-FLOPPY CONTROLLER

FEATURES

- o SOFT SECTOR FORMAT COMPATIBILITY
- o AUTOMATIC TRACK SEEK WITH VERIFICATION
- o READ MODE
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- o WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- o PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- o SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

WESTERN DIGITAL CORPORATION

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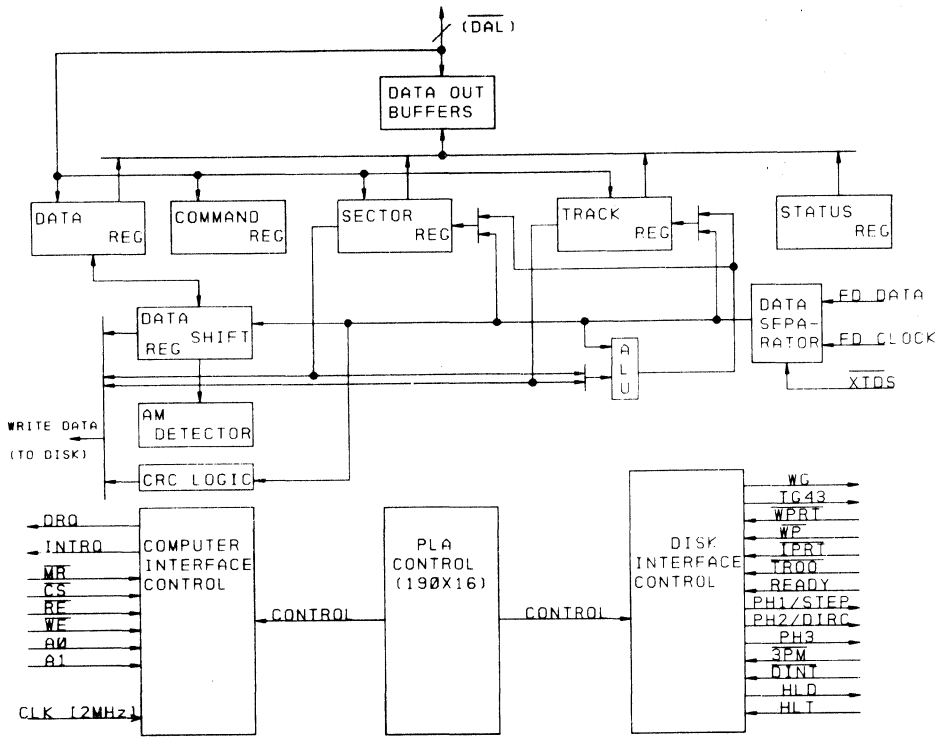

FD1771 BLOCK DIAGRAM
FIG 3

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on Page 2. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

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The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector - The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control - All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and AO, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-AØ	READ (RE)	WRITE (WE)
Ø Ø	Status Register	Command Register
Ø 1	Track Register	Track Register
1 Ø	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing, (may be 1.0 MHz for mini floppy.)

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and O of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three Phase Motor or a Step-Direction Motor through the device interface. When the 3PM input is connected to ground the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2 and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input 3PM open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds width. The Phase 2 pin PH2 becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 us prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track

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Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

TABLE 1
STEPPING RATES

r1	r0	1771-01 CLK=2MHZ TEST=1	1771-01 CLK=1MHZ TEST=1	1771 or-01 CLK=2MHZ TEST=0	1771 or-01 CLK=1MHZ TEST=0
0	0	6ms	12ms	*APPROX. 400us	*APPROX. 800us
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is sssumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A low logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded before stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 KHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 KHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 KHz data clock. The 500 KHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator (XTDS) INPUT. When the Read Data input makes a high to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8 bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic o in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 usec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write}}$ Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminated the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

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Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in table 2.

COMMAND SUMMARY*

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2

* = Shown in true form.

FLAG SUMMARY

TYPE 1

h = Head Load Flag (Bit 3)
- h=1, Load head at beginning
- h=0, Do not load head at beginning

V = Verify flag (Bit 2)
- V=1, Verify on last track
- V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u=1, Update Track register
- u=0, No update

TABLE 3

TYPE II

m = Multiple Record flag (Bit 4)
- m =0, Single Record
- m =1, Multiple Records

b = Block length flag (Bit 3)
- b =1, IBM format (128 to 1024 bytes)
- b =0, Non-IBM format (16 to 4096 bytes)

a_1a_0 =Data Address Mark (Bits 1-0)
- a_1a_0 =00, FB (Data Mark)
- a_1a_0 =01, FA (User defined)
- a_1a_0 =10, F9 (User defined)
- a_1a_0 =11, F8 (Deleted Data Mark)

TABLE 4

TYPE III

s =Synchronize flag (Bit 0)
- $\overline{s}$=0, Synchronize to AM
- $\overline{s}$=1, Do Not Synchronize to AM

TYPE IV

Ii =Interrupt Condition flags (Bits 3-0)
- I_0=1, Not Ready to Ready Transition
- I_1=1, Ready to Not Ready Transition
- I_2=1, Index Pulse
- I_3=1, Immedate interrupt

E =Enable HLD and 10 msec Delay
- E=1, Enable HLD, HLT and 10 msec Delay
- E=0, Head is assumed Engaged and there is no 10 msec Delay.

TABLE 5

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK STEP, STEP-IN, AND STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

The type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command HLD output is made active). If h = 0,HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

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During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt, (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U = 1, the track register is updated by one for each step. When U = o, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r1r0r field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

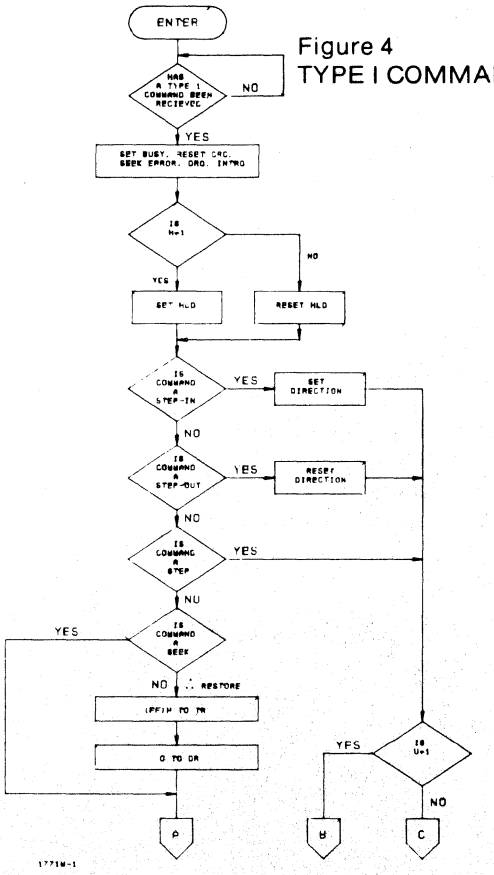

Figure 4
TYPE I COMMAND FLOW

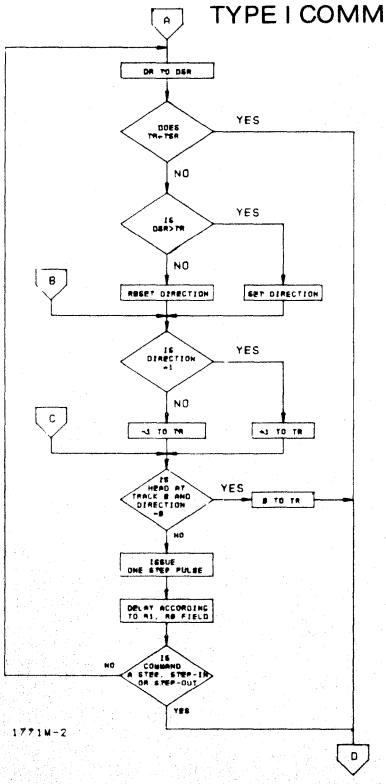

Figure 5
TYPE I COMMAND FLOW

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STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on the Track Register is incremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

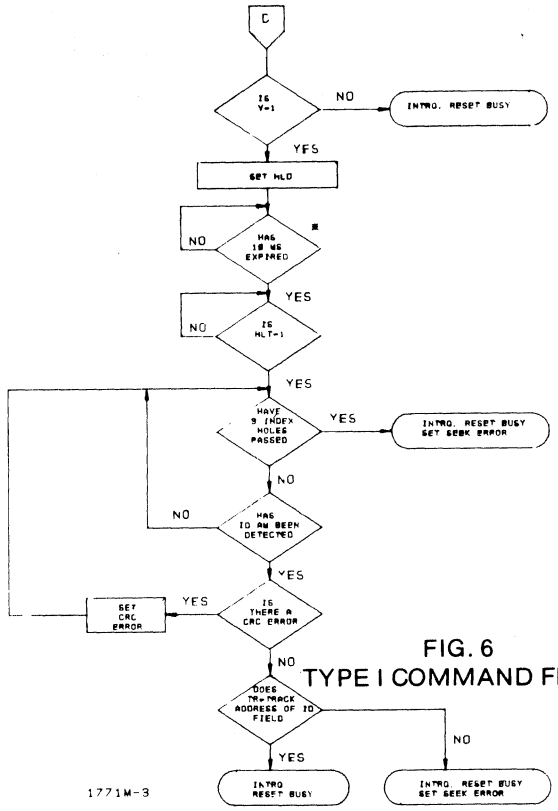

FIG. 6
TYPE I COMMAND FLOW

*NOTE: IF $\overline{TEST}$-0, THERE IS NO 10MS DELAY
IF $\overline{TEST}$-1 AND CLK=1MHZ
THIS IS A 20MS DELAY.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the type II command, the busy status Bit is set. If the E flag =1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1771 compares the Track Number of the ID field with the Track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1771 must find an Id field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark – DATA=$(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark – DATA=(F8, F9, FA, or FB), CLK = $(C7)_{16}$

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Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128 x 2^n where n - 0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

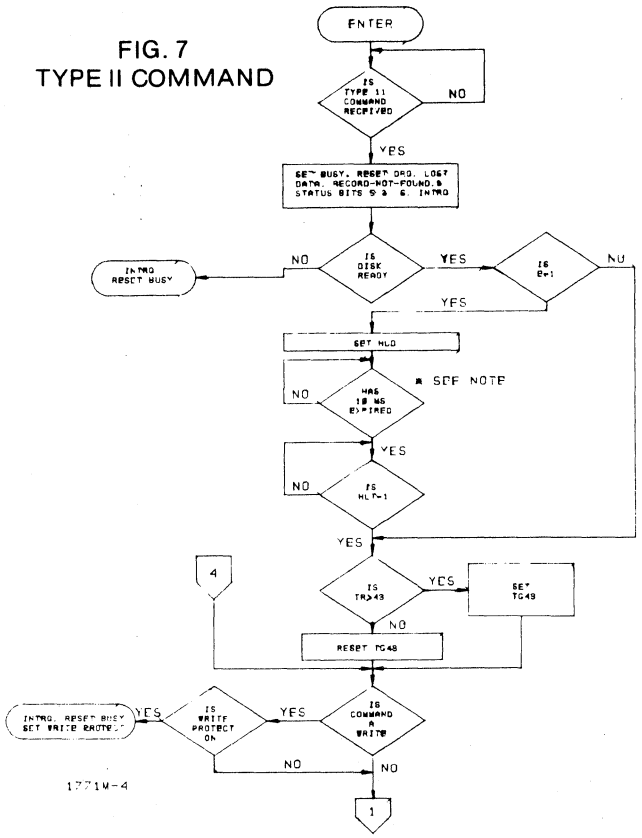
When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

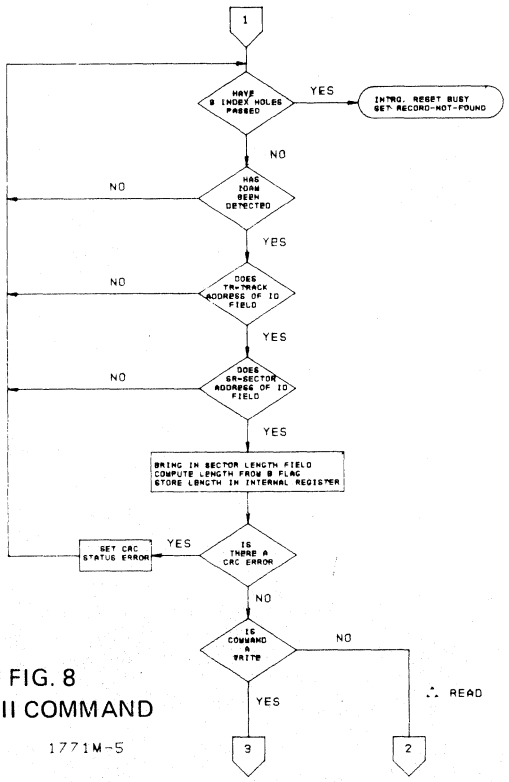
Each of the type II commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = o a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1 , multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

FIG. 7
TYPE II COMMAND



* 1. IF $\overline{TEST}$-0, THERE IS NO 10MS DELAY
2. IF $\overline{TEST}$-1 AND CLK=1MHZ, THIS IS A 20MS DELAY.

FIG. 8
TYPE II COMMAND



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READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

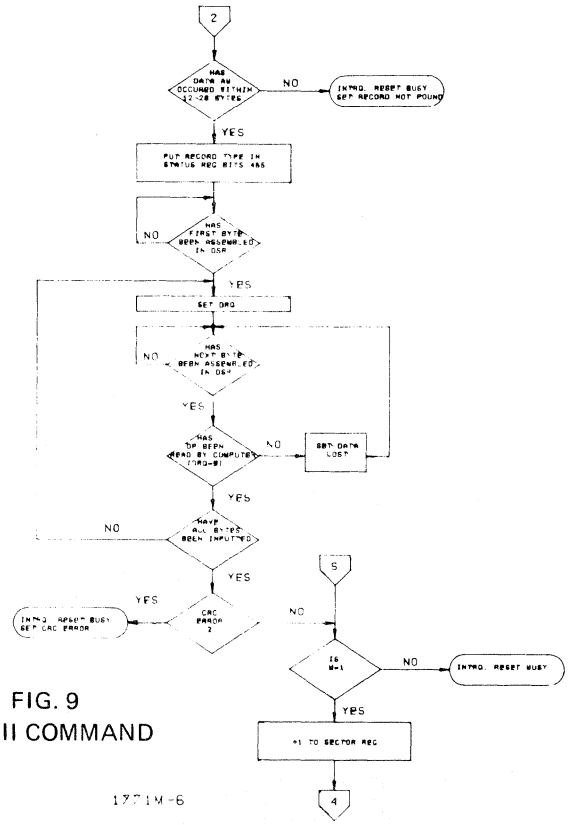

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FIG. 9
TYPE II COMMAND

WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a1	a0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The FD1771 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

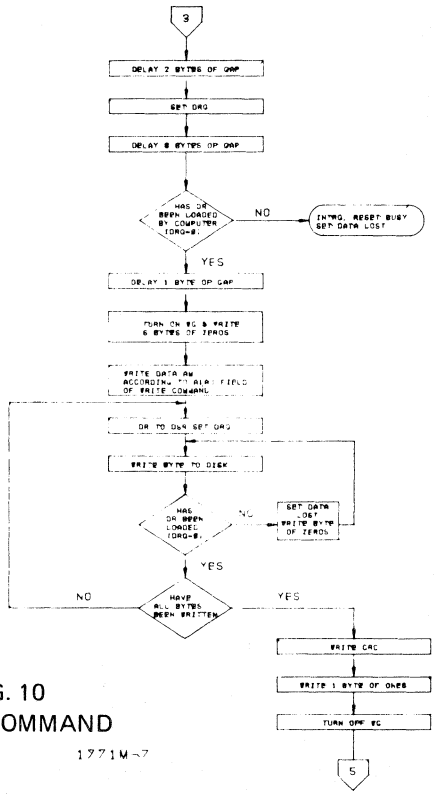

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FIG. 10
TYPE II COMMAND

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TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the BUSY Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit O (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon recieving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR When needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command will not execute if the $\overline{\text{DINT}}$ input is grounded; instead if the Write Protect Status bit is set and the interrupt is activated. Note that one F7 pattern generates 2 CRC characters.

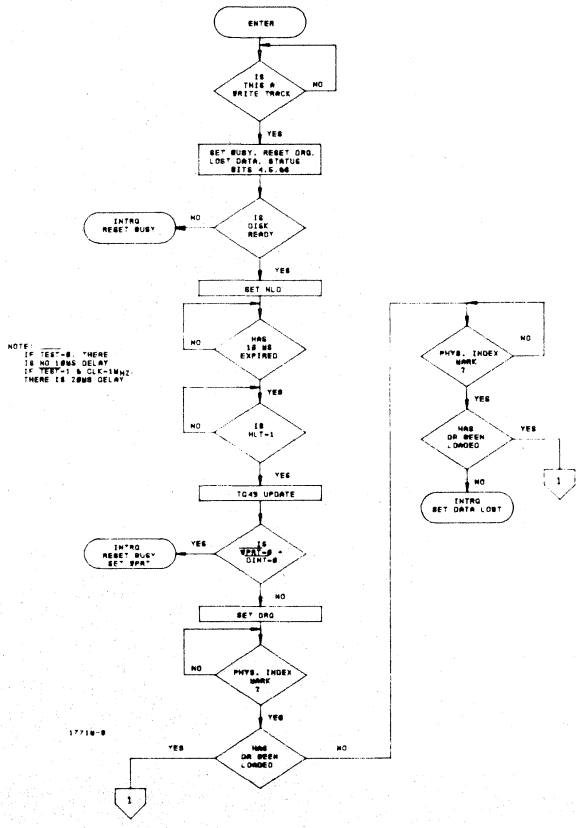

FIG. 11
TYPE III COMMAND
WRITE TRACK

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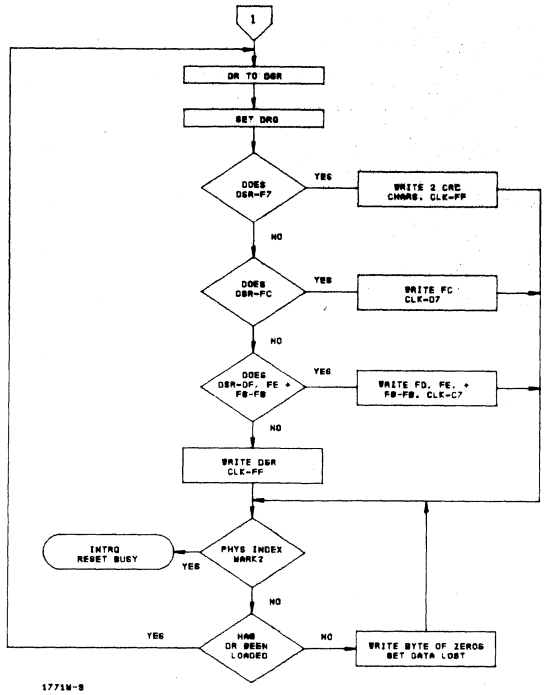

FIG. 12
TYPE III COMMAND
WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0I_3=0,, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the BUSY Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, theBUSY Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 6

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STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: In indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

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FORMATTING THE DISK
(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/0 or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD 1771 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru Fe must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS - 128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	00 or FF
	6	00
	1	FC (Index Mark)
	26	00 or FF
*	6	00
*	1	FE (ID Address Mark)
*	1	Track Number (0 thru 4C)
*	1	00
*	1	Sector Number (1 thru 1A)
*	1	00
*	1	F7 (2 CRC's written)
*	11	00 or FF
*	6	00
*	1	FB (Data Address Mark
*	128	Data (IBM uses E5)
*	1	F7 (2 CRC's written)
*	27	00 or FF
	247**	00 or FF

* Write bracketed field 26 times
** Continue writing until FD1771 interrupts out. Approx. 247 bytes.

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NON-IBM FORMATS

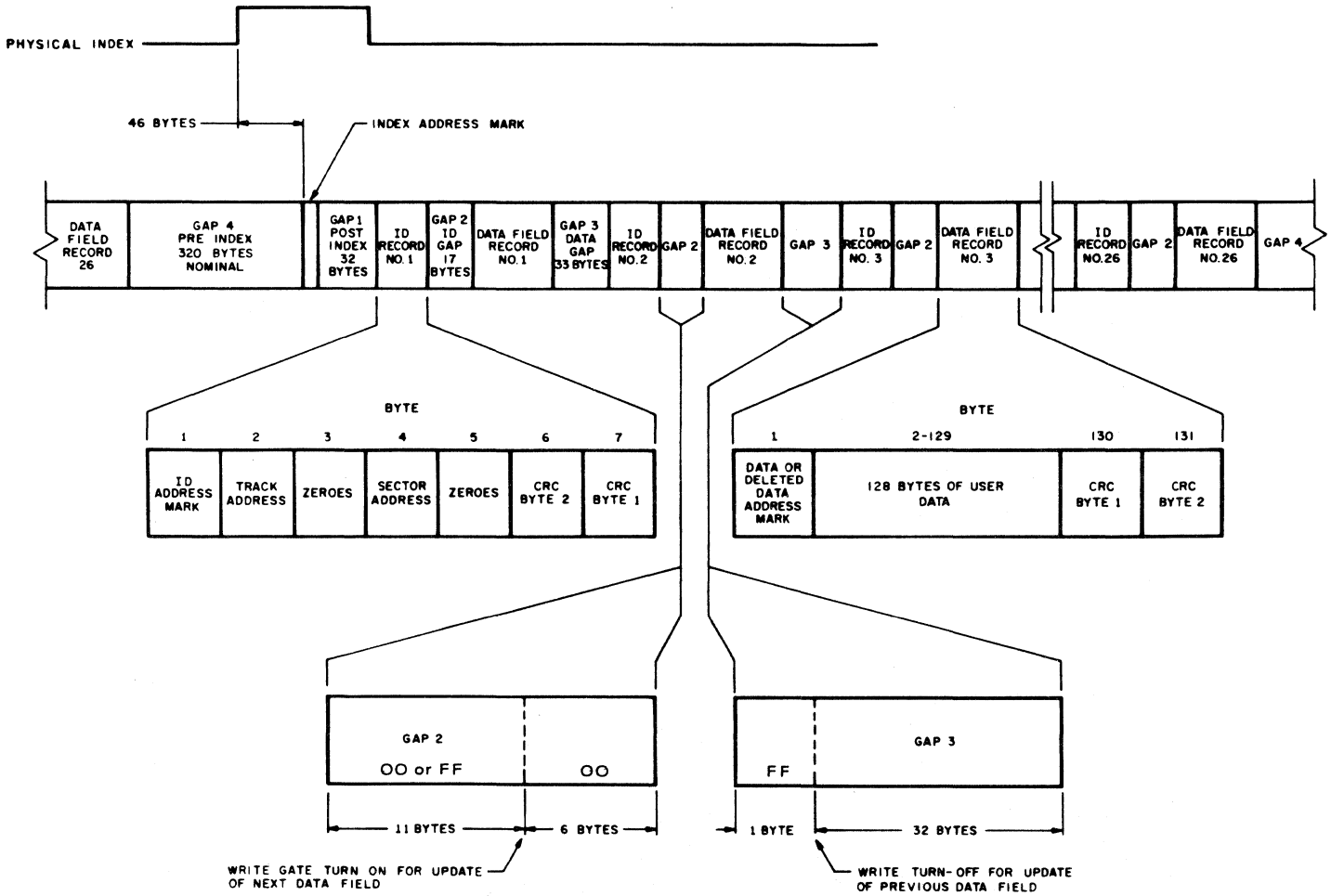
Non IBM Formats are very similar to the IBM formats except a different algorithum is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to section V, Type II commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

1) IBM Diskette OEM Information GA21-9190-1
2) SA900 IBM Compatibility Reference Manual - Shugart Associates.

FIG.13
TRACK FORMAT



ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+20 to −0.3V
Max Voltage to Any Input With Respect to V_{BB}	+20 to −0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +125°C

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OPERATING CHARACTERISTICS (DC)

T_A = ØºC to 7ØºC, V_{DD} = +12.ØV ± .6V, V_{BB} = –5.Ø ± .5V, V_{SS}= ØV, V_{CC} = +5V ± .25V
V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal, V_{BB} = 0.4 ua Nominal

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leagage			10	uA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	uA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = –100 uA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA

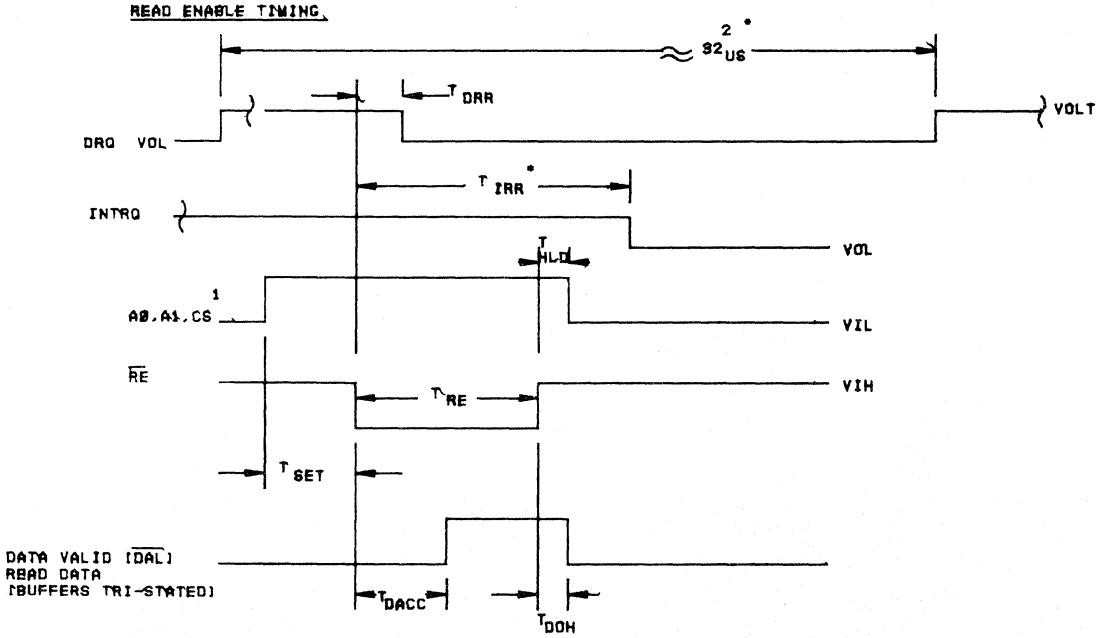
NOTE: Vol ≤.4V when interfacing with low Power Schottky parts (1_O<1 ma)

TIMING CHARACTERISTICS

T_A = ØºC to 70ºC, V_{DD} = +12V ± .6V, V_{BB} = –5 ± .25V, V_{SS} = ØV, V_{CC} = +5 ± .25V
NOTE: Timings are given for 2 MHZ Clock. For those timings noted, values will double when chip is operated at 1 MHZ. Use 1 MHZ when using mini-floppy.

Read Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			150	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	C_L= 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED. * *
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12 TO 32 USEC WHEN S=Ø.

* TIME DOUBLES WHEN CLK=1 MHZ

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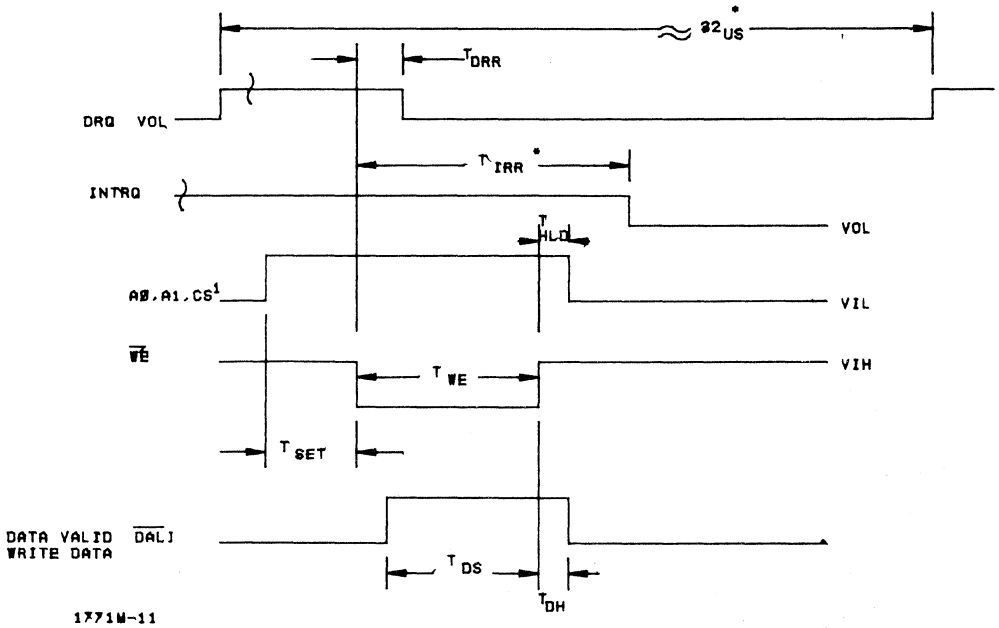
Write Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			150	nsec	See Note
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

WRITE ENABLE TIMING



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NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGESTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8_{USEC} AFTER THE RISING EDGE OF $\overline{WE}$ WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12_{USEC} LATER. THESE TIMES ARE DOUBLED WHEN CLK=$1M_{HZ}$.

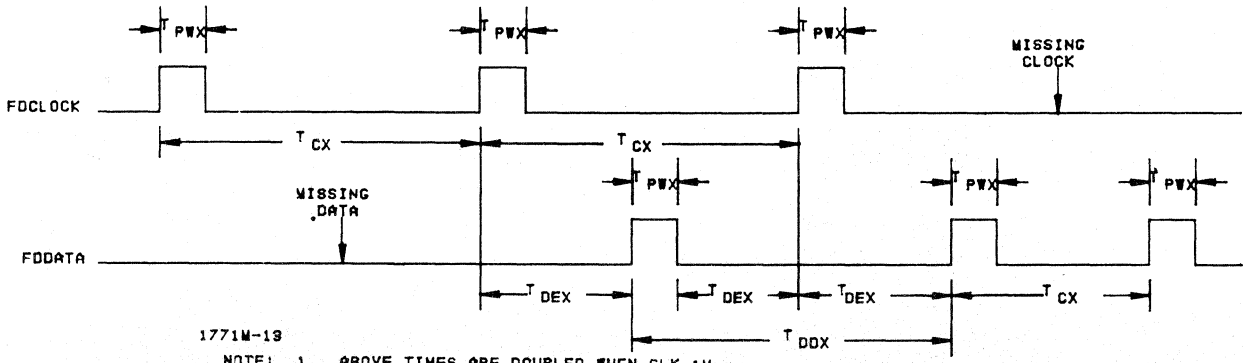
* = Time doubles when CLK = 1 MHZ

External Data Separation ($\overline{XTDS}$ = 0)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWX	Pulse Width Rd Data & Rd Clock	150		350	nsec	
TCX	Clock Cycle Ext	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	

READ TIMING

$\overline{XTDS}$-0
EXTERNAL DATA SEPERATION



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NOTE: 1. ABOVE TIMES ARE DOUBLED WHEN CLK=$1M_{HZ}$.
2. CONTACT WDC FOR EXTERNAL CLOCK/DATA SEPERATOR CIRCUITS.

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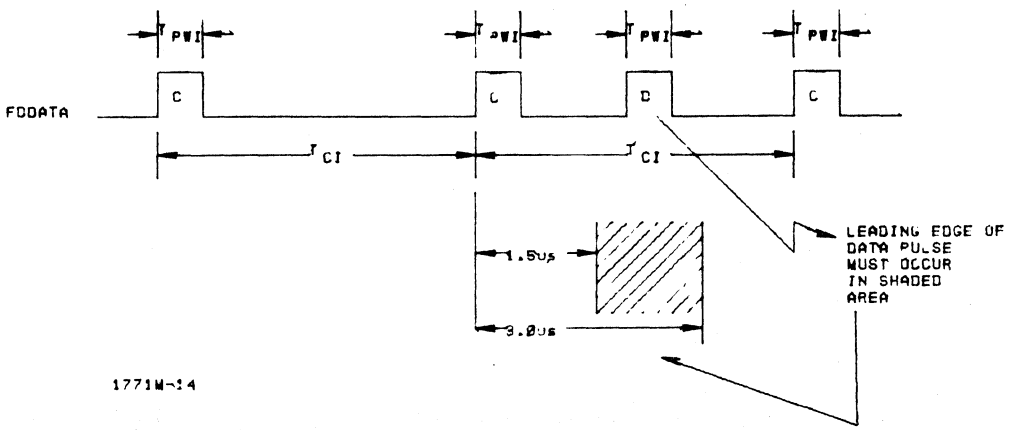
Internal Data Separation (XTDS = 1)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWI	Pulse Width Data & Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

READ TIMING
XTDS=1
INTERNAL DATA SEPERATION
RDCLOCK MUST BE TIED HIGH

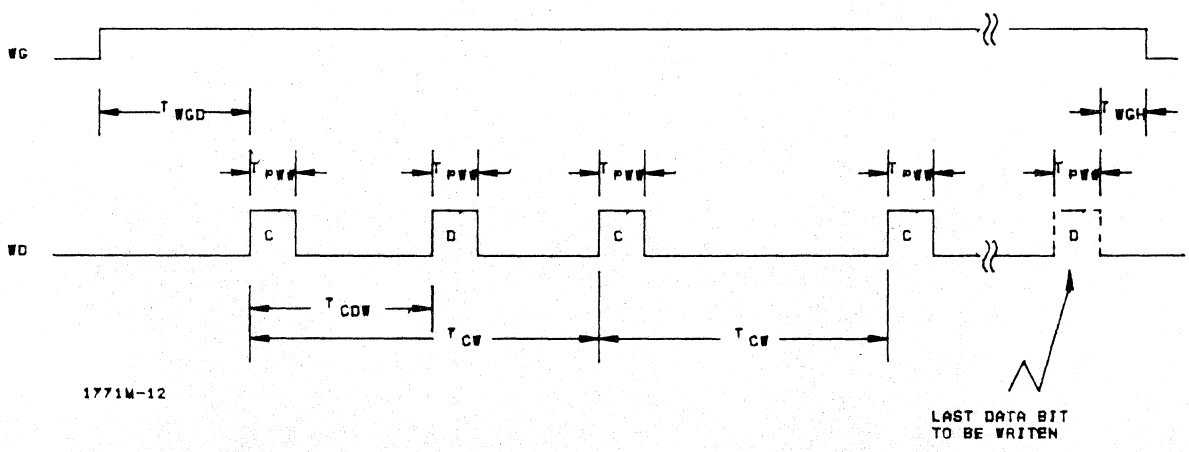


NOTE: INTERNAL DATA SEPERATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, WDC RECOMMENDS EXTERNAL DATA SEPERATION BE USED.

Write Data Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	±0.5%± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	±0.5%± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

WRITE DATA TIMING



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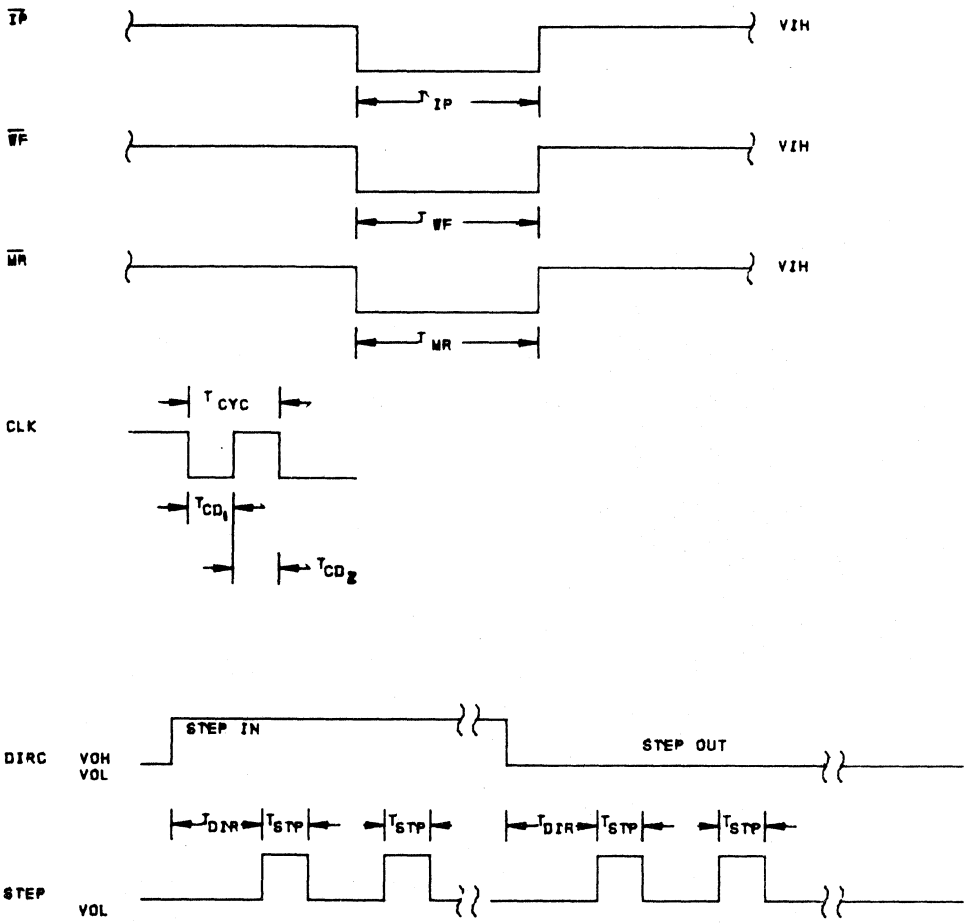
Miscellaneous Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2MHZ ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	These times doubled when CLK = 1 MHZ
TDIR	Dir Setup to Step	24			usec	
TMR	Master Reset Pulse Width	10			usec	
TIP	Index Pulse Width	10			usec	
TWF	Write Fault Pulse Width	10			usec	

MISCELLANEOUS TIMING



PIN OUTS

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	Power Supplies	V_{BB}	−5V
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	• A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.

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PIN NO	PIN NAME	SYMBOL	FUNCTION
Computer Interface:			
7-14	DATA ACCESS LINES	$\overline{DAL}$Ø-$\overline{DAL}$7	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0, A1	•These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	•A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	•A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	•This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	•This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	•This input requires a free-running 2 MHz + 1% square wave clock for internal timing reference.
Floppy Disk Interface:			
25	EXTERNAL DATA SEPERATION	XTDS	•A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	•This input receives the externally separated clock when XTDS = 0. If XTDS = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	•This input receives the raw read disk data if XTDS = 1, or the externally separated data if XTDS = 0.
31	WRITE DATA	WD	•This output contains both clock and data bits of 500 ns duration.
28	HEAD LOAD	HLD	•The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	Phase 1/Step	PH1/STEP	•If the 3PM input is a logic low the three phase motor control is selected and PH1, PH2, and $\overline{PH3}$ outputs form a one active low signal out of three. PH1 is active low after MR. If the 3PM input is a logic high the step and direction motor control is selected. The step output contains a 4usec high signal for each step and the direction output is active high when stepping; active low when stepping out.
16	Phase 2/Direction	PH2/DIRC	
17	Phase 3	$\overline{PH3}$	
18	3 Phase Motor Select	3PM	

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PIN NO.;	PIN NAME;	SYMBOL;	FUNCTION
29	Track Greater Than 43	TG43	•This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	•This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	•This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	•This input detects writing faults indications from the drive. When WG = 1 and WF goes low the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	•This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	•Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	•This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DISK INTIALIZATION}}$	$\overline{\text{DINT}}$	•The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$ = 0, the operation is terminated and the Write Protect Status bit is set.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	•This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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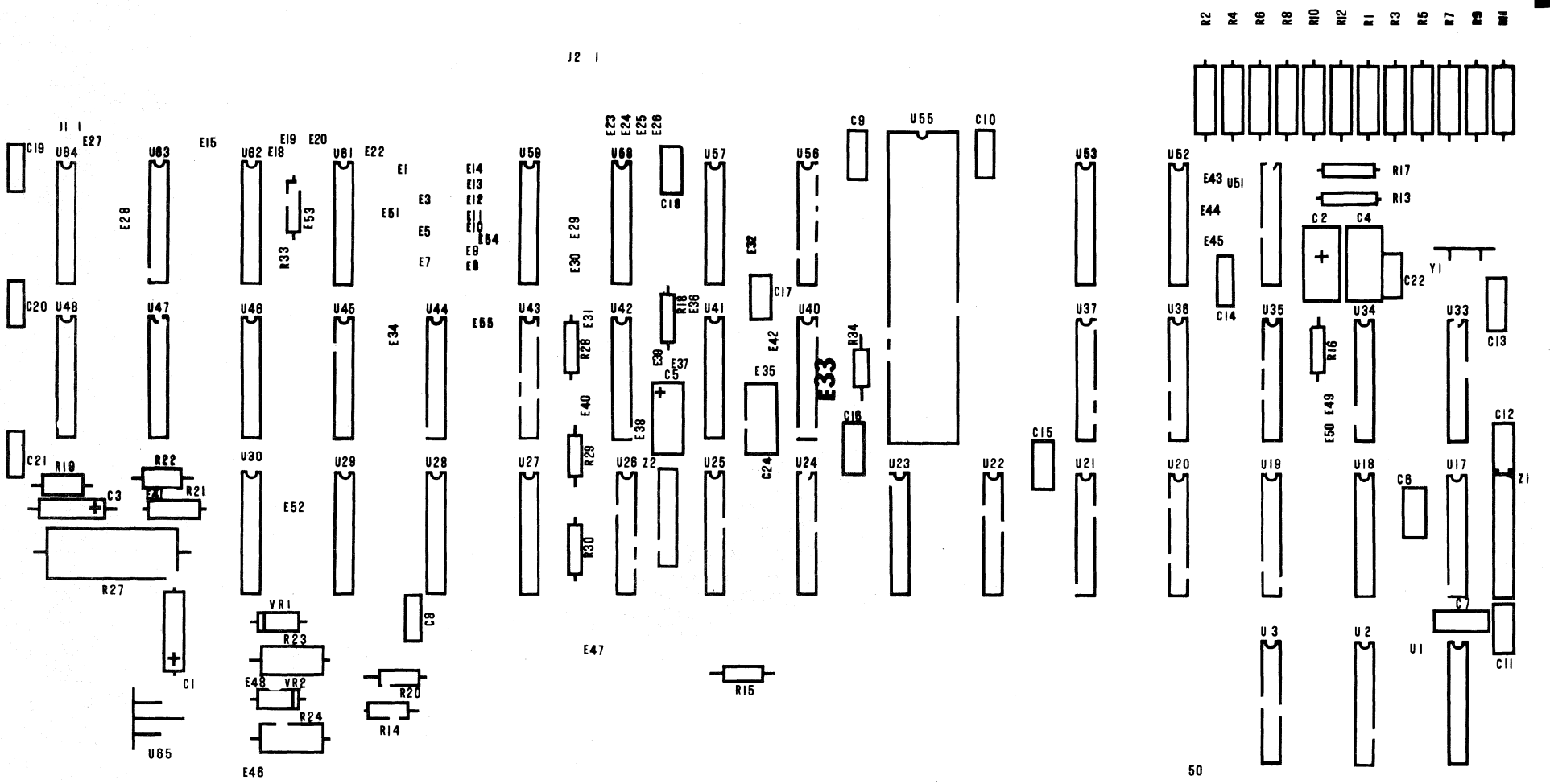
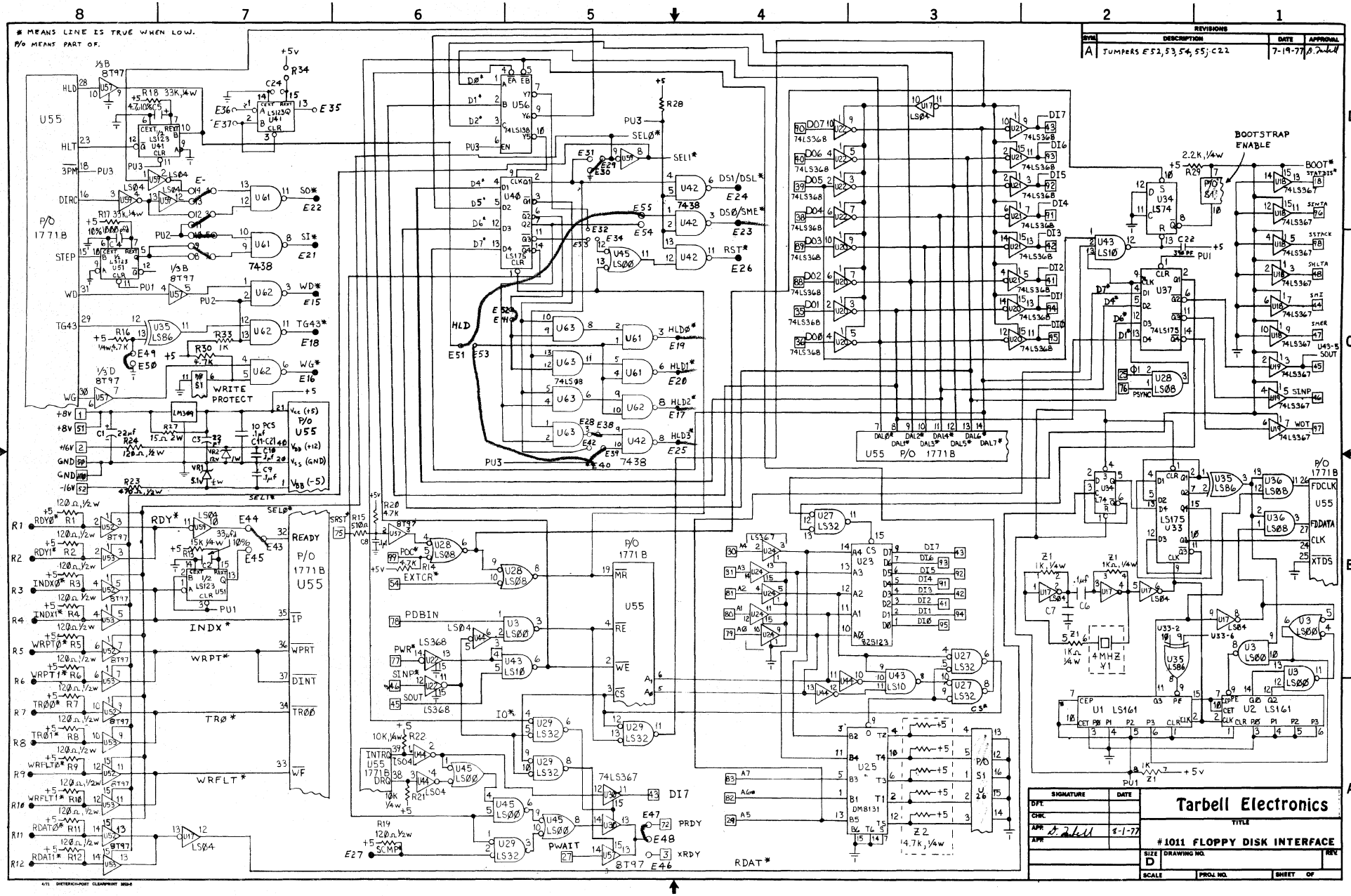


TARBELL MDL 1011 SILKSCREEN


* MEANS LINE IS TRUE WHEN LOW.
P/O MEANS PART OF.
REVISIONS
LTR | DESCRIPTION | DATE | APPROVAL
A | JUMPERS E52,53,54,55; C22 | 7-19-77
Tarbell Electronics
#1011 FLOPPY DISK INTERFACE
SIZE D | DRAWING NO. | REV.
SCALE | PROJ. NO. | SHEET OF
DFT. | CHK. | APP. D. Tarbell 8-1-77 | APP.
SIGNATURE | DATE
U55
P/O 1771B U55
BOOTSTRAP ENABLE
INDX*
WRPT*
TRØ*
WRFLT*
READY
P/O 1771B U55
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
HLDØ*
HLD1*
HLD2*
HLD3*
DS1/DSL*
DSØ/SME*
RST*
SELØ*
SEL1*
WD*
WG*
TG43*
SO*
SI*
STEP
DIRC
HLT
3PM
WD
WG
TG43
RDATØ*
RDAT1*
PRDY
XRDY
PWAIT
RDAT*
WRITE PROTECT
— Jumpers
= DIP SWITCH