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Sun-3/160M/160C Functional Overview

Sun-3/160M/160C Functional Overview

This chapter describes the function of the basic Sun-3/160M and Sun-3/160C components and their interaction. The models 160M and 160C SunStations are identical in physical appearance and design, with the exception of hardware present in the Sun-3/160C that relates to the function of the color monitor.

The two models are therefore treated as one in text that describes components that are common to both models. Subsections that deal with components present only in the Sun-3/160C, such as the color video board, are included under headings such as *Sun-3/160C Color Video Board.*

The Sun-3/160M and Sun-3/160C are both stand-alone workstations that include a 19-inch monitor, keyboard and mouse, and a deskside pedestal that houses the microcomputer, memory subsystem, power supply, and associated circuitry. Both models can also be nodes on a local area network.

The list of applicable documents at the front of this manual refers to other sources of theory on components that are briefly described in this chapter.

This overview begins with the microcomputer boards that are housed in the 12-slot VME card cage inside the desk-side pedestal. The CPU and memory expansion boards are the heart of Sun-3 architecture, and are discussed first. Optional boards and the remaining major workstation subassemblies are described next.

Figure 1-1 illustrates the relationship of the components discussed in this chapter, which are presented in this order:

- CPU board
- Memory Expansion Board
- Backplane
- Color Video Board
- VME SCSI Board
- VME/Multibus Adapter Board
- Optional Graphics Processor Board
- Optional Graphics Buffer Board
- VME/VME Adapter Board
- Memory Subsystem (Mass Storage and Interfaces)
- Power supply
- Monitors; Keyboard and Mouse

Figure 1-2 *CPU Board Overview*

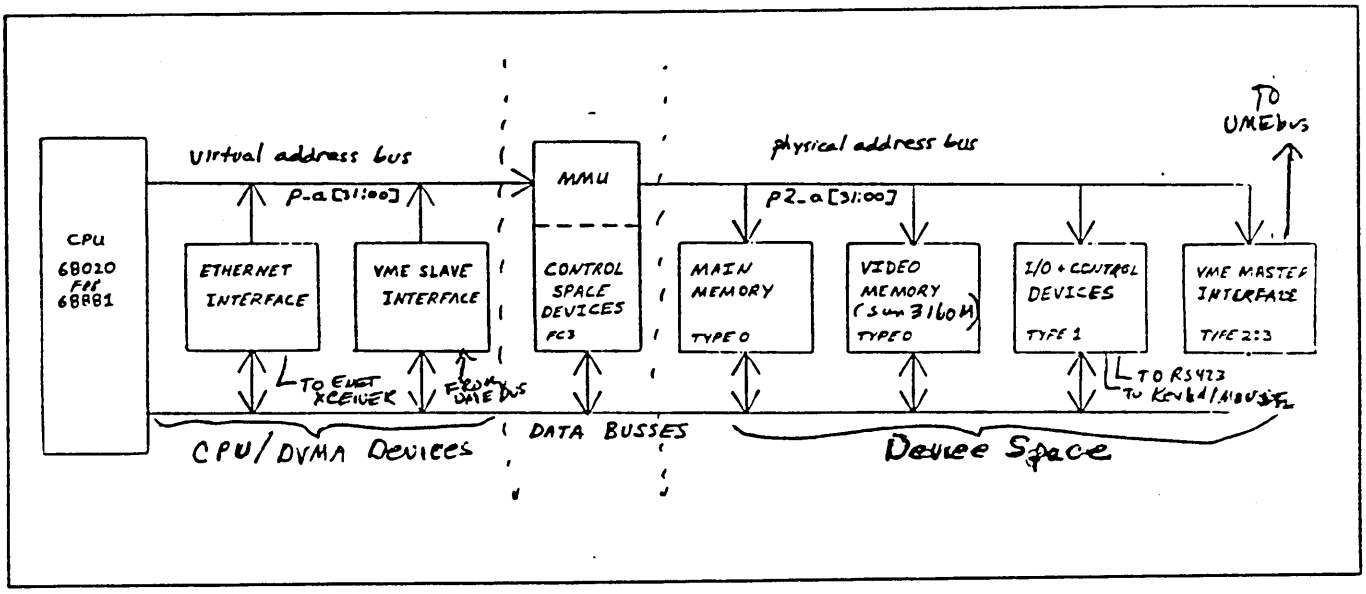


Figure 1-2 is a simplified block diagram of the 2060 CPU board. The CPU and DVMA devices depicted on the left side of the diagram supply virtual addresses to the MMU and arbitrate for control via the DVMA controller.

The MMU and control space devices (in the center of the diagram) are accessed in Function Code 3 space. Processor function codes further define virtual addresses and provide additional available address space.

The control space devices include processor extensions such as the bus error register, the system enable register, the diagnostic register, and the ID PROM.

The ID PROM stores basic information on the machine type; the node's unique 48-bit Ethernet address; a unique serial number for software licensing and distribution, the date the PROM was generated; and a checksum.

The MMU translates the virtual addresses into physical addresses to provide access to devices such as main and video memory, the VMEbus master interface, and I/O. It protects and manages these devices, and allows them to be shared.

The 8-bit buses service these components:

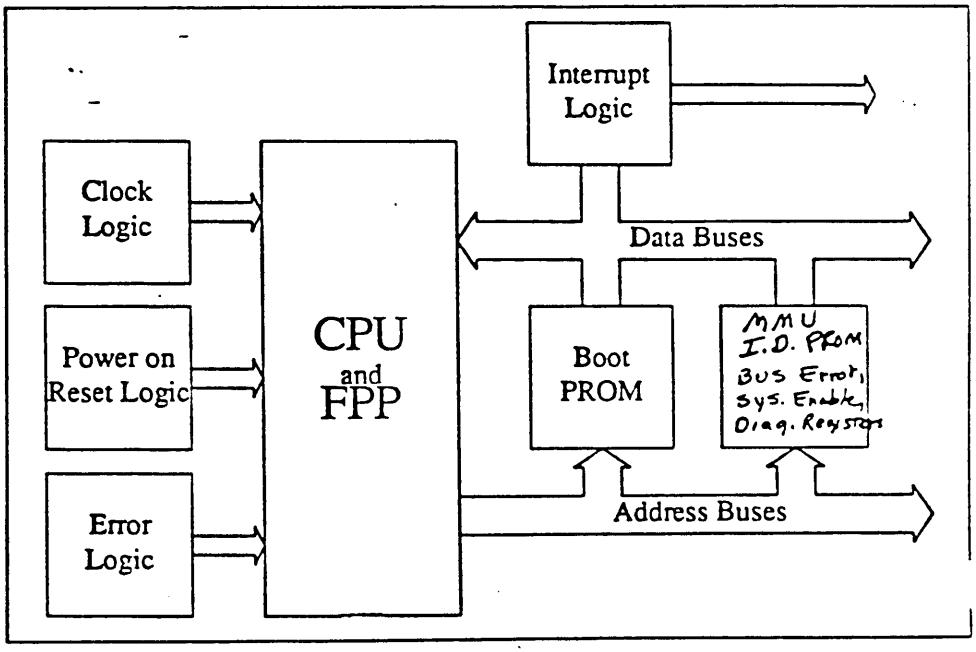
Table 1-1 *CPU Board 8-Bit Data Buses*

	MOS BUS	TTL BUS
Device Space Components	Keyboard/Mouse RS423 Port Time of Day Clock EEPROM EPROM	Parity Error Register Parity Address Latch Ethernet Control Register Interrupt Register
Control Space Components (Processor Extensions)		I.D. PROM Segment/Page Maps Diagnostic Register User DVMA Register System Enable Register Bus Error Register Context Register

CPU Logic and DVMA Devices

The functional blocks that comprise processor logic are shown in Figure 1-5, and discussed in the text that follows.

Figure 1-5 *Processor Logic Diagram*



The MC68020 CPU

The CPU board is based on the Motorola MC68020 virtual memory microprocessor, which runs at 16.67 Mhz and uses 32-bit addresses, as well as 32-bit registers and data paths. The CPU also features on-chip instruction cache and full IEEE floating point support (implemented with the 68881 FPP).

The MC68020 CPU uses sixteen 32-bit general-purpose data and address registers; a 32-bit program counter, a 16-bit status register, a 32-bit vector base register; two 3-bit alternate function code registers and two 32-bit cache handling registers.

On-Chip Cache Memory

The 256 byte direct mapped instruction cache is organized as 64 long-word entries. Each cache entry consists of a tag field made up of the upper 24 address bits, the Function Code 2 (user/supervisor) value, one valid bit, and 32 bits of instruction data.

The instruction cache stores a copy of previously executed instructions that are stored in main memory which effectively decreases main memory access time. The CPU first checks the cache for the next instruction; if the required instruction is found there, no instruction fetch is required, which increases system performance.

Processor Supporting Logic

Logic supporting the MC68020 includes programmed array logic (PAL) chips that perform CPU space decoding, reset, bus error detection, data transfer acknowledge, and interrupt priority encoding/acknowledgment. Boot-up and diagnostic code is stored in 64Kbytes of eraseable, programmable read-only memory (EPROM).

System Reset

The power-on/reset logic provides a means of starting a processor and/or system initialization sequence in response to fluctuations in supply voltage; a reset signal from an external bus or the watchdog reset switch; or a halt in the CPU processing cycle.

Power-on reset is active for a minimum 100 msec after the power supply voltage reaches 4.5V. Power-on reset results in the following:

- CPU Reset
- System Enable Register Clear
- Forced Boot State
- Diagnostic Register Reset (lights LEDs)
- FPP Reset
- Memory Error/Interrupt Register Reset
- Keyboard/Mouse; RS423 Port Reset
- VMEbus Reset
- Ethernet Interface Reset
- All State Machine PALs Reset

If the CPU board is jumpered to enable a VME bus arbiter other than the CPU board, the VME bus SYSRESET signal, initiated off-board, can cause a power-on reset.

A double bus fault that causes a CPU halt results in a watchdog reset, which invokes the PROM monitor program. The User Reset Switch, located on the rear edge of the CPU board, provides a manual watchdog reset.

Interrupt Logic

The 2060 board interrupt logic prioritizes interrupt requests from internal and external logic groups that are directed to the CPU.

The various levels of VME interrupts are mapped to the corresponding on-board levels.

On-board interrupts receive higher priority than off-board VME interrupts at the same level. On-board interrupts are autovectored on all levels, with the exception of level 6, which represents the serial communications controllers (SCC)s. SCCs provide their own vector for functions such as transmit and receive, which eliminates time that interrupt software would take to determine which part of the SCC originated the interrupt.

Direct Virtual Memory Access

Direct virtual memory access (DVMA) allows devices to use the MMU to read from and write to memory. DVMA devices include the Ethernet interface, the VMEbus slave interface, and refresh circuitry.

A DVMA cycle is initiated when inputs from either the memory refresh logic, the Ethernet control or the VMEbus slave interface are synchronized and presented to the DVMA controller. The controller then generates a processor bus request and waits for a bus grant signal. The CPU issues the bus grant, which the DVMA controller acknowledges by asserting a bus grant acknowledge and removing the bus request.

The controller then determines the priority level of the request; sends a DMA enable signal to the requester, and, for VME slave or Ethernet requests, asserts the P2 DVMA address strobe. Following an acknowledge from memory or video circuitry, the transaction is ended with removal of the address strobe and bus grant acknowledge, and then the DMA enable signal.

DVMA handling for refresh circuitry differs slightly from that for other DVMA devices, in that the controller does not issue a P2 address strobe and waits for a special R.SSAS refresh signal rather than an acknowledge signal.

The refresh circuitry receives highest priority, followed by the Ethernet and VMEbus slave interfaces. The Ethernet interface can issue a HOLD signal along with the bus request to retain bus mastership for the 82586 FIFO circuitry.

User DVMA

A User DVMA Enable Register provides an external VME device with 256 MBytes of accessable memory for each of eight contexts.

User DVMA occurs with user function codes when a VME device accesses the top two gigabytes of 32-bit address space on the VMEbus, provided that the corresponding context is enabled in the User DVMA Enable Register.

Type bits divide memory addressing in this way:

Type 0: Main and Video Memory

Type 1: I/O and Control Devices

- Keyboard/Mouse Interface
- Serial I/O Ports
- EEPROM
- EPROM
- Time of Day Clock
- Parity Error Registers
- Interrupt Register
- Ethernet Control Register
- Data Cyphering Processor

Type 2: 16-Bit Data VME Master Interface

Type 3: 32-bit Data VME Master Interface

On-Board Main Memory Logic

Sun-3 memory architecture is based on the concept of virtual memory, in which only a small portion of the total logical address space is mapped onto the physical memory resident on the boards. The balance of the maximum available memory space is located either on a secondary storage device (e.g. a large capacity disk drive) or on the network, and accessed via the DVMA scheme.

When the CPU attempts to access a virtual memory address location that is not currently residing in physical memory, a page fault occurs, and the data is fetched from the secondary storage device.

Memory Refresh Logic

The refresh logic provides a refresh cycle for memory every 15.7 usec. This logic is composed of a PAL and a pair of counters. The first (8-bit) counter generates a clock pulse, which is used by the DVMA control logic to produce an enable signal for the second (refresh) counter. The refresh counter then sends a refresh address to memory.

Main Memory

Main memory consists of 144 256Kx1, 120 nsec DRAMs, divided into four 1Mbyte banks. The 2060 board is also available with 2Mbytes of on-board RAM, divided into two banks.

A jumper on the optional expansion memory board (illustrated in Appendix B) enables two or four megabytes of additional memory.

The main memory address decode logic, which includes RAS and CAS PALs, and a row/column multiplexer, determines which bank of memory is being addressed. Memory access occurs when the write data and the read/write control signals are valid at the same time that CAS is valid.

A sequence of 16 states, continuously executed by the state machine, determines when the cycles are performed. Idle and processor update cycles are executed during the first eight states; the video refresh cycle is executed during the last eight.

Video Sync Control Logic

Video sync control logic is composed of horizontal and vertical state machines that generate horizontal and vertical sync signals, respectively. The video controller register latches state machine outputs, which are then transmitted to the video monitor.

Video Shift Logic

Video shift logic consists of a TTL-to-ECL converter and a 100MHz shift register. Video data is loaded from video memory into the TTL to ECL converter and clocked through the 100 Mhz shift register. The converter supplies differential ECL video to the monitor.

Serial Communications Interface

Two 8530 Serial Communication Controllers (SCCs) implement communication between the CPU board and the keyboard, mouse and the RS-423 interface.

One SCC is dedicated to the keyboard and mouse; the other to RS-423 communication. The SCCs function as Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) to serialize parallel data that is transmitted from the CPU board, and route it to the respective interfaces. The inverse is true for incoming serialized data.

Each SCC provides two high-speed, fully symmetrical, programmable serial channels with built-in baud rate generators.

The SCC that supports the Sun-3/160M/160C RS423 interface supplies serial I/O from Channel A to the rear panel serial port A, and serial I/O from Channel B to to the serial port B. Channels A and B can also be shared for synchronous transfers.

The SCC that services the keyboard and mouse functions as an asynchronous receiver/transmitter, using Channel A for the keyboard, and Channel B for the mouse.

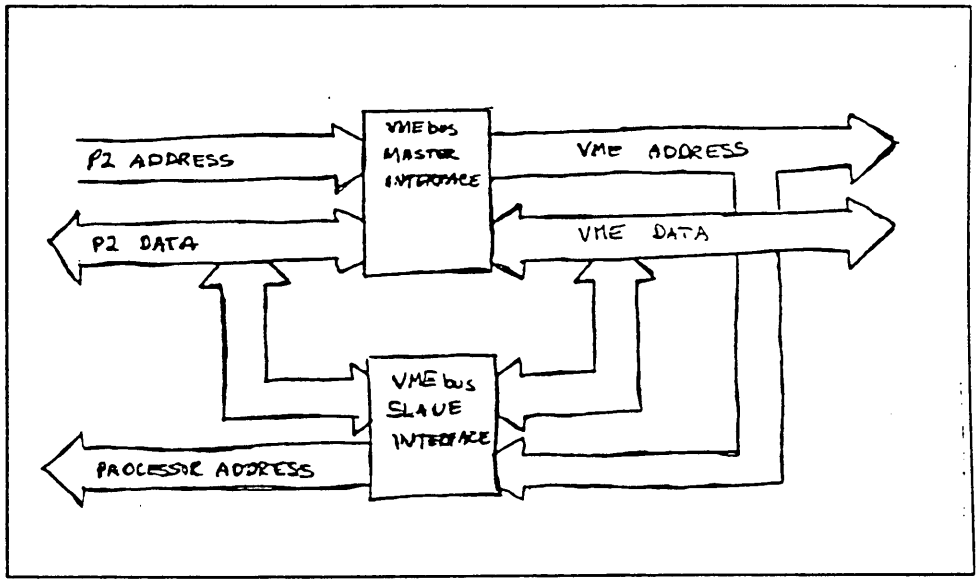
Ethernet Interface

The primary components of the Ethernet interface are an Ethernet controller PAL, an Intel 82586 Ethernet Data Link Controller (EDLC), phase locked loop encoding/decoding circuitry, and address and data buffers, which interact to provide the hardware necessary for communication between the Sun-3/160M/160C and other nodes connected to the Ethernet. Figure 1-8 illustrates Ethernet interface logic.

VMEbus Interface

The VMEbus interface provides bidirectional data access between the CPU board and any device connected to the VMEbus. The interface logic consists of bus arbitration and request circuitry, as well as logic that allows the CPU board to act as the bus master or as a bus slave. Figure 1-9 is a block diagram of VMEbus interface logic.

Figure 1-9 *VMEbus Interface*



VMEbus Arbitration

Two PALs and a pair of registers monitor bus request levels and arbitrate requests, using a level daisy chain. When the CPU requests the bus (in order to perform a read/write cycle, or to acknowledge an interrupt), it sends a bus select signal to one of the PALs.

If the arbitration logic does not control the bus, it will assert a VME bus request signal to request bus mastership. If the arbiter currenty controls the bus, it will retain control until another bus master requests it.

When the arbitration logic has attained VME bus mastership, the CPU may access any slaves on the bus via the VMEbus master interface. When the CPU relinquishes bus mastership, it becomes a bus slave, and may be accessed by other VMEbus masters, via the VMEbus slave interface.

VME Master Read/Write Cycles

During a VME Master read or write cycle, the type bits coming out of the MMU indicate either an access to Type 2 or Type 3 space (refer to the MMU subsection). VME address and data strobes are then generated, and the CPU board waits for a DTACK signal from the VME device being addressed. Upon receipt of data transfer acknowledge, the VME bus master will negate the address and data strobes, ending the transfer.

1.4. The 160C Color Graphics Board

The color board provides high resolution color graphics for the Sun-3/160C workstation. This board replaces the monochrome video logic resident on the CPU board, which is enabled only for the Sun-3/160M workstation.

The board is a bit-mapped graphics subsystem that features a 1152x900x8, 66Hz non-interlaced display; a frame buffer that appears as a million 8-bit-deep pixels that each define one-out-of-256 shades of red, blue or green; and 8-plane "RasterOp" support.

Color board logic is separated into the following functional blocks:

- VMEbus interface
- frame buffer logic
- memory timing and synchronization circuitry
- color maps
- digital-to-analog converters (DACs).

Figure 1-10 presents a functional block diagram of color video board logic.

Figure 1-10 *Sun-3/160C Color Video Board Logic*

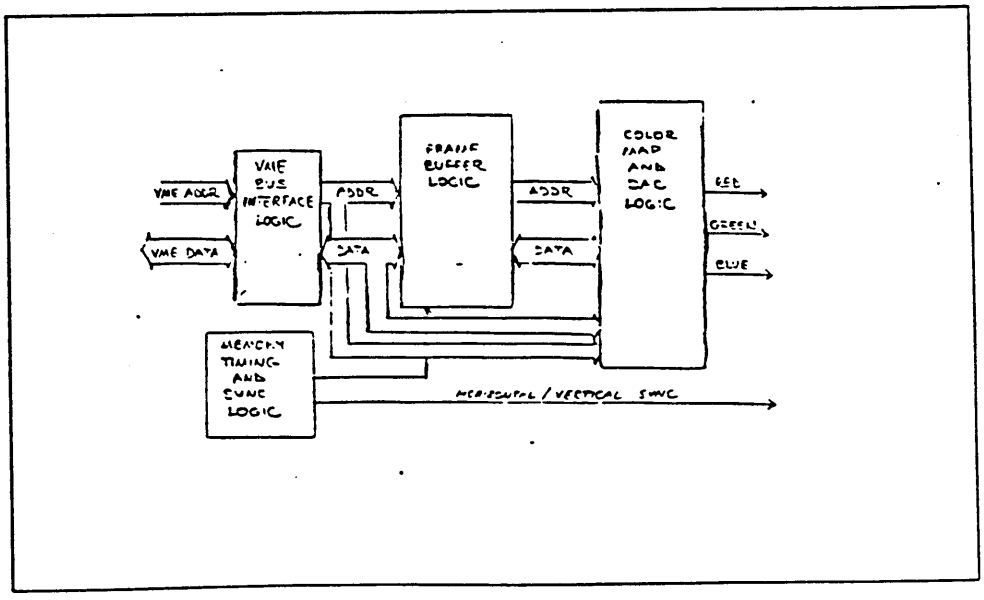
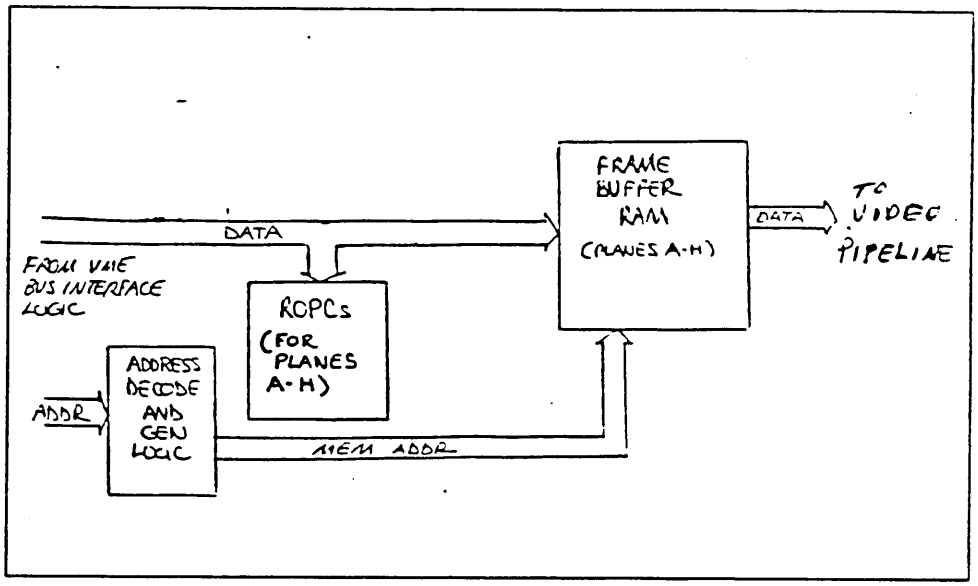


Figure 1-12 *Color Board Frame Buffer Logic*



Frame Buffer Memory

The frame buffer is separated into eight planes, labeled A through H. It consists of 128 64K RAM chips and is organized as eight memory planes with 16 RAM chips per plane.

Frame Buffer Addressing

The frame buffer receives addresses from either of two sources; the VME address bus or the video refresh logic. During updates to the frame buffer memory, the VME address lines are multiplexed to form the CAS and RAS addresses.

Specific bits in the VME address are also used to select the possible addressing modes: word mode, pixel mode, or ROP mode. The word mode and pixel mode counters each generate an address, which, when selected, is driven to the frame buffer inputs. Video refresh memory cycles and inactive read/write cycles take their addresses from a pair of 16-bit counters and the Word-Pan Base Address register.

Address Modes

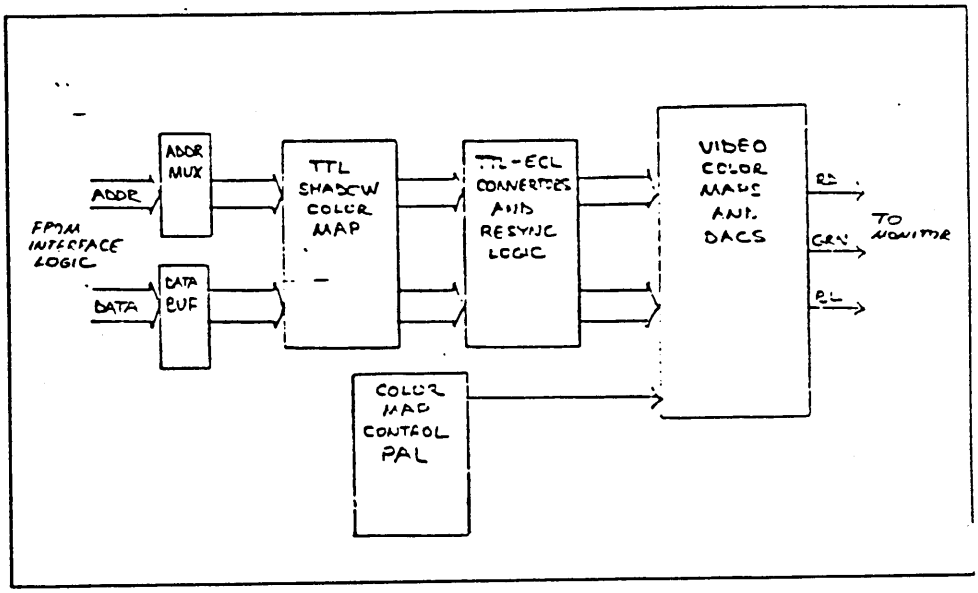
The data input to the frame buffer is dependent upon the frame buffer addressing mode. Ten addressing modes are available: word-mode memory, pixel-mode memory and four word and four pixel modes controlled by the RasterOp chips (ROPCs).

Raster and other operations that use less than eight bits per pixel use word mode accesses, while drawing, shading algorithms and other imaging related applications use pixel mode accesses.

Color Maps and DACs

Color map and DAC logic consists of the color map video translation tables, the video digital-to-analog converters (DACs), the TTL shadow color map, the color map control PAL and associated circuitry. Figure 1-14 illustrates this logic.

Figure 1-14 *Color Map and DAC Logic*



The color map video translation tables and the video digital-to-analog converters are housed in a single hybrid ECL device. This device outputs red, green and blue color signals to the monitor.

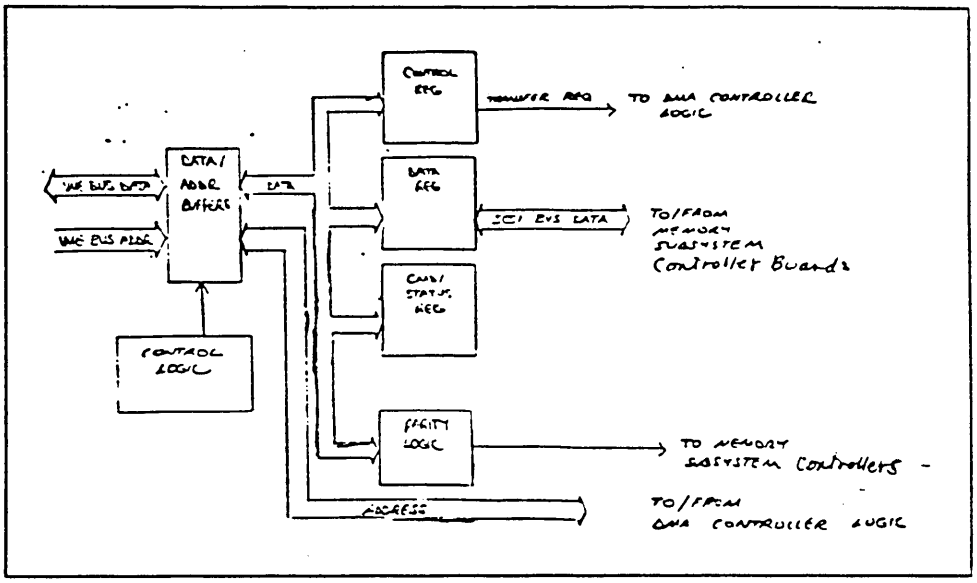
The TTL color map consists of a pair of 1K x 4-bit static RAMs. Because of the real-time constraints involved in updating the internal ECL color maps, the TTL color map is used to provide read/write access. Transmission of TTL color mapped data and addresses to the ECL color map occurs during vertical retrace.

The VME address bus routes color mapped addresses to the TTL shadow color map. The shadow color map also receives 8 bits from the VME data bus. During the vertical blanking interval, data stored in the shadow color map is output to TTL-to-ECL converters and presented to the internal ECL color maps. The color map control PAL selects from the red, green or blue color maps.

SCSI Bus Interface Logic

The SCSI bus interface logic consists of the interface control, data and command/status registers, as well as the parity logic and control circuitry. The SCSI bus interface logic is illustrated in the block diagram in Figure 1-16.

Figure 1-16 *SCSI Bus Interface Logic*



The interface control register manages the interface between the VME bus and the SCSI bus via 8 bits from the VME data bus and 8 control lines from the SCSI bus. The control lines and data bits are input to the control PAL, which generates control signals for use by the SCSI board. The original control and data bits are then buffered back onto the VME data bus.

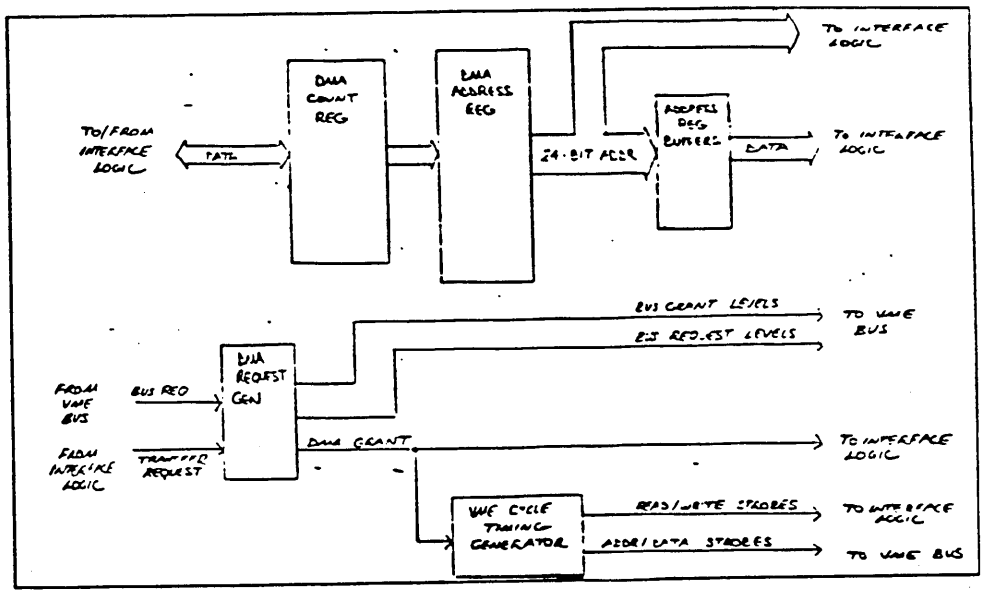
The data register is used to transfer data between the VME and SCSI buses. The mechanics of data transfers between the 16-bit VME bus and the 8-bit SCSI bus are described in the paragraph that discusses byte sequencing.

The command/status register transfers commands and status between the two buses. The command/status register is 8 bits wide on both the VME and SCSI bus sides.

The parity logic generates odd parity for data being output onto the SCSI bus and verifies the odd parity of incoming SCSI bus data. The control PAL latches parity errors and the control interface register buffers them back to the VME data bus.

The SCSI bus interface circuitry is responsible for byte sequencing, the SCSI bus request/acknowledge handshake and interrupt generation. This circuitry operates under the influence of two modes: DMA enable or word mode.

Figure 1-17 *DMA Controller Logic*



The DMA count register is a 16-bit counter which may be written to or read from the VME bus. Its function is to determine how many bytes of data have been transferred utilizing DMA, and to enforce a maximum count. Sixteen bits of data are passed through the counter to provide inputs for the DMA address register. Because of the counter's tracking function, it increments in unison with the address register.

The DMA address register is 24 bits wide. It produces a 24-bit address from the 16-bit data bus by utilizing the lower 8 bits twice. The register output is placed on an internal address bus, where it is routed to both the VME address bus and the SCSI board's internal data bus.

The DMA cycle timing generator runs the DMA cycle. The generator is primarily composed of two PALs, which supply read/write strobes for the data register as well as data and address strobes for the CPU board.

The control register outputs a transfer request signal to initiate a DMA request. This signal is input to the bus requester PAL, which then transmits the appropriate bus request level to the VME bus.

All bus arbitration capability for the SCSI board resides in the CPU board arbiter logic (refer to the CPU board functional overview). The CPU arbiter logic assert bus-grant-in signal at the appropriate level, which is presented to the bus requester PAL. The PAL then grants control of the bus to the SCSI board.

both the VMEbus and Multibus.

The adapter board must translate VMEbus vectored interrupts, even though Multibus does not support them. The adapter board generates a vectored interrupt via DIP switch settings when the Multibus board interrupts on only one level or if a multi-level interrupt vectors to the same place. If the Multibus board interrupts on more than one level and a separate vector is required for each level, a PROM generates the vector.

Adapter board jumpers enable bus and constant clock signals for Multibus boards that require them. Appendix A provides a VME-Multibus component layout, and Appendix B contains a list of board jumper options.

The Graphics Processor Board

The optional Graphics Processor (GP) board is designed to enhance the graphics performance of the Sun-3/160C. The GP runs in parallel with the host processor (located on the CPU board) and performs many of the image display tasks currently done by the host, while remaining under host processor control.

Graphics Processor board logic is designed as two pipelined processors: the viewing processor and the painting processor. These processors, along with their associated logic, are illustrated in Figure 1-19.

Figure 1-19 *Graphics Processor Board Logic*

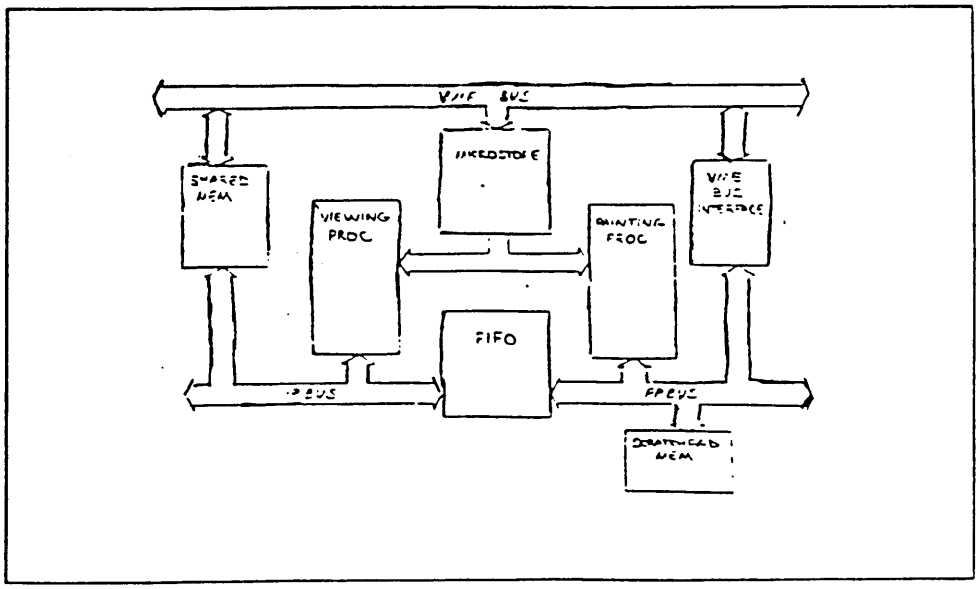
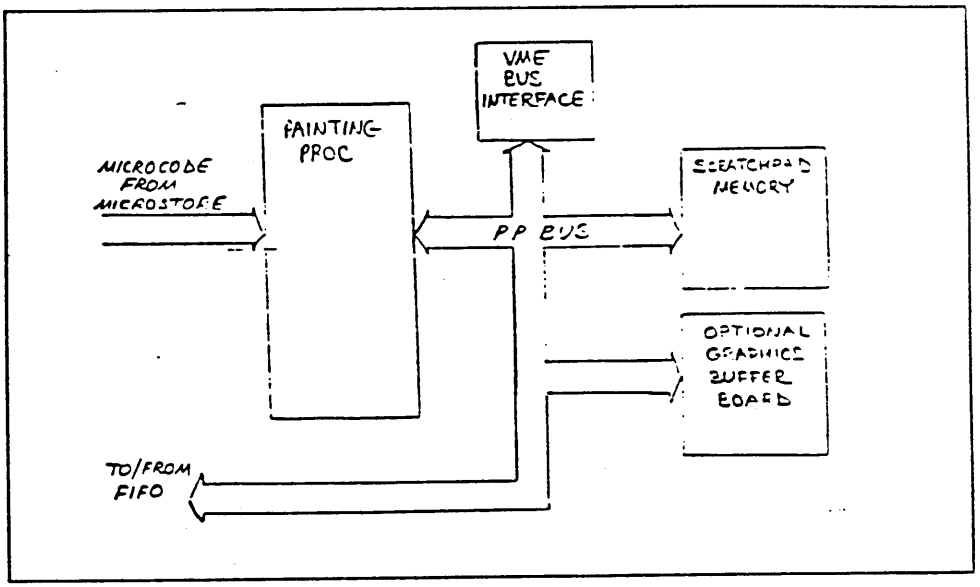


Figure 1-21 *Painting Processor Logic*



The painting processor uses the board's VMEbus interface logic to access the color board's frame buffer. While the VME interface is primarily used as a link between the GP and the color board, it may be used to access any other device on the VMEbus, including the host memory and the viewing processor's shared memory. The VMEbus interface also allows the GP board to generate and transmit an interrupt to the host processor.

Static RAM scratchpad memory is provided by 4Kx16 bit static RAM chips, and used to perform various algorithms necessary to painting processor function.

The 16-bit PPBUS transfers commands and data between the various painting processor components.

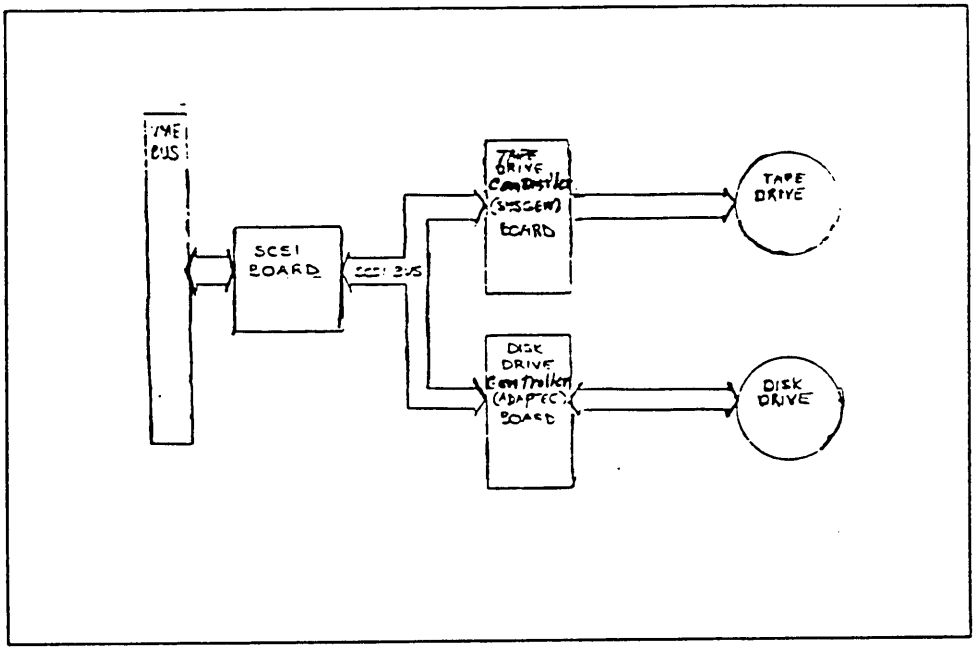
Processor Associated Logic

Viewing processor and painting processor logic share microstore logic and the FIFO buffer. Refer to the overview of the GP board logic in Figure 1-19 for an illustration of the relationship of this logic to the processors.

Microstore logic holds microcode for both the viewing and the painting processors. The two processors run 180 degrees out of phase, and therefore may share the microstore. A third port is available to allow access via the VME bus, but is active only when both the viewing and painting processors are halted.

The FIFO buffer is the pipeline mechanism between the viewing and painting processors. It provides 512 x 16 bits of transfer storage and is "reversible", allowing data to be transmitted back and forth between the VPBUS and the PPBUS.

Figure 1-22 *Memory Subsystem*



During a write to the memory subsystem, the SCSI board (as described earlier) transmits data and commands via the SCSI bus to either the tape drive or disk drive controller board. Each of the controller boards functions as a translator between the SCSI board and its respective tape or disk drive. The reverse of this operation occurs in order to read data and status from the subsystem.

The drives and their associated controller boards are mounted on a tray, located in the top of the Sun-3/160M/160C pedestal. Chapter 3 of this manual provides information required for removal and replacement of these assemblies.

1.8. The Power Supply

The 850 Watt power supply is located in the front end of the Sun-3/160M/160C pedestal. This supply generates four regulated voltages, available at the back-plane:

- +5VDC
- -5VDC
- +12VDC
- -12VDC

The power supply removal procedure in chapter 3 provides a wiring diagram that shows the supply inputs and outputs and their respective voltages.

The supply must shutdown or limit voltage if any output exceeds the value shown below. Input voltage may be recycled to restart the supply.

Table 1-4 *DC Output Limits*

Output	Shutdown Voltage
+5V	+6.2V ± 0.3V
–5V	–6.2V ± 0.3V
+12V	+13.5V ± 0.3V
–12V	–13.5V ± 0.3V

The supply can withstand 125% of the nominal line voltage for 60 msec. without damage, thermal shutdown, or loss of output regulation. Overheating causes a thermal shutdown and requires recycling of the AC input voltage before operation is resumed.

The monochrome monitors share these operational characteristics:

Table 1-5 *Monochrome Monitor Characteristics*

Visual Display	900 x 1152 pixels (Version A) 1024 x 1024 pixels (Version B)
Horizontal Scan Freq.	62.5KHz
Vertical Scan Freq.	66.67Hz
Horizontal Retrace	4.48usec
Vertical Retrace	600usec

Chapter 3 contains monitor removal and replacement procedures. Detailed descriptions of monitor hardware as well as maintenance and adjustment procedures are found in vendor service manuals (refer to the list of applicable documents at the beginning of this manual).

1.10. The Sun-3/160M/160C Keyboard and Mouse

This subsection will contain a brief overview of the differences between the keyboard and mouse for each of the two models, and point out the new mouse cabling.