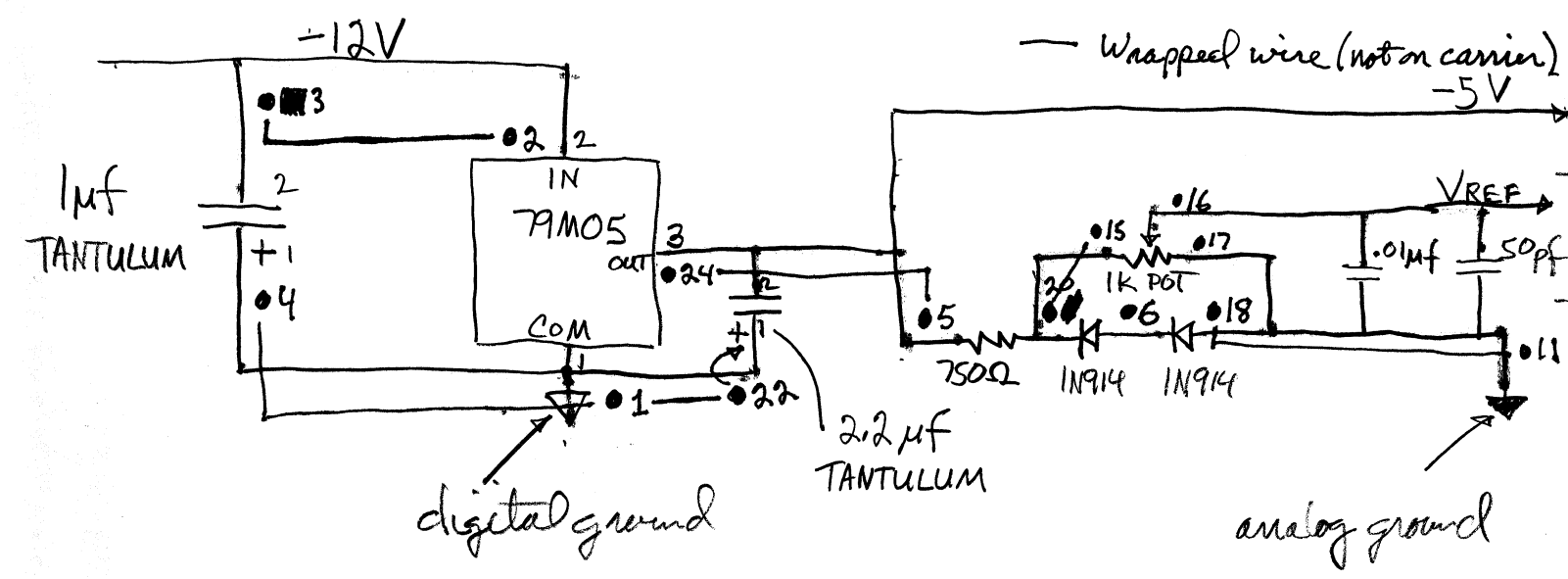


-5V → VREF

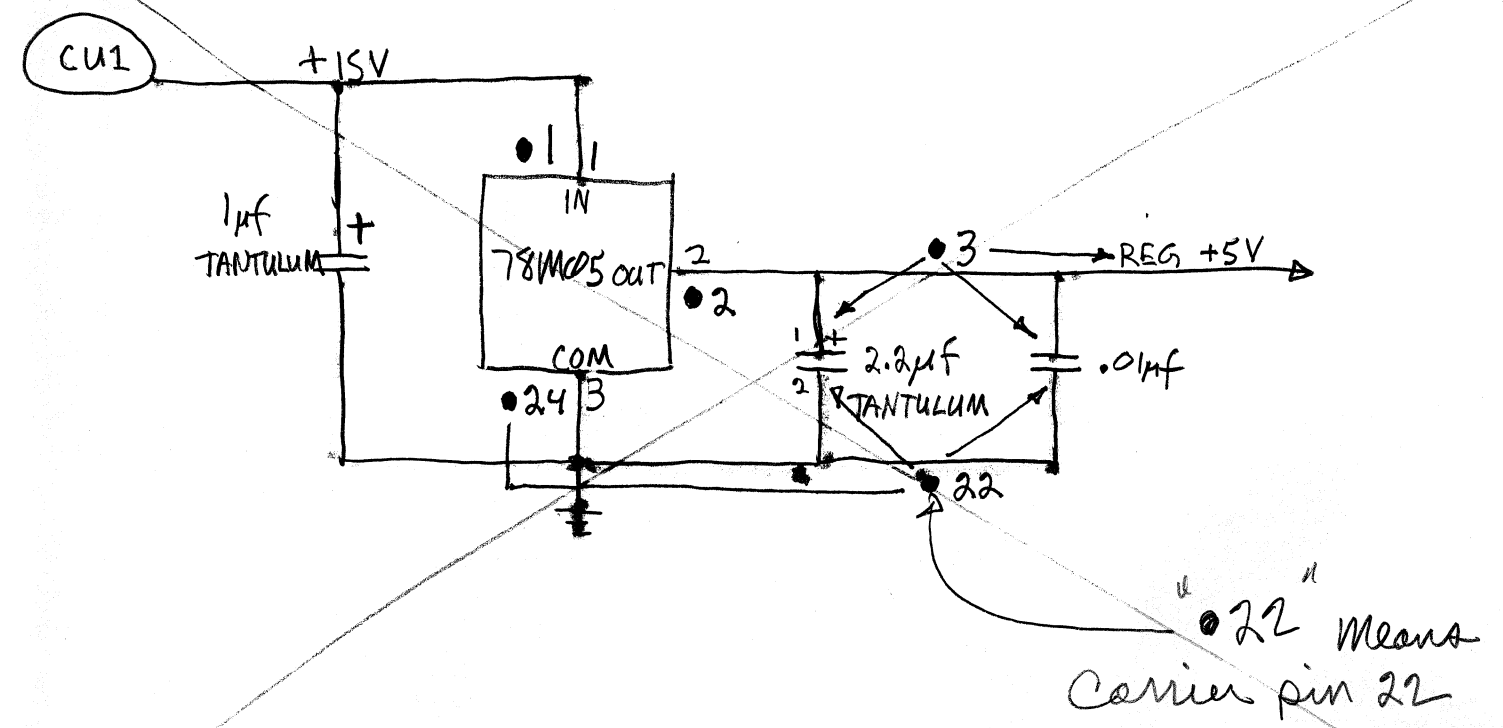
AH11 = PIN 1

●x  
 R 24 pin carrier  
 pin assignment

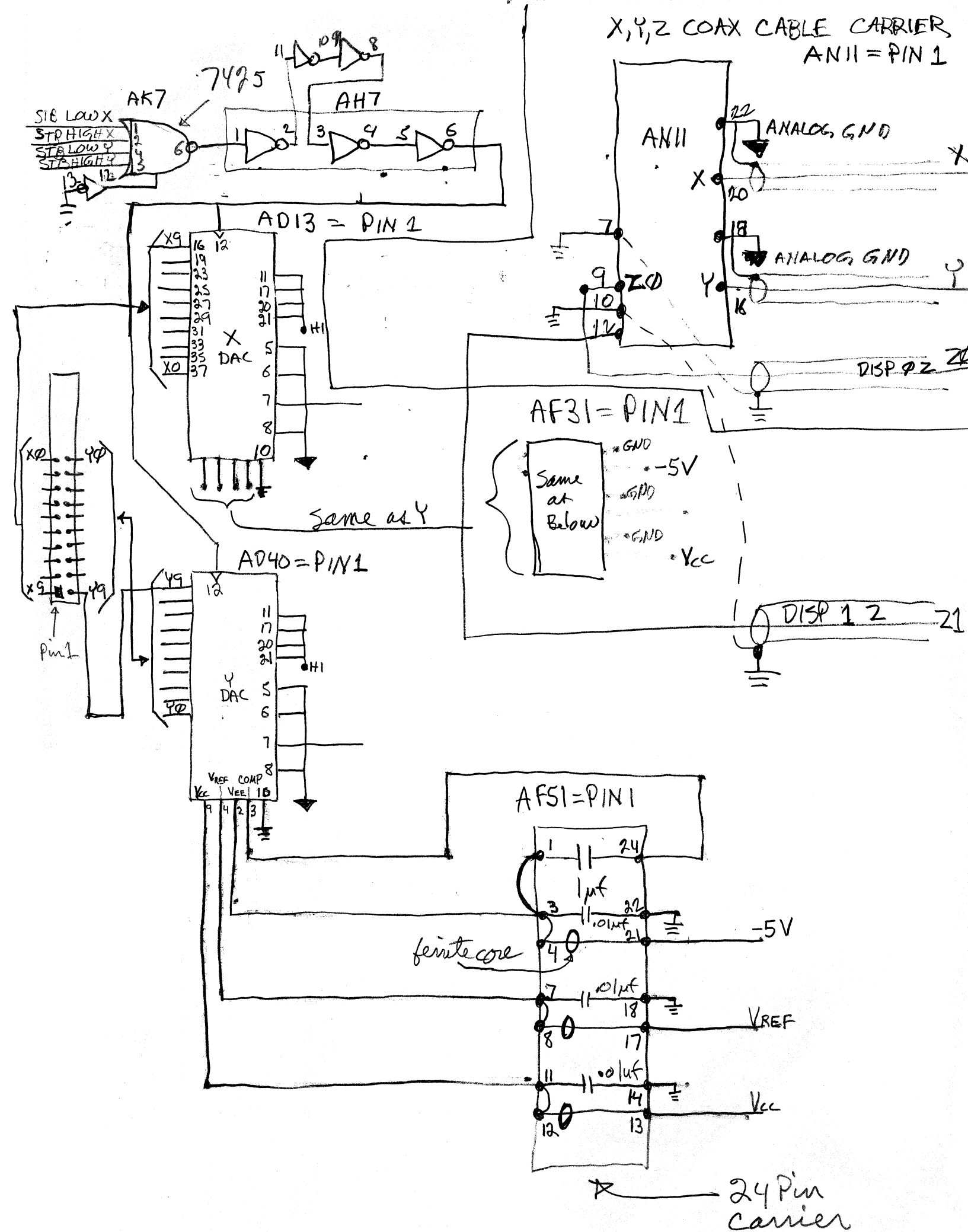


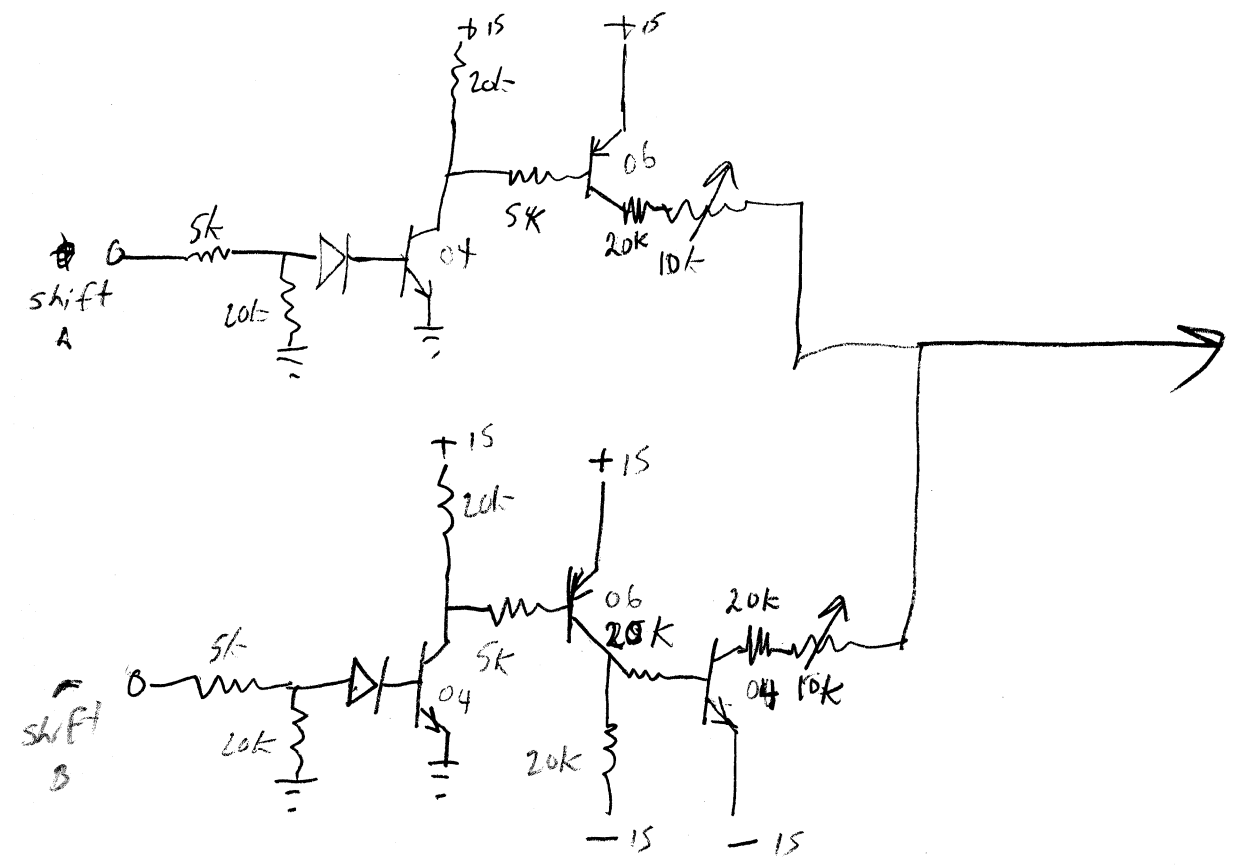
+5V REG

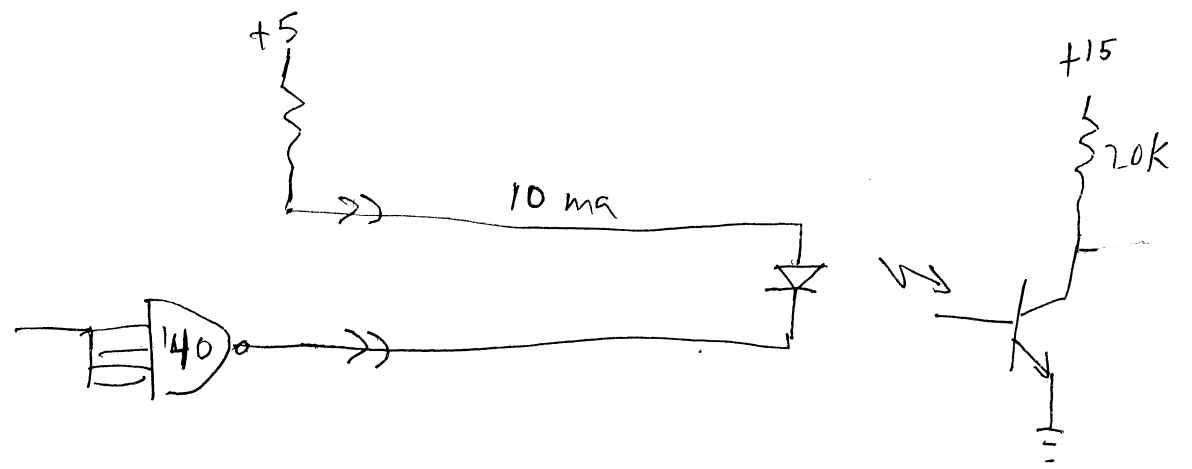
AH31 = PIN 1



●22 means  
 carrier pin 22

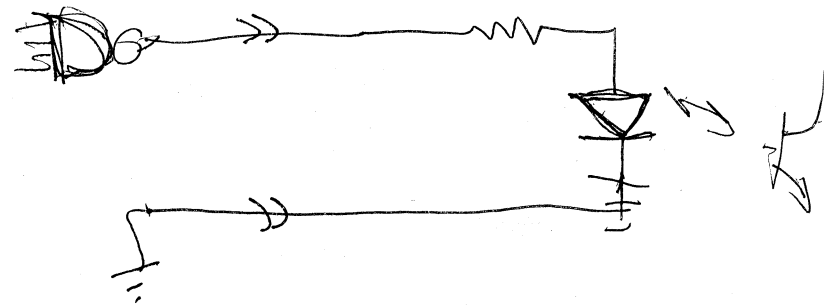


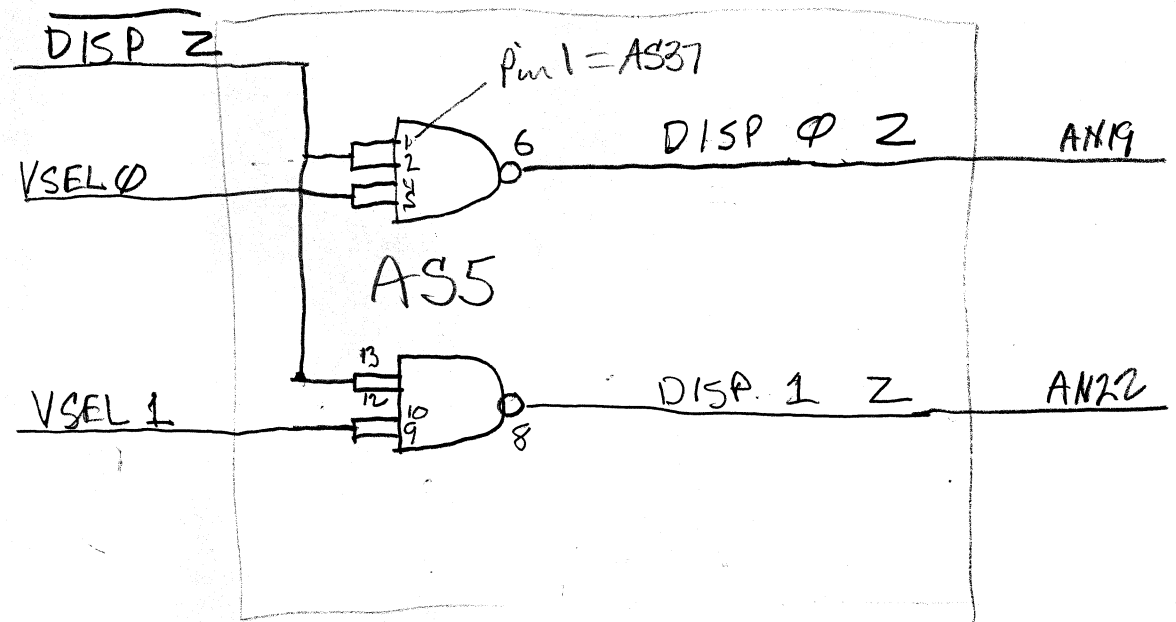
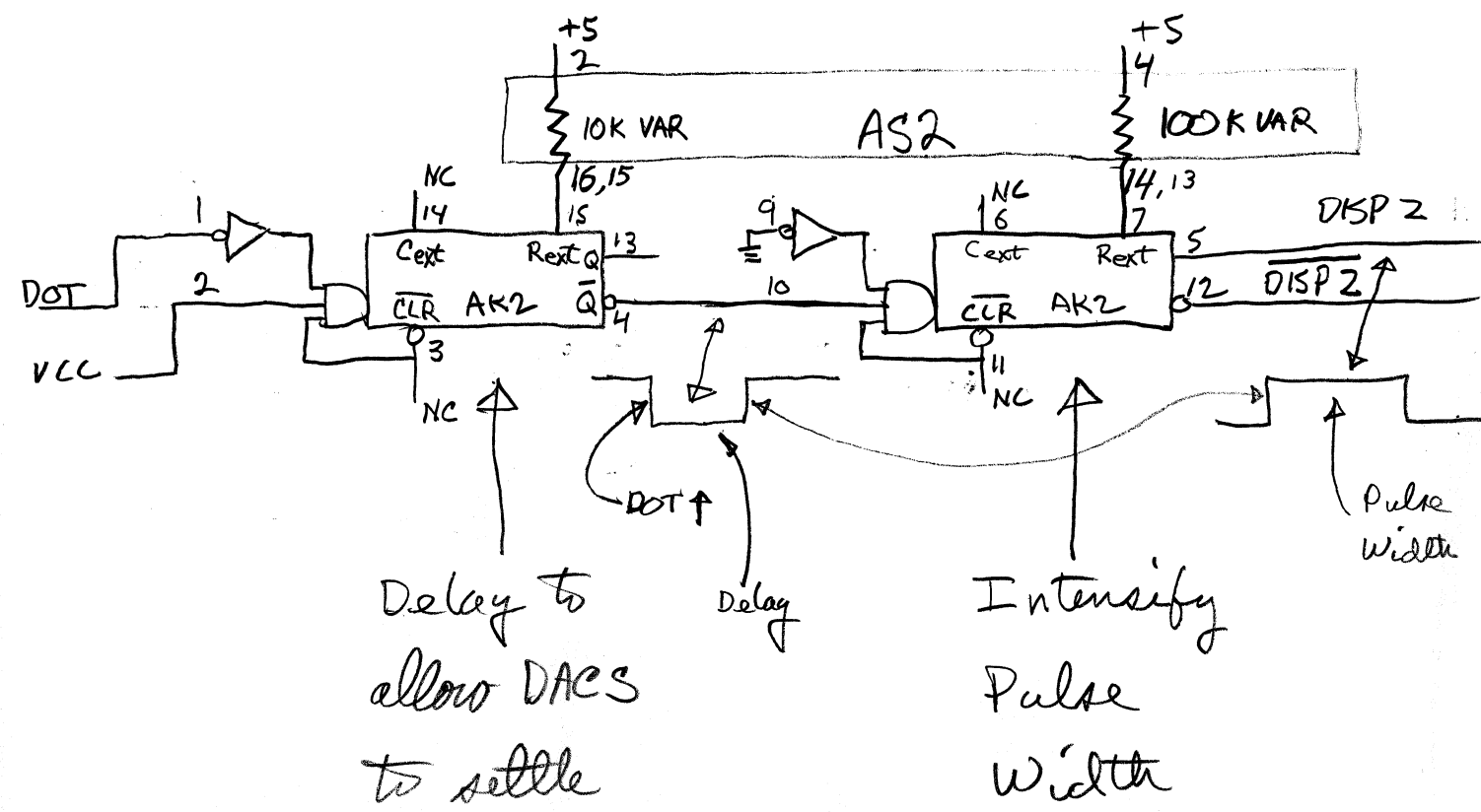


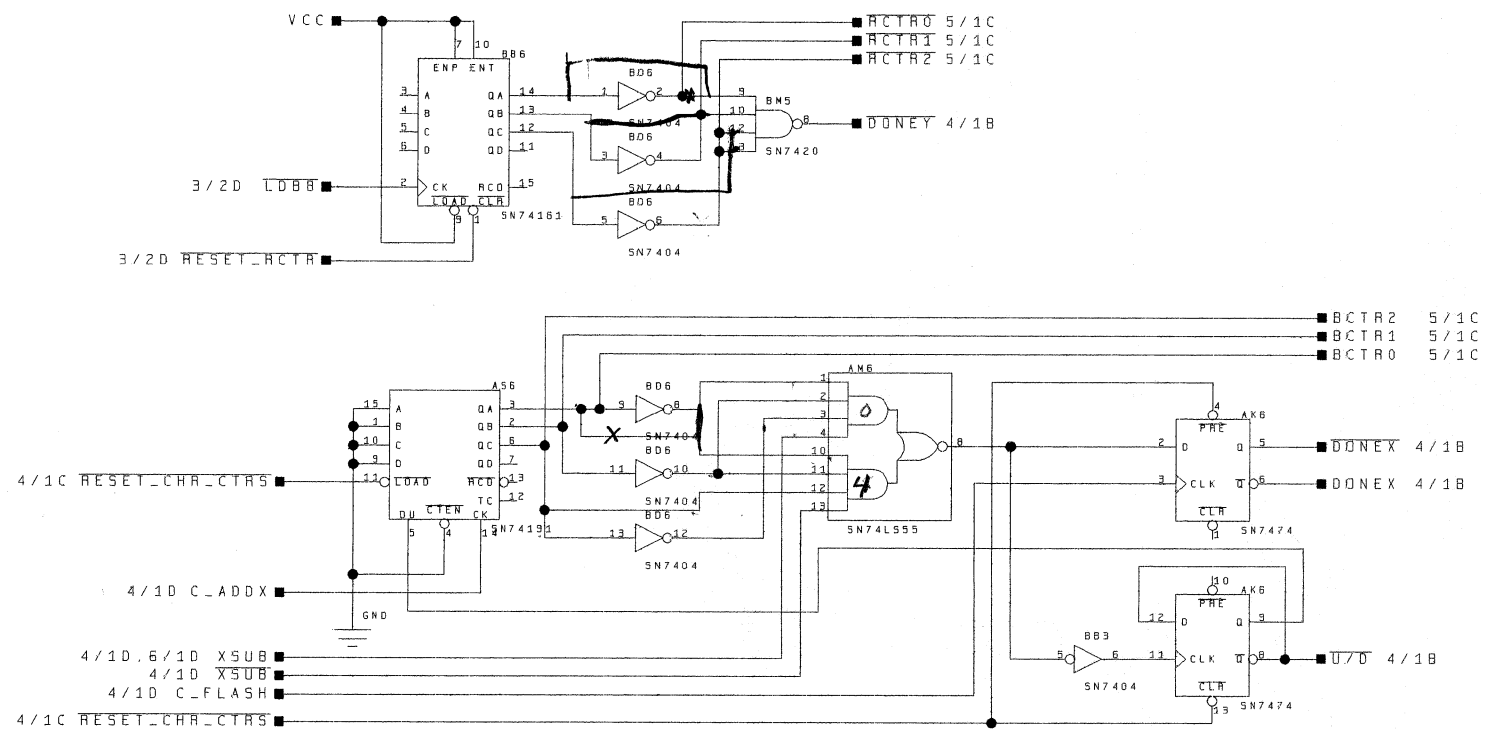


~~4V~~  

$$\frac{4V}{10\text{ mA}} = 400\Omega$$



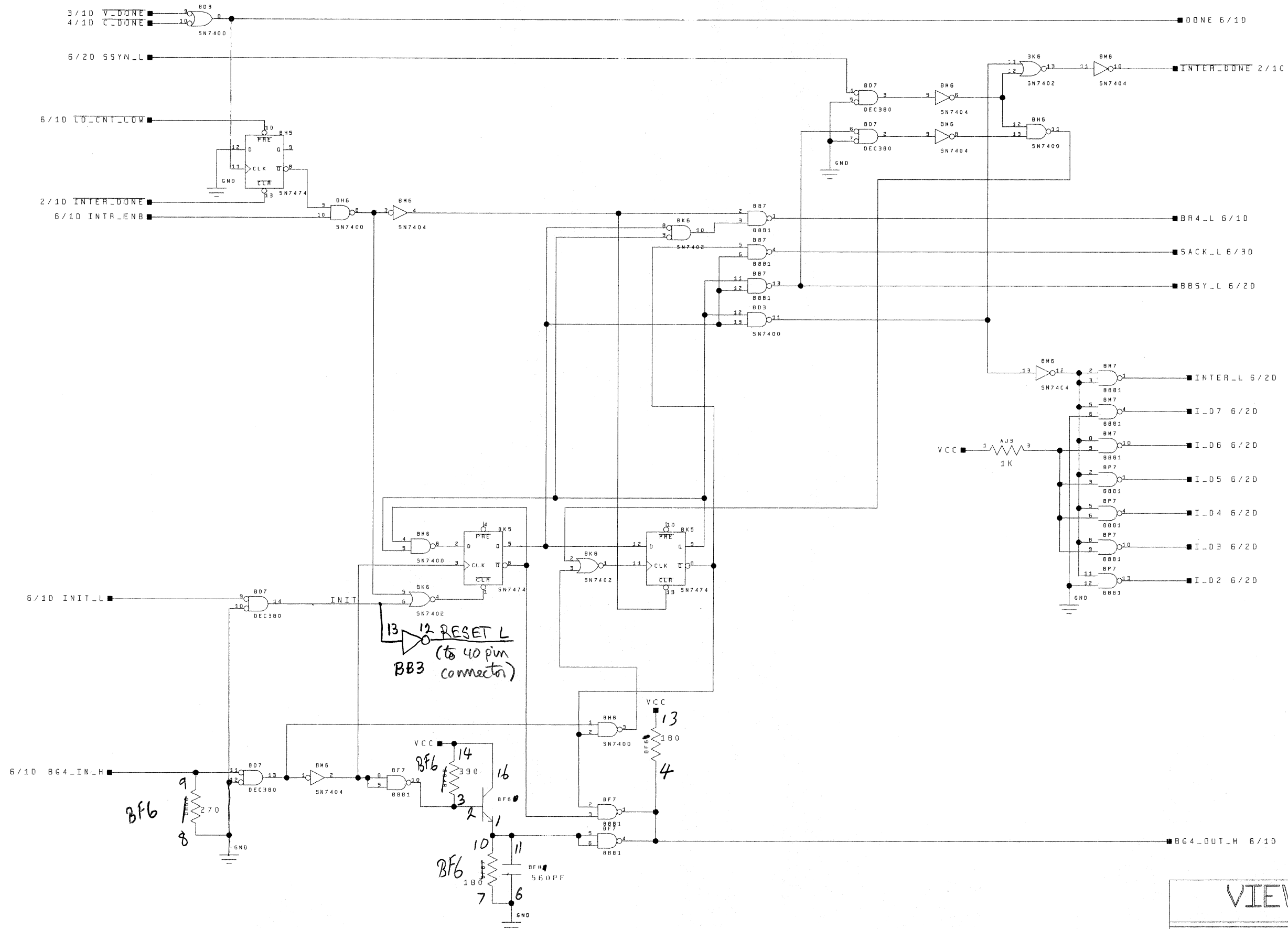




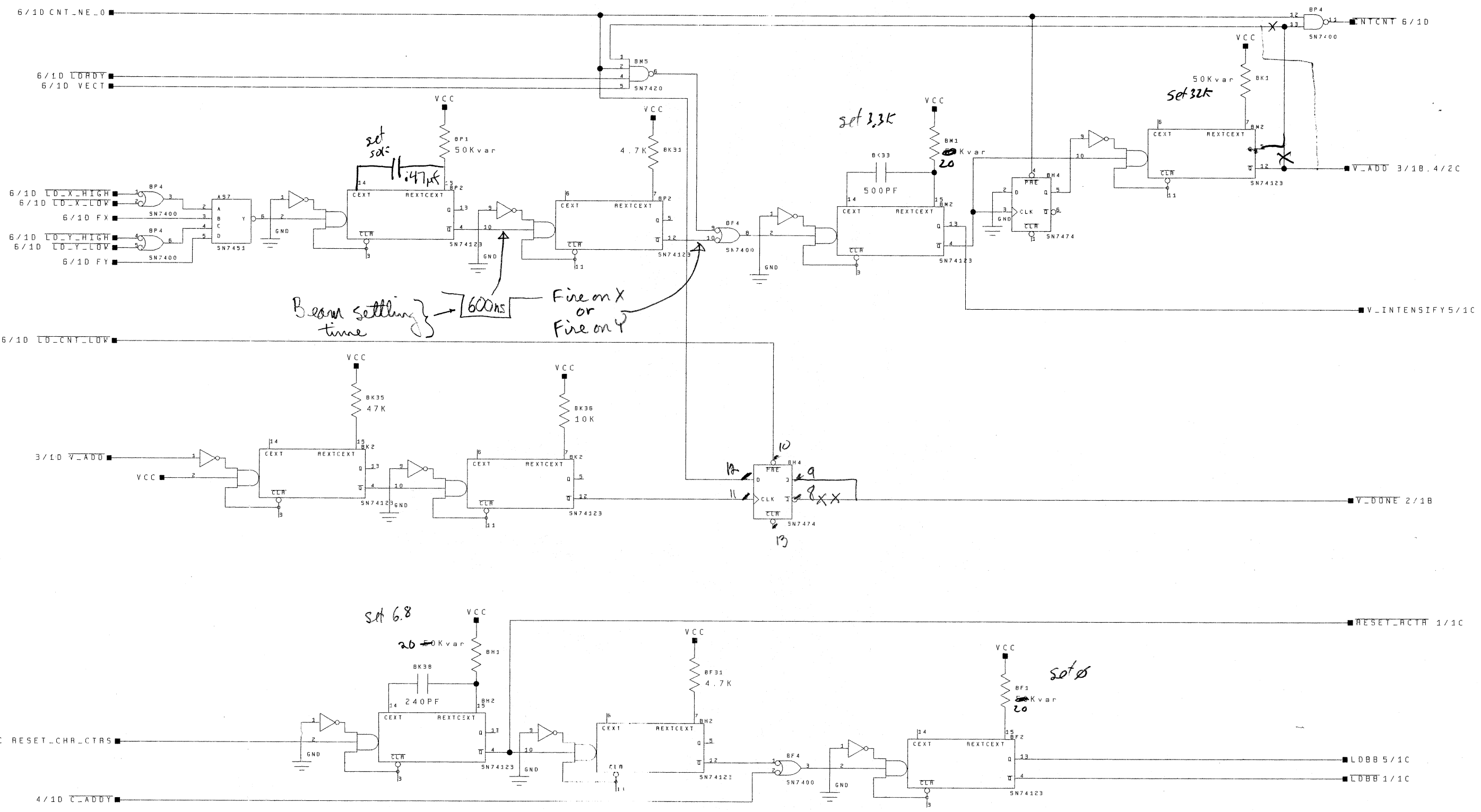
VIEWlogic

CHAR CTRL

ctrl ①



VIEWlogic  
 INTERRUPT LOGIC  
 CTL ②

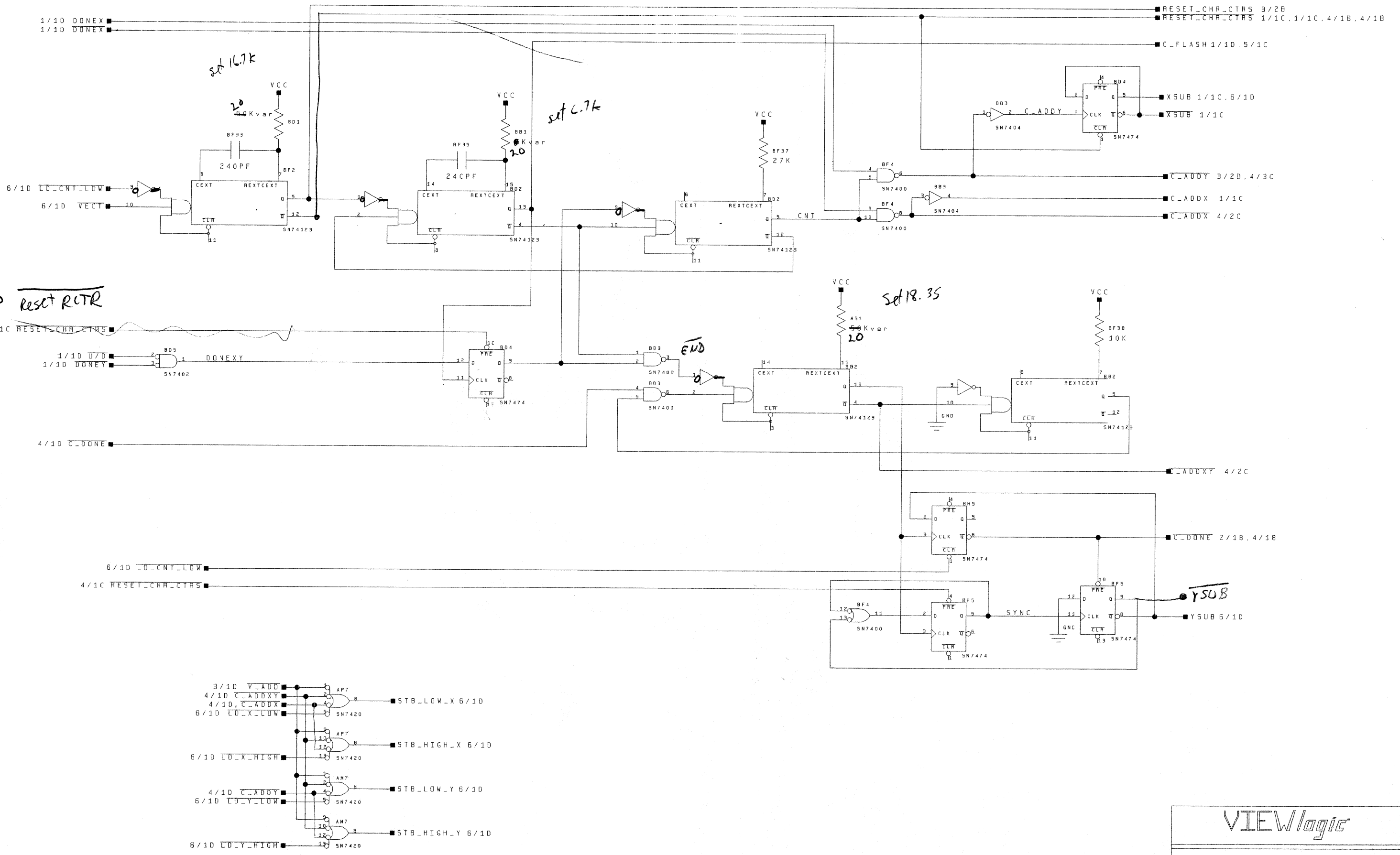


VIEWlogic

MAKE DOT, V\_DONE, RESET CHR CTRS

CTL (3)





3/30 reset RCTR

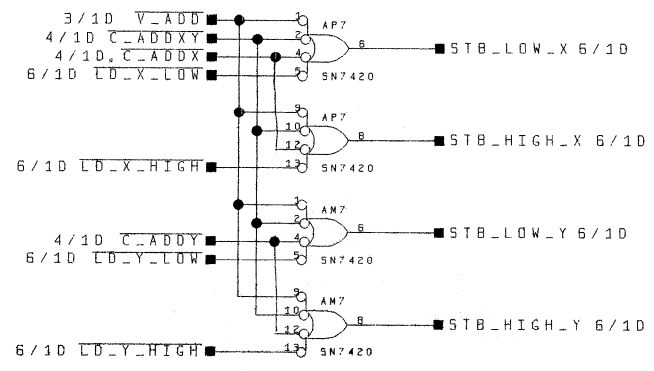
set 16.7k

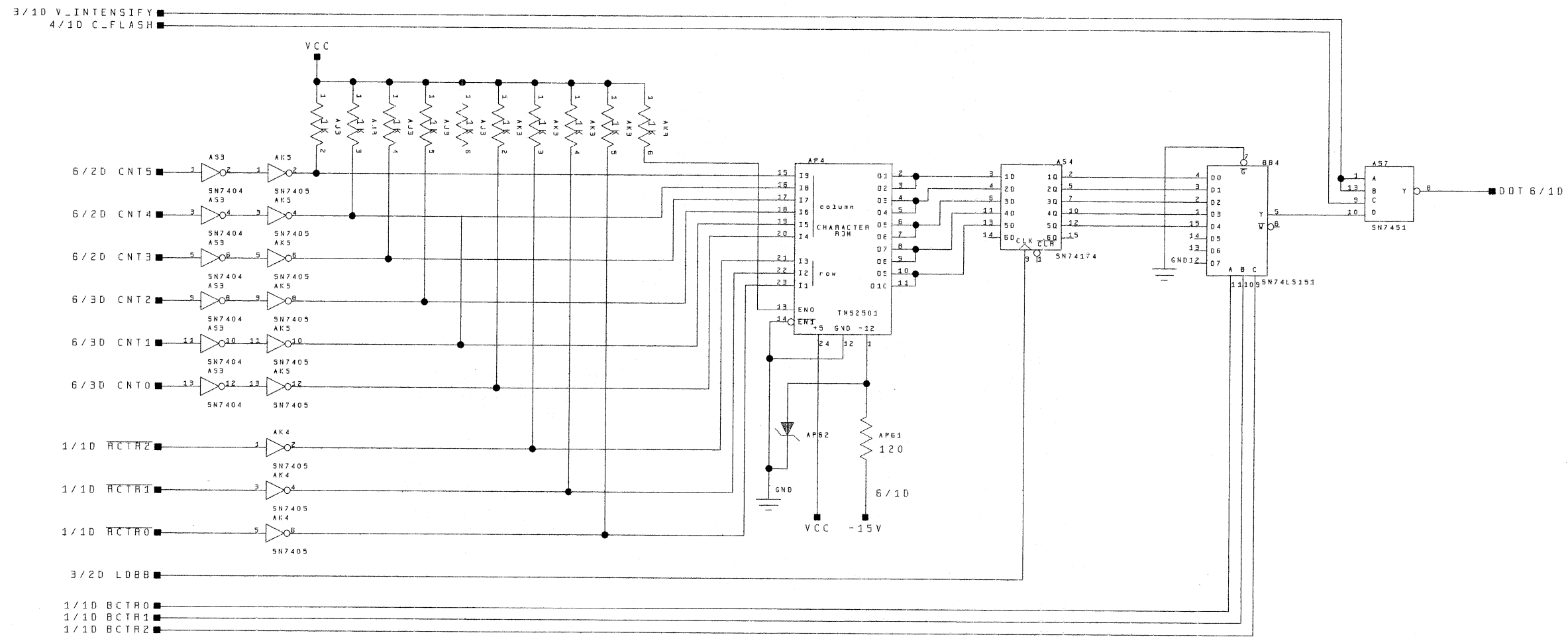
set 6.7k

set 18.35

END

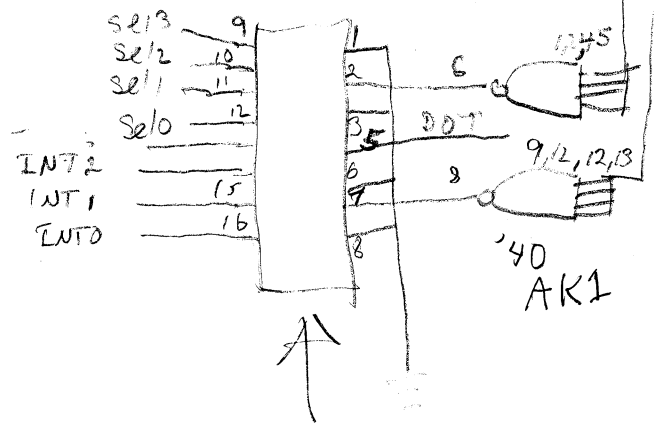
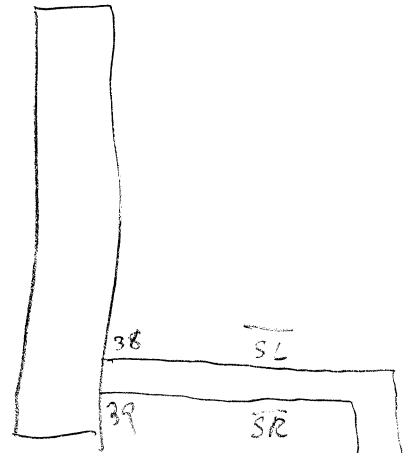
VIEWlogic  
 CHAR CTR CTRL  
 CTL 4



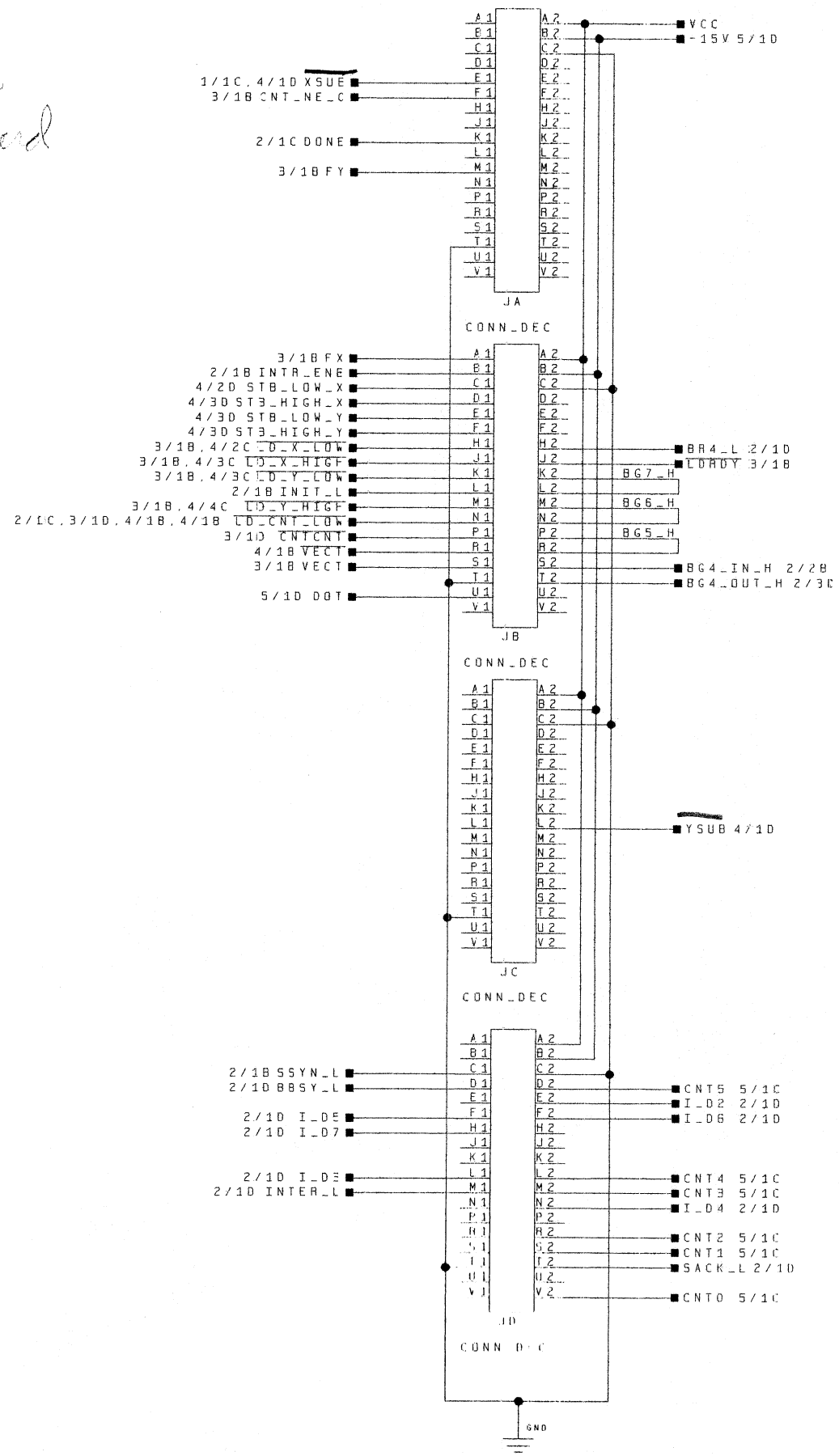


VIEWlogic  
 CHAR ROM  
 CTL 5

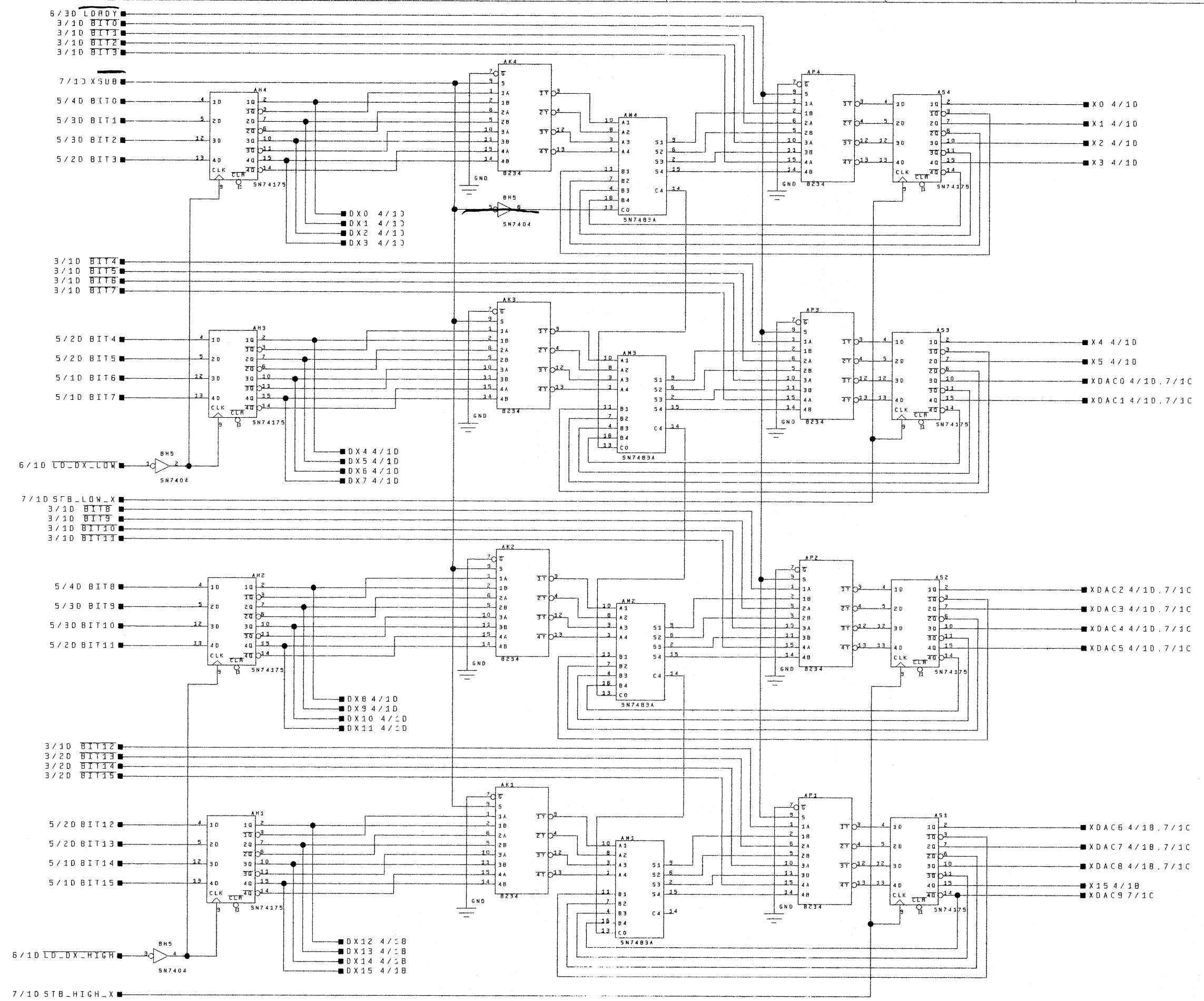
40 pin connector  
from Data Board



SR/SL  
16 Pin  
Connector



VIEWlogic  
CONNECTORS  
CTL 6

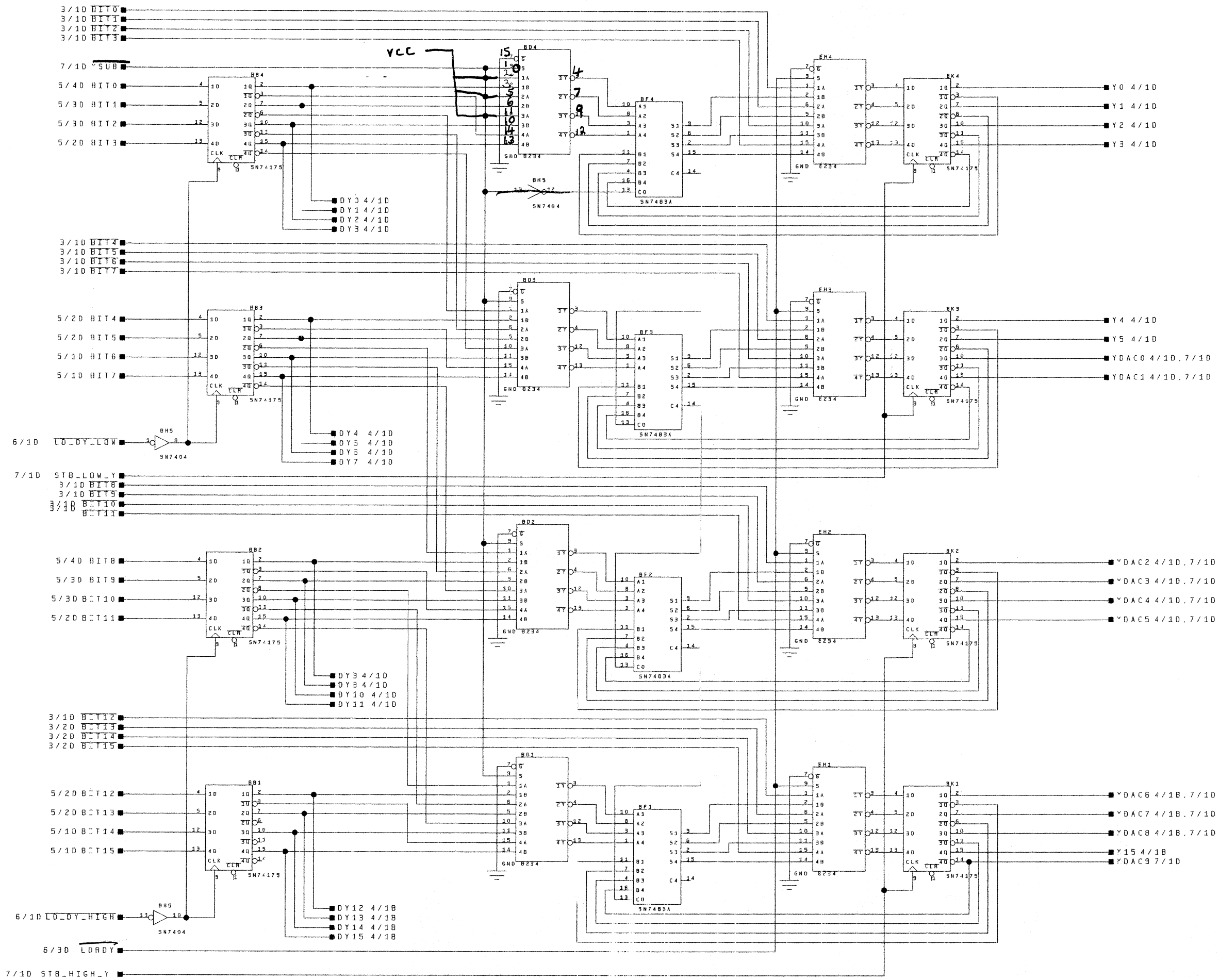


DX REG

X ADDR

X REG

VIEWlogic
XREG, DXREG, XADDR
Data ①

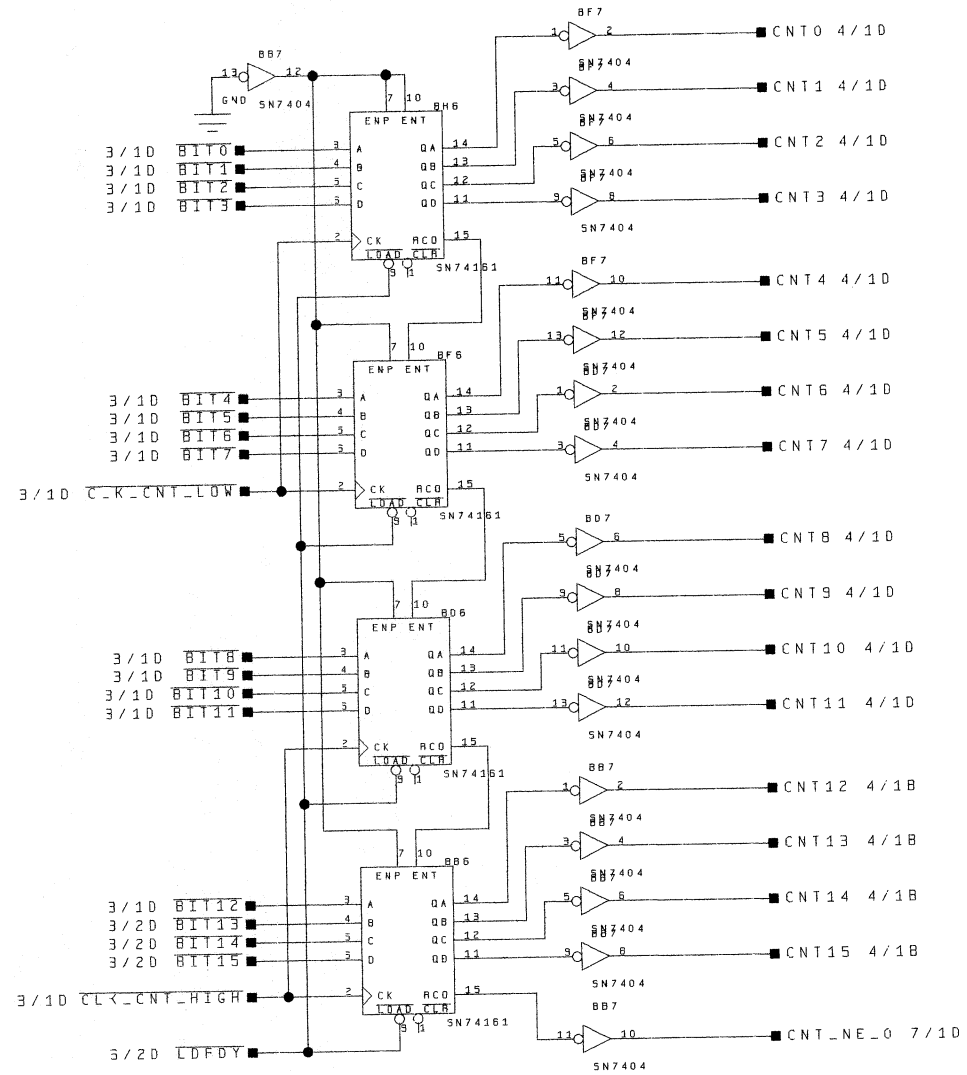
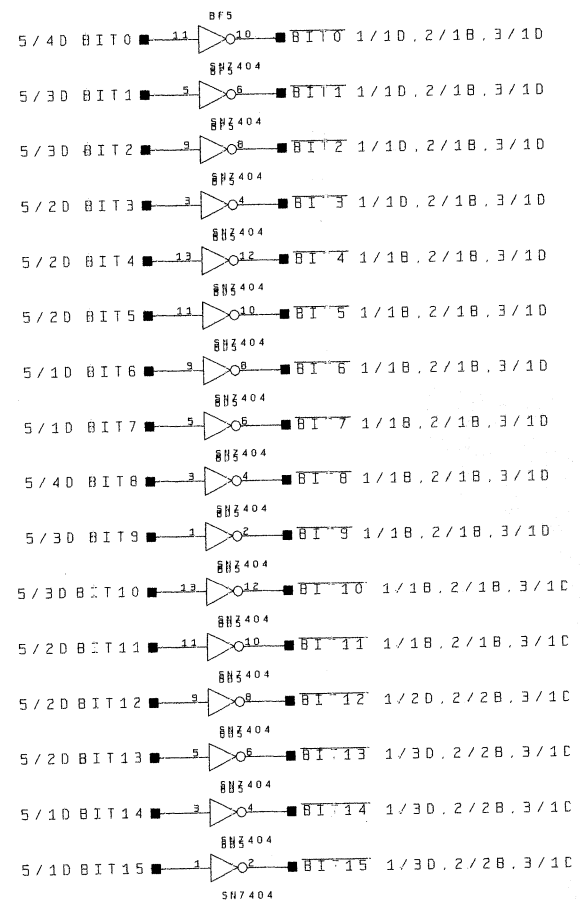
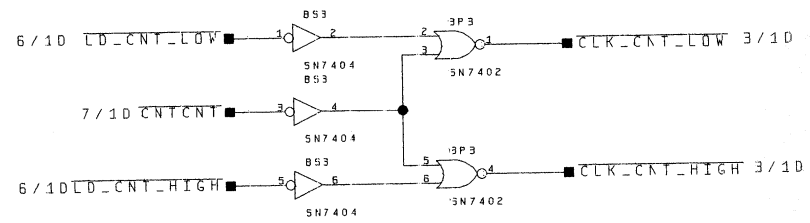


VIEWlogic  
 YREG, DYREG, YADDR  
 Data ②

DY REG

Y ADDR

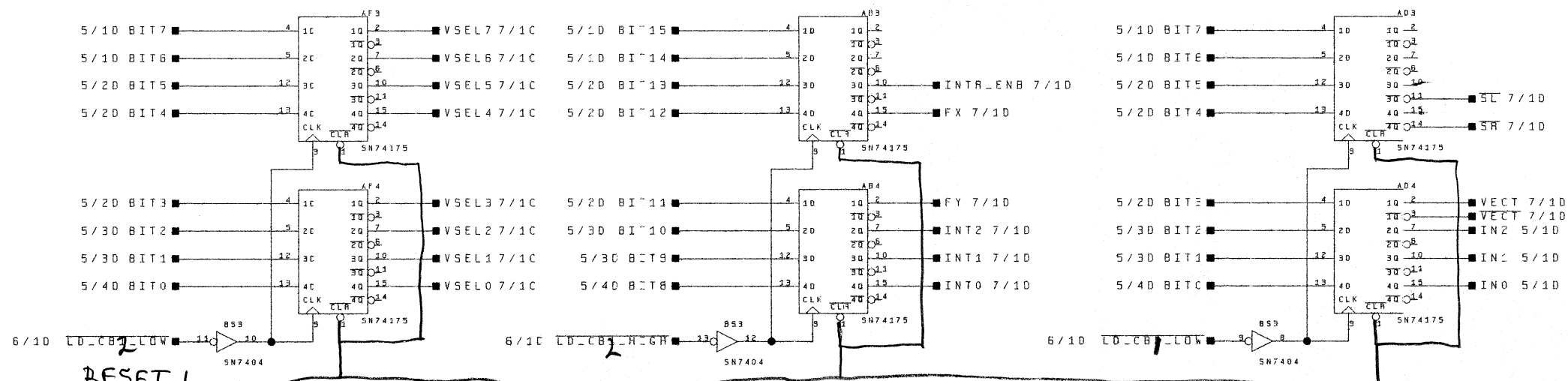
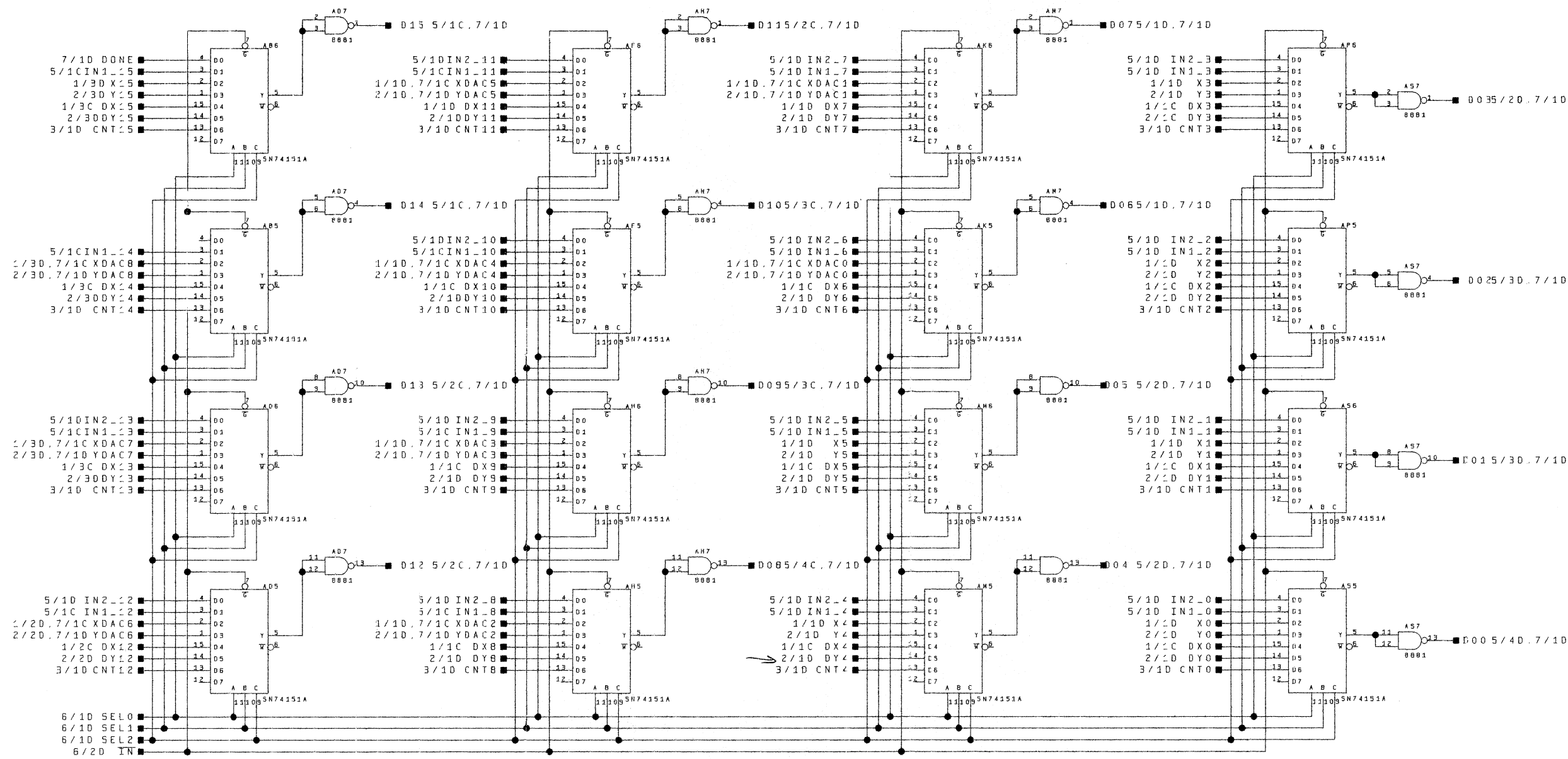
Y REG



VIEWlogic

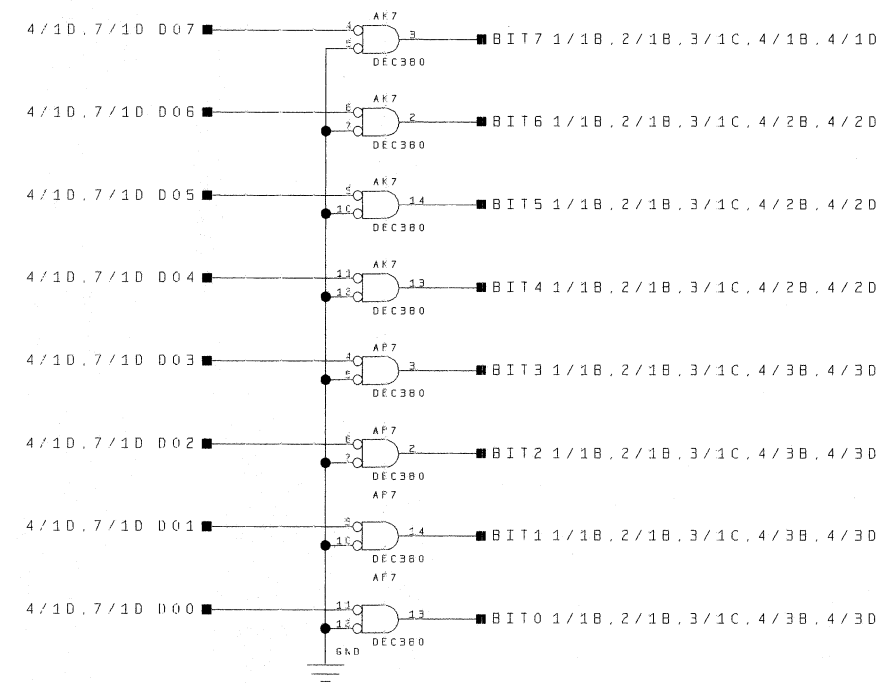
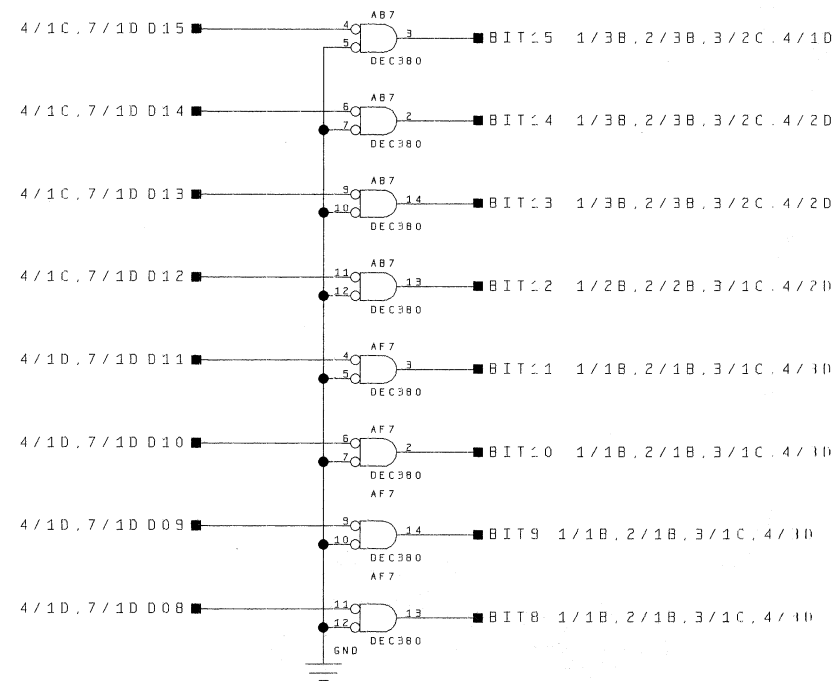
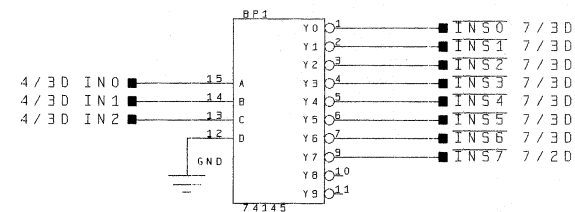
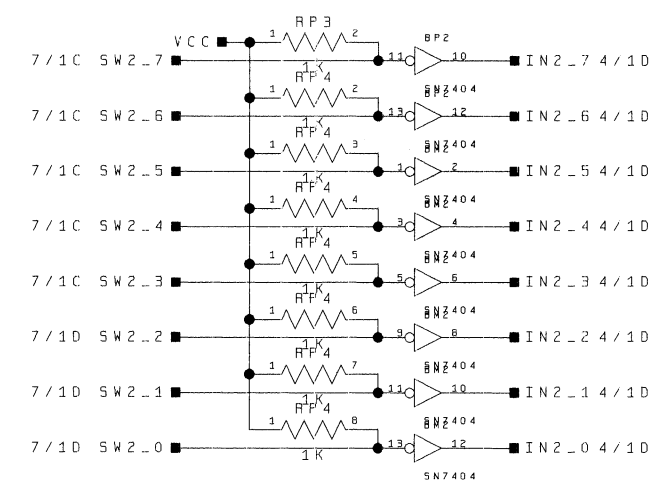
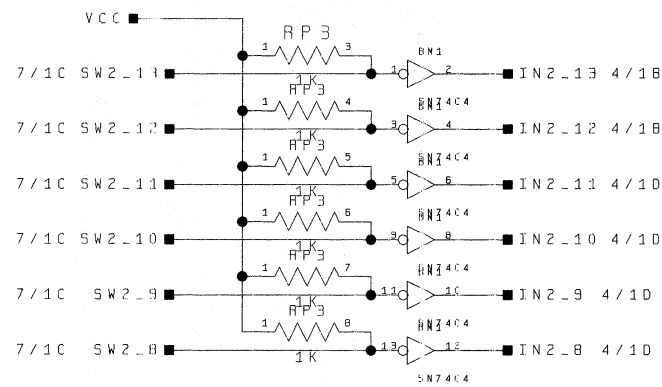
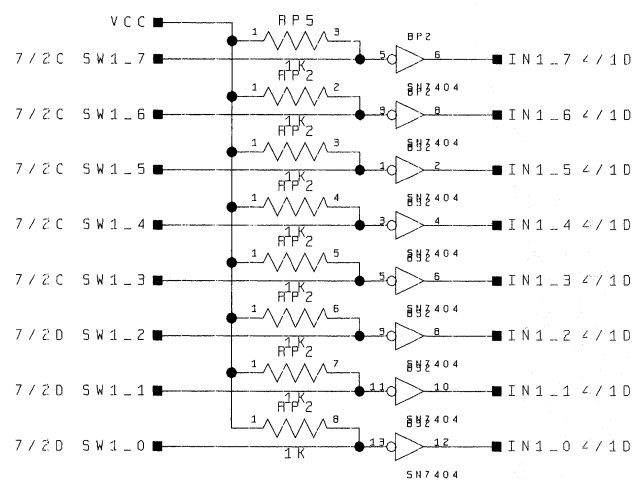
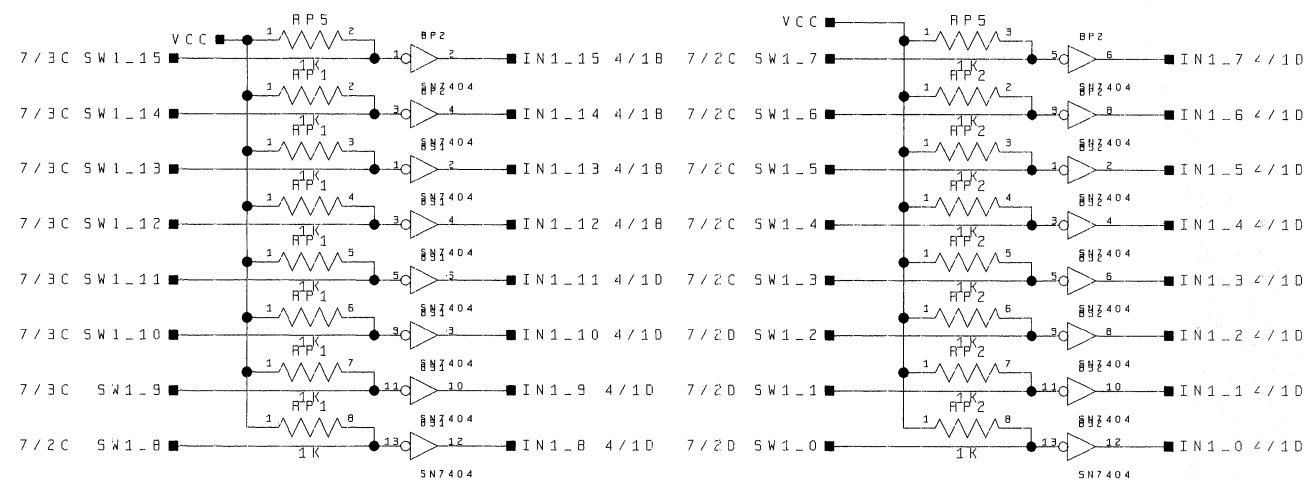
CNT REG

Data 3



RESET L  
(from 40 pin connector)

VIEWlogic  
READ REGS & CBI, 2 REGS  
Data 0

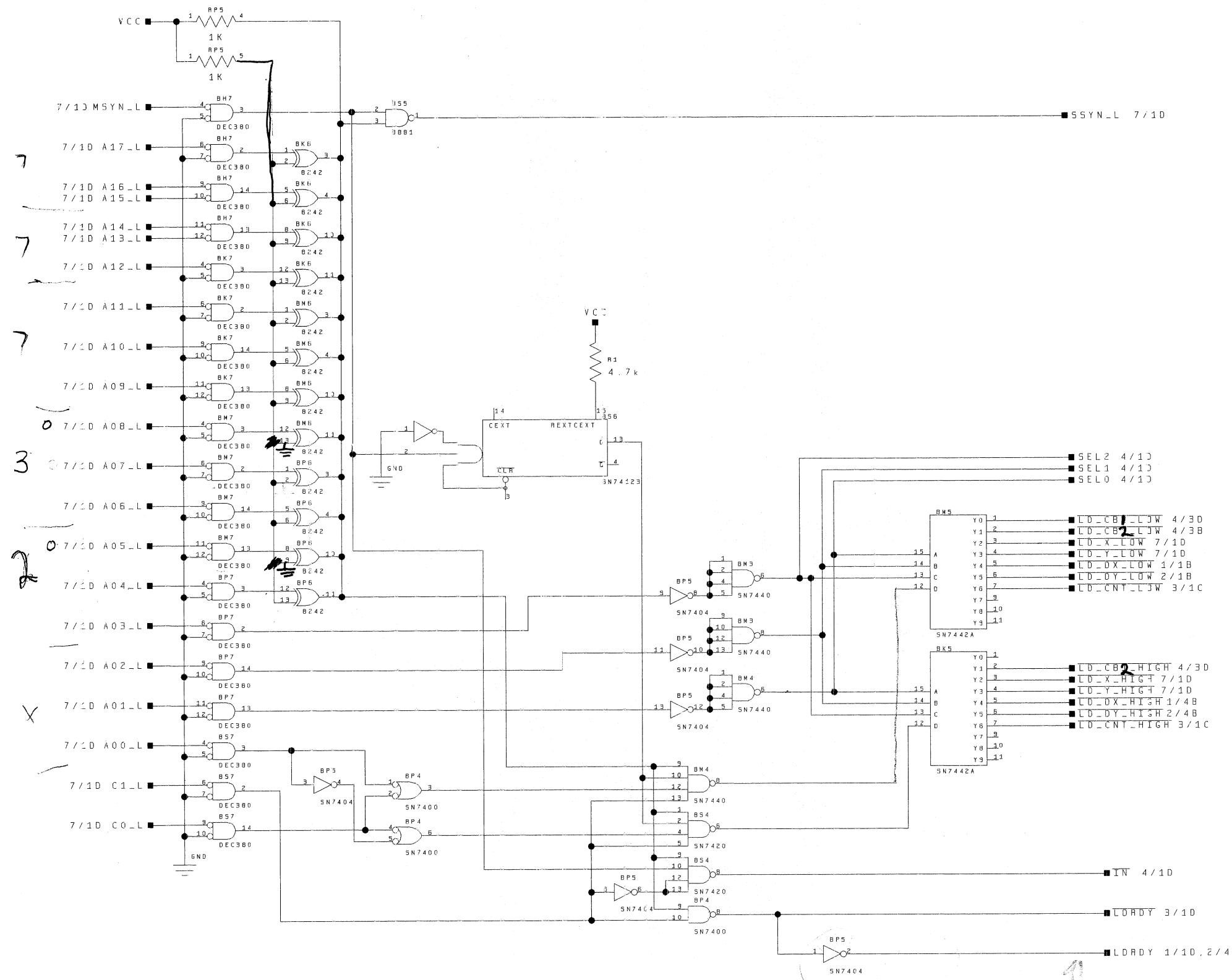


VIEWlogic

SWITCHES, UNIBUS DATA RECVRS

Data 5

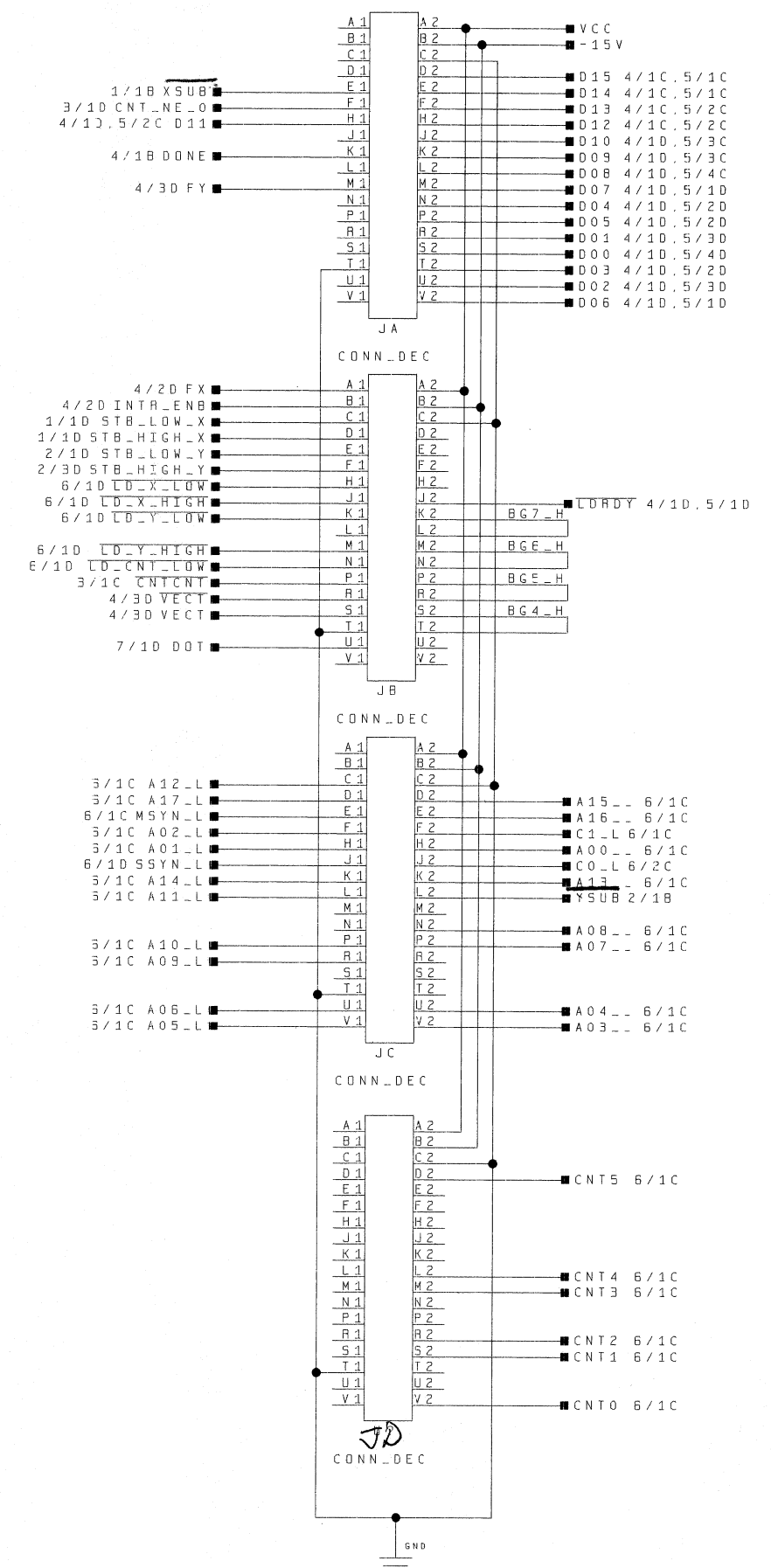
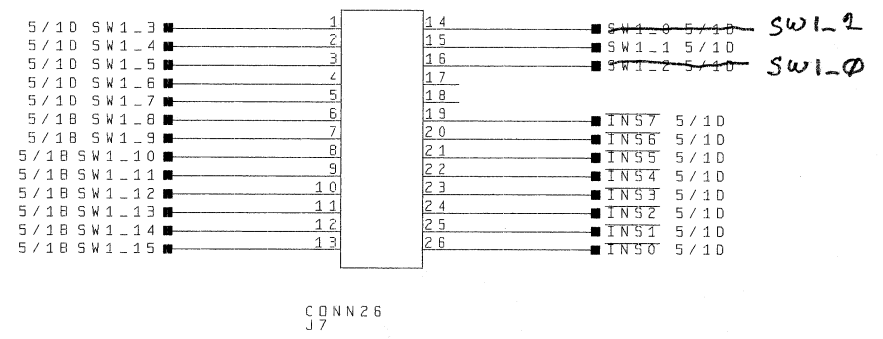
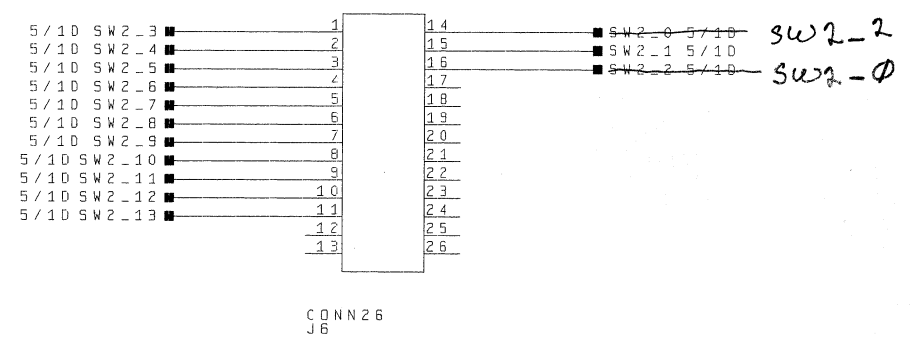
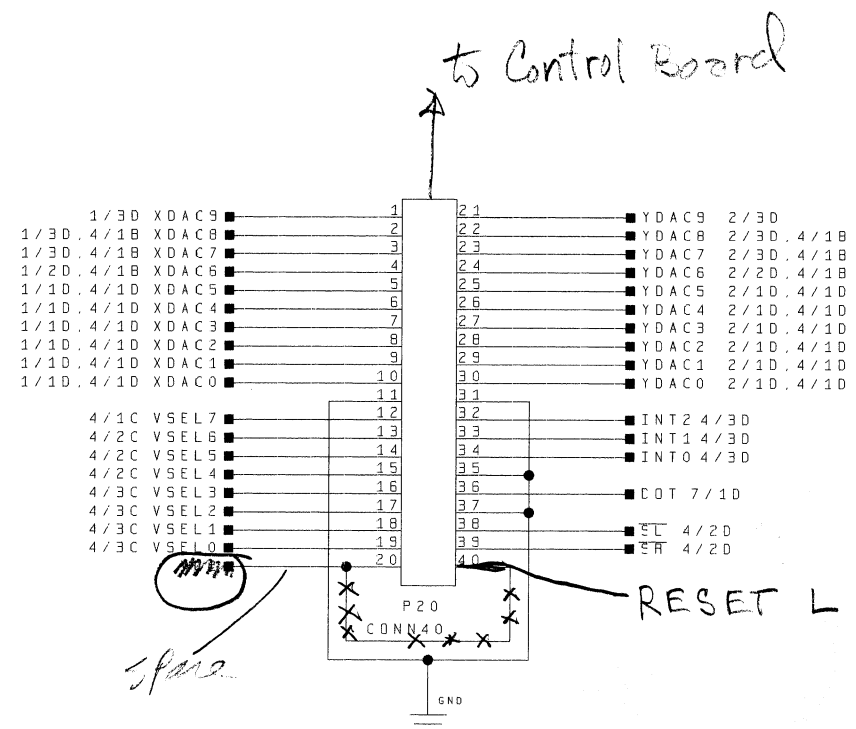




7  
7  
7  
7  
0  
3  
2  
X

↑  
not used

VIEWlogic
ADDR DECODE
Data 6



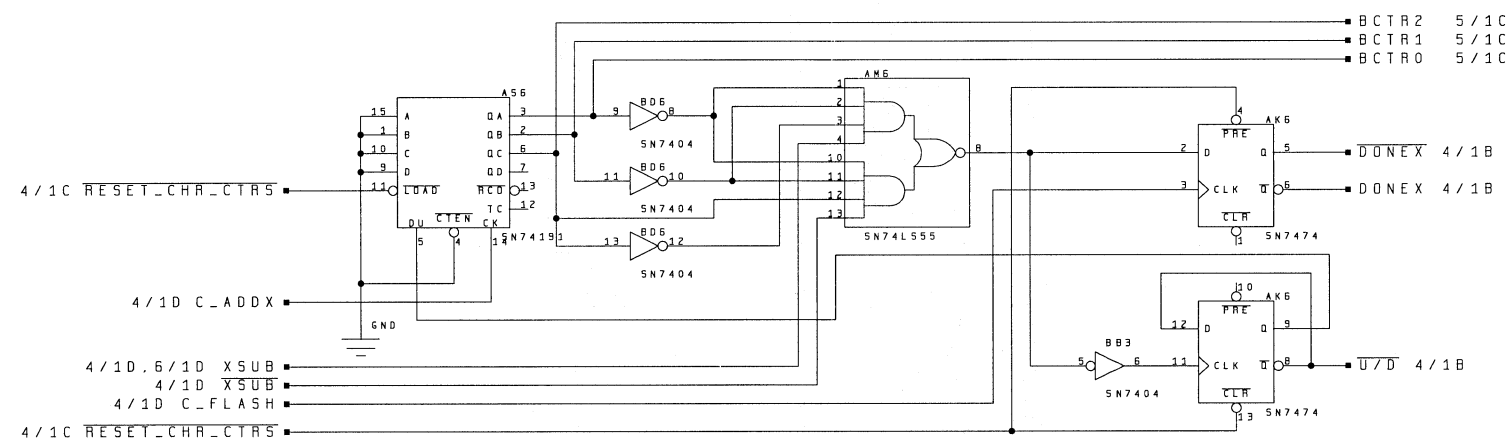
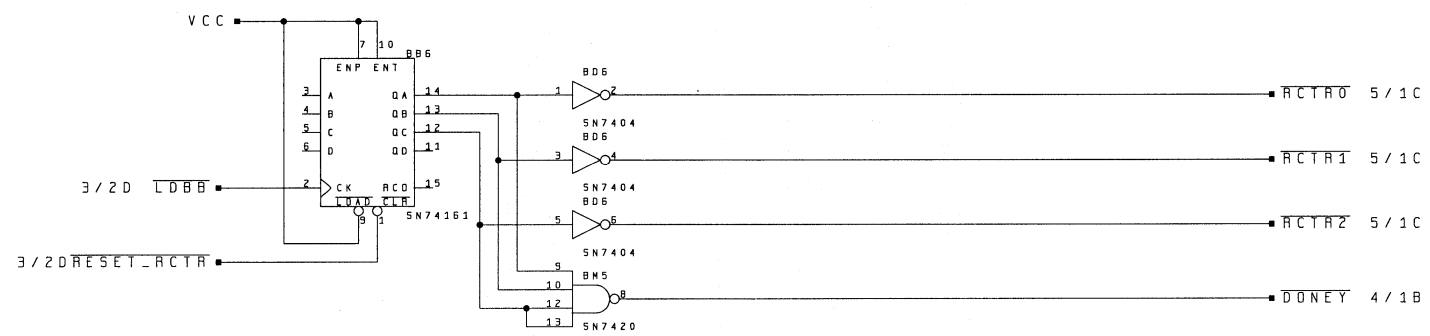
VIEWlogic

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CONNECTORS

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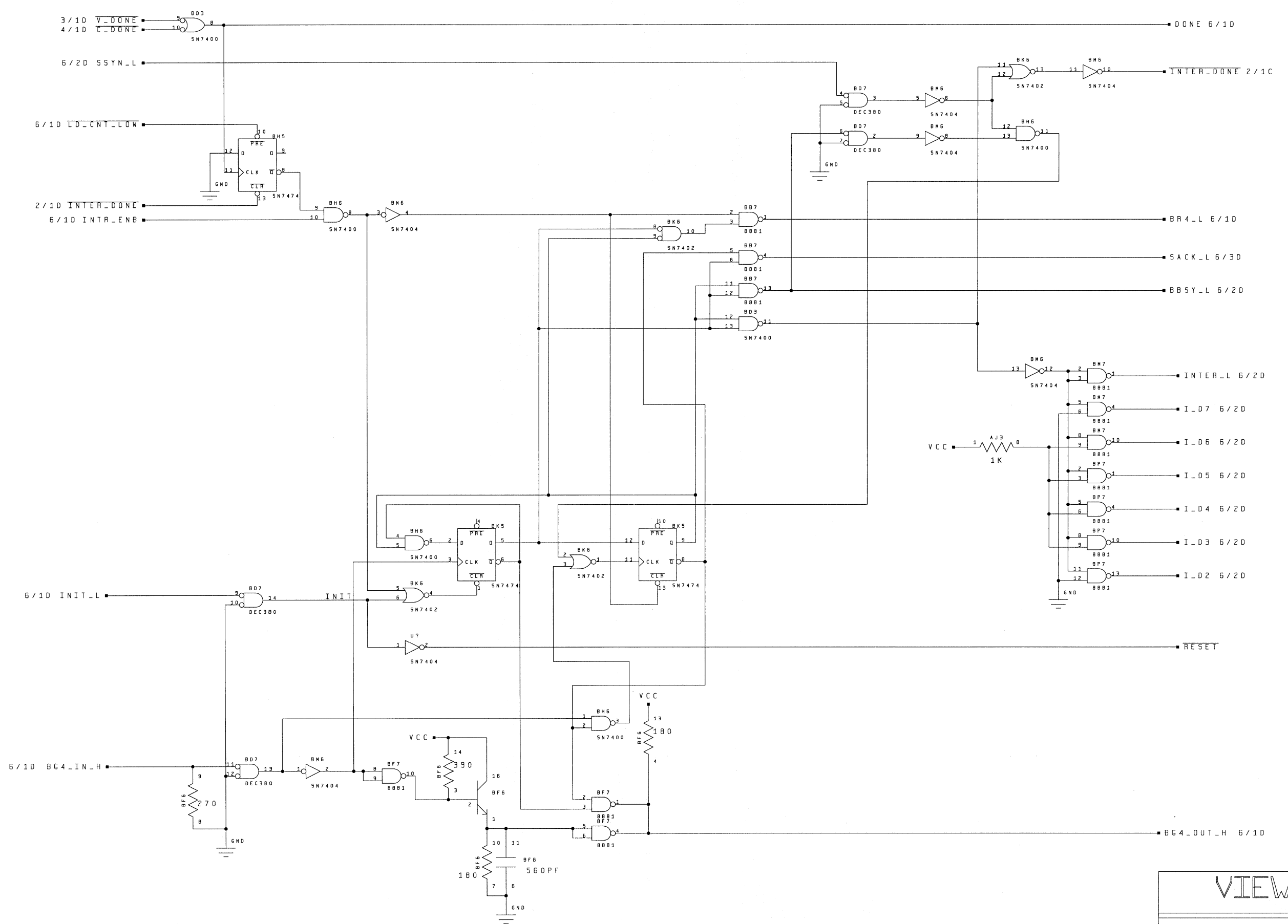
Data 7



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
CONTROL BOARD, SHEET 1

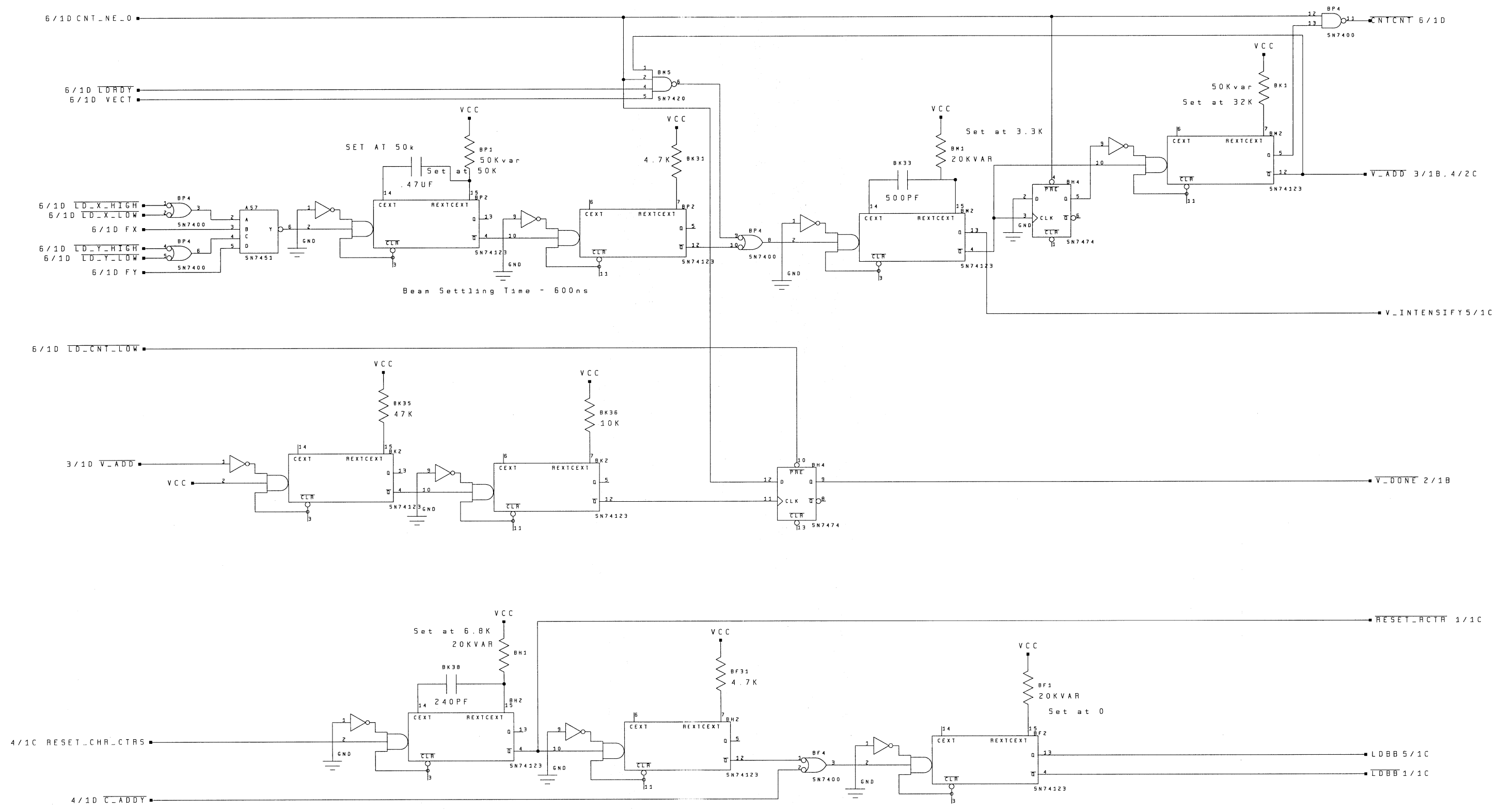
CHARACTER CONTROL

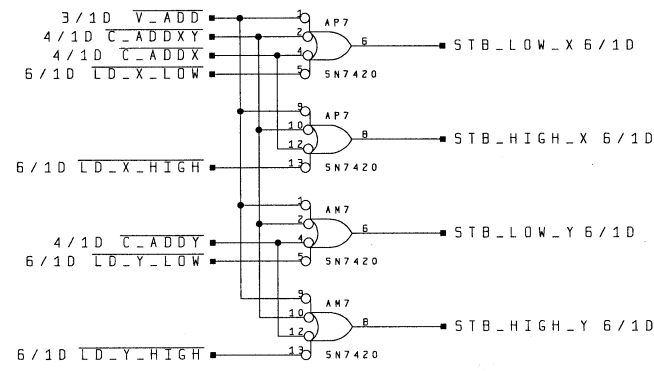
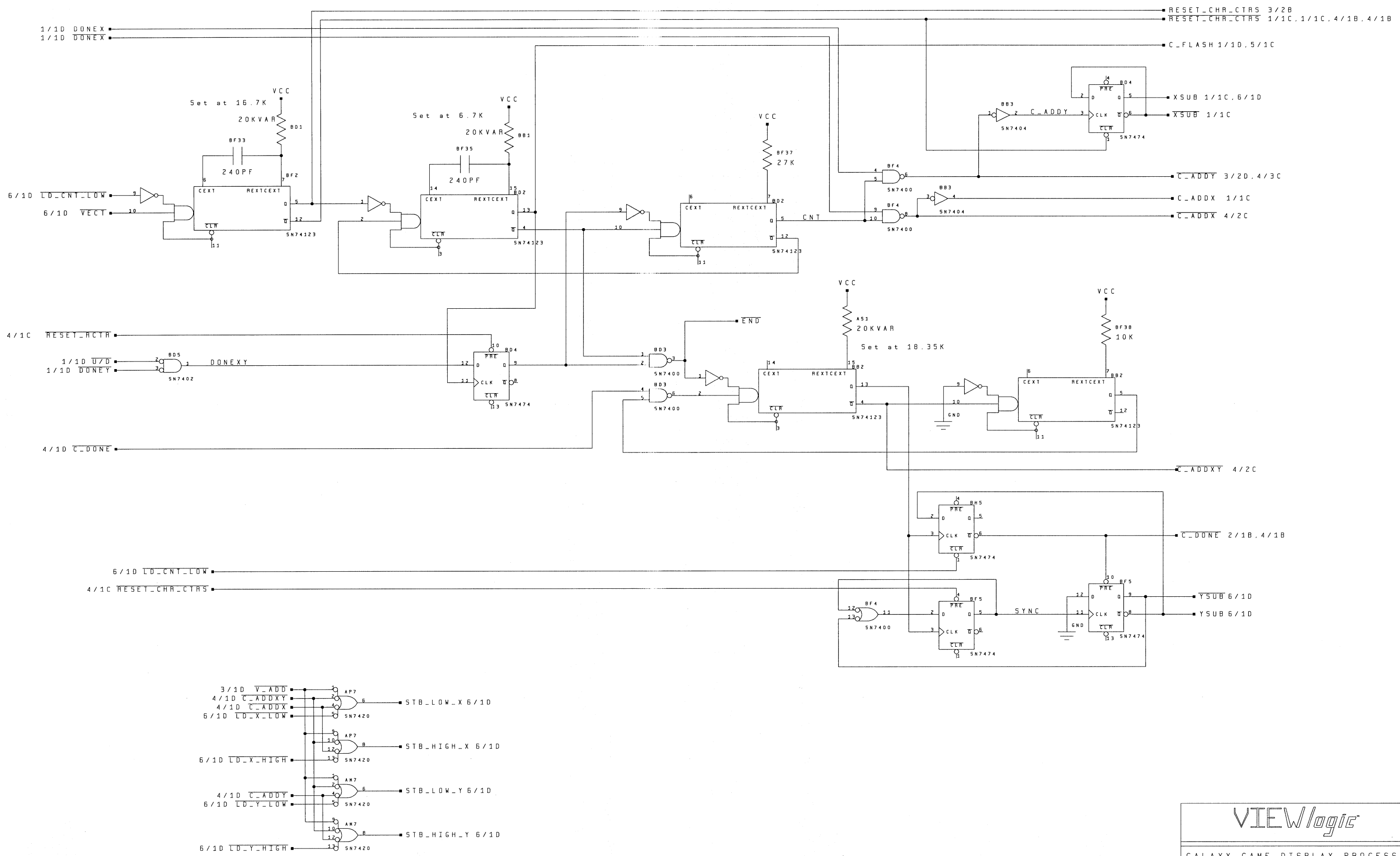


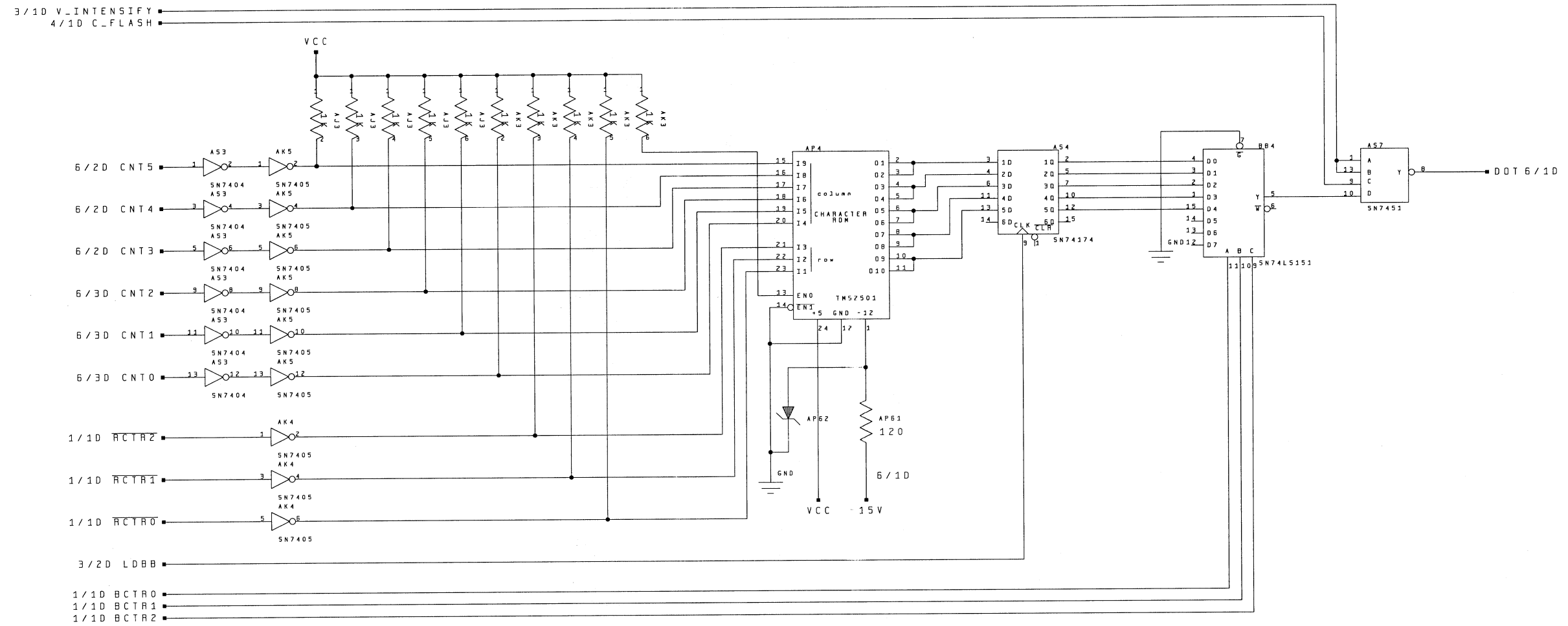
VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
CONTROL BOARD, SHEET 2

INTERRUPT LOGIC



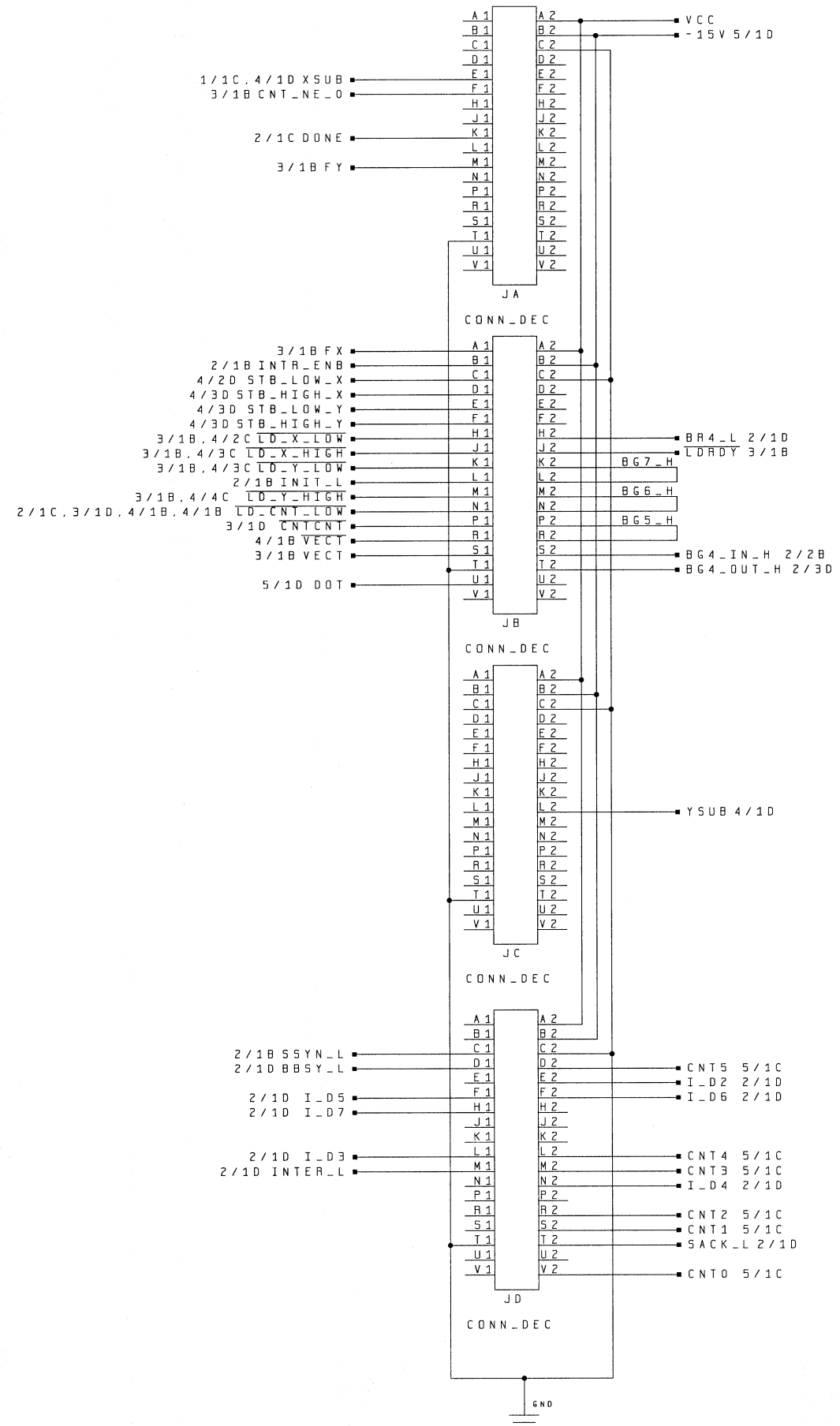
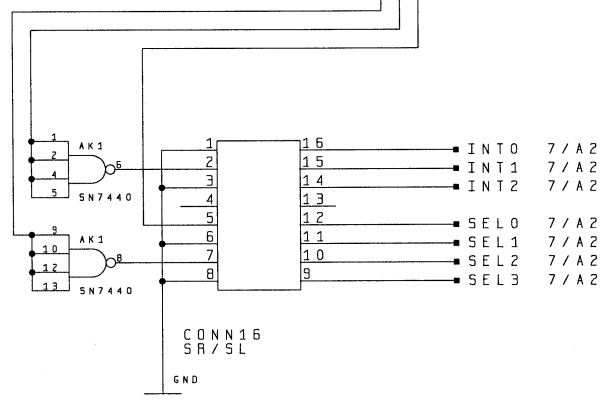
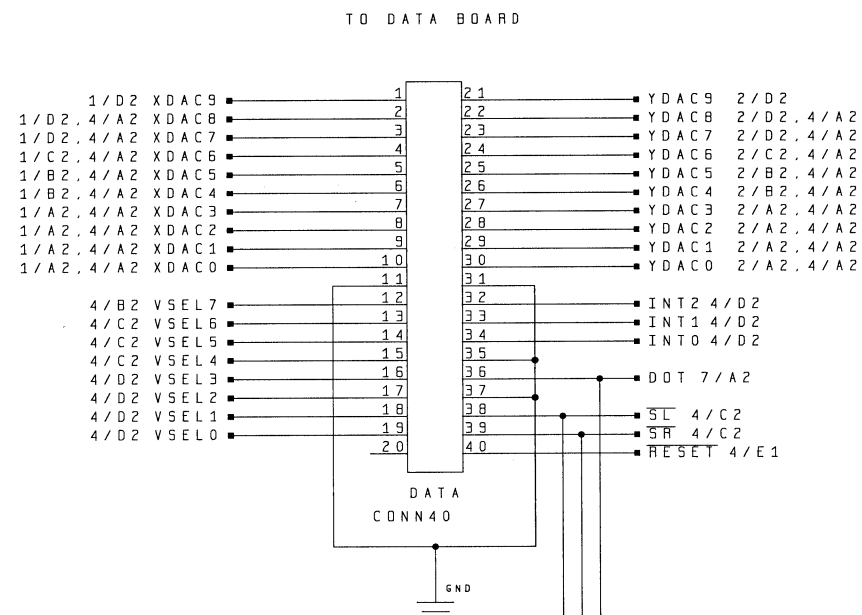




VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
CONTROL BOARD, SHEET 5

CHARACTER ROM



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
 CONTROL BOARD, SHEET 5

CONNECTORS



6/C2.7/A2 LDRDY  
 3/A2 BIT0  
 3/A2 BIT1  
 3/A2 BIT2  
 3/A2 BIT3

7/A2 XSUB  
 5/E2 BIT0  
 5/D2 BIT1  
 5/D2 BIT2  
 5/C2 BIT3

3/A2 BIT4  
 3/A2 BIT5  
 3/A2 BIT6  
 3/A2 BIT7

5/C2 BIT4  
 5/C2 BIT5  
 5/B2 BIT6  
 5/B2 BIT7

6/A2 LD\_DX\_LOW

7/A2 STB\_LOW\_X  
 3/A2 BIT8  
 3/B2 BIT9  
 3/B2 BIT10  
 3/B2 BIT11

5/E2 BIT8  
 5/D2 BIT9  
 5/D2 BIT10  
 5/C2 BIT11

3/B2 BIT12  
 3/C2 BIT13  
 3/C2 BIT14  
 3/C2 BIT15

5/C2 BIT12  
 5/C2 BIT13  
 5/B2 BIT14  
 5/B2 BIT15

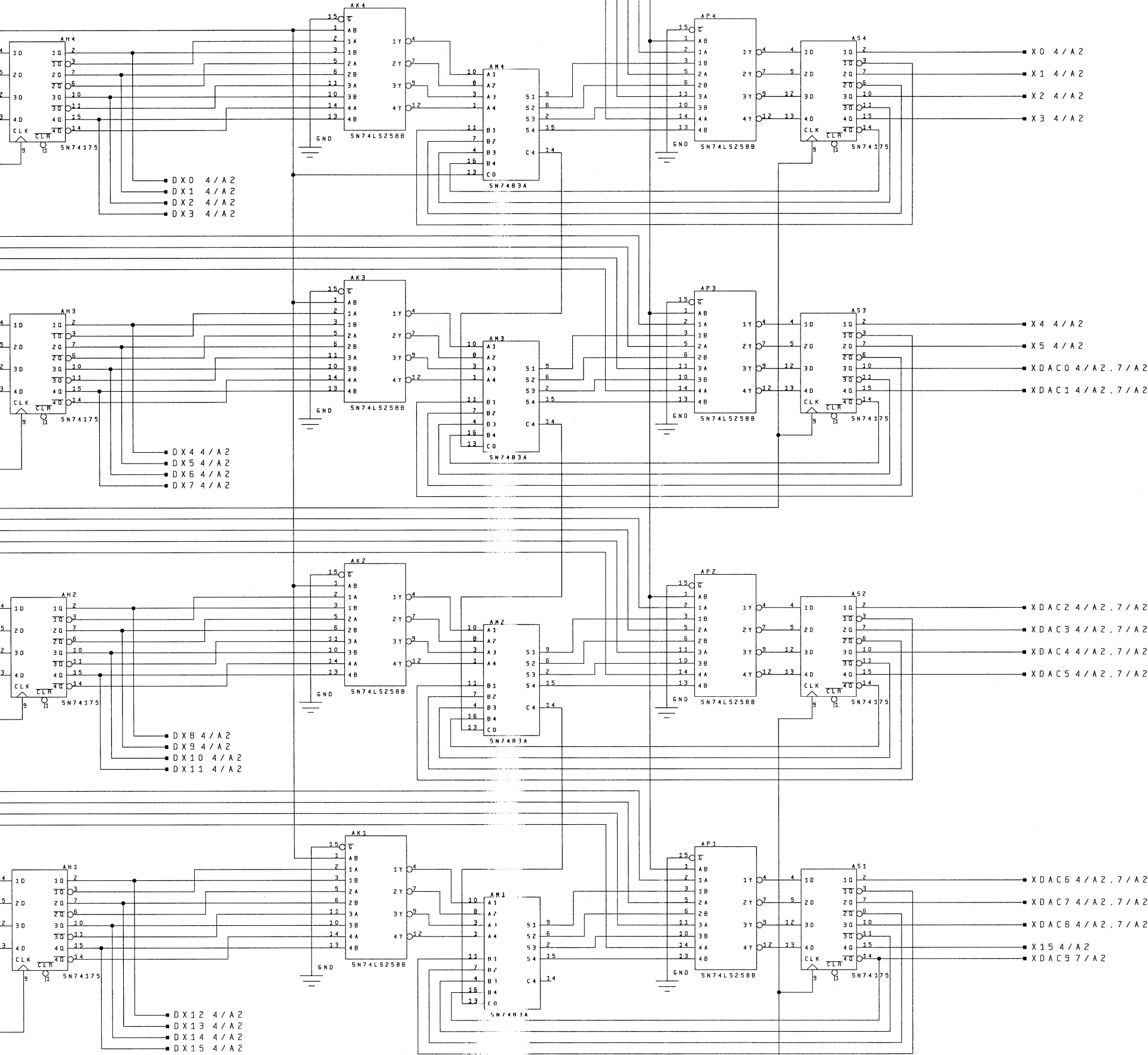
6/B2 LD\_DX\_HIGH

7/A2 STB\_HIGH\_X

DX REG

X ADDIH

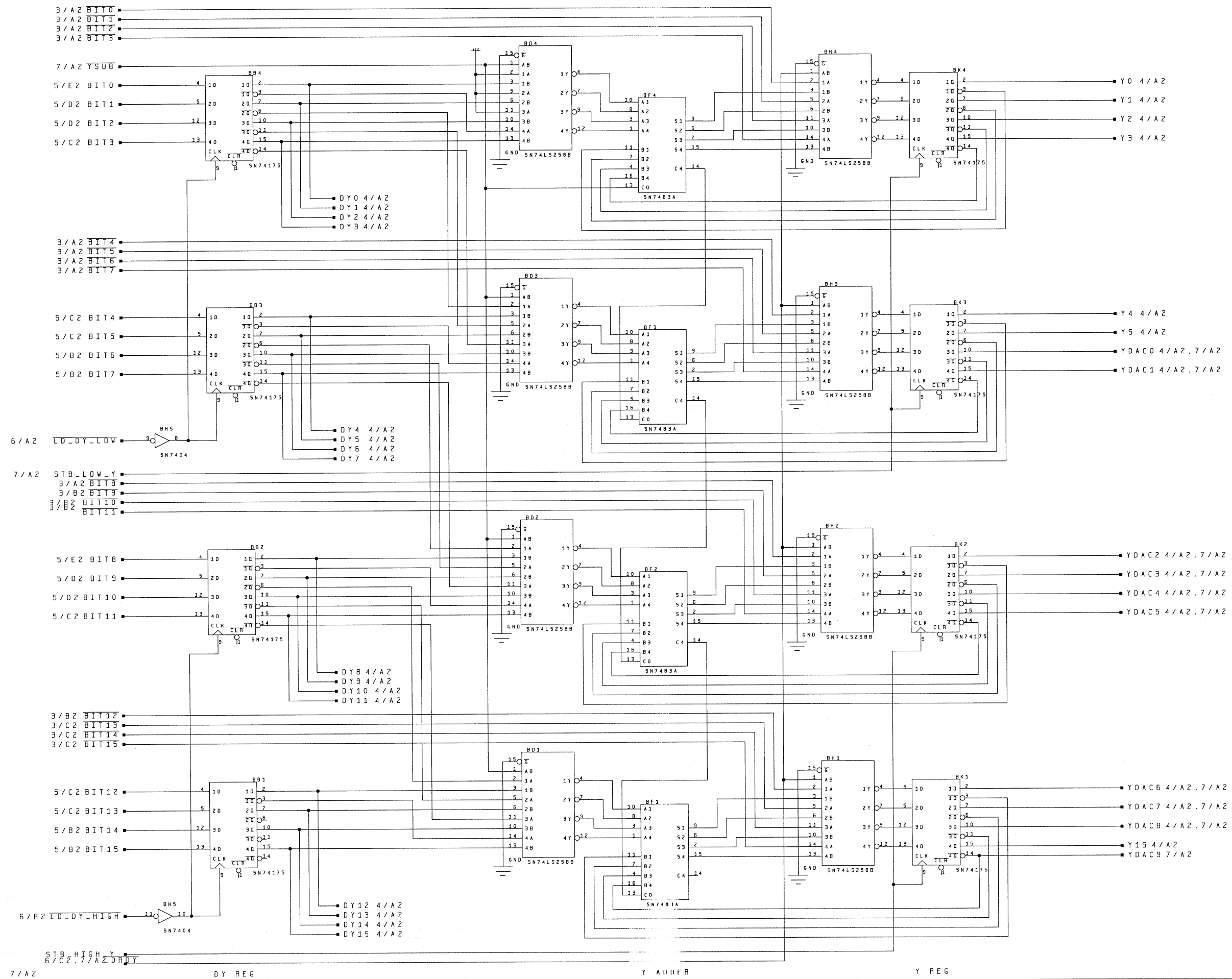
X REG



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
 DATA BOARD, SHEET 1

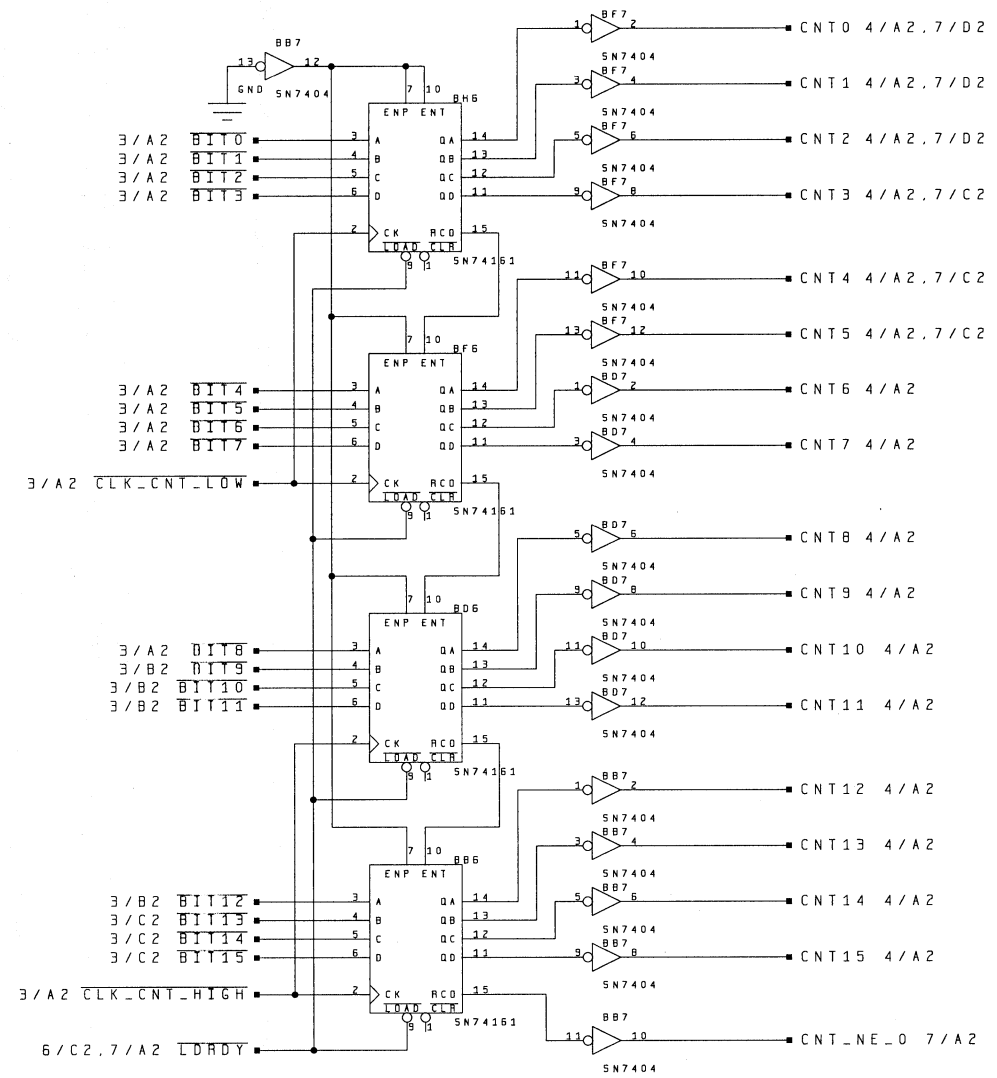
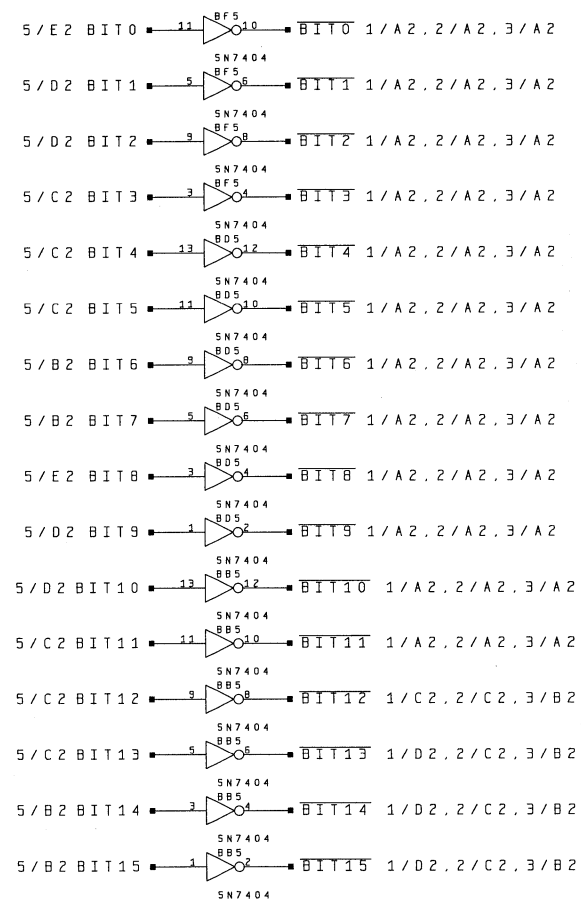
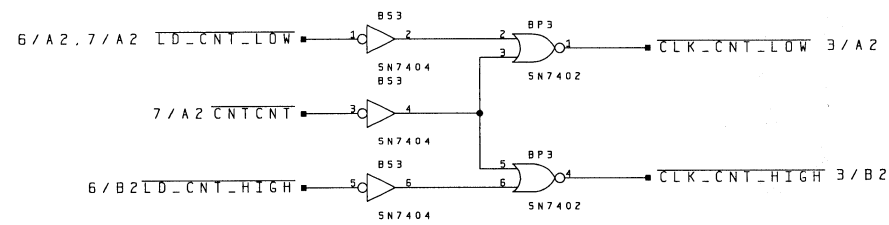
X REG, DX REG, X ADDER



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 2

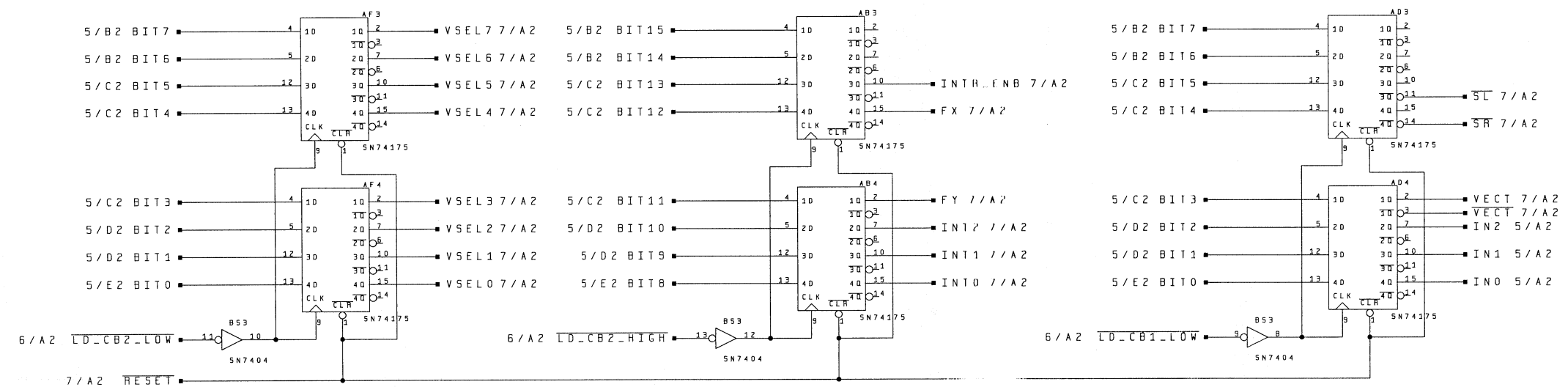
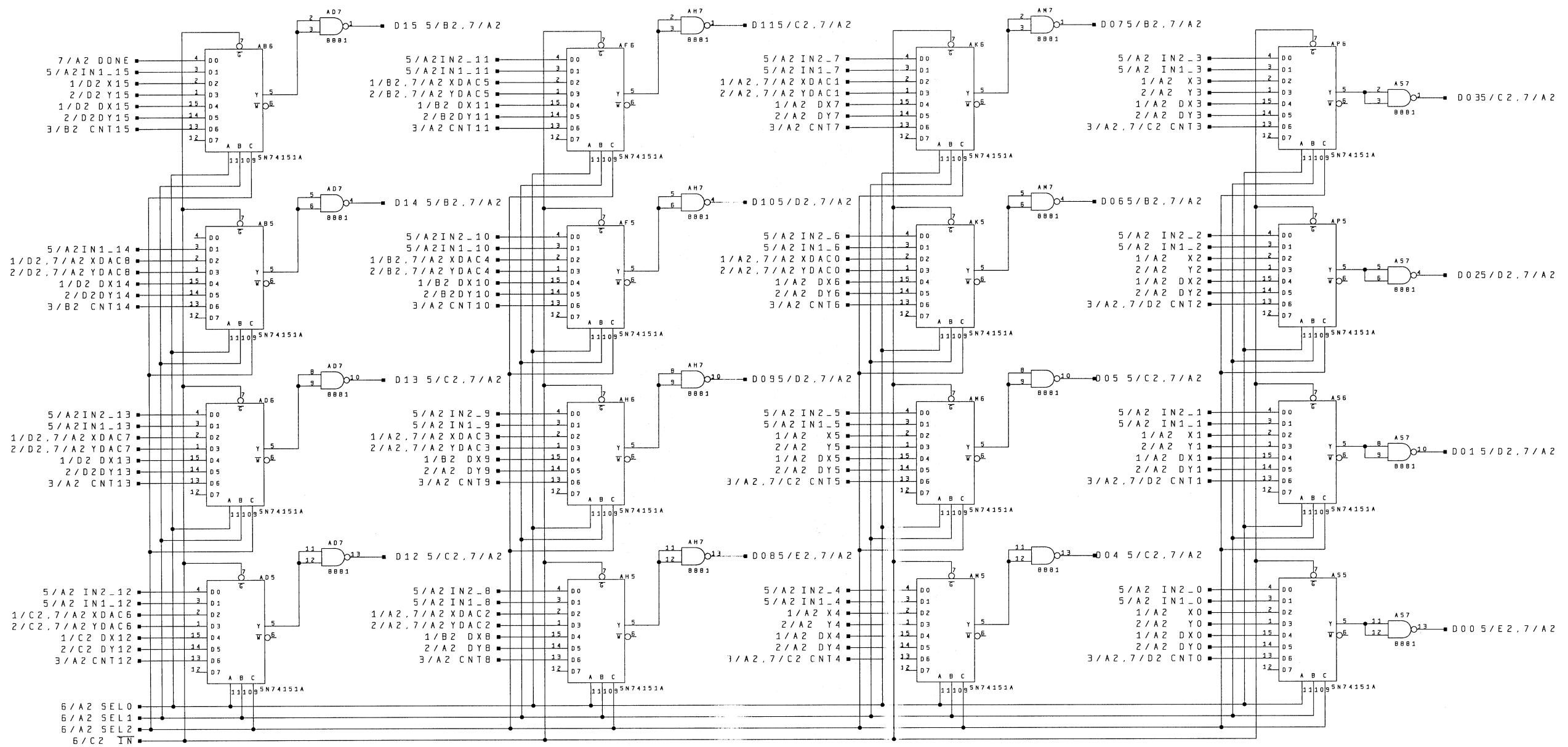
X REG, DX REG, X ADDER



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 3

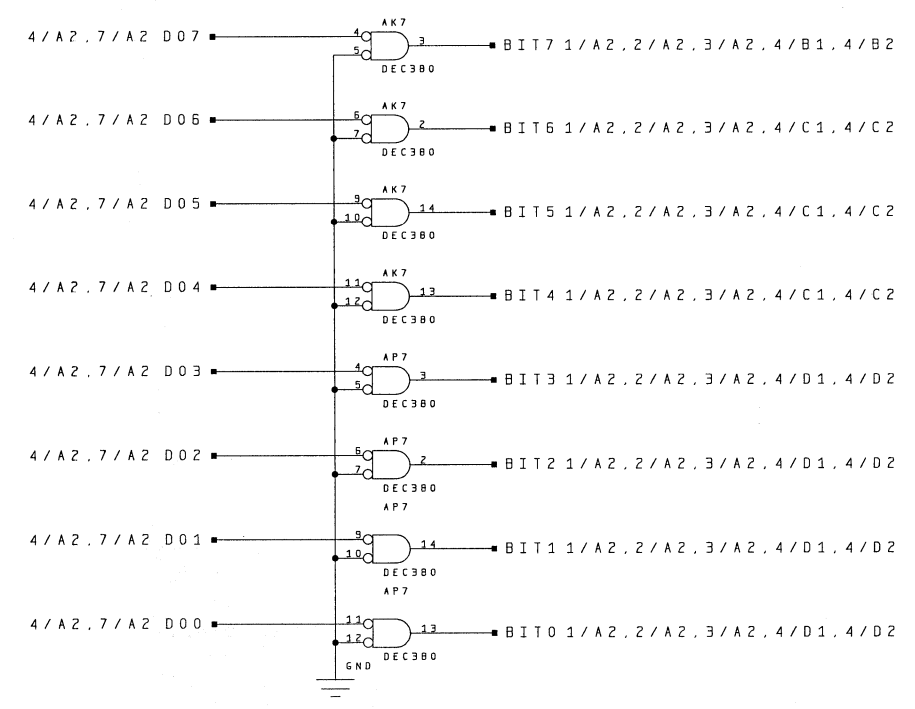
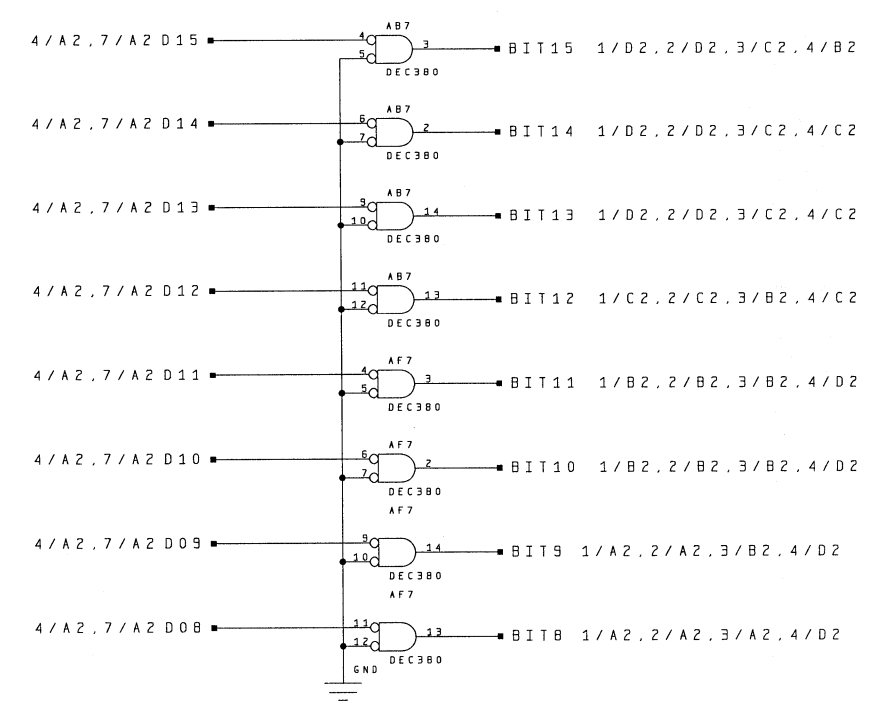
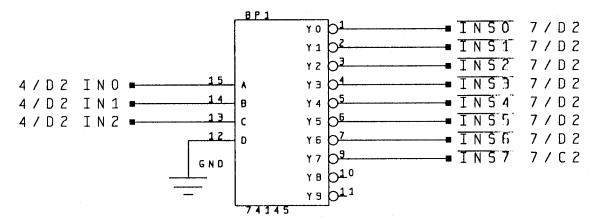
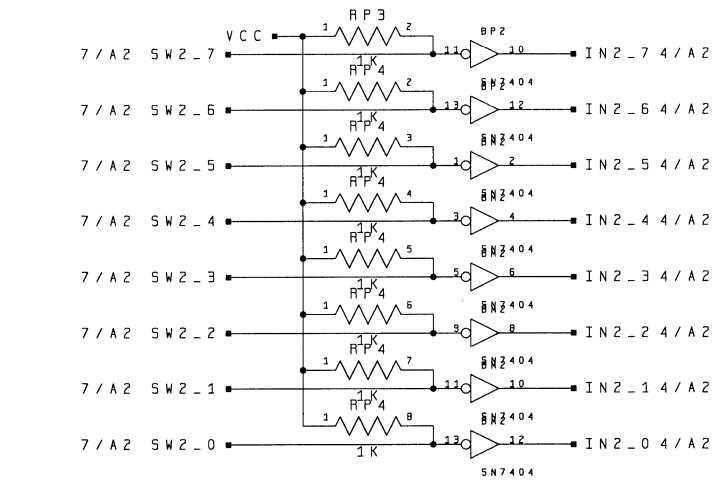
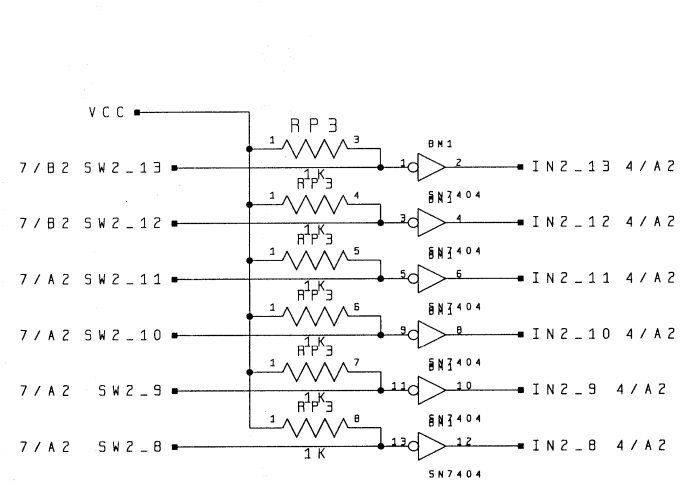
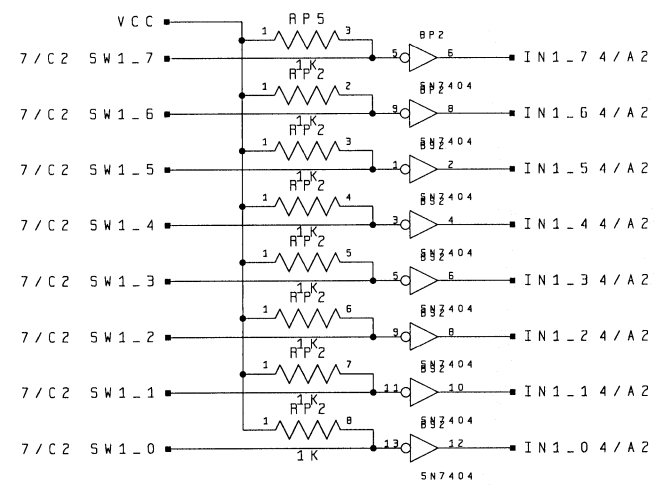
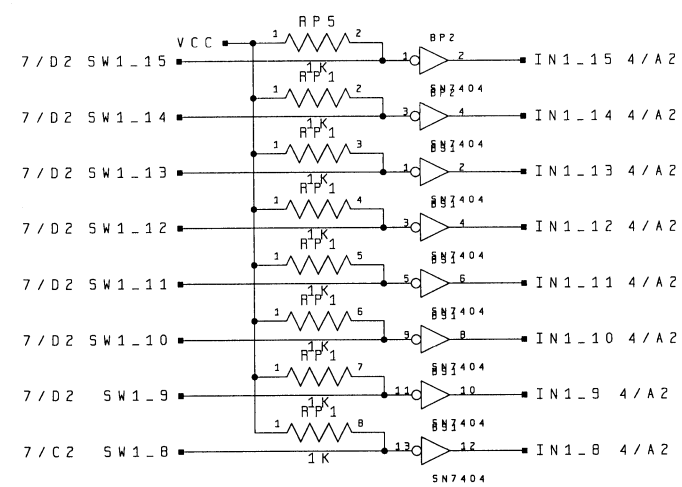
CNT REG



**VIEWlogic**

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 4

READ REGS, CB1,2 REGS

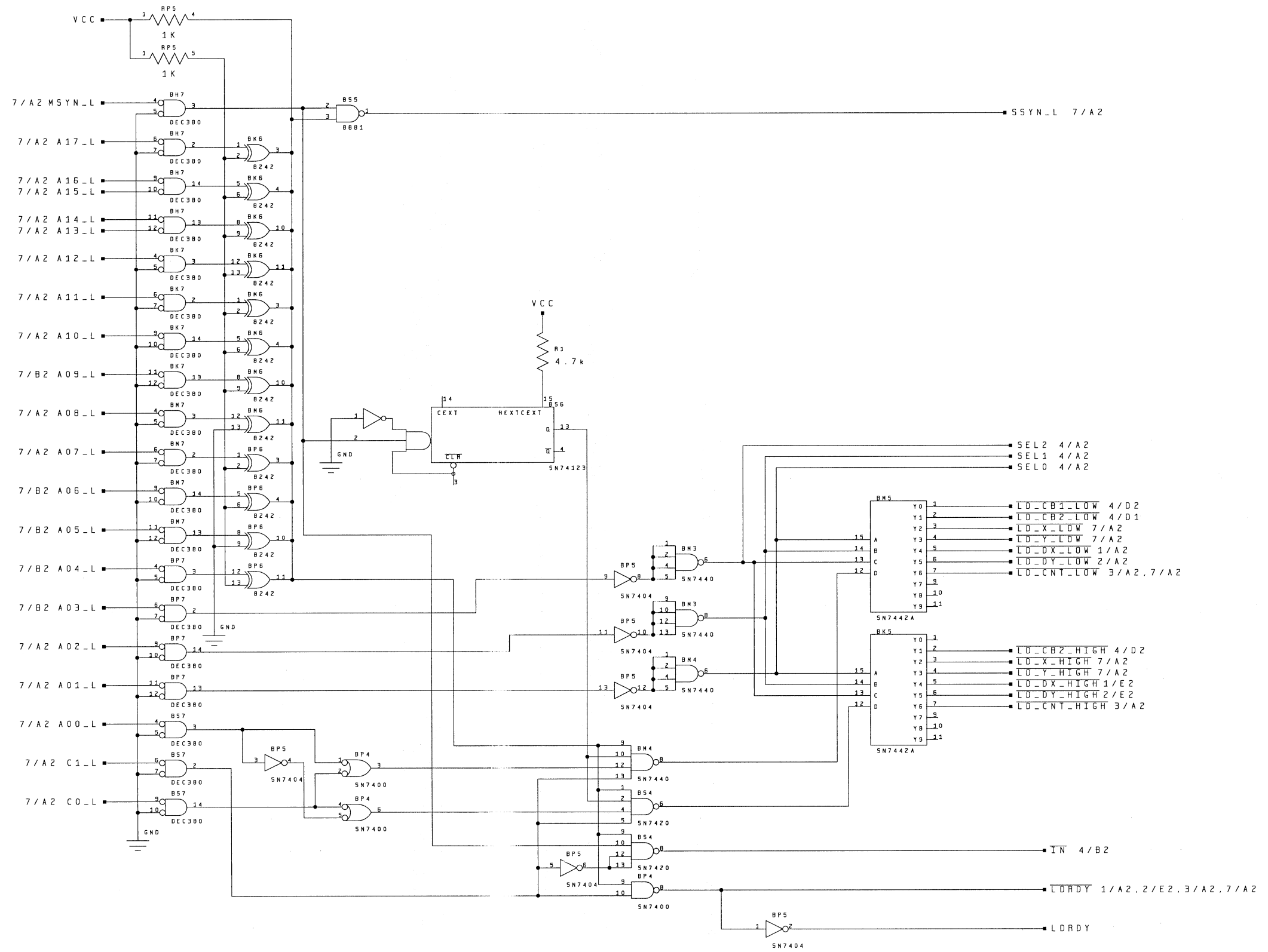


**VIEWlogic**

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 5

SWITCHES, UNIBUS DATA RECEIVERS

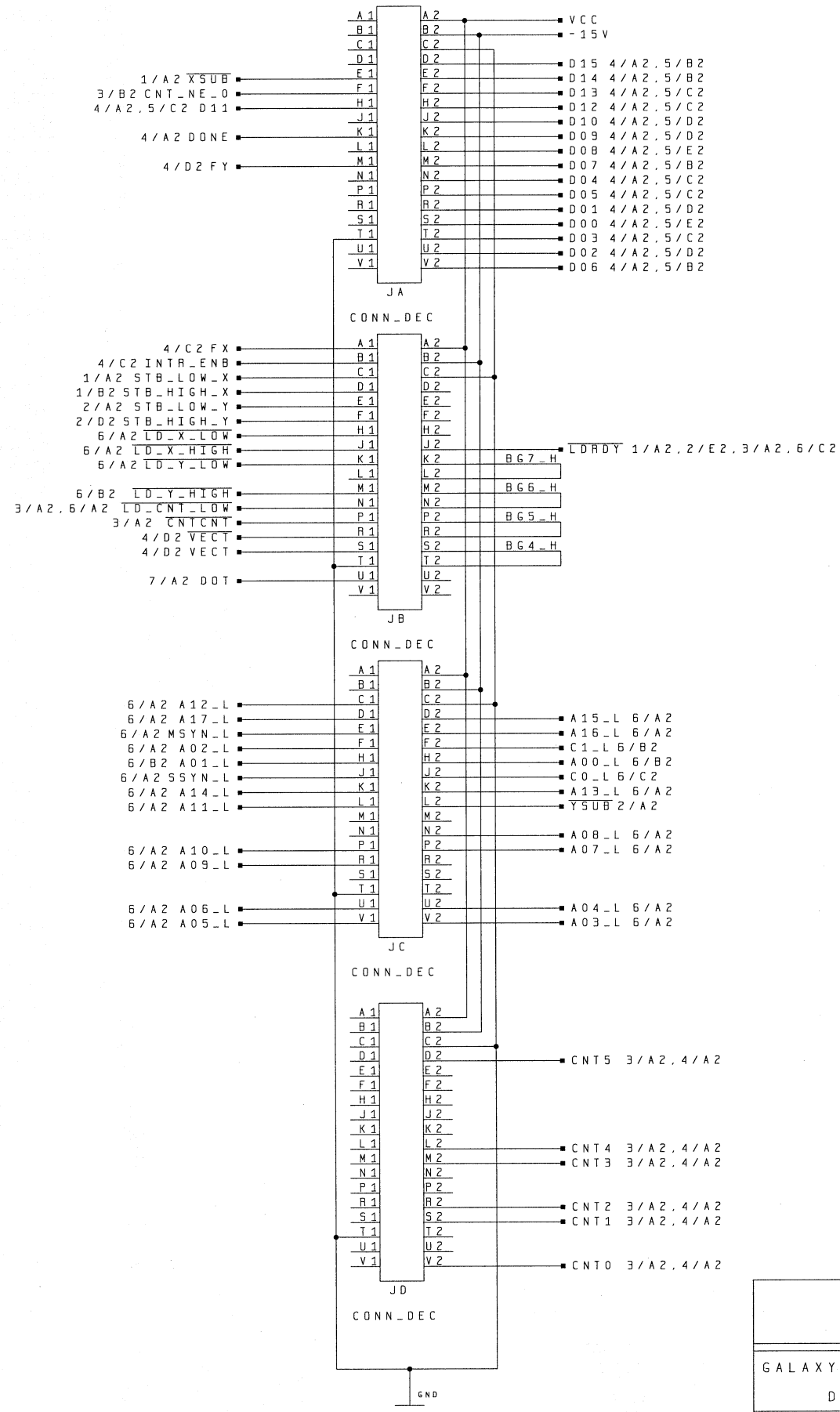
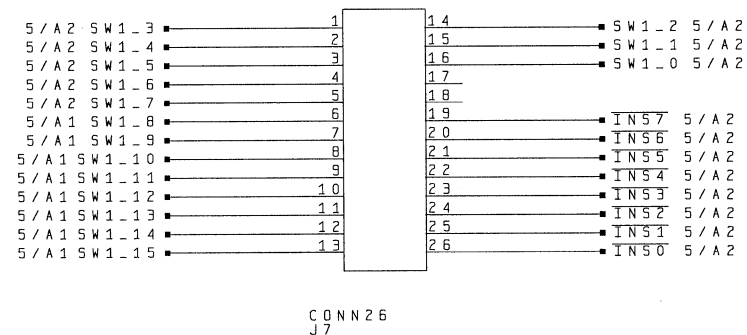
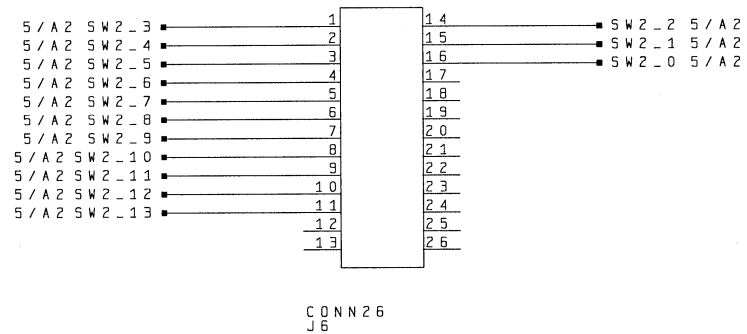
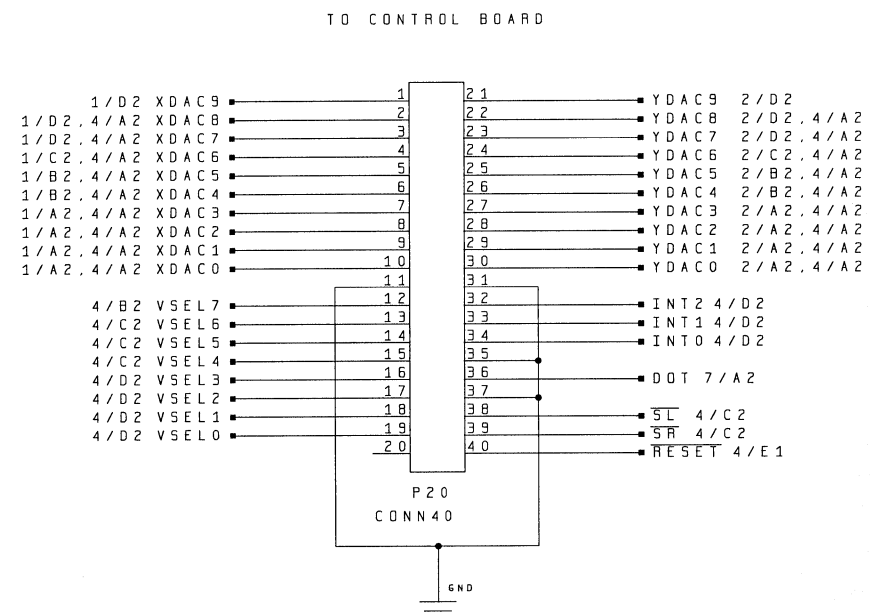
ADDRESS = 77732X



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 6

ADDRESS DECODE



VIEWlogic

GALAXY GAME DISPLAY PROCESSOR  
DATA BOARD, SHEET 7

CONNECTORS