SPECTRA 14

Perkin-Elmer Emulating Disk Controller

PRODUCT SPECIFICATION

Approvals:

Engineering _____

Software _____

Marketing _____

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1.0 INTRODUCTION

The SPECTRA 14 is an emulating disk controller for Perkin-Elmer (Interdata) computers. The controller interfaces to Perkin-Elmer models 70, 74, 80, 7/16, 7/32, 8/32, 3220 and 3240 via the selector channel (SELCH, ESELCH, or BSELCH). The SPECTRA 14 is contained on a single 15" x 15" Perkin-Elmer compatible printed circuit board and attaches any mix of four Storage Module (SMD) compatible disk drives.

The SPECTRA 14 emulates the Perkin-Elmer MSM-80 and MSM-300 Mass Storage Module subsystems using a wide range of SMD compatible disk drives. The standard hardware and firmware set of the SPECTRA 14 attaches any mix of up to four SMD, CMD, or FMD compatible disk drives. Through option switches, a wide range of disk capacities can be accomodated.

The SPECTRA 14 offers additional features such as 32 bit ECC , support of overlapped seeks, and the ability to handle disk data transfer rates up to 2.0MB per second.

2.0 FEATURES

2.0.1. Performance

The SPECTRA 14 provides important performance features such as:

Error Correction Code (ECC) - Corrects burst errors up to 11 bits in length. Data is corrected transparently within the controller's local data buffer after one retry.

Overlapped Seek - Seeks overlapped on up to four drives to improve access time.

Data Buffering - A 1536 byte RAM data buffer provides for up to 6 sector buffering during read commands, and 2 sector buffering during write commands.

Multiple Sector Transfer - A single read or write command may transfer blocks of data limited only by the capacity of the drive. Head switching is performed automatically by the controller.

2.0.2. Single Printed Circuit Board

The SPECTRA 14 occupies a single slot in the Perkin-Elmer (Interdata) computer. The single board design provides cost savings in chassis, power, maintenance, spares, and enhanced reliability.

2.0.3. Full Emulation

The SPECTRA 14/A is fully transparent to Perkin-Elmer OS/16MT and OS/32MT operating systems software. Emulation of the Perkin-Elmer MSM-80 and MSM-300 subsystem is provided by the SPECTRA 14/A and 14/B when used with 80MB and 300MB SMD compatible disk drives.

2.0.4. System Compatibility

The SPECTRA 14 is compatible with Perkin-Elmer Models 70, 74, 80, 7/16, 7/32, 8/32, 3220, and 3240. Interfacing is via the SELCH, ESELCH, or BSELCH. The SPECTRA 14 supports the optional protocol for high speed transfers for Perkin-Elmer models so equipped.

2.0.5. Disk Drive Attachment

Any mix of up to four SMD, CMD, or FMD compatible drives may be attached in the standard emulation mode. SMD compatible drives of any capacity using removable media, fixed Winchester, or combination fixed/removable media (CMD) drives may be attached.

2.0.6. Advanced Architecture

A dual bipolar bit slice microprocessor architecture provides simultaneous control of the disk interface and host interface (SELCH). This provides potential performance improvements and simplifies firmware configuration changes.

2.0.7. Reliability and Maintainability

The SPECTRA 14 provides high reliability through a single PCB, use of pre-tested IC's, elimination of multi-PCB interconnects and power supplies. An on-board DC-DC converter provides -5V for the disk drive interface line drivers/receivers, requiring only +5Vdc from the host computer. On-board self-test microdiagnostics are provided upon power up, with LED error display to aid in fault isolation. In addition, system level diagnostics may be used to verify controller operations.

3.0 FUNCTIONAL CHARACTERISTICS

3.0.1. Computer Interface

The controller interfaces to any 16 or 32 bit Perkin-Elmer computer through the SELCH, ESELCH, or BSELCH (selector channel). Data transfers are handled using standard or optional protocol over the 16 bit data bus.

3.0.2. Disk Interface

The disk interface is compatible with the industry standard Storage Module Drive flat cable interface. Any mix of up to four disk drives utilizing either removable media or fixed media may be attached. The control cable is daisy chained to all drives from the controller. The data cables are attached radially to each drive.

3.0.3. Software Transparency

The SPECTRA 14 emulates the Perkin-Elmer Mass Storage Module 80MB and 300MB subsystems when attaching SMD, CMD, or FMD compatible disk drives. Option switches allow different capacities to be mixed on the SPECTRA 14.

3.0.4. Design Architecture

The SPECTRA 14 uses a high performance dual bipolar bit slice microprocessor design to provide separate and dedicated control of both the SELCH and disk interfaces. This provides concurrent control and allows flexibility in future disk attachments.

3.0.5. Data Buffering

A 1536 byte high speed RAM data buffer is provided for buffering up to 6 sectors of data between the disk and SELCH. The buffer eliminates "data overflow" conditions and achieves optimum speeds by smoothing the differences in transfer rates between the disk and SELCH. Up to 6 sectors are buffered during Read commands, and up to 2 sectors during Write commands. During all non-format Write commands, 254 bytes will be transferred into the buffer, and the header field then read from the specified disk sector and checked for errors. If no errors are detected, the operation will continue and the two remaining bytes for that sector

transferred from the SELCH. If the error is detected in the header, the operation will be terminated and the SELCH starting memory address should be adjusted for retry.

3.0.6. Configurations

Option switches are used to configure any mix of SMD, CMD, or FMD compatible disk drives without the need for hardware or firmware changes.

3.0.7. Error Detection and Correction

A 32 bit ECC polynomial is used to detect and correct data errors up to 11 consecutive bits in length. Error detection occurs on the fly, with error correction being performed transparent to the system within the controller's local data buffer. If desired, automatic error correction may be disabled by selecting the appropriate option switch setting. The controller always performs one automatic reread prior to invoking error correction.

3.0.8. Defective Sectors

Defective sector flagging is provided under software control during formatting. After formatting, the controller will detect defective sectors when it reads the header field by testing for the defective sector bit.

3.0.9. Write Protect

Sectors may be write protected by system software setting the WP bit in the header field during a format write using the Write Format command. When the controller detects the WP bit set during the header verification phase of a Write w/Protect command, termination will occur and no data will be written in that sector. The WP status bit will be set to inform the software.

3.0.10. Position Verification

Automatic position verification is performed by the controller reading and comparing the cylinder, head, and sector numbers contained in the header prior to any non-format read or write operations. An automatic 16 bit CRC check is also performed on the header information to ensure its validity.

3.0.11. Self-Test

An automatic microdiagnostic self-test is performed upon each power up. If an error is detected, an LED is lit to provide visual indication.

3.0.12. Addressing

The controller and each logical disk unit have separate addresses. These are controlled by two separate DIP switches. The controller should be set to the lower hexadecimal address and the four drives following in

sequence by adding one to the least significant hexdigit. Standard Perkin-Elmer hex addresses are:

X'FB' = Controller
X'FC' = Drive Ø
X'FD' = Drive 1
X'FE' = Drive 2
X'FF' = Drive 3

3.0.13. Interrupt Priority

The controller's firmware will establish priority between the drives and controller based on a switch setting contained in an option DIP switch. Normally, the controller will have priority over the four disk drives, and the order among the drives will be Drive Ø (highest priority) to Drive 3 (lowest priority). The controller generates an interrupt when its 'Controller Idle' status bit switches from a zero to a one. The disk drives generate an interrupt if a seek, restore, or servo offset is completed or if a command is directed to a drive, and it is not in a condition to accept the command.

Firmware will store the Interrupt Disarm, Disable, or Enable function given in the command during an OC and respond accordingly when interrupt conditions occur. Example: If Enable is indicated and a seek then completes, the ATN signal will be activated. Then when ACK goes true to acknowledge the interrupt, the interrupting device address (FB, FC, FD, FE, FF) is presented on bits 08 to 15 and SYNC activated.

The interrupt control functions are:

Disarm	=	No queing of interrupts.
Disable	=	Queueing of interrupts.
Enable	=	Permits interrupts.

3.0.14. Dual Port

The SPECTRA 14 supports suitably equipped dual port disk drives.

4.0 PROGRAMMING SUMMARY AND REGISTER SET

4.0.1. I/O Instructions

The following I/O instructions are used to communicate with the controller and attached disk drives:

Sense Status - used to interrogate the controller and drives to ensure that data transfers are completed correctly.

Output Command - used to select the desired mode of operation and control disk operations.

Write Data or Write Halfword - used to load the cylinder, head, and sector address into the controller registers and to load the cylinder and head address into the drive registers.

Read Data or Read Halfword - used to read the rotational postion (sector counter) of the selected drive. The SPECTRA 14 will always return sector 64 for this instruction. RPS is not supported.

Acknowledge Interrupt - used to service the controller and drive interrupts. The interrupting device address is returned with this instruction.

4.0.2. Register Set

Controller Command (OC)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	DIS	ENB	X	PROT	RST	FMT	WR	RD

The controller command register is loaded by issuing an OC to device address 'FB'.

DIS	EN	X	PROT	RST	FMT	WR	RD		
X	X	X	0	0	0	0	1	=	Read
X	X	X	0	0	0	1	0	=	Write w/o Protect
X	X	X	1	0	0	1	0	=	Write w/Protect
X	X	X	0	0	0	1	1	=	Read Check
X	X	X	0	0	1	0	1	=	Read Format
X	X	X	0	0	1	1	0	=	Write Format
0	0	X	0	1	0	0	0	=	Reset

Command Definitions

Disable - When bit is set and Enable is reset, any interrupts occuring are queued up and no ATN is generated.

Enable - When bit is set and Disable is reset, any interrupt occuring is presented; ATN is set.

Disarm - When Enable and Disable bits are both set, no interrupts are generated or queued. All pending interrupts will be cleared.

Read - This command causes the controller to perform a read data from the selected disk. Before the command is issued, the heads must be positioned, the memory buffer starting and ending address written to the SELCH, and the disk addressing information loaded into the controller and drive registers. Normally 256 bytes are read per sector, with all transfers to the SELCH in halfword mode (16 bits per halfword). Multiple sectors may be read; if the SELCH keeps Status Request (SR) active true after the last halfword of the sector is transferred or if SELCH BUSY (SBSY) remains true, the controller continues to read the next sector. The SBSY signal only applies to channels equipped for the optional protocol. A partial sector may be read on the last sector to be transferred by the SELCH terminating early. In this instance, no further Data Requests (DR) will be generated, SR and SBSY will both be false. The controller terminates the operation in this case if no DR, SR, or SBSY is seen and less than 256 bytes (128 halfwords) have been transferred from its buffer. The controller always reads a full sector into its buffer and checks for an ECC error before transfer to the SELCH. Upon termination, the controller sets its Controller Idle status bit and sets ATN if interrupts are enabled. The controller always reads and buffers N+1 sectors beyond the termination point while transferring sector N to the SELCH. A subsequent read command issued for sector number N+1 will cause the data stored in the buffer to start transferring immediately to the SELCH without having to first access the disk. The controller will again however, read the next sector (N+2) from the disk into the buffer.

Write w/o Protect - This command causes data to be written to the selected drive. As in Read, the heads must be positioned, the SELCH given the memory addresses, and the controller and drive address registers loaded. Normally, 256 bytes (128 halfwords) are written per sector. To perform multiple sector writes, if the SELCH continues to activate Data Available (DA) or maintains SBSY after transferring 256 bytes, the controller will continue to the next sector. If the SELCH terminates before a full sector (256 bytes) is transferred (last sector to write), the controller will fill the remainder of that sector with the last halfword transferred into its buffer. The controller generates and appends 4 ECC bytes to every sector. Upon termination the controller sets its Controller Idle status bit and sets ATN if interrupts are enabled.

Write w/Protect - This command also writes data to the disk, but only if the Write Protect bit is false in the sectors header field. If a sector is found to have Write Protect = 1, the Examine Status bit, Write Protect bit, and the Controller Idle status bit are set at the end of that sector. Except for the Write Protect Function, this command operates the same as Write w/o Protect.

Read Check - This command causes the controller to read a single sector to check it for errors, with no data transfer occurring to the SELCH. The SELCH must not be started. When the ECC has been checked at the end of the sector, the Controller Idle status bit is set and ATN set if interrupts are enabled.

Read Format - This command causes the controller to read the sector header field and data if the format switch is set. Normally, 527 bytes per two sectors are read in this mode. Otherwise, the command functions as a normal Read.

Write Format - This command is used when formatting the pack to write header fields and data if the format switch is set. Normally, 527 bytes per two sectors are written in this mode.

Reset - This command acts upon the controller like a System Clear and should not be used in normal programming sequences. All interrupts will be disarmed, all drives deselected, the Busy and Controller Idle status bits set (others reset). The Cylinder Overflow status is not affected. If a data transfer was in process, it is terminated immediately for a read and at the end of sector data on a write. Reset does not affect a Seek in progress.

Controller Sector (WD Ø)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	S_{128}	S_{64}	S_{32}	S_{16}	S_8	S_4	S_2	S_1

The Controller Sector is loaded by issuing a WD as the first of a 3 byte sequence to device address 'FB'. A byte operation occurs, but the sector number is specified only in bits 8 - 15.

Controller Head and Cylinder High (WD 1)

Standard Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{32}	H_{16}	H_8	H_4	H_2	H_1	C_{512}	C_{256}

Expanded Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{128}	H_{64}	H_{32}	H_{16}	H_8	H_4	H_2	H_1

The Controller Head and Cylinder High is loaded in standard emulation mode as the second byte of a three byte sequence by issuing the second WD to device 'FB'. During expanded emulation, this halfword is redefined to contain the head number only, as shown.

Controller Cylinder (WD 2)

Standard Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

Expanded Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	0	0	0	0	0	C_{1K}	C_{512}	C_{256}
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

The Controller Cylinder is loaded in standard emulation mode as the third byte of a three byte sequence by issuing WD to device 'FB'. During expanded emulation, additional byte is defined containing the three most significant bits of the cylinder number. This byte will be transferred as the third of a four byte sequence with the fourth defined as the least significant byte of the cylinder number.

Controller Status (SS)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	WP	HF	DS	CO	BSY	EX	CI	DE

The Controller Status is read by issuing a Sense Status to device 'FB'.

BIT	NAME	FUNCTION
(15)	DE	Data Error is set if the controller detects an ECC error at the end of a sector, and the error is uncorrectable, or if automatic error correction is disabled. The controller will peform an automatic re-read upon the first ECC error detected. If an error is again detected, the controller then attempts error correction in its local buffer, transparent to the system. If the ECC error is uncorrectable, Data Error status is set and the operation terminated.
(14)	CI	Controller Idle is set when the controller is free to accept another command. Drive status is only valid if CI is set. A controller interrupt (ATN) is generated when CI sets at the completion of an operation, if interrupts are enabled. CI also sets when a RESET is issued.
(13)	EX	Examine is set if any of bits 8-11 are set.
(12)	BSY	Busy is set during data transfers if a new halfword is not ready during Read, or if the last halfword has not been accpeted by the controller during Write.
(11)	CO	Cylinder Overflow is set when a data transfer is attempted across the last cylinder boundary. CO sets Examine and Controller Idle. CO is reset when a new Set Head command is issued to the selected drive.
(10)	DS	Defective Sector is set during a Read, Read Check, or Write if the header read from the selected disk contains DS=1. DS also sets Examine.

(9) HF — Header Failure is set during Read, Read Check, or Write if the header read from the selected disk does not compare with the cylinder, head, and sector number stored in the controller. HF also will set if a CRC error is detected at the end of the header field. HF sets Examine, and Controller Idle is set at the end of the sector.

(8) WP — Write Protect is set if the WP bit is set in the Header Field Read when a Write with protect is attempted. WP also sets if a Format Write or Format Read is issued and the Format Switch is off. WP sets Examine, and Controller Idle is set at the end of the sector.

Drive Command (OC)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	DIS	EN	SET HD	SET CYL	—	—	SEEK	RE-
		STORE													

The Drive Command is issued with an OC to devices 'FC', 'FD', 'FE' or 'FF'. The command byte definitions are as follows when bits 10 and 11 are not both 1:

Disable - When this bit is set and Enable is reset, any interrupts which occur are queued and not passed on to the system.

Enable - When this bit is set and Disable is reset, any interrupt occuring is presented to the system.

Disarm - When both the Enable and Disable bits are set, no interrupts are generated or queued by the device. All pending interrupts are cleared.

Seek - When command bit is set, the selected drive positions the heads to the cylinder previously loaded by a Set Cylinder command. If the drive cannot complete the Seek, the Seek Incomplete status bit is set. A Restore command must be issued to clear Seek Incomplete. When seek overlaps are attempted by issuing seeks to multiple drives, the program must wait for Controller Idle to set before issuing each Seek. No controller interrupt is generated in this case. A drive interrupt is generated and ATN set when a seek operation completes, provided interrupts are enabled.

Restore - When command bit is set, the selected drive moves its heads to cylinder 000. A drive interrupt occurs when the restore operation is completed, if interrupts are enabled.

Set Head - This command bit causes the head address to be loaded to the selected drive.

Set Cylinder - This command bit causes the cylinder address to be stored in a register for a seek command.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	RLS	CLR FLT	1	1	SOP	SOM	DSE	DSL

When the command is issued (OC) with bits 10 and 11 both set, the definition is:

BIT	NAME	FUNCTION
(8)	RELEASE	This command bit releases the drive in dual port operations, allowing alternate channel access.
(9)	CLEAR FAULT	This command bit resets the Drive Unsafe status bit and turns off the fault lamp on the drive if a fault no longer exists.
(12)	SERVO OFFSET PLUS	This command bit causes the heads to be offset from the on-cylinder position towards the spindle. This command is used only for Read and must not be used with Write.

(13)	SERVO OFFSET MINUS	This command bit causes the heads to be offset from the on-cylinder position away from the spindle. This command also is used with Read and must not be used with Write.
(14)	DATA STROBE EARLY	This command bit causes the drive to shift the data window early in each bit cell during Read.
(15)	DATA STROBE LATE	This command bit causes the drive to shift the data window late in each bit cell during Read.

NOTE: The Data Strobe Early, Data Strobe Late, Servo Offset Plus, and Servo Offset Minus bits are all used individually to aid in recovering marginal data.

Drive Cylinder High (WD ø)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	0	0	0	0	0	C_{1K}	C_{512}	C_{256}

The Drive Cylinder High address is loaded as the first byte of a 3 byte sequence by issuing a WD to device 'FC', 'FD', 'FE', or 'FF'.Drive Cylinder Low (WD 1)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

The Drive Cylinder Low address is loaded as the second byte of a 3 byte sequence by issuing a WD to device 'FC', 'FD', 'FE', or 'FF'.

Drive Head (WD 2)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{128}	H_{64}	H_{32}	H_{16}	H_8	H_4	H_2	H_1

The Drive Head address is loaded as the third byte of a 3 byte sequence by issuing a WD to device 'FC', 'FD', 'FE', or 'FF'.

Drive Status (SS)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	WP	—	ALT CBSY	DR UNS	DR NOT RDY	EX	SKI	OFFL

The Drive Status byte is read by issuing a Sense status to device 'FC', 'FD', 'FE', or 'FF'. Status definitions are:

BIT	NAME	FUNCTION
(15)	OFFL	Off-line Status is set for the selected drive if it is off-line or unsafe. If a Sense status is issued to a non-existent drive, Drive Not Ready and Off-Line are returned.
(14)	SKI	The Seek Incomplete bit is set when a drive fails to complete a seek to a valid cylinder, a restore, or a servo offset within a set time. Seek Incomplete also sets if the cylinder address given to the drive is invalid.
(15)	EX	The Examine bit is set whenever the Write Protect, Drive Unsafe or ALT CBSY status bits are set.
(12)	DR NOT RDY	The Drive Not Ready status bit is set when the Drive is not in a ready state or during an access positioning operation.
(11)	DR UNS	The Drive Unsafe status bit is set when the drive detects an unsafe condition or fault. Drive Unsafe may be reset by a Clear Fault command if the fault no longer exists.
(10)	ALT CBSY	The Alternate Channel Busy bit is set in dual port operations if the drive is reserved or selected by the opposite channel and selection is attempted.
(8)	WP	The Write Protect status bit is set if the Write Protect switch on the drive is set.

5.0 ERROR CORRECTION CODE

The disk storage subsystem supports error detection and correction to help maintain data integrity. The ECC feature detects all error bursts contained within 21 or fewer contiguous bits in a sector, and corrects all error bursts contained within 11 or less contiguous bits. A large class of additional errors may also be detected, but a small possibility exists that the correction algorithm will indicate erroneous corrections on error bursts that exceed 11 bits.

When the subsystem writes a sector, the ECC hardware divides the data field by the polynomial shown below, and appends the generated remainder to the end of the data field. During a read, the data plus the appended checkword is divided by the same generator polynomial. If a transcription error occurs, the resulting remainder is non-zero (except for a small class of errors which are undetectable due to the cyclic properties of the generator polynomial), and the controller's ECC error flag sets.

The generator polynomial is:

$$(X^{11} + X^2 + 1)(X^{21} + 1) =$$

$$X^{32} + X^{23} + X^{21} + X^{11} + X^2 + 1$$

6.0 HARDWARE

6.0.1. Single P.C. Board

The controller is contained on one 15" x 15" Perkin-Elmer compatible printed circuit board. The controller mounts in one slot of the CPU or expansion chassis. The embedded single board design saves space, provides high reliability, and ease of maintenance.

6.0.2. Error Display

Two sets of LED's, one for each microprocessor, display error status to allow convenient user diagnosis.

6.0.3. Drivers and Receivers

SMD compatible balanced line drivers and receivers assure reliable operation of the disk drives up to 50 feet from the Perkin-Elmer system.

6.0.4. Cable Connectors

A 60 pin control cable ('A' cable) connector is provided at the back edge of the PCB; mates to 30 TWP flat cable.

Four 26 pin data cable ('B' cable) connectors are provided at the back edge of the PCB, allowing attachment of up to 4 SMD disk drives; mate to 26 conductor flat shielded ribbon cables.

6.0.5. Power

Uses internal +5V at 9 amps maximum.

6.0.6. Environmental

Exceeds all Perkin-Elmer (Interdata) temperature and humidity specifications.

7.0 DRIVE INTERFACE

The disk drive interface is the industry standard SMD compatible interface. The SPECTRA 14 attaches up to 4 disk drives using SMD compatible flat cables. The signal assignment and pin assignments are defined in the following figures.

"A" CABLE

CONTROLLER			DRIVE LO, HI	
Unit Select Tag			22, 52	
Unit Select 2^0			23, 54	
Unit Select 2^1			24, 54	
Unit Select 2^3			27, 57	
Tag 1	2*		1, 31	
Tag 2	2*		2, 32	
Tag 3	2*		3, 33	
Bit 0	2*		4, 34	
Bit 1	2*		5, 35	
Bit 2	2*		6, 36	
Bit 3	2*		7, 37	
Bit 4	2*		8, 38	
Bit 5	2*		9, 39	
Bit 6	2*		10, 40	
Bit 7	2*		11, 41	
Bit 8	2*		12, 42	
Bit 9	2*		13, 43	
Open Cable Detector			14, 44	
Index	2*		18, 48	
Sector	2*		25, 55	
Fault	2*		15, 45	
Seek Error	2*		16, 46	
On Cylinder	2*		17, 47	
Unit Ready	2*		19, 49	
Address Mark Found	2*		20, 50	
Write Protected	2*		28, 58	
Power Sequence Pick			29	(one twisted pair)
Power Sequence Hold			59	
Busy	2*	1**	21, 51	
Bit 10	2*	3*	30, 60	

NOTE: 60 Position, 28 Awg., 30 twisted pair, straight flat cable, 100 ft. max.

1** Dual Channel units Only. 2* Gated by unit selected.

3* Bit 10 used for cylinder 1024 Bit for drives so equipped.

"B" CABLE

CONTROLLER	DRIVE LO, HI
Write Data	8, 20
Ground	7
Write Clock	6, 19
Ground	18
Servo Clock	2, 14
Ground	1
Read Data	3, 16
Ground	15
Read Clock	5, 17
Ground	4
Seek End	10, 23
Unit Selected	22, 9
Ground	21
Reserved for Index	12, 24
Ground	11
Reserved for Sector	13, 26
Ground	25

NOTES:

1. 26 conductor shielded flat cable
   Maximum length - 50 ft.
2. No signals gated by Unit Selected.

8.0 VERSIONS

The SPECTRA 14 provides Perkin-Elmer operating systems compatibility by emulating the MSM disk subsystem when using 80MB or 300MB SMD compatible disk drives.

Through an option switch, the SPECTRA 14 supports the CDC FMD 9775 675MB disk drive and its fixed head option which provides 1.9MB of fast access data located at cylinders 896 to 898.

The SPECTRA 14 supports fixed and removable combination CMD 9448 or equivalent type drives. Formatted capacities are 27.0MB, 53.9MB, and 80.9MB. The CMD 9448 is treated as two separate volumes; one removable and one fixed. The removable volume capacity is 13.5MB formatted. The fixed volume capacity ranges from 13.5MB to 67.4MB.

SPECTRA 14 CHARACTERISTICS

P-E Emulation	MSM-80	MSM-300	MSM	MSM-80	Various
SMD Compatible Drives	CDC 9762 SMD CDC 9730 MMD Ampex 980 Century Data T-82	CDC 9766 Ampex 9300 Century Data T302	CDC 9775 FMD	CDC CMD9448 Ampex DFR-900 Century Data Hunter	Other SMD compatible drives
Drive Capacity (MB)	80	300	675	32/64/96	Several
Media Type	Removable; Fixed Winchester	Removable	Fixed Winchester	Fixed-Removable	Various
Emulation Mode	Standard	Standard	Expanded	Expanded	Expanded
Sector per Track	64	64	64	64	—
Track per Cylinder	5	19	40	2/4/6	—
Cylinder per Drive	823	823	843	823	—
Sector Size(Bytes)	256	256	256	256	256
Formatted Capacity (MB)	67.4	256.4	552.5	27.0/53.9/80.9	Various

9.0 FORMAT

Gap1	S2	Header	CRC	GAP2	S2	Data1	ECC1	Gap3	S3	Data2	ECC2	Gap4
27	1	7	2	16	1	256	4	16	1	256	4	19

By using the above dual sector format, 33 physical or 66 logical sectors are provided. This formatting scheme allows for two alternate sectors since only 64 are used during normal operation. Unused sectors must have all ones written into the sector address portion of the header field.

Header Format

BYTE Ø							
DEF	WR						
SEC1	PROT1	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	2	3	4	5	6	7

BYTE1							
DEF	WR						
SEC2	PROT2	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	2	3	4	5	6	7

BYTE2							
Ø	Ø	S_{32}	S_{16}	S_8	S_4	S_2	S_1
Ø	1	2	3	4	5	6	7

BYTE3							
Ø	Ø	H_{32}	H_{16}	H_8	H_4	H_2	H_1
Ø	1	2	3	4	5	6	7

BYTE4							
Ø	Ø	Ø	Ø	Ø	C_{1K}	C_{512}	C_{256}
Ø	1	2	3	4	5	6	7

BYTE5							
C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1
Ø	1	2	3	4	5	6	7

During the Write Format or read Format operations, the 6 header bytes plus 512 data bytes and 8 bytes of ECC per logical sector pair are transferred.

The 9775 disk drive may require entire tracks to be flagged depending on the media defect information supplied by the drive manufacturer. If defects are located so that more than one defect falls within the same sector, the ECC may miscorrect, and the track should not be used.

SPECTRA 14
Sector Format
66 Sectors/Track

Sector Pulse

Gap_1 S_1 ID CRC Gap_2 S_2 $Data_1$ ECC_1 Gap_3 S_3 $Data_2$ ECC_2 Gap_4

GAP_1	=	23 bytes of zeros
$SYNC_1$	=	1 byte of 19_{16}
ID	=	6 bytes; F_1 F_2 H C_H C_L (flag, sector, head, cylinder)
CRC	=	2 bytes cyclic check code; $X^{16} + X^{15} + X^2 + 1$
GAP_2	=	17 bytes of zeros
$SYNC_2$	=	1 byte of 19_{16}
$DATA_1$	=	256 bytes of data
ECC_1	=	4 bytes error correction code; $X^{32} + X^{23} + X^{21} + X^{11} + X^2 + 1$
GAP_3	=	23 bytes of zeros
$SYNC_3$	=	1 byte of 19_{16}
$DATA_2$	=	256 bytes of data
ECC_2	=	4 bytes of error correction code
GAP_4	=	16 bytes; 2 bytes of zeros plus 17 bytes undefined.
		610 bytes per physical sector

33 physical sectors per track
66 logical sectors per track; 64 system sectors + 2 spares.

NOTE: Each ID will contain a flag byte for Write Protect and Bad Sector flags for each logical sector. Flag Byte 1 is associated with Data Field 1, Flag Byte 2 with Data Field 2.