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SPECTRA 14

PRODUCT REFERENCE MANUAL

SPECTRA LOGIC

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1.0 INTRODUCTION

The SPECTRA 14 is a single board disk controller for use on Perkin-Elmer Corporation computers. The SPECTRA 14 interfaces to the Selector Channel (SELCH) on all Perkin-Elmer CPU models including the 7/16, 7/32, 3220, and 3240. The SPECTRA 14 emulates the P-E MSM-80 and MSM-300 disk subsystems when used with 80 and 300MB SMD type disk drives. All P-E operating systems software (OS/16 or OS/32) runs without modification on the SPECTRA 14/SMD disk subsystems. P-E diagnostics for the MSM-80/300 may be utilized with the SPECTRA 14 disk controller, providing additional ease of maintenance.

The SPECTRA 14 employs a dual microprocessor architecture using bit slice technology. This design approach provides high performance and flexibility to support any SMD type disk drive. The standard hardware and firmware set provides for attachment of any mix of up to four SMD, MMD, CMD, or FMD compatible disk drives. In addition to the full emulation of the MSM-80/300, the SPECTRA 14 can be used in an expanded emulation mode which utilizes parameter changes to P-E software. These optional parameter changes allow other than 80/300MB capacity drives to be attached under the OS/16 MT2 and OS/32 MT operating system software.

The SPECTRA 14 offers additional features such as 32 bit ECC, overlapped seek support, and capability to handle disk data transfer rates up to 2.0 MB per second.

1.1 General Information

The SPECTRA 14 provides many important benefits in cost, reliability, maintainability, and performance. The SPECTRA 14 offers the most cost effective package available in emulating controllers which attach 80, 300, or 675MB disk drives to Perkin-Elmer computers. Cost savings are realized not only in the purchase price of the controller, but also by providing the advantage of buying independent disk drives. Cost savings will continue throughout the life of the SPECTRA 14 due to reliability, ease of maintenance, and adaptability.

High reliability is achieved in the SPECTRA 14 through reduced parts count of the single PCB, use of pretested IC's, elimination of multi-board interconnections and external supplies. Extensive use is made of low-power Schottky and standard Schottky integrated circuits on a 4 layer PCB with internal power and ground planes. On-board self-test microdiagnostics execute upon each initalization of the system and provide LED indications to aid in fault isolation and maintenance.

System level diagnostics may be used to verify controller operation within the complete subsystem. Most P-E diagnostics run without modification on the SPECTRA 14, and those which do not have a patch list provided in a later section of this manual.

The SPECTRA 14 is compatible with Perkin-Elmer operating systems: OS/16 MT2 and OS/32 MT. The SPECTRA 14 combined with an 80MB or 300MB SMD compatible disk drive emulates the Perkin-Elmer MSM-80 or MSM-300 and runs the operating systems without modification.

Features of the SPECTRA 14 include:

* Single 15"x15" P-E compatible PCB packaging.
* Dual microprocessor, microprogrammed bit slice architecture.
* Full emulation of the MSM-80 and MSM-300 subsystems.
* P-E operating system software transparency.
* P-E diagnostic software compatibility.
* Attachment of up to four SMD, MMD, CMD, or FMD compatible disk drives of any mix providing up to 2700 MB of on-line storage.
* Error Correction Code (ECC) provides up to 11 bit burst error correction transparently in the SPECTRA 14's local buffer.
* 1536 byte RAM data buffer provides up to 6 sector buffering during reads and up to 2 sectors during writes.
* Overlapped seek capability.
* Multiple sector data transfers.
* Automatic head switching.
* Capability for attaching removable media, fixed media Winchester, or combination fixed/removable media SMD compatible drives in any mix.
* Automatic position verification.
* Cycle Redundancy Check (CRC) on each physical sector header field.
* Advanced architecture using dual bipolar microprocessors to provide simultaneous control of the disk interface and SELCH interface.
* Automatic microdiagnostic self-test performed on each initialization.

Spectra Logic Corporation provides a limited warranty of the SPECTRA 14 for one year. PCB repair of units returned to Spectra Logic will be effected within three working days after receipt of the failing PCB. Spectra Logic policy is to put warranty PCB repair ahead of new production in priority. Repair of PCB's out of warranty will be performed at a nominal charge.

1.2 Specifications

Specifications of the SPECTRA 14 emulating disk controller are summarized below:

Functional Characteristics

Disk Drive Attachment	4
Disk Interface Connection:	
Control	Daisy Chain
Data	Radial
Controller Address (optional)	FB_{16} standard
Drive Addresses (optional)	FC_{16} (DR 0) FD_{16} (DR 1) FE_{16} (DR 2) FF_{16} (DR 3)
Interrupt Priority (optional)	Controller (1) Drive 0 (2) Drive 1 (3) Drive 2 (4) Drive 3 (5)
Sector Addressing	Contiguous: 00 to 63
Data Buffer	1536 byte RAM

Data Transfer Length	1 to 16K words
Data Field Integrity	
Error Correction Code (Correction Optional)	11 bit burst error detection and correction; 32 bit ECC polynomial.
Header Field Integrity	
Cyclic Redundancy Check	16 bit CRC. Cylinder, head, and sector comparison.
Auto Position Verification	
Seek Control	Explicit and overlapped.
Dual Port Drive Control	Four dual ported drives supported.

Performance Characteristics

Error Correction Time	Less than 6ms in local buffer.
Bus Transfer Rate Maximun	3.0 MB/Sec

Storage Capacity Characteristics

	MSM-80	MSM-300
Bytes/Pack Unformatted	80MB	300MB
Bytes/Pack Formatted	67.4MB	256.2MB
Cylinders/Pack	823	823
Tracks/Cylinder	5	19
Sectors/Track	64	64
Bytes/Sector	256	256
Sectors/Pack	263,360	1,000,768

Physical Characteristics

PCB Size	Single 15"x15", 4 layer.
Cable Connections	One 60-pin flat cable connector and four 26-pin flat cable connectors mounted at edge of PCB.

Environmental

Exceeds Perkin-Elmer temperature and humidity specifications.

Power Requirement

+5Vdc ±5% @ 9 amps maximum.

2.0 INSTALLATION

This section contains the information needed to install a SPECTRA 14 disk controller. The SPECTRA 14 can be installed in any PERKIN-ELMER model CPU. Interfacing is accomplished via the SELCH, and therefore the slot used must contain the SELCH private I/O bus.

Maintenance personnel should be familiar with both the P-E hardware and the specific SMD type drive being installed.

2.1 Installation Procedures

2.1.1 Inspection

Perform a thorough visual inspection of the SPECTRA 14 PCB and SMD interface cables upon removal from their shipping container. Note all damage and notify the freight carrier immediately as Spectra Logic's warranty does not cover shipping damage. The damage claim is to be filed through the carrier with its insurance company.

Check for any broken components or bent pins, and ensure that all IC's in sockets are securely in place. DO NOT remove IC's from sockets unless absolutely necessary to reseat properly. If any IC's are reinserted, observe correct seating with relation to Pin 1 of the socket.

Inspect the SMD cables for cut or broken wires, and ensure that the connectors are not damaged.

2.1.2 Configuration Verification

The SPECTRA 14 is set up at the factory for P-E standard addresses; however, the switch settings should be visually verified. Ensure that the controller address, drive address, and drive configuration switches are set to the desired value.

Refer to section 2.2 for switch settings.

2.1.3 PCB Installation

The SPECTRA 14 PCB is to be installed only after inspection, switch setting, and backpanel preparation below is complete. Typically, the SPECTRA 14 will be installed in the CPU chassis or an expansion chassis. Ensure that the components face in the same direction as on other boards in the chassis.

Ensure that all required SELCH private I/O bus signals, power, and ground are available on the slot selected for installation. Refer to P-E documentation for backpanel signals.

Check that RACKO on pin 122-1 and TACKO on 222-1 of the backpanel on the slot intended for use are not jumpered together. Also ensure that RACKO is wired to the slot from the previous higher priority unit and that TACKO is propagated (wired) to the next lower priority unit.

After completing the above checks and backpanel preparation, ensure that power is off and then insert the PCB. Insertion of the PCB should be accomplished without forcing it into the backpanel. Ensure that the guide pin blocks on the PCB line up with the backpanel guide pins, then press the PCB firmly until it is fully seated.

2.1.4 SMD Cable Installation

After installing the SPECTRA 14 PCB, connect the 60-conductor "A" cable into the J1 header on the PCB. Ensure that pin 1 of the cable connector mates with pin 1 of the PCB header. Pin 1 is designated on both by a small arrowhead.

Next, connect the 26-conductor "B" cable to any one of the four 26-pin headers on the PCB. Again, ensure that pin 1 of the cable mates with pin 1 of the header, designated by a small arrowhead.

Route the cables out of the chassis neatly, using folds if necessary. Make sure the cables do not interfere with covers or PCB retainers.

Connect the other end of the 60-conductor "A" cable to the first drive's "A" cable input header. Connect the 26-conductor "B" cable to the "B" cable input of the drive. Ensure that a terminator is installed on the last drive, and if multiple drives are installed, connect a "daisy chain" cable between units.

2.1.5 Power ON

Proceed to power up the system; run the formatter program and diagnostics to verify subsystem operations. Be sure to set the Format Switch "On" noting that its LED is lit before starting the format program. Once formatting is complete, turn the Format Switch "Off".

2.2 Configuration Switches

2.2.1 Controller Address

The Dip Switch in location 8T and two jumpers establish the controller address on the SPECTRA 14. The switches allow any of 256 addresses to be set. Jumpers W3 and W5 normally establish address bits 8 and 9 as 0's.

Switch	1	2	3	4	5	6	7	8
	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
Addr Bit	A7	A6	A5	A4	A3	A2	A1	A0
	8	4	2	1	8	4	2	1
			F				B	

A switch set to the ON position corresponds to a logical "0", and a switch OFF to a logical "1".

2.2.2 Drive Address

The Dip Switch in location 8S establishes four contiguous drive addresses. The P-E MSM standard addresses are:

Drive 0 = "FC"
Drive 1 = "FD"
Drive 2 = "FE"
Drive 3 = "FF"

Switch	2	3	4	5	6	7	Drive 0 - 3
	OFF	OFF	OFF	OFF	OFF	OFF	

Addr Bit	A7	A6	A5	A4	A3	A2	A1	A0
	8	4	2	1	8	4	2	1
				F		C,D,E,F		

A switch set to the ON position corresponds to a logical "0", and a switch OFF to a logical "1".

Switch 1 is not used. Switch 8 is used during manufacturing testing to switch the phase of the clock on which it will stop when using the SPECTRA LOGIC TEST PANEL.

2.2.3 Drive Configuration Switches

The switch in location 10L and a portion of the switch in location 10R provide capability to select one of eight drive types/parameters for each logical unit, 0 - 3. Each logical unit address has three switches assigned in hardware to that address; however, the drive itself may be attached to any one of the four physical "B" cable ports on the controller. The drive type select switches are:

S_A	S_B	S_C	Logical Unit	P-E Address
10L-8	10L-7	10L-6	3	'FF'
10L-5	10L-4	10L-3	2	'FE'
10L-2	10L-1	10R-8	1	'FD'
10R-7	10R-6	10R-5	0	'FC'

Switch Position Code:

S_A	S_B	S_C	Logical Heads/Drive
0	0	0	5
0	0	1	19
0	1	0	4
0	1	1	10
1	0	0	2 CMD-32
1	0	1	4 CMD-64
1	1	0	6 CMD-96
1	1	1	40

Any combination of drive types or their equivalents, with the number of logical heads above, may be attached using appropriate switch settings for each drive. Fixed head option supported only on the 9775 FMD.

2.2.4 Option Switches

The option switches in locaton 10R are to be set according to the system operation desired. Switch definitons are:

10R	Function
SW 1	ECC Correction: OFF enables ECC correction of data errors in the buffer. ON disables ECC correction.
SW 2	Protocol Select: ON selects optional protocol and generates the Switch to New Sequence (SNS) signal true. OFF selects standard protocol; SNS false.
SW 3	Interrupt Priority: OFF gives the controller priority, which is normal. ON gives the drives priority over the controller.
SW 4	Write with Protect: OFF enables the Write with Protect function; ON disables it.

2.2.5 Miscellaneous

Ensure the attached disk drive(s) has Index and Sector in the "A" cable and that the interface is set to gate those signals only when selected.

Ensure the Drive is set to 33 sectors per track (33 will have equal lengths, and a 34th will occur that is unusable which the controller ignores).

During system power up, ensure the disk drive is powered on after the Perkin-Elmer CPU and during power down that the disk is powered off first.

3.0 THEORY OF OPERATION

The SPECTRA 14 controller is based on a dual microprocessor design employing a bit slice implementation. The two microprocessors perform independent functions to simultaneously control the SELCH interface and the SMD interface. The microprocessor controlling the SELCH interface is referred to as the Host Microprocessor (HM) and the SMD interface microprocessor as the Disk Microprocessor (DM).

The HM controls SELCH interfacing functions and controller registers: Controller Command, Controller Sector, Controller Head/Cylinder High, Controller Cylinder Low, Controller Status, and Interrupts. The HM is also responsible for decoding and initiating commands, performing data transfers between the SELCH and the controller's local buffer, command termination, and ending status.

The DM controls the SMD interface and disk formatter functions such as the serializer/deserializer, sector format, read/write control, CRC, and ECC. The DM also controls the drive registers: Drive Command, Drive Cylinder High, Drive Cylinder Low, Drive Head, and Drive Status. The DM decodes and initiates drive position commands and maintains current status for each attached drive.

The two microprocessors communicate with each other through the first 512 bytes of a 2K byte RAM buffer. In addition, two hardware flags (CMD and HDR STAT) are used to signal between microprocessors. The "CMD" flag is generated by the HM to inform the DM that an operation is to be performed. The "HDR STAT" is generated by the DM to inform the HM when to proceed during write operations.

Up to 6 sectors (1536 bytes) of data may be buffered on a read. Data transfer to the SELCH starts after reading one sector from the disk and testing for errors. During writes, 252 bytes are transferred to the buffer from the SELCH before starting to write on the disk. On non-format writes, the header field will be read and tested for errors/flags before proceeding to write the data field. The last four bytes of a logical sector will always be transferred from the SELCH to the buffer after writing to the disk starts. This is necessary in order to get software to readjust the SELCH starting memory address to point to the location for the beginning of the sector in the event an error or write protect flag is found when the header field is tested.

A 25MHZ oscillator generates clock signals to drive both microprocessors. Each microprocessor is operated on opposite phases of the master clock in order to avoid contention problems when accessing the buffer.

Interrupt priority is established between the drives and controller by firmware based on the Interrupt Priority switch. Normally, the controller has priority over the four disk drives and the order among the drives is Drive 0 (highest) to Drive 3 (lowest). The controller generates an interrupt when its "Controller Idle" status bit switches from a zero to a one. The disk drives generate an interrupt if a Seek, Restore, or Servo Offset is completed, or if a command is directed to a drive which is not in a condition to accept the command. The Interrrupt Disarm, Disable, or Enable function given in the command during an OC is stored in RAM by firmware to cause the HM to respond appropriately when interrupt conditions occur.

The Interrupt Control functions are:

Disarm= No queueing of interrupts.
Disable= Queueing of interrupts.
Enable= Permits interrupts.

The SPECTRA 14 implements a 32 bit ECC polynomial used to detect and correct data errors up to 11 consecutive bits in length. Error detection occurs on-the-fly in hardware, with error correction being performed by the microprocessor within the local data buffer transparent to the system. Prior to invoking error correction, the controller always performs one automatic re-read of the failing sector. If the error persists on the re-read, then correction is performed in the buffer. If the error is found uncorrectable, the controller transfers the data and terminates with Data Error status.

The Disk format contains 33 physical sectors containing a header field and two 256 byte data fields. This provides 64 logical sectors (plus one spare) for P-E operating system transparency. Automatic position verification is performed on the cylinder, head, and sector numbers contained in the write or read operations. A 16 bit CRC check is also performed on the header to ensure its validity.

3.1 Register Definitions

The following paragraphs provide specific bit assignments and definition of each register visible to the system software. The following I/O instructions are used to communicate with the controller and attached drives:

Sense Status
Output Command
Write Data or Write Halfword
Read Data or Read Halfword
Acknowledge Interrupt

3.1.1 Controller Command

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	DIS	ENB	X	PROT	RST	FMT	WR	RD

The controller command register is loaded by issuing an OC to device address 'FB'.

DIS	EN	X	PROT	RST	FMT	WR	RD		
X	X	X	0	0	0	0	1	=	Read
X	X	X	0	0	0	1	0	=	Write w/o Protect
X	X	X	1	0	0	1	0	=	Write w/ Protect
X	X	X	0	0	0	1	1	=	Read Check
X	X	X	0	0	1	0	1	=	Read Format
X	X	X	0	0	1	1	0	=	Write Format
0	0	X	0	1	0	0	0	=	Reset

Command Definitions

Disable - When bit is set and Enable is reset, any interrupts occuring are queued up and no ATN is generated.

Enable - When bit is set and Disable is reset, any interrupt occuring is presented and ATN is set.

Disarm - When Enable and Disable bits are both set, no interrupts are generated or queued. All pending interrupts will be cleared.

Read - This command causes the controller to perform a read data from the selected disk. Before the command is issued, the heads must be positioned, the memory buffer starting and ending address written to the SELCH, and the disk addressing information loaded into the controller and drive registers. Normally 256 bytes are read per sector, with all transfers to the SELCH in halfword mode (16 bits per halfword). Multiple sectors may be read; if the SELCH keeps Status Request (SR) active true after the last halfword of the sector is transferred or if SELCH BUSY (SBSY) remains true, the controller continues to read the next sector. The SBSY signal only applies to channels

equipped for the optional protocol. A partial sector may be read on the last sector to be transferred by the SELCH terminating early. In this instance, no further Data Requests (DR) will be generated, SR and SBSY will both be false. The controller terminates the operation in this case if no DR, SR, or SBSY is seen and less than 256 bytes (128 halfwords) have been transferred from its buffer. The controller always reads a full sector into its buffer and checks for an ECC error before transfer to the SELCH. Upon termination, the controller sets its Controller Idle status bit and sets ATN if interrupts are enabled. The controller always reads and buffers N+1 sectors beyond the termination point while transferring sector N to the SELCH. A subsequent READ will then cause data to be transferred immediately to the SELCH without having to first access the disk. The controller will again, however, read the next sector (N+2) from the disk into the buffer.

Write w/o Protect- This command causes data to be written to the selected drive. As in Read, the heads must be positioned, the SELCH given the memory addresses, and the controller and drive address registers loaded. Normally, 256 bytes (128 halfwords) are written per sector. To perform multiple sector writes, if the SELCH continues to activate Data Available (DA) or maintains SBSY after transferring 256 bytes, the controller will continue to the next sector. If the SELCH terminates before a full sector when the last halfword is transferred (last sector to write), the controller will fill the remainder of that sector with the last halfword transferred into its buffer. The controller generates and appends 4 ECC bytes to every sector. Upon termination the controller sets its Controller Idle status bit and sets ATN if interrupts are enabled.

Write w/Protect - This command also writes data to the disk, but only if the Write Protect bit is false in the sector's header field. If a sector is found to have Write Protect = 1, the Examine Status bit, Write Protect bit, and the Controller Idle status bit are set at the end of that sector. Except for the Write Protect Function, this command operates the same as Write w/o Protect.

Read Check - This command causes the controller to read a single sector to check it for errors, with no data transfer occurring to the SELCH. The SELCH must not be started. When the ECC has been checked at the end of the sector, the Controller Idle status bit is set and ATN set if interrupts are enabled.

Read Format - This command causes the controller to read the sector header field and data if the format switch is set. Normally, 526 bytes per two sectors are read in this mode. Otherwise, the command functions as a normal Read.

Write Format - This command is used when formatting the pack to write header fields and data if the format switch is set. Normally, 526 bytes per two sectors are written in this mode.

Reset - This command acts upon the controller like a System Clear and should not be used in normal programming sequences. All interrupts will be disarmed, all drives deselected, and the Busy and Controller Idle status bits set (others reset). The Cylinder Overflow status is not affected. If a data transfer is in process, it is terminated immediately for a Read and at the end of sector data for a Write. Reset does not affect a Seek in progress.

3.1.1.2 Controller Sector (WD 0)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	S_{128}	S_{64}	S_{32}	S_{16}	S_8	S_4	S_2	S_1

The Controller Sector is loaded as the first byte of a three byte sequence by issuing a WD to device "FB". A byte operation occurs, but the sector number is specified only in bits 8 - 15.

3.1.1.3 Controller Head and Cylinder High (WD 1)

Standard Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{32}	H_{16}	H_8	H_4	H_2	H_1	C_{512}	C_{256}

Expanded Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{128}	H_{64}	H_{32}	H_{16}	H_8	H_4	H_2	H_1

The Controller Head and Cylinder High is loaded in standard emulation mode as the second byte of a three byte sequence by issuing a WD to device "FB". For expanded emulation, this halfword is redefined to contain the head number only, as shown.

3.1.1.4 Controller Cylinder (WD 2)

Standard Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

Expanded Emulation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	0	0	0	0	0	C_{1K}	C_{512}	C_{256}

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

The Controller Cylinder is loaded in standard emulation mode as the third byte of a three byte sequence by issuing WD to device "FB". For expanded emulation, an additional byte is defined containing the three most significant bits of the cylinder number. This byte will be transferred as the third of a four byte sequence with the fourth defined as the least significant byte of the cylinder number.

3.1.1.5 Controller Status (SS)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	WP	HF	DS	CO	BSY	EX	CI	DE

The Controller Status is read by issuing a Sense Status to device "FB".

BIT	NAME	FUNCTION
15	DE	Data Error is set if the controller detects an ECC error at the end of a sector, and the error is uncorrectable, or if automatic error correction is disabled. The controller will perform an automatic re-read upon the first ECC error detected. If an error is again detected, the controller then attempts error correction in its local buffer, transparent to the system. If the ECC error is uncorrectable, Data Error status is set and the operation terminated.
14	CI	Controller Idle is set when the controller is free to accept another command. Drive status is only valid if CI is set. A controller interrupt (ATN) is generated when CI sets at the completion of an operation, if interrupts are enabled. CI also sets when a RESET is issued.
13	EX	Examine is set if any of bits 8-11 are set.
12	BSY	Busy is set during data transfer if a new halfword is not ready during Read, or if the last halfword has not been accepted by the controller during Write.
11	CO	Cylinder Overflow is set when a data transfer is attempted across the last cylinder boundary. CO sets Examine and Controller Idle. CO is reset when a new Set Head command is issued to the selected drive.
10	DS	Defective Sector is set during a Read, Read Check, or Write if the header read from the selected disk contains DS=1. DS also sets Examine.
9	HF	Header Failure is set during Read, Read Check, or Write if the header read from the selected disk does not compare with the cylinder, head, and sector number stored in the controller. HF also will set if a CRC error is detected at the end of the header field. HF sets Examine, and Controller Idle is set at the end of the sector.
8	WP	Write Protect is set if the WP bit is set in the Header Field Read when a Write with Protect is

attempted. WP also sets if a Format Write or Format Read is issued and the Format Switch is "Off". WP sets Examine, and Controller Idle is set at the end of the sector.

3.1.1.6 Drive Command (OC)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	DIS	EN	SET HD	SET CYL	—	—	SEEK	RE-STORE

The Drive Command is issued with an OC to devices "FC", "FD", "FE" or "FF". The command byte definitions are as follows when bits 10 and 11 are not both 1:

Disable - When this bit is set and Enable is reset, any interrupts which occur are queued and not passed on to the system.

Enable - When this bit is set and Disable is reset, any interrupt occuring is presented to the system.

Disarm - When both the Enable and Disable bits are set, no interrupts are generated or queued by the device. All pending interrupts are cleared.

Seek - When this command bit is set, the selected drive positions the heads to the cylinder previously loaded by a Set Cylinder command. If the drive cannot complete the Seek, the Seek Incomplete status bit is set. A Restore command must be issued to clear Seek Incomplete. When Seek overlaps are attempted by issuing Seeks to multiple drives, the program must wait for Controller Idle to set before issuing each Seek. No controller interrupt is generated in this case. A drive interrupt is generated and ATN set when a Seek operation completes, provided interrupts are enabled.

Restore - When this command bit is set, the selected drive moves its heads to cylinder 000. A drive interrupt occurs when the Restore operation is completed, if interrupts are enabled.

Set Head - This command bit causes the head address to be loaded to the selected drive.

Set Cylinder - This command bit causes the cylinder address to be stored in a register for a Seek command.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	RLS	CLR	1	1	SOP	SOM	DSE	DSL

When the command is issued (OC) with bits 10 and 11 both set, the definition is:

BIT	NAME	FUNCTION
8	RELEASE	This Command bit releases the drive in dual port operations, allowing alternate channel access.
9	CLEAR FAULT	This command bit resets the Drive Unsafe status bit and turns off the fault lamp on the drive if a fault no longer exists.
12	SERVO OFFSET PLUS	This command bit causes the heads to be offset from the on-cylinder position towards the spindle. This command is used only with Read and must not be used with Write.
13	SERVO OFFSET MINUS	This command bit causes the heads to be offset from the on-cylinder position away from the spindle. This command is used only with Read and must not used with Write.
14	DATA STROBE EARLY	This command bit causes the drive to shift the data window early in each bit cell during Read.
15	DATA STROBE LATE	This command bit causes the drive to shift the data window late in each bit cell during Read.

NOTE: The Data Strobe Early, Data Strobe Late, Servo Offset Plus, and Servo Offset Minus bits are all used individually to aid in recovering marginal data.

3.1.17 Drive Cylinder High (WD 0)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	0	0	0	0	0	C_{1K}	C_{512}	C_{256}

The Drive Cylinder High address is loaded as the first byte of a three byte sequence by issuing a WD to device "FC", "FD", "FE", or "FF".

3.1.18 Drive Cylinder Low (WD 1)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

The Drive Cylinder Low address is loaded as the second byte of a three byte sequence by issuing a WD to device "FC", "FD", "FE", or "FF".

3.1.1.19 Drive Head (WD 2)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	H_{128}	H_{64}	H_{32}	H_{16}	H_8	H_4	H_2	H_1

The Drive Head address is loaded as the third byte of a three byte sequence by issuing a WD to device "FC", "FD", "FE", or "FF".

3.1.1.20 Drive Status (SS)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	X	X	WP	—	ALT CBSY	DR UNS	DR NOT RDY	EX	SKI	OFFL

The Drive Status byte is read by issuing a Sense status to device "FC", "FD", "FE", or "FF". Status definitions are:

BIT	NAME	FUNCTION
15	OFF	Off-line Status is set for the selected drive if it is off-line or unsafe. If a Sense status is issued to a non-existent drive, Drive Not Ready and Off-Line are returned.
14	SKI	The Seek Incomplete bit is set when a drive fails to complete a Seek to a valid cylinder, a Restore, or a Servo Offset within a set time. Seek Incomplete also sets if the cylinder address given to the drive is invalid.
15	EX	The Examine bit is set whenever the Write Protect, Drive Unsafe, or ALT CBSY status bits are set.
12	DR NOT RDY	The Drive Not Ready status bit is set when the Drive is not in a ready state or during an access positioning operation.
11	DR UNS	The Drive Unsafe status bit is set when the drive detects an unsafe condition or fault. Drive Unsafe may be reset by a Clear Fault command if the fault no longer exists.
10	ALT CBSY	The Alternate Channel Busy bit is set in dual port operations if the drive is reserved or selected by the opposite channel and selection is attempted.
8	WP	The Write Protect status bit is set if the Write Protect switch on the drive is set.

3.2 Hardware Description

The major logic sections and busses of the SPECTRA 14 are described briefly below. Figure 1 presents a functional block diagram of the SPECTRA 14.

3.2.1 Host Microprocessor

The Host Microprocessor (HM) is a bit slice design using four 2901's. Two major busses in this section are the HMY BUS and HMD BUS. The HMY BUS is a 16 bit wide data path used for 2901 "Y" output destination. The HMD BUS is a 16 bit wide data path providing the four 2901's an input source on their "D" inputs. The firmware may select several destinations for the HMY BUS data and a variety of sources for the HMD BUS input data.

A 74S138 decoder determines the HMD BUS source by decoding the HMD BUS C0-C2 field of the microcode word. Similarly, a 74S138 decodes the HMREG C0-C2 field to control HMY BUS destinations.

Two other 74S138's decode the literal field to provide pulsed outputs used to set or clear control flip-flops.

A 9334 addressable latch decoding the literal field provides latched flags to control various interface functions.

The Sequencer for the HM consists of three 2911's. The 2911 sequencer provides the capability for addressing the control store from its program counter, performing jumps, conditional jumps, subroutine jumps, and subroutine returns. Up to 4 levels of subroutines may be nested in the 2911's. Up to 16 individual jump conditions can be tested, and all 16 bits of the HMY BUS can be individually tested for jumping. Additionally, two 74S374's provide a multi-way (or vector) jump to any location in the control store. The 2901 outputs on the HMY BUS (0-9) of the previous instruction may be used to supply the target address of the multi-way jump. The 2911 outputs are disabled during the multi-way jump taken from the two 74S374's.

The instruction width of the Host Microprocessor is 48 bits. 1Kx4 PROMs are used to form a 1Kx48 control store containing the firmware for the HM. The instruction word is defined below:

BIT	FUNCTION
47	HM FLAG ENABLE; Enables pulsed or latched flag generation from the literal field.
46	Spare.
44 - 45	HMY BUS CONTROL; defines the source of data supplied to the Y BUS.
41 - 43	HM REGISTER CONTROL; defines the destination register into which data on the Y BUS is directed.

38 - 40	HMD BUS CONTROL; defines the source of data to the 2901's on the D BUS.
37	HM CARRY IN; forces a carry-in to the ALU.
28 - 36	HM INSTRUCTION; these nine inputs to the 2901's determine the internal ALU data input, ALU function, and ALU destination (Q Reg, RAM Stack, or F Output).
24 - 27	HM A/B ADDRESS; selects one of sixteen registers in the 2901 RAM Stack.
19 - 23	HM BRANCH CONDITION SELECT; these four lines determine which branch/jump condition is selected to test for a true or false condition during jump type instructions.
16 - 18	HM NEXT ADDRESS CONTROL; these three lines are decoded by a 74S288 to control the 2911's and determine whether the address supplied to the control store is from the 2911's program counter, a branch target address, or from the address stored in the multi-way branch register. The 2911 stack is also controlled by the S288 decoder outputs to perform push or pop.
0 - 15	LITERAL FIELD; bits 0-10 of this field provide a base target address for jumps. If HM FLAG ENABLE equals zero, and a continue for a subroutine return instruction is specified, all 16 bits of the literal field supply a constant value, as microprogrammed, to the 2901 data inputs. If the FLAG ENABLE bit is on, literal field bits 11-15 are decoded to generate pulsed flags and bits 0-10 may be used for a destination address or a 10-bit constant or latched flags.

3.2.2 Disk Microprocessor

The Disk Microprocessor (DM) is a bit slice design using two 2901's. The DM is similar to the HM, but has an 8 bit data path. The DPY BUS is an 8 bit wide data path used for the 2901's input source on their "D" inputs. The firmware selects the destination register for the data on the DPY BUS and may select a variety of input sources on the DPD BUS.

Major destination register control is provided using a 74S138 to decode the DP register control field. Major source input control is provided with a 74S138 decoding the DP DATA BUS CONTROL field.

A 9334 addressable latch IC provides latched flags to control various SMD interface functions by decoding the DPNA BUS when the DP FLAG ENABLE bit within the instruction is "On".

The sequencer for the DM consists of three 2911's, as used in the HM. The 2911 sequencer provides addressing capability for the DM control store PROM's. Up to 16 individual conditions can be tested for jump instructions. No multi-way branch capability is provided in the DM.

The instruction width of the Disk microprocessor is 48 bits. 1Kx4 PROM's are used to form a 1Kx48 control store to contain the firmware. Definition of the DM instruction word is:

BIT	FUNCTION
47	DP FLAG ENABLE; enables pulsed or latched flag generation from the DPNA BUS bits 0 - 10.
46	LOAD S/D CONTROL (LDSDC); loads the S/D control register from data on the DPY BUS.
45	CARRY IN; generates a carry into the least significant 2901 ALU during arithmetic operations.
42 - 44	DP REG CONTROL; these three bits are decoded to determine the destination of data on the DPY BUS.
39 - 41	DP DATA BUS CONTROL; these three bits are decoded to determine the input sources to the 2901's on the DPD BUS.
38	D to Y ENABLE; this bit controls the gating of data on the DPD BUS directly onto the DPY BUS, bypassing the 2901's.
35 - 37	DP NEXT ADDRESS CONTROL; these three lines are decoded by a 74S288 to control the 2911 sequencers. Next address to the control store may be the 2911's program counter or a branch target address. Stack push/pop control is provided by the decode of these lines also.
31 - 34	BRANCH CONDITION; selects one of sixteen branch conditions to test during a jump type instruction.
22 - 30	DP INSTRUCTION BUS; these nine inputs to the 2901's determine the internal ALU input, ALU function, and ALU destination.
18 - 21	DP A BUS; selects one of sixteen registers in the 2901's RAM Stack.
14 - 17	DP B BUS; selects one of sixteen registers in the 2901's RAM Stack.

11 - 13	DP PULSED FLAGS; these three lines are decoded to generate pulsed flags to control various logic functions.
0 - 10	DP NEXT ADDRESS BUS; these lines provide a base target address during jump instructions, or a constant value, as microprogrammed, if CONSTANT ENABLE is true.

3.2.3 Disk Interface

The SMD disk interface is controlled by the Disk Microprocessor. The firmware transmits information on the SMD bus lines and tag lines by loading 74LS273 registers. MC3453 quad line drivers drive the SMD interface lines; MC3450 quad line receivers are used to receive signals on the SMD interface. The DM controls selection of the logical disk drive, interrupt status from the drive, cylinder/head selection, and selects one of four "B" cable ports for data transfer.

The serializer/deserializer uses a 74S299 eight bit shift register to convert data from parallel to serial during Writes and from serial to parallel during Reads. Parallel data is transferred 8 bits at a time from the Data Buffer comprised of four 2149 RAM's to two 74S374 registers during Write operations on the BUFD BUS. The data is then loaded into the 74S299 shift register, on a byte basis, over the BUF SD BUS. During Read operations, data is transferred from the S/D shift register into two 74LS374's a byte at a time and then into the Data Buffer.

The DM firmware is synchronized to the SMD interface by a bit counter which sets a word available flip-flop, WRD FF, each time the counter overflows (count 16). All format field switches, such as CRC, ECC, etc. occur at this time. The firmware pre-loads these controls into a holding register in the previous word time.

A 25LS2521 eight bit comparator is used to compare the SYNC byte read from the disk against a pre-defined, hardwired constant (HEX 19). This comparison is enabled when searching for SYNC during Reads or non-format Writes.

A 9401 IC is used to generate a CRC code appended to the header field . The CRC polynomial is $X^{16}+X^{15}+X^{2}+1$. The header information is divided by this polynomial during format Writes, and the remainder generated by the 9401 is appended to the last byte of the header. Then, when the header is read, the 9401 again divides the data read in the header by the same polynomial and compares the result with the CRC Read. Other than a zero output from the 9401 at the end of the CRC field is an error.

Each logical sector's data field has four bytes of ECC code appended. The ECC polynomial used is $X^{32}+X^{23}+X^{21}+X^{11}+X^{2}+1$. The ECC polynomial is implemented using four 74S273 register IC's with five 74S86 "exclusive or" gates forming the feedback terms. The ECC polynomial divides the data field as it is written, and the 32 bit ECC

is then appended to the data field. When the ECC is being written, it is shifted out without any feedback and acts as 32 bit shift register. When a sector's data field is read, the ECC hardware again divides it by the fixed polynomial. The ECC registers are tested at the end of the ECC field, and if found to be non-zero, the data is in error. Firmware first re-reads the sector, and if the error occurs again, the ECC correction routine is entered to determine the bit(s) in error and location within the sector. The data is then corrected within the data buffer before transfer to the SELCH.

Figure 1 presents a block diagram of the hardware described above.

3.3 FORMAT

Gap_1	S_1	Header	CRC	Gap_2	S_2	$Data_1$	ECC_1	Gap_3	S_3	$Data_2$	ECC_2	Gap_4
23	1	6	2	17	1	256	4	23	1	256	4	16

By using the above dual sector format, 33 physical or 66 logical sector are provided. This formatting scheme allows for an alternate sector since only 64 are used during normal operation. Unused sectors must have all "ones" written into the sector address portion of the header field.

Header Format:

Byte 0

0	1	2	3	4	5	6	7
Def Sec_1	Write $Prot_1$	0	0	0	0	0	0

Byte 1

0	1	2	3	4	5	6	7
Def Sec_2	Write $Prot_2$	0	0	0	0	0	0

Byte 2

0	1	2	3	4	5	6	7
0	0	S_{32}	S_{16}	S_8	S_4	S_2	S_1

Byte 3

0	1	2	3	4	5	6	7
0	0	H_{32}	H_{16}	H_8	H_4	H_2	H_1

Byte 4

0	1	2	3	4	5	6	7
0	0	0	0	0	C_{1K}	C_{512}	C_{256}

Byte 5

0	1	2	3	4	5	6	7
C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

During the Write Format or Read Format operations, the 6 header bytes plus 512 data bytes and 8 bytes of ECC per logical sector pair are transferred.

The 9775 disk drive may require entire tracks to be flagged depending on the media defect information supplied by the drive manufacturer. If defects are located so that more than one defect falls within the same sector, the ECC may miscorrect, and the track should not be used.

SPECTRA 14
Sector Format
66 Sectors/Track

Sector Pulse

Gap_1 S_1 Header CRC Gap_2 S_2 $Data_1$ ECC_1 Gap_3 S_3 $Data_2$ ECC_2 Gap_4

GAP_1	=	23 bytes of zeros
$SYNC_1$	=	1 byte of 19_{16}
HEADER	=	6 bytes: F_1, F_2, S, H, C_H, C_L (flag, sector, head, cylinder)
CRC	=	2 bytes cyclic check code: $X^{16} + X^{15} + X^2 + 1$
GAP_2	=	17 bytes of zeros
$SYNC_2$	=	1 byte of 19_{16}
$DATA_1$	=	256 bytes of data
ECC_1	=	4 bytes error correction code: $X^{32} + X^{23} + X^{21} + X^{11} + X^2 + 1$
GAP_3	=	23 bytes of zeros
$SYNC_3$	=	1 byte of 19_{16}
$DATA_2$	=	256 bytes of data
ECC_2	=	4 bytes of error correction code
GAP_4	=	16 bytes: 2 bytes of zero plus 14 bytes undefined.
		610 bytes per physical sector
		33 physical sectors per track
		66 logical sectors per track: 64 system sectors + 1 alternate.

NOTE: Each Header will contain a flag byte for Write Protect and Bad Sector flags for each logical sector. Flag Byte 1 is associated with Data Field 1, Flag Byte 2 with Data Field 2.

4.0 DIAGNOSTICS

4.1 Introduction

The diagnostic supplied with the SPECTRA 14 disk controller is a modified version of Perkin-Elmer's MSM Disc Test program. The differences can be summarized as follows:

(1) The SPECTRA 14 has a different physical format than the MSM controller. Therefore, all tests using format write/format read operations have been modified.

(2) The SPECTRA 14 does not utilize RPS or the off-line format write/format read operations. Therefore tests 18, 19 and 1C have been eliminated.

(3) Two new options have been added.

(a) LPCNT 0100
All tests which formerly did 1500 iterations now do "LPCNT" iterations, with a default of 256.

(b) FMT 0000
A "fast format" option has been provided under Test 17 if "FMT" is set to FFFF. This is the first operation which should be performed on a virgin pack to write the proper header information in all sectors on the pack. After this has been done, "FMT" should be set back to 0000 so that Test 17 and all re-formatting is done normally.

(4) Many disk types are available under the "PACTYP" option.

PACTYP	Cylinders	Heads	Disk Type	
0	823	5	80MB	
1	823	19	300MB	
2	842	40	675MB	With 2MB head per track
3	823	1	16MB	Removable cartridge
4	823	1	16MB	Fixed
5	823	3	48MB	Fixed
6	823	5	80MB	Fixed
7	823	4	66MB	
8	823	10	160MB	

Perkin-Elmer's MSM Disc Format program is not supported and is not necessary on the SPECTRA 14, because it utilizes the off-line format write/format read operations to perform an extensive pack analysis. The same results can be achieved using the "fast format" option on the modified MSM Disc Test program. Furthermore, the fact that the SPECTRA 14 utilizes ECC should significantly reduce the number of defective sectors flagged.

4.2 Operating Instructions

The SPECTRA 14 Diagnostic Tape consists of a RELLDR followed by the diagnostic. It should be loaded using the standard "50 Sequence" and started at A00. (The default I/O device specifier at A10 is 0202)

(1) Set all options desired including DISCON, PACTYP, and INBUF=10000, OUTBUF=1C000.

(2) SET FMT=FFFF and do a "fast format" using Test 17.

(3) Set HICYL= number of cylinders, FMT=0, SECNUM=3F and run Test 15 to read check the entire pack. At this point the pack is initialized and ready for further diagnostics or for OS/32 use.

5.0 SYSTEM SOFTWARE

The SPECTRA 14 runs under standard Perkin-Elmer OS/32 operating system software. If running on an 80MB or 300MB drive, no parameter changes are needed in the DCB. If running on a drive with different physical characteristics, the DCB must be modified to reflect these volume changes as follows:

(1) Find the address of the desired DCB in the SYSGEN map, e.g. "xxxx"

(2) BIAS xxxx

(3) Find the volume size and # of tracks/cylinder in the DCB listing. This is in the Device Dependent portion at locations 98-9E:

```
            98      0004    04C0    ;cylinders * tracks * 64
            9C      0040            ;64 sectors/track
            9E      0005            ;# tracks
```

(4)
```
        EXA     98      0004    04C0    0040  0005  . . .

        MOD     98      mmmm,   llll,   0040, tttt

                where   mmmm    = # of total sectors (MSB)
                        llll    = # of total sectors (LSB)
                        tttt    = # of tracks
```

(5) Restart at 60.

NOTE: Fixed/Removable Cartridge drives are only supported in Version 5.3 (and later) of OS/32.

APPENDIX A

SMD INTERFACE

The SMD interface is shown on the next two pages. The control signal cable, or "A" cable, is a 60 twisted pair flat cable. This cable is connected between the controller and first drive and is typically 10 or 15 feet long. Additional drives may be attached by daisy chaining a 6 foot twisted-pair flat cable between drives. A drive terminator must be installed on the last drive. All drives have a 26 conductor flat ribbon cable, "B" cable, connected radially between each drive and the controller. Normally a ground braid or wire must also be attached from the first drive to the system, and between drives. Spectra Logic does not supply this ground wire.

"A" CABLE

CONTROLLER			DRIVE LO, HI	
Unit Select Tag			22, 52	
Unit Select 2^0			23, 54	
Unit Select 2^1			24, 54	
Unit Select 2^3			27, 57	
Tag 1	2*		1, 31	
Tag 2	2*		2, 32	
Tag 3	2*		3, 33	
Bit 0	2*		4, 34	
Bit 1	2*		5, 35	
Bit 2	2*		6, 36	
Bit 3	2*		7, 37	
Bit 4	2*		8, 38	
Bit 5	2*		9, 39	
Bit 6	2*		10, 40	
Bit 7	2*		11, 41	
Bit 8	2*		12, 42	
Bit 9	2*		13, 43	
Open Cable Detector			14, 44	
Index	2*		18, 48	
Sector	2*		25, 55	
Fault	2*		15, 45	
Seek Error	2*		16, 46	
On Cylinder	2*		17, 47	
Unit Ready	2*		19, 49	
Address Mark Found	2*		20, 50	
Write Protected	2*		28, 58	
Power Sequence Pick			29	(one twisted pair)
Power Sequence Hold			59	
Busy	2*	1**	21, 51	
Bit 10	2*	3**	30, 60	

NOTE: 60 Position, 28 Awg., 30 twisted pair, flat cable, 100 ft. max.
1** Dual Channel units Only. 2* Gated by unit selected.
3* Bit 10 used for cylinder 1024 Bit for drives so equipped.

"B" CABLE

CONTROLLER	DRIVE LO, HI
Write Data	8, 20
Ground	7
Write Clock	6, 19
Ground	18
Servo Clock	2, 14
Ground	1
Read Data	3, 16
Ground	15
Read Clock	5, 17
Ground	4
Seek End	10, 23
Unit Selected	22, 9
Ground	21
Reserved for Index	12, 24
Ground	11
Reserved for Index	13, 26
Ground	25

NOTES:

1. 26 conductor shielded flat cable
   Maximum length - 50 ft.

2. No signals gated by Unit Selected.

	INITIAL RELEASE	7/10/86	MJ

HOST PROCESSOR

SCLR
CLOT
→ SYS RESET → RESET

SR
DR
DA
CMD
HW
BNE
SCHK
SYNC
SDSY
→ SELCH CONTROL → BRANCH COND INPUTS
→ CONTROL FLAGS

ADRS → CONTROLLER/DEVICE ADDRESS MATCH

CONTROL SEQUENCER 2911(x2) ← NEXT ADDR CONT ← BRANCH COND
CONTROL STORE 1K x 48
48
PIPELINE REGISTER
CONTROL
H→PDBUS 0-15
ALU 2901(x4)
SWITCHES → MUX
SELCH P DATA BUS TRANSCVR'S
SBUS 0-15
D00-D15
ACK DR
STATUS
SR
H→PYBUS 0-15
H→PDBUS 0-15

RACK
TACK
ATN
INTR CONT
→ ACK (BRANCH)
→ CLR ATN
→ SET ATN

BUFF WR REG 0-15
BUFF RD REG 0-15

DISK PROCESSOR

BRANCH COND ← NEXT ADDR CONT ← CONTROL SEQUENCER 2911 (x2)
CONTROL STORE 1K x 48
48
PIPELINE REGISTER
CONTROL
DPDBUS
ALU 2901 (x2)
DPYBUS
SERDES CONT
ECC/CRC CONT
FLAGS

HP BUFF ADDR CNTR
DP BUFF ADDR CNTR
BUFMA 0-9
DATA BUFF RAM 1K x 9 (x2)
BUF D BUS 0-15
BUFF WR REG
BUFF RD REG

SMD INTERFACE

DCLO → OPEN CABLE CIRCUIT
SMD REG A
"A" CABLE OUT DRIVERS → USEL TAG, USEL 0-2, TAG 1-3, BIT 0-9, OPEN CABLE
"A" CABLE IN REGISTER ← FAULT, SEEK END, ON CYL, U RDY, INDEX, SECTOR, WR PROT, BUSY
"B" CABLE IN RECVR'S (9 DRIVES) ← BRANCH INPUTS, SI DATA, RD DATA → (x4) U SELTD, RD DATA, RD CLK, SERVO CLK
"B" CABLE OUT DRIVERS (9 DRIVES) → (x4) WR DATA, WR CLK
ECC ERROR
ECC
CRC ERROR
CRC 9401
MUX
BYTE/WRD CNTR
BYTE/WRD LOGIC
BRANCH INPUTS
RD DATA
CLK
SER/DES
BUF SD BUS

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN MJ	7/10/86
CHECKED	

SPECTRA LOGIC

SPECTRA 14
BLOCK DIAGRAM

SCALE | SIZE D | DRAWING NO.

DO NOT SCALE DRAWING | SHEET