OMTI 5060

Scientific Micro Systems, Inc.

OMTI 5060
DMA BUFFER CONTROLLER CHIP
REFERENCE MANUAL
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GENERAL DESCRIPTION

1.1 INTRODUCTION

The OMTI 5060 Direct Memory Access Controller (DMAC) is an application-specific CMOS/VLSI integrated circuit mounted in a 68-pin plastic leaded chip carrier. The OMTI 5060 manages the flow of block-level information between memory and peripheral interfaces in advanced disk, tape and other controller designs.

A dual-bus structure is used so the peripheral transfers and the microprocessor can be operating at the same time without impacting the peripheral transfer rate or the performance of the microprocessor.

The OMTI 5060 DMAC provides five megabyte/second data transfers using four independently programmable DMA channels with bus access based on preassigned channel priority with channel 0 having the highest priority and channel 3 the lowest. Each channel has 16-bit Address and Count registers. The memory access cycle timing is programmable to match the DMA to different speed memories.

The device can be configured to interface with both Small Computer System Interface (SCSI) protocol and Quarter Inch Cartridge (QIC-02) protocol buses.

The 5060 DMAC is designed to be used with the OMTI 5050 Data Sequencer, the OMTI 5080 SCSI Controller or the OMTI 5090 bus controller, a RAM buffer and a byte-oriented microprocessor.

1.2 FEATURES

* Supports high performance dual-bus architecture.
* Four independent DMA channels.
* 5 megabyte device bandwidth.
* 16-bit Address and Count registers for each channel.
* Independent mask for channel-end interrupt.
* Configurable SCSI and QIC-02 Request/Acknowledge handshake protocol.
* Bus access resolved on channel priority basis.
* Strobe logic to read/write external registers on the microprocessor bus.
* Logic to latch and output the low order microprocessor address.
* Programmable Request/Acknowledge and interrupt polarity.
* Programmable auto count re-initialization.
* Programmable memory access cycle timing (2 to 5 clock cycles).
* Single 5-volt supply.
* Surface mount plastic 68-pin leaded chip carrier package.
* Low power consumption.

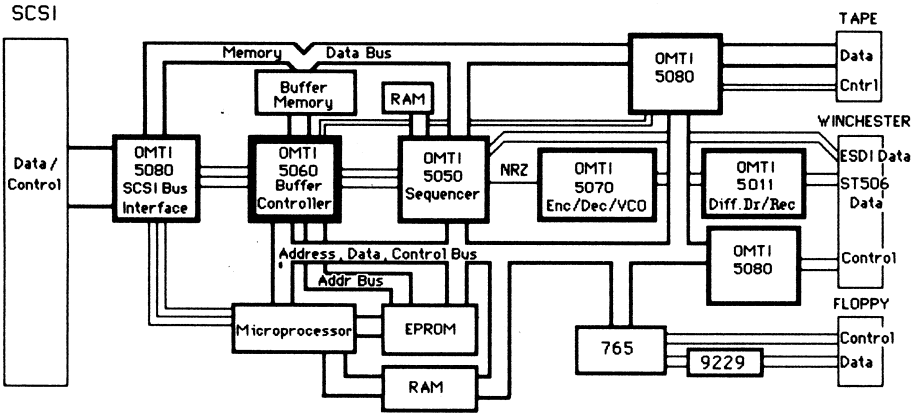


Figure 1-1 SYSTEM CONFIGURATION

Illustrated above is a typical system configuration, incorporating the OMTI 5060 DMAC chip. Also included in the diagram is the OMTI 5050 Data Sequencer, the OMTI 5080 bus controller chip and the OMTI 5070 VCO/Encode/Decode chip, and the OMTI 5011 Driver/Receiver chip.

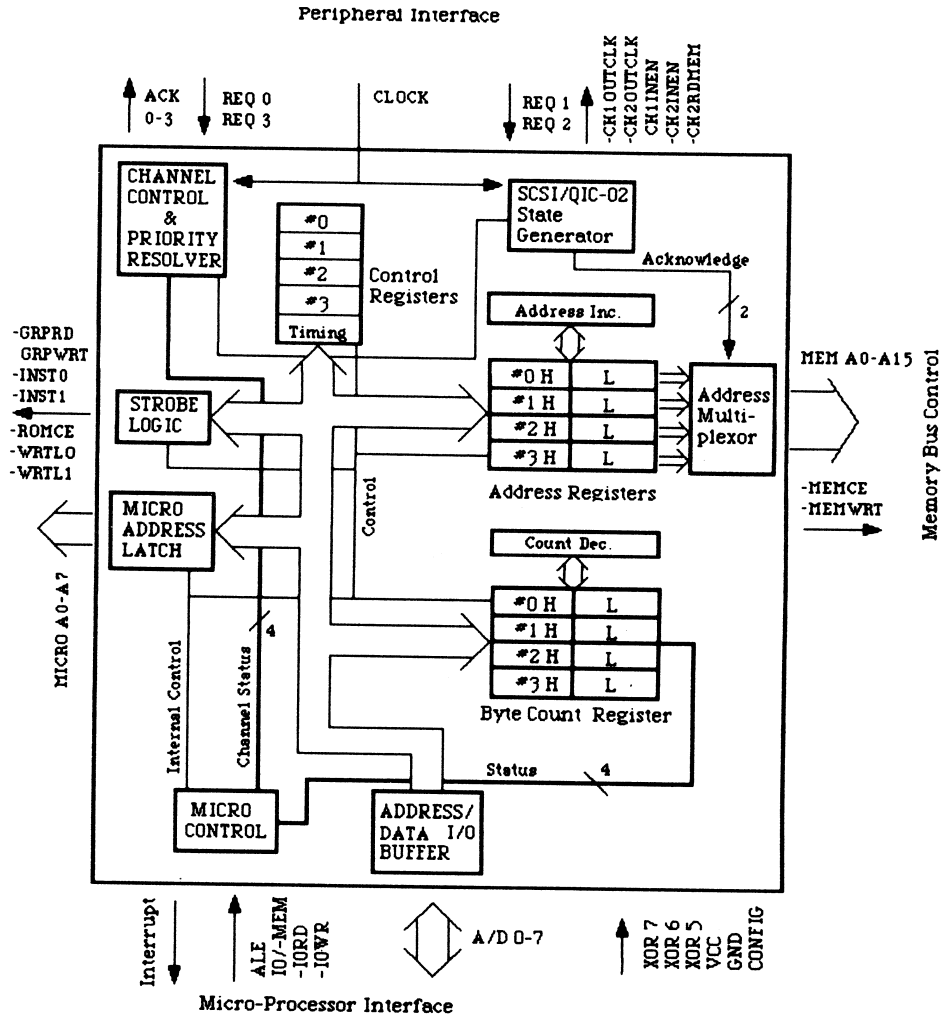


Figure 1-2 OMTI 5060 FUNCTIONAL BLOCK DIAGRAM

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The OMTI 5060 DMAC has four DMA channels which can be independently configured by software. Channel 1 can be programmed to interface to a QIC-02 bus, and Channel 2 can be programmed to interface to a SCSI bus (typically using the OMTI 5080 SCSI chip). The OMTI 5060 is designed to interface easily to a Z8- or 8051-type microprocessor. (Refer to the Timing Diagrams and Pin Descriptions for details.)

There are 13 Control registers and one Status register. The microprocessor can write the Control registers and read the Status register. Eight of the control registers are 16-bit registers, and five are 8-bit registers. Associated with each channel is a 16-bit Address register, a 16-bit Count register and an 8-bit Channel Control register. The DMAC also has a common Timing and Interrupt Polarity register. The Status register is an 8-bit register.

In addition to the registers, there are 12 decoded addresses that the microprocessor can use to read or write external registers. The addresses are given in the Register and Decode Address table. Four of these addresses are fully decoded in the chip and generate output strobes that can be used to latch data into an external register from the microprocessor bus (two outputs) or enable an external register onto the microprocessor bus (two outputs). The additional outputs are decoded as groups of four read and four write addresses which may be further decoded externally to the chip. The chip also has logic that latches the microprocessor address bits (MICRO A0-A7) and can be used to provide the low order address bits for the microprocessor external ROM and RAM.

2.2 REGISTERS

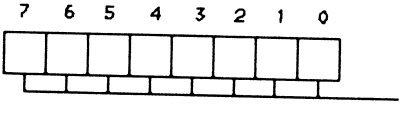
OMTI 5060 REGISTER AND DECODE ADDRESSES

A/D0-7	Write Functions		Read Functions	
00	WR00	Channel 0 Address, Lo Byte	RR00	Channel Status
01	WR01	Channel 0 Address, Hi Byte	RR01	Not Used
02	WR02	Channel 0 Word Count, Lo Byte	RR02	Not Used
03	WR03	Channel 0 Word Count, Hi Byte	RR03	Not Used
04	WR04	Channel 1 Address, Lo Byte	RR04	Not Used
05	WR05	Channel 1 Address, Hi Byte	RR05	Not Used
06	WR06	Channel 1 Word Count, Lo Byte	RR06	Not Used
07	WR07	Channel 1 Word Count, Hi Byte	RR07	Not Used
08	WR08	Channel 2 Address, Lo Byte	RR08	Not Used
09	WR09	Channel 2 Address, Hi Byte	RR09	Not Used
0A	WR0A	Channel 2 Word Count, Lo Byte	RR0A	Not Used
0B	WR0B	Channel 2 Word Count, Hi Byte	RR0B	Not Used
0C	WR0C	Channel 3 Address, Lo Byte	RR0C	Not Used
0D	WR0D	Channel 3 Address, Hi Byte	RR0D	Not Used
0E	WR0E	Channel 3 Word Count, Lo Byte	RR0E	Not Used
0F	WR0F	Channel 3 Word Count, Hi Byte	RR0F	Not Used
10	WR10	Channel 0 Control	RR10	Not Used
11	WR11	Channel 1 Control	RR11	Not Used
12	WR12	Channel 2 Control	RR12	Not Used
13	WR13	Channel 3 Control	RR13	Not Used
14	WR14	Timing and Interrupt Polarity	RR14	Not Used
15	WR15	Not Used	RR15	Not Used
16	WR16	Not Used	RR16	Not Used
17	WR17	Not Used	RR17	Not Used
18	WA18	External Out Strobe 0	RA18	External in Strobe 0
19	WA19	External Out Strobe 1	RA19	External in Strobe 1
1A	WA1A	Not Used	RA1A	Not Used
1B	WA1B	Not Used	RA1B	Not Used
1C	WA1C	External Out Group Strobe	RA1C	External In Group Strobe
1D	WA1D	External Out Group Strobe	RA1D	External In Group Strobe
1E	WA1E	External Out Group Strobe	RA1E	External In Group Strobe
1F	WA1F	External Out Group Strobe	RA1F	External In Group Strobe

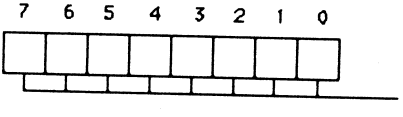
WR = Write Register. RR = Read Register.
WA = Write Address. RA = Read Address.

2.2.1 ADDRESS REGISTERS

WRITE REGISTERS 0, 4, 8, 12 (Hex) MEMORY ADDRESS 0-7



WRITE REGISTERS 1, 5, 9, 11 (Hex) MEMORY ADDRESS 8-15

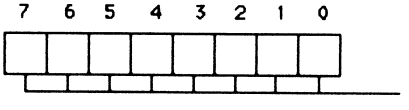


Each channel has a 16-bit Address register that is asserted on the memory address bus during the DMA cycle. After each DMA transfer, the Address register is incremented. When the address FFFF(hex) is incremented, it goes to 0000.

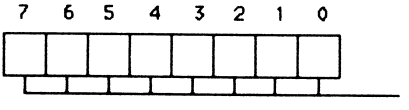
The Address register should be loaded with the starting address of the DMA data block that is going to be transferred. Legal values are 0000 through FFFF.

2.2.2 COUNT REGISTERS

WRITE REGISTERS 2, 6, A, E (Hex) WORD COUNT 0-7



WRITE REGISTERS 3, 7, B, F (Hex) WORD COUNT 8-15



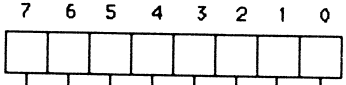
Each channel has a 16-bit count register that contains the number of DMA cycles +1 remaining to complete the block transfer. This register should be loaded with the number of cycles -1 required to transfer the block. The number of cycles is equal to the number of bytes in the block if the memory bus is an 8-bit bus.

The count register is decremented at the end of each DMA cycle. Legal counts are 0000 through FFFF.

2.2.3 Channel Control register addresses: CHANNEL 0 - WR10(HEX)
CHANNEL 1 - WR11(HEX)
CHANNEL 2 - WR12(HEX)
CHANNEL 3 - WR13(HEX)

CHANNEL CONTROL REGISTERS

WRITE REGISTERS 10,11,12,13(HEX): CHANNEL CONTROL
(CH 0 = 10, CH 1 = 11, CH 2 = 12, CH 3 = 13)



0 = Channel Disable
1 = Channel Enable

0 = Read RAM (Write Peripheral)
1 = Write RAM(Read Peripheral)

0 = Count Register
Auto Re-Load Disabled
1 = Count Register
Auto Re-Load Enabled

0 = Channel Interrupt Disable
1 = Channel Interrupt Enable

0 = Transfer Count Complete =
Channel Disable
1 = Channel Always Enabled

0 = Request Low to High Edge
1 = Request High to Low Edge

0 = Acknowledge Low Strobe
1 = Acknowledge High Strobe

CHANNEL 0 Bit 7 is reserved. Set = 0.

CHANNEL 1 0 = DMA REQ/ACK Protocol
1 = QIC-02 XFER/ACK Protocol

CHANNEL 2 0 = DMA REQ/ACK Protocol
1 = SCSI REQ/ACK Protocol

CHANNEL 3 Bit 7 is reserved. Set = 0.

Bit 0 Channel Enable/Disable: Bit 0 specifies if the channel is enabled or disabled. If Bit 0 is set (1) the channel is enabled and if it is cleared, the channel is disabled.

Bit 1 Transfer Direction: Bit 1 specifies the direction of data transfers: when set (1), data is transferred from the memory (memory read) to the peripheral; when cleared (0), data is transferred from the peripheral device to the memory (memory write).

Bit 2 Count/Auto Re-Load Register: Bit 2 enables or disables the automatic reloading of the Count register. If bit 2 is set (1), the channels Count register will be reloaded with its initial value at the completion of each transfer. If bit 2 is cleared (0), the Count register will not be reloaded. If the automatic reload feature is not used but the count is being used, (bit 4 set (1)) the Count register should be loaded before every transfer. The auto-reload feature allows a sequence of blocks to be transferred via DMA without requiring re-initialization of the channel's Address and Count registers prior to each transfer.

Bit 3 Channel Interrupt: Bit 3 enables or disables the setting of the INTERRUPT signal. If bit 3 is set (1), then the clearing of the Channel Enable bit will set the INTERRUPT signal. If bit 3 is cleared (0), the setting of the INTERRUPT signal is inhibited. If the Channel Interrupt Enable bit, bit 3, is set (1) and bit 4 is cleared (0), then the INTERRUPT signal will be set when a transfer completes and the Channel Enable bit is cleared. The INTERRUPT signal is cleared on any write to the control register of the channel that set it.

Bit 4 Disable Channel on Transfer Complete: Bit 4 controls whether the channel transfer count is used to disable the channel when the block transfer is complete. If bit 4 is cleared (0), the channel enable bit (Bit 0) will be cleared when the transfer is complete (number of DMA cycles = count +1.) If bit 4 is set (1), exhausting the transfer count has no effect on the channel enable.

Bit 5 Request Polarity: Each channel can be programmed to respond to the high to low or low to high transition of its request signal. When bit 5 is cleared (0), the request is initiated by a low to high transition. When bit 5 is set (1), the request is initiated by a high to low transition.

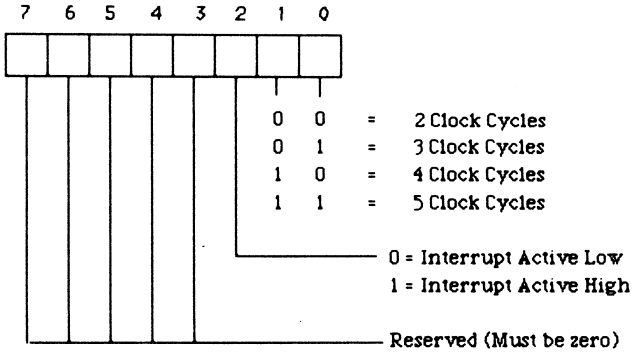
Bit 6 Acknowledge Polarity: The acknowledge strobes for each channel can be programmed to be high active or low active signals. When bit 6 is cleared (0), the acknowledge strobe is low active. When bit 6 is set (1), the acknowledge strobe is high active. The programmability of the request and acknowledge signals is useful for matching the DMA chip to the external hardware.

Bit 7 Channel:

CHANNEL 0: Bit 7 is reserved and should be 0 in all channel 0 commands.
CHANNEL 1: Bit 7 selects the QIC-02 transfer/acknowledge data transfer handshake protocol or the standard DMA memory request/acknowledge protocol for channel 1 peripheral transfers. When bit 7 is cleared (0), the channel will use the standard DMA memory request/acknowledge protocol. When bit 7 is set (1), the channel uses the QIC-02 transfer/acknowledge data transfer handshake protocol.
CHANNEL 2: Bit 7 selects the SCSI request/acknowledge data transfer handshake protocol or the standard DMA memory request/acknowledge protocol for channel 2 peripheral transfers. When bit 7 is cleared (0), the channel will use the standard DMA memory request/acknowledge protocol. When bit 7 is set (1), the channel uses the SCSI transfer/acknowledge data transfer handshake protocol.
CHANNEL 3: Bit 7 is reserved and should be 0 in all channel 3 commands.

2.2.4 Timing and Interrupt Register

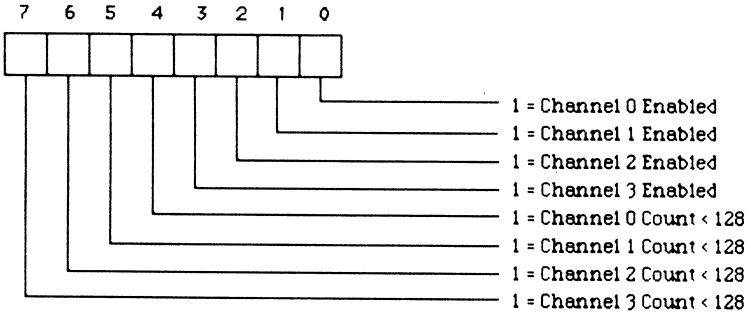
WRITE REGISTER 14(Hex)
MEMORY CYCLE TIMING and INTERRUPT POLARITY



Bits 0 and 1 specify the number of clock cycles used in the memory cycle for each memory transfer. This feature is provided to allow the Memory Controller to accommodate both low-speed and high-speed memories.
Bit 2 specifies the polarity of the DMA's Interrupt line (pin 60). When bit 2 is cleared (0), the INTERRUPT is an active low signal. When bit 2 is set (1), the INTERRUPT is an active high signal.
Bits 3-7 are reserved. (Must be set to zero)

2.2.5 Status Register

READ REGISTER 00(HEX): STATUS



The 8-bit Status register provides information about each channel and may be read at any time. The Channel Status Enable bits (Bits 0 thru 3) reflect the state of the respective Channel Enable bits. The Channel Status Count bit (Bits 4 thru 7) are set when the count in that channel's Count register is 00 to 7F(HEX). This allows the microprocessor to monitor the progress of data transfers and manage the loading and unloading of the buffer accordingly.

NOTE: The count in the Count registers, when a transfer is complete, is FFFF(HEX) so the Count Status bit will be 0.

2.3 OTHER LOGIC

2.3.1 STROBE LOGIC

In addition to the above registers, there are addresses in the chip address space that can be read/written by the microprocessor to read or write an external register.

WRITE ADDRESSES WA18 thru WA1F:

Address 18(HEX):External Out Strobe 0:Asserts -WRTL0 (Pin 55)
Address 19(HEX):External Out Strobe 1:Asserts -WRTL1 (Pin 56)
Address 1C(HEX):External Out Group Strobe:Asserts -GRPWRT(Pin 50)
Address 1D(HEX):External Out Group Strobe:Asserts -GRPWRT(Pin 50)
Address 1E(HEX):External Out Group Strobe:Asserts -GRPWRT(Pin 50)
Address 1F(HEX):External Out Group Strobe:Asserts -GRPWRT(Pin 50)

READ ADDRESSES RA18 thru RA1F:

Address 18(HEX):External In Strobe 0:Asserts -INST0 (Pin 53)
Address 19(HEX):External In Strobe 1:Asserts -INST1 (Pin 51)
Address 1C(HEX):External In Group Strobe:Asserts -GRPRD(Pin 49)
Address 1D(HEX):External In Group Strobe:Asserts -GRPRD(Pin 49)
Address 1E(HEX):External In Group Strobe:Asserts -GRPRD(Pin 49)
Address 1F(HEX):External In Group Strobe:Asserts -GRPRD(Pin 49)

2.3.2 MICRO-PROCESSOR ADDRESS LOGIC (ALE Bus Latch)

There is logic in the chip to demultiplex and latch the address from the microprocessor A/D bus. The address is available on the bus lines MICROA0-A7. This address may be used to access the microprocessor's external ROM and RAM.

2.4 INITIALIZATION

The OMTI 5060 chip should be initialized before its first use after power-up. The control registers should be loaded to disable the channels, to clear any interrupts and to set the correct polarity for the request and acknowledge signals. The memory cycle timing and interrupt signal polarity also need to be initialized. The Count and Address registers can be initialized now to save time later, but it is not necessary if they will be loaded with the correct values before any transfers are done on their channel.

Initialization flowchart: This flowchart is being provided to facilitate your firmware development. It is supplied as a guide and should be used as such.

Flowchart To Initialize OMTI 5060 DMAC

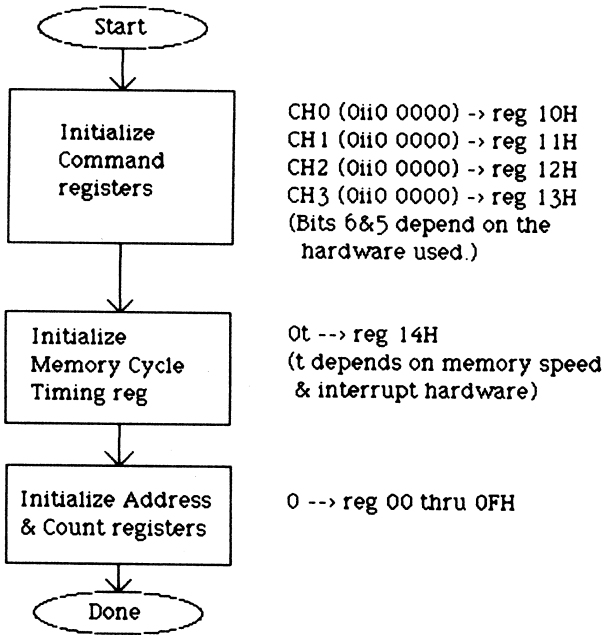


Figure 2-1

SECTION 3

INTERFACING

3.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
ACK0 ACK1 ACK2 ACK3	O O O O	25 23 21 19	DMA Acknowledge. (Active High.) These signals notify the individual peripherals when one has been granted a memory cycle. Polarity of all ACK outputs is programmable (Bit 6, Channel Control register.) When channel 1 is configured for the QIC-02 protocol, ACK 1 is configured for the QIC-02 XFER signal; when channel 2 is configured for the SCSI protocol, ACK 2 is configured for the SCSI REQ signal.
A/D0- A/D7	I/O	2-9	Address/Data Bus. (Active High, 3-state.) These multiplexed lines interface with the low-order 8 bits of the microprocessor's Address/Data bus. Addresses are latched into the DMA's address buffer on the falling edge of ALE. If the address is within the range of the internal chip select, data is either written into or read from the DMA's registers.
ALE(8051 mode) -AS(Z8 mode)	I	68	Address Latch Enable. (Active High.) Address Strobe (Active Low) When in the 8051 mode, the falling edge of this signal is used to latch the address on the microprocessor bus (A/D0-A/D7) into the internal address buffer. When in the Z8 mode, the rising edge is used to latch the address.
-CH1OUTCLK	O	57	Channel 1 Out Clock. (Active Low.) This output is used to strobe data from a memory read cycle into a register of the QIC-02 interface.
-CH2OUTCLK	O	46	Channel 2 Out Clock. (Active Low.) This output is used to strobe data from a memory read cycle into a register of the SCSI interface.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Type	Pin #	Name and Function
CH1INEN	O	58	Channel 1 Input Enable. (Active High.) This output signal is used to enable data for the memory write cycle from a QIC-02 interface register.
-CH2INEN	O	47	Channel 2 Input Enable. (Active Low.) This output signal is used to enable data for the memory write cycle from a SCSI interface register.
-CH2RDMEM	O	48	Channel 2 Read Memory. (Active Low.) This output is used for the SCSI I/O interface signal and is a direct output of bit 1 of the Channel 2 Control register.
CLOCK	I	51	Clock. (Active High.) This input controls the internal arbitration of all REQ and ACK signals. It also controls the programmable memory-cycle timing (WR20), as well as the SCSI and QIC-02 protocol sequences (See Timing Diagrams.) The maximum clock frequency is 20 MHZ.
CONFIG	I	64	Configuration. (Active High.) This input is pulled up internally to select the microprocessor strobe inputs. When this line is grounded, the chip is configured for an 8051-type processor. When the line is left open, the chip is configured for a Z8-type processor, with the following interface changes: -IORD = -DATA STROBE, -IOWR = R/-W, ALE = -AS, IO/-MEM = -DM. (Refer to A. C. characteristics.)
-GRPRD	O	49	Group Read Strobe. (Active Low.) This output is strobed whenever the micro-processor reads addresses RA1C, RA1D, RA1E or RA1F. It can be used to enable status onto the microprocessor bus (A/DO-7). It can be further decoded external to the chip.

PIN DESCRIPTIONS (CONTINUED)

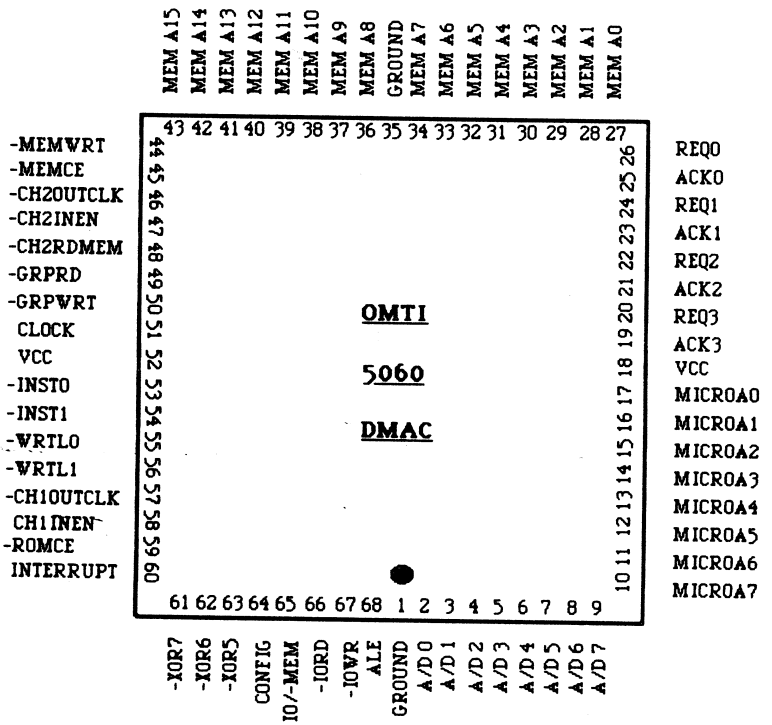
Symbol	Type	Pin #	Name and Function
-GRPWRT	O	50	Group Write Strobe. (Active Low.) This output is strobed whenever the microprocessor does a write to addresses WA1C, WA1D, WA1E or WA1F. It can be used to latch information from the microprocessor bus (A/D0-7) into an external register. It can be further decoded external to the chip.
-INST0	O	53	In Status 0-1. (Active Low.) These outputs are internally decoded I/O read strobes (enabled by reading from RA18 or RA19, respectively), used by the microprocessor to read device status via an external buffer to the microprocessor bus (A/D0-7).
-INST1	O	54	
INTERRUPT	O	60	Interrupt. (Active High.) INTERRUPT is asserted whenever the Channel Interrupt Enable bit, in that channel's Control register, is set and Channel Enable goes to a zero. It is de-asserted whenever the microprocessor does a write to the Channel Control register of the interrupting channel. The polarity of the interrupt line is specified by bit 2 in the Memory Cycle Timing register (WR14).
IO/-MEM (8051 mode)	I	65	I/O/-Memory (I/O Active High, Memory Active Low.)
-DM(Z8 mode)			-Data Memory (Active Low.) This signal is used for active high chip enable. When in 8051 mode, this line is connected to the 8051's IO/MEM line; in Z8 mode, this line is an active low chip enable.
-IORD (8051 mode)	I	66	I/O Read. (Active Low.) This input, when low, enables the -DS(Z8 mode) information from the register selected by the previously latched address onto the microprocessor bus (A/D0-7).
			Data Strobe. (Active Low.) This input, when low, provides the timing for data movement to or from selected registers and the microprocessor bus (A/D0-7).

PIN DESCRIPTIONS (CONTINUED)

Symbol	Type	Pin #	Name and Function
-IOWR (8051 mode) R/-W(Z8 mode)	I	67	I/O Write. (Active Low.) When this input is low, it gates information from the microprocessor bus (A/D0-7) into the register selected by the previously latched address. Read/Write. (Active High.) This signal determines the direction of the data transfer. When low, data is written from the microprocessor bus (A/D0-7) to the DMA. It is high when not doing writes.
MEMA0-7 MEMA8-15	O O	27-34, 36-43	Memory Address. (Active High.) The Memory Address bus is used to output the contents of the Address register of the currently selected channel to the DMA buffer memory.
-MEMCE	O	45	Memory Chip Enable. (Active Low.) -MEMCE is an active low strobe used to enable the DMA buffer memory addressed by MEMA0-15.
-MEMWRT	O	44	Memory Write. (Active Low.) When both this output and -MEMCE are asserted, data is written to the selected memory location in the DMA buffer memory. When this output is de-asserted and -MEMCE is asserted, data is enabled from the selected memory location in the DMA onto the buffer memory bus.
MICROA0-MICROA7	O	17-10	Micro Address. (Active High.) This 8-bit address bus is the address demultiplexed from the microprocessor's A/D bus, which is latched on the falling edge of ALE. This bus may be used to access the microprocessor's external memory and peripherals.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Type	Pin #	Name and Function
REQ0	I	26	DMA Request. (Active High.)
REQ1	I	24	These lines are asynchronous request
REQ2	I	22	inputs used by peripheral devices to
REQ3	I	20	obtain DMA service. The priority is fixed, with REQ0 having the highest priority, and REQ3 the lowest. Polarity of all REQ inputs is programmable. When channel 1 is configured for the QIC-02 protocol, REQ1 is configured for the QIC-02 ACK signal; when channel 2 is configured for the SCSI protocol, REQ2 is configured for the SCSI ACK signal.
-ROMCE	O	59	ROM Chip Enable. (Active Low.) This output is true when -IORD is true and both -IOWR and IO/-MEM are false.
-WRTL0	O	55	Write Latch 0-1. (Active Low.)
-WRTL1	O	56	These outputs are internally decoded write strobes (enabled by writing to WA18 or WA19, respectively), used by the microprocessor to write device control information to an external buffer from the A/D0-7 bus.
-XOR 5	I	63	Exclusive OR Address. (Active Low.)
-XOR 6	I	62	These internally pulled up signals are
-XOR 7	I	61	used for internal chip select. They control the polarity of the corresponding address lines. If another group chip select is required, the appropriate line must be grounded.
VCC	I	18, 52	+5 V.
GND	I	35, 1	Ground.



OMTI 5060 DIRECT MEMORY ACCESS CONTROLLER

Figure 3-1

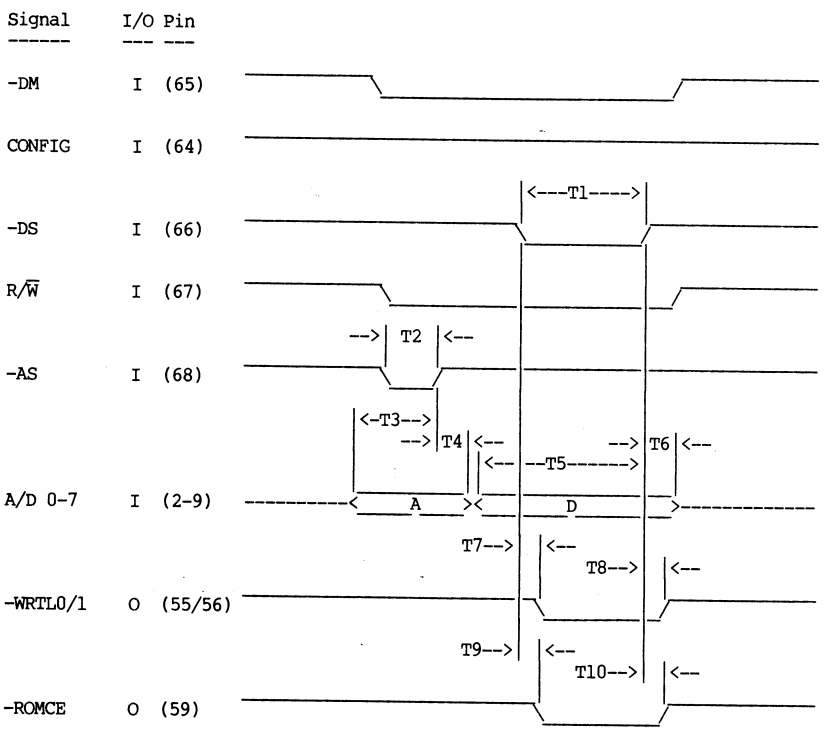
3.2 A. C. CHARACTERISTICS

The two relevant timing diagrams and A.C. characteristics for interfacing the 5060 Memory Controller are given below. (For more information about these chips, the reader is referred to Zilog's Z8681/82 ROMless Z8 Microcomputer Product Specification or Intel's 8051 Single Chip 8-Bit N-Channel Microprocessor Data Sheet.)

Z8 Mode Timing Characteristics (Configuration = 1)

Number	Parameter	Min (ns) (10 MHz)	Max (ns) (10 MHz)
1	-AS Low Pulse Width	50	
2	Address Setup to -AS High	25	
3	Address Hold after -AS High	25	
4	-AS High to -DS Low	50	
5	-DS Low Pulse Width	100	
6	-DS High to -AS Low	40	
7	Data Setup to -DS (Write)	25	
8	Data Hold after -DS (Write)	25	
9	-DS Low to Data Valid (Read)		50
10	-DS High to Data Invalid (Read)	0	
11	-DS High to Data Float (Read)		35

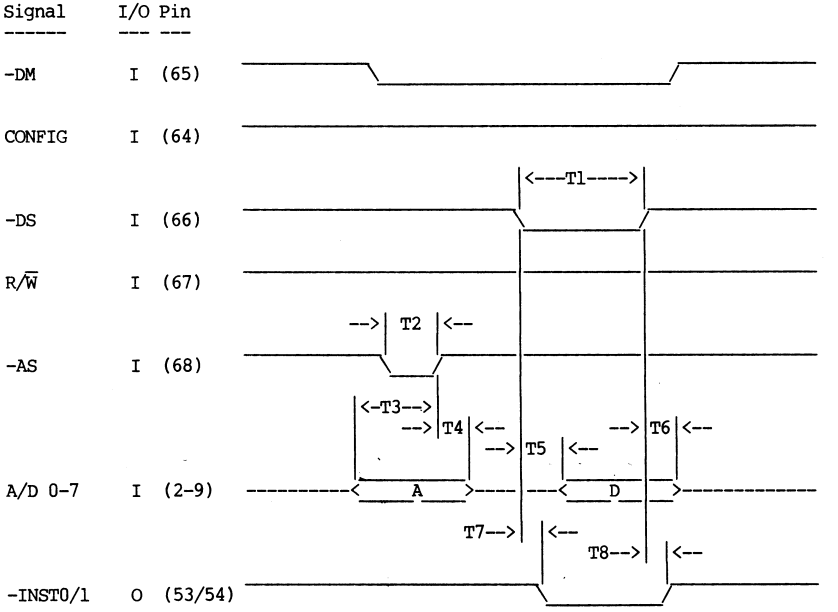
WRITE OPERATION, Z8 CONFIGURATION



VCC = 5.0V, TA = 25°C

Symbol	Item	min	typ	max	unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS High	25			ns
T4	Address Hold after -AS High	25			ns
T5	Data Setup to -DS High	25			ns
T6	Data Hold After -DS High	25			ns
T7	-DS _ to -WRLT0/1 _ Delay		28		ns
T8	-DS _/ to -WRLT0/1 _/ Delay		20		ns
T9	-DS _ to -ROMCE _ Delay	24			ns
T10	-DS _/ to -ROMCE _/ Delay	25			ns

3.2.2 READ OPERATION, Z8 CONFIGURATION



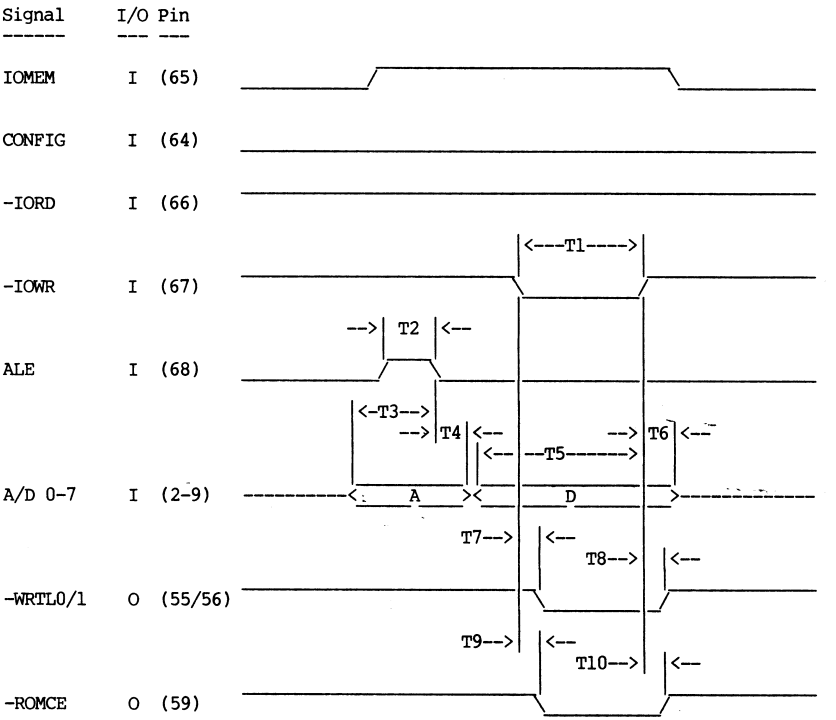
VCC = 5.0V, TA = 25°C

Symbol	Item	min	typ	max	unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS High	25			ns
T4	Address Hold after -AS High	25			ns
T5	Data Valid from -DS Low			50	ns
T6	Data Float After -DS High		35		ns
T7	-DS \ to -INST0/1 \ Delay		30		ns
T8	-DS / to -INST0/1 / Delay		20		ns

8051 Mode Timing Characteristics (Configuration = 0)

Number	Parameter	Min (ns) (10 MHz)	Max (ns) (10 MHz)
1	ALE High Pulse Width	50	
2	Address Setup to ALE Low	25	
3	Address Hold after ALE Low	25	
4	ALE Low to -IORD/-IOWR Low	50	
5	-IORS/-IOWR Low Pulse Width	100	
6	Data Setup to -IOWR High	40	
7	Data Setup after -IOWR High	25	
8	Data Hold after -IOWR High	25	
9	-IORD Low to Valid Data		50
10	-IORD High to Data Invalid	0	
11	-IORD High to Data Float		35

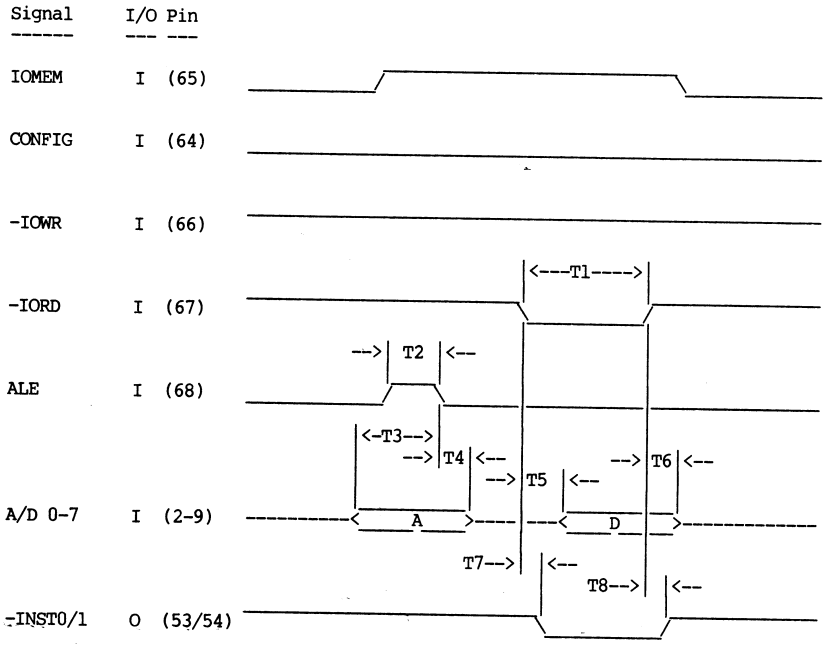
3.2.3 WRITE OPERATION, 8051 CONFIGURATION



VCC = 5.0V, TA = 25°C

Symbol	Item	min	typ	max	unit
T1	-IOWR Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE Low	25			ns
T4	Address Hold after ALE Low	25			ns
T5	Data Setup to -IOWR High	25			ns
T6	Data Hold After -IOWR High	25			ns
T7	-IOWR \ to -WRLT0/1 \ Delay		28		ns
T8	-IOWR _/ to -WRLT0/1 _/ Delay		20		ns
T9	-IOWR \ to -ROMCE \ Delay	24			ns
T10	-IOWR _/ to -ROMCE _/ Delay	25			ns

3.2.4 READ OPERATION, 8051 CONFIGURATION

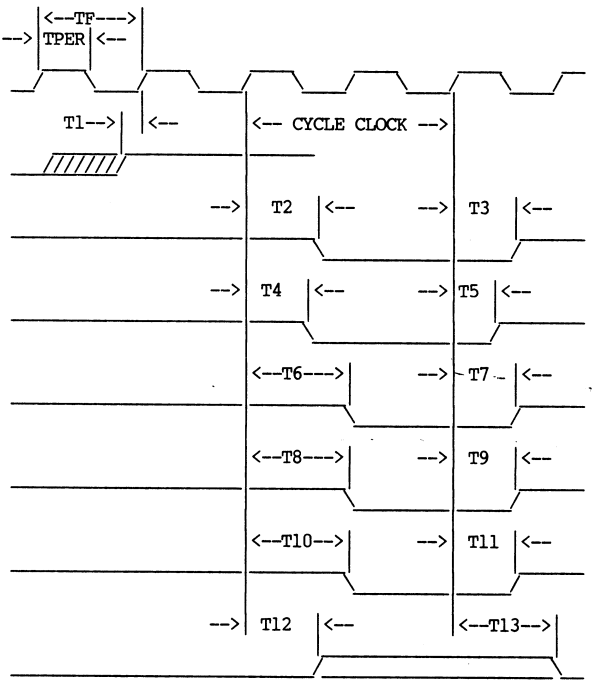


VCC = 5.0V, TA = 25°C

Symbol	Item	min	typ	max	unit
T1	-IORD Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE Low	25			ns
T4	Address Hold after ALE Low	25			ns
T5	Data Valid from -IORD Low			50	ns
T6	Data Float After -IORD High		35		ns
T7	-IORD \ to -INST0/1 \ Delay		30		ns
T8	-IORD _/ to -INST0/1 _/ Delay		20		ns

3.2.5 DMA MEMORY WRITE/READ

Signal	I/O	Pin
CLOCK	I	(51)
REQ 0,1, 2,3	I	(26,24 22,20)
-ACK 0,1, 2,3	O	(25,23, 21,19)
-MEMCE	O	(45)
-MEMWRT	O	(44)
-CH1,2 OUTCLK	O	(57,46)
-CH1,2 INEN	O	(58,47)
MEM A 0-15	O	(27-34, 36-43)

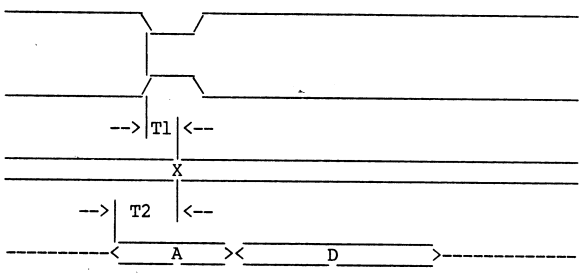


Symbol	Item	min	typ	max	unit
TF	CLOCK frequency			20	MHZ
TPER	Duty Cycle		60/40		%
T1	REQ to CLOCK Setup		25		ns
T2	CLOCK _/ to -ACK true delay		54		ns
T3	CLOCK _/ to -ACK false delay		50		ns
T4	CLOCK _/ to -MEMCE true delay		42		ns
T5	CLOCK _/ to -MEMCE false delay		36		ns
T6	CLOCK _/ to -MEMWRT true delay		74		ns
T7	CLOCK _/ to -MEMWRT false delay		46		ns
T8	CLOCK _/ to -OUTCLK true delay		52		ns
T9	CLOCK _/ to -OUTCLK false delay		53		ns
T10	CLOCK _/ to -INENABLE true delay		52		ns
T11	CLOCK _/ to -INENABLE false delay		53		ns
T12	CLOCK _/ to ADDRESS valid delay		54		ns
T13	CLOCK _/ to ADDRESS invalid delay		78		ns

CYCLE CLOCKS ARE 2 - 5 CLOCK PERIODS, AS PROGRAMMED

3.2.6 MICRO A 0-7, Z8 / 8051 CONFIGURATION

Signal	I/O	Pin
-AS (Z8)	I	(68)
ALE (8051)	I	(68)
MICRO A 0-7	O	(17-10)
A/D 0-7	I	(2-9)



VCC = 5.0V, TA = 25°C

Symbol	Item	min	typ	max	unit
T1	-AS/ALE to MICRO A 0-7 Valid Delay	36			ns
T2	A/D 0-7 to MICRO A 0-7 Valid Delay	26			ns

Multiplication factors to convert from nominal environment:

Process	+1 std. deviation	1.35
	-1 std. deviation	0.65
Voltage	4.75V	1.06
	5.25V	0.95
Temperature	$0^{o}C$	0.93
	$70^{o}C$	1.15

3.3 D. C. INFORMATION

Absolute Maximum Ratings:

* Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.

* Ambient operating temperature is 0 degrees C. to +70 degrees C.

* Storage temperature ranges from -65 degrees C. to +150 degrees C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

Standard Test Conditions:

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

* +4.75 V < VCC < +5.25 V

* GND = 0 V

* 0 degrees C. < TA < +70 degrees C.

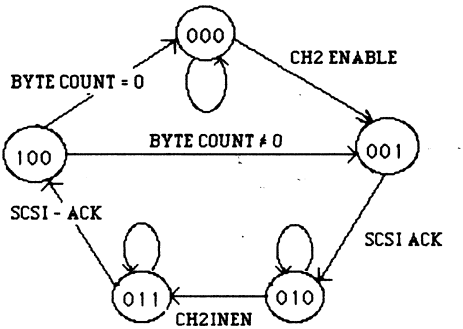
D. C. Characteristics:

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2	VCC	V		
Output Low Voltage		0.4	V		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

APPENDIX A

APPLICATION NOTES

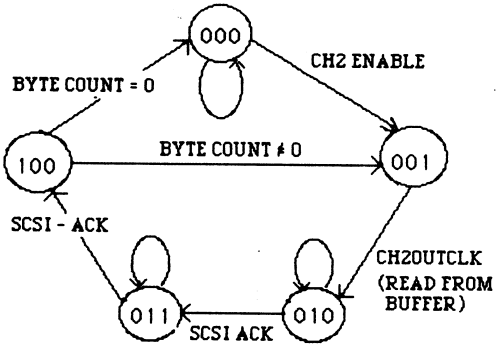
Transfer from host to memory via SCSI



STATE	ACTION	WAIT FOR
000		Channel 2 Enable
001	Assert SCSI REQ	SCSI -ACK
010	Assert internal memory REQ De-assert SCSI REQ Memory write	
011	De-assert internal request	SCSI -ACK
100	Check byte count If count 0: De-assert Enable & if Int enabled: Assert INT	

Figure A1

Transfer from memory to host via SCSI



STATE	ACTION	WAIT FOR
000		Channel 2 Enable
001	Assert internal memory REQ	
	Memory read	
010	Assert SCSI REQ	SCSI -ACK
	De-assert internal request	
011	De-assert SCSI REQ	SCSI -ACK
100	Check byte count	
	If count 0: De-assert Enable &	
	if Int enabled: Assert INT	

Figure A2

FLOWCHART TO SHOW TRANSFER OF DATA TO THE HOST USING OMTI 5080 SCSI CHIP, WITH INTERRUPTS AFTER EACH BLOCK IS TRANSFERRED.

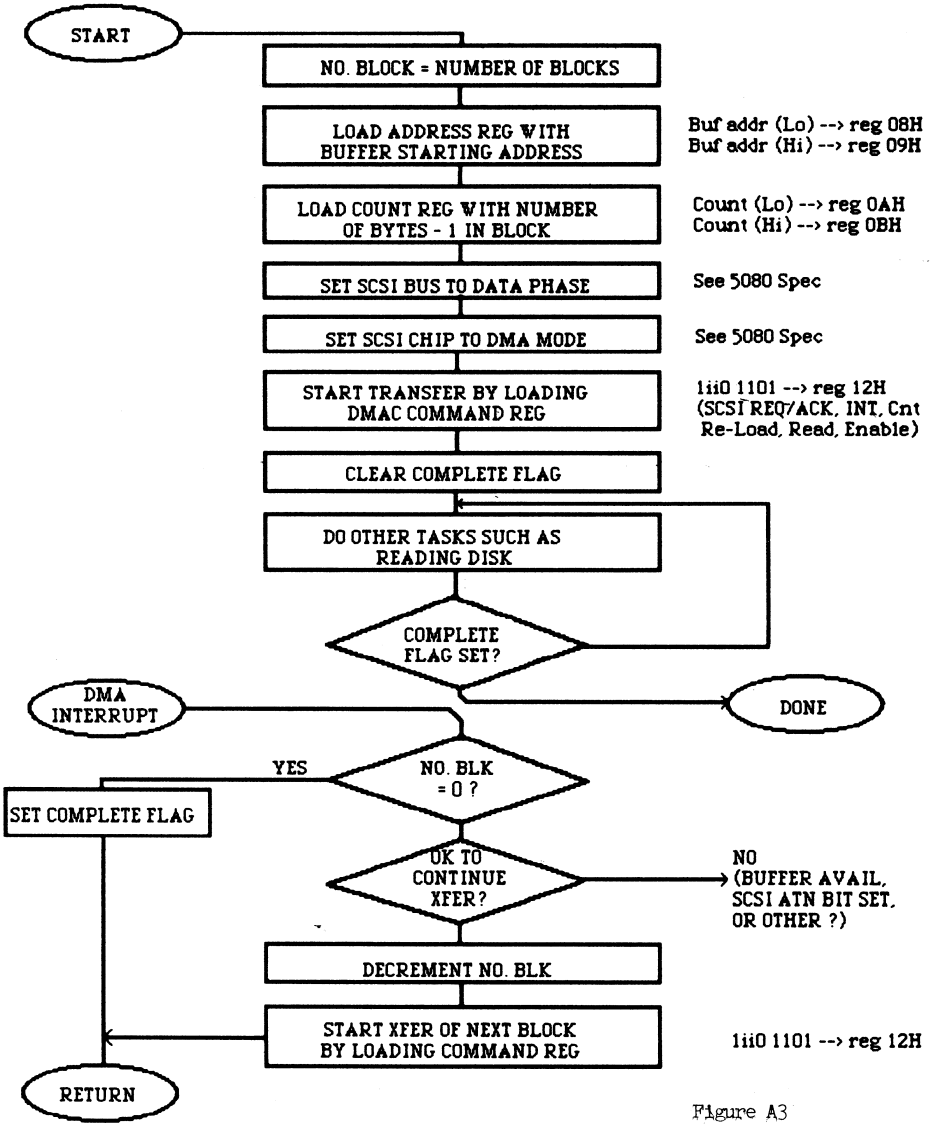
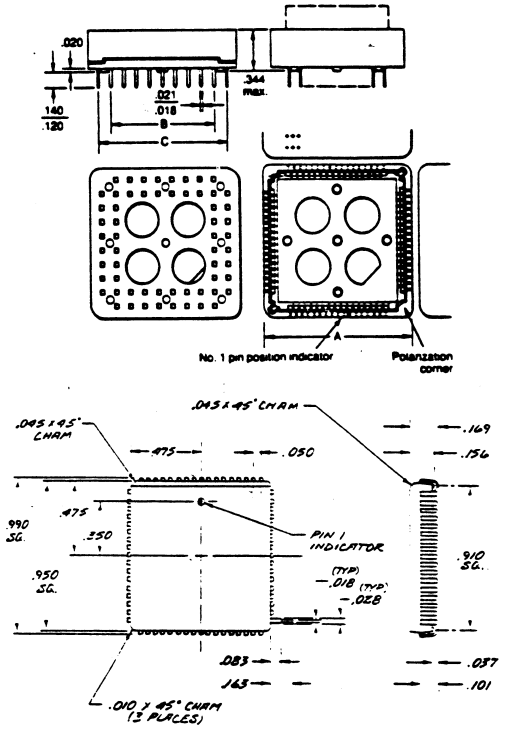


Figure A3



Socket and Package Dimensions

Figure A4

EXAMPLES OF COMMANDS USING CHANNEL 0:

[1] Command to transfer block of data from peripheral to RAM, with interrupt when done.

Command = 0ii0 1111 (Write to register 10(HEX)) (i = value used at initialization).

Bit 7 should be cleared.
Bits 6 and 5 depend on the hardware scheme used. They should be loaded with the same value they were loaded with during the initialization.
Bit 4: Only transferring one block, then stopping.
Bit 3: Interrupt when block transfer complete.
Bit 2: Reload the count so it will not be necessary to reload for the next block. Assumes the blocks are the same size.
Bit 1: Direction of transfer is from peripheral to RAM.
Bit 0: Enable channel to start transfer. When the last byte is transferred, the channel will be disabled because bit 4 is set.

[2] Command to continuously transfer data from the peripheral to RAM whenever the peripheral requests a transfer. No interrupt.

Command = 0ii1 1x11 (Write to register 10(HEX)) (i = value used at initialization, x = do not care.)

Bit 7 should be cleared.
Bits 6 and 5 depend on the hardware scheme used. They should be loaded with the same value with which they were loaded during the initialization.
Bit 4: Continuous transfer. The microprocessor can stop the transfer any time it wants to by writing the same command with the enable bit cleared (0).
Bit 3: No interrupts.
Bit 2: Count not used.
Bit 1: Direction of transfer is from peripheral to RAM.
Bit 0: Enable channel to start transfer.