SMF-V100
Multifunction Module for LSI-11
Manual

Σ Sigma Information Systems

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Manual

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Section 1
General Information

1.1 MANUAL CONTENTS

This manual provides the necessary information to install and operate the SMF-100 multifunction board manufactured by Sigma Information Systems, Anaheim, CA.

The material is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the SMF-V100. Specifications are included.

Section 2 - INSTALLATION AND OPERATION. This section contains the necessary information to install and operate the SMF-V100. Included are address selection, baud rate selection, bootstrap and backplane installation information.

Section 3 - FUNCTIONAL DESCRIPTION. This section contains a functional description of the serial line registers and clock registers for the SMF-V100.

1.2 GENERAL DESCRIPTION

The Sigma Information Systems' SMF-V100 combines two serial ports, a clock, and a multi-device bootstrap on a single dual wide printed circuit board. This high density multifunction board saves backplane slots, reducing cost and improving functionality of the small system. The SMF-V100 is completely Q bus* compatible with LSI-11 hardware and software. The two serial ports can be configured as standard general purpose serial interfaces (EIA RS-232C, RS-423 or RS-422 compatible) with connector pin-outs and functions identical to those of the DEC* DLV11J. One of the serial ports can be configured as the console. On-board switches are provided to allow the user to easily configure the serial ports for baud rate, line parameters, control addresses and vector interrupts.

The SMF-V100 generates a crystal controlled clock to be used as a line time clock. This clock drives the Q bus BEVENTL line and can be controlled via a register on board. Optionally, the SMF-V100 can enable or disable the BEVENTL signal if supplied by the power supply via the same register.

The SMF-V100 provides a bootstrap which is interactive with the console terminal. Upon power-up, or upon starting at the initial bootstrap address, the SMF-V100 displays a prompt which indicates it is waiting for a 2- or 3- character mnemonic from the console terminal.

The bootstrap program provides as standard the RK05 (DK), RX01 (DX), RX02 (DY), RL01/RL02 (DL), RP02/RP03 (DP), and TM11 (MT).

Bootstraps for most standard DEC devices are available upon request when ordering the SMF-V100.

*DEC and Q bus are registered trademarks of Digital Equipment Corporation.

1.3 SPECIFICATIONS

1.3.1 Physical Specifications

The SMF-V100 is contained on one dual wide printed circuit board: Width 5.2'' (13.2cm), Height 8.9'' (22.8cm)

The circuit board is multilayered with inner layers dedicated to power and ground and logic traces on component and solder sides.

1.3.2 Electrical Specifications

Power Requirements	5VDC 1.00A (typical) 12VDC 0.25A (typical)
Control Addresses	Individually Switch Selectable per Line
Interrupt Addresses	Individually Switch Selectable per Line
Baud Rates	300 to 38.4K - Individually Switch Selectable per Line
Character Format	5 to 8 Data Bits 1 or 2 Stop Bits Odd, Even or No Parity Individually Jumper Selectable per Line
Interfaces	RS-232C, RS-422 or RS-423 Individually Jumper Selectable per Line
Error	Overrun Error, Frame Error and Parity Error
Clock	Line Time Clock. Jumper Selection of control from internal crystal oscillator, or from Q bus BEVENT control. Clock register at 177546.

1.3.3 Environmental Specifications

Temperature	Operating	0°C to 50°C
	Storage	-45°C to 85°C
Humidity	0% to 95% non-condensing	
Altitude	Operating	0 ft to 10,000 ft
	Storage	0 ft to 30,000 ft

Section 2
Installation & Operation

2.1 UNPACKING AND INSPECTION

The SMF-V100 shipping carton is designed to provide maximum protection during shipping. It is recommended that the container be saved in the event that the board requires reshipment.

The SMF-V100 assembly is P/N 400 400165-100. Check the module for the correct part numer and serial number per the packing list. Visually inspect for any damage that might have occurred during shipment. If any damage has occurred, contact Sigma immediately.

2.2 CONFIGURATIONS

Figure 2-1 illustrates the location of switches and jumpers needed to configure the SMF-V100. Before installing the SMF-V100 into the backplane, ensure that switch settings and jumper locations are correct.

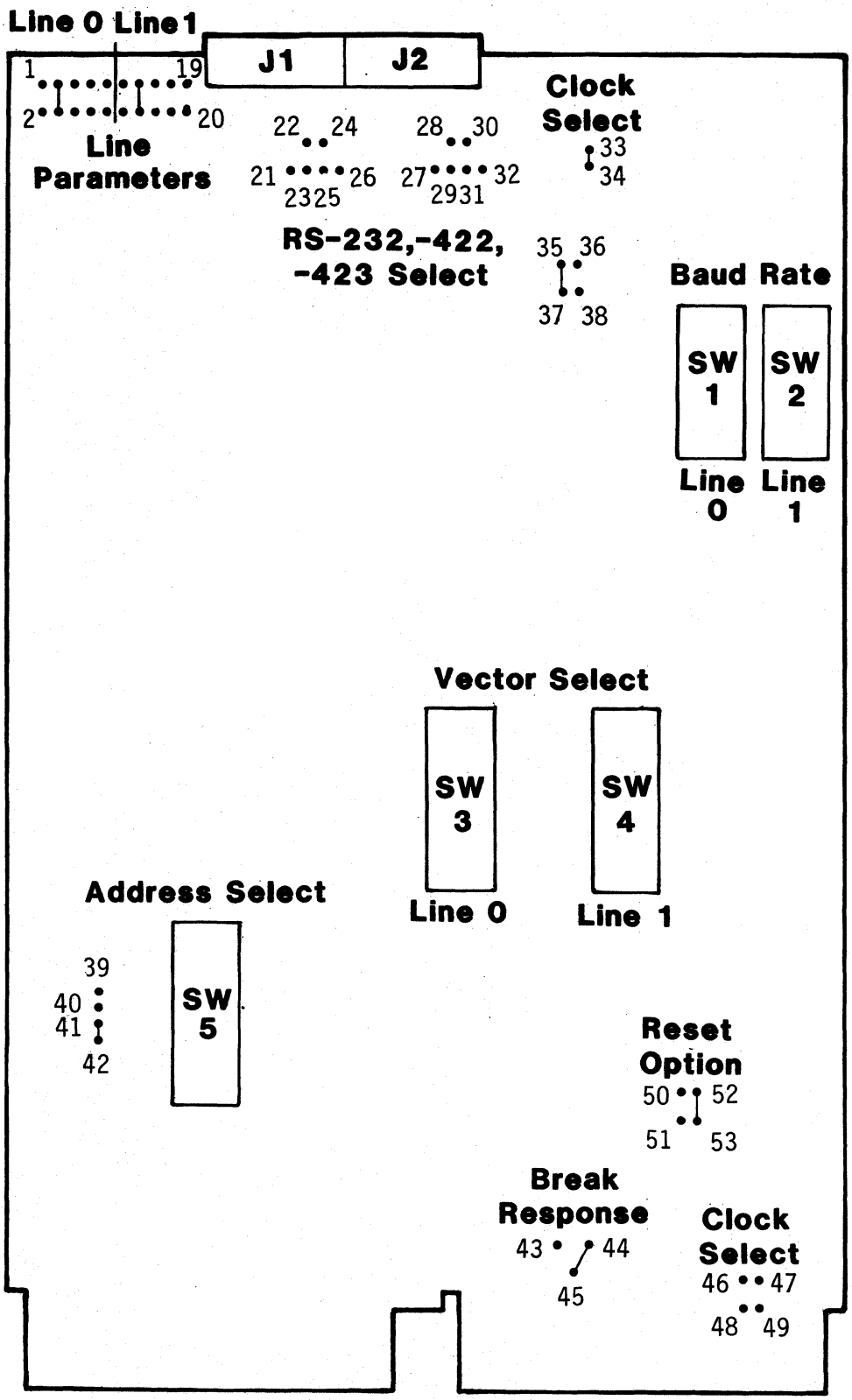

FIGURE 2-1: SWITCH AND JUMPER LOCATIONS

2.2.1 Address Selection

The addresses for the two serial ports are set via switch SW5 which is defined in Table 2-1 below. The address of the clock register is fixed at 177546 and the address of the bootstrap PROM is fixed starting at 173000.

Address selection switch settings allow either Line 0 or Line 1 to be used as the console (177560-17566), or Line 1 to be used as the standard serial line printer (177510-177516). All other address switch settings establish lines 0 and 1 as standard DL lines.

CSR ADDRESS	SWITCH SW5 POSITIONS 1	2	3	4	5	E39-E40	E41-E42
177560-177566*	0	X	X	X	X	OUT	IN
176500-176506	X	X	0	X	X	OUT	IN
176510-176516	X	X	X	0	X	OUT	IN
176520-176526	X	X	X	X	0	OUT	IN
176530-176536	X	0	X	X	X	IN	OUT
176540-176546	X	X	0	X	X	IN	OUT
176550-176556	X	X	X	0	X	IN	OUT
176560-176566	X	X	X	X	0	IN	OUT
177560-177566	0	X	X	X	X	IN	OUT

Console

*Console Device X = Out, 0 = In

for console

TABLE 2-1: LINE 0 ADDRESS SWITCH SW 5 SELECTION

CSR ADDRESS	SWITCH SW5 POSITIONS 6	7	8	9	10	E39-E40	E41-E42
177560-177566*	0	X	X	X	X	OUT	IN
176500-176506	X	X	0	X	X	OUT	IN
176510-176516	X	X	X	0	X	OUT	IN
176520-176526	X	X	X	X	0	OUT	IN
176530-176536	X	0	X	X	X	IN	OUT
176540-176546	X	X	0	X	X	IN	OUT
176550-176556	X	X	X	0	X	IN	OUT
176560-176566*	X	X	X	X	0	IN	OUT
177510-177516**	X	0	X	X	X	OUT	IN

*Console Device, **Line Printer X = Out, 0 = In

TABLE 2-2: LINE 1 ADDRESS SWITCH SW5 SELECTION

2.2.2 Vector Selection

The interrupt vectors for Line 0 and Line 1 are selected via switches SW3 and SW4 respectively. Either line can be selected as console (60 octal) but only Line 1 accepts a line printer (200 octal). Refer to Table 2-3 for Line 0 and Table 2-4 for Line 1 vector switch settings.

	SWITCH SW3 POSITIONS					
VECTOR	3	4	5	6	7	9
Console 60	0	X	X	0	0	0
300	0	0	0	X	X	0
310	X	0	0	X	X	0
320	0	X	0	X	X	0
330	X	X	0	X	X	0
340	0	0	X	X	X	0
350	X	0	X	X	X	0
360	0	X	X	X	X	0
370	X	X	X	X	X	0

X = Off, 0 = On

TABLE 2-3: LINE 0 VECTOR SWITCH SW3 SETTINGS

	SWITCH SW4 POSITIONS							
VECTOR	1	2	3	4	5	6	7	8
60	0	X	0	X	X	0	0	0
300	0	X	0	0	0	X	X	0
310	0	X	X	0	0	X	X	0
320	0	X	0	X	0	X	X	0
330	0	X	X	X	0	X	X	0
340	0	X	0	0	X	X	X	0
350	0	X	X	0	X	X	X	0
360	0	X	0	X	X	X	X	0
370	0	X	X	X	X	X	X	0
200*	X	0	0	0	0	0	X	0

*Standard Line Printer Vector X = Off, 0 = On

TABLE 2-4: LINE 1 VECTOR SWITCH SW4 SETTINGS

When a peripheral device interfaced to the SMF-V100 needs service, the module can, if enabled, interrupt the computer routine. The interrupt logic can initiate two types of interrupts: (1) a receiver interrupt, and (2) a transmitter interrupt. These interrupts are handled through separate receiver and transmitter channels.

For an interrupt transaction to occur, the program must have set the interrupt enable bit (6) in the Line CSR. Next, the interrupt logic must recognize a condition requiring service (indicated by the setting of bit 7), and then assert the interrupt request line (BIRQ L) on the Q bus. When the interrupt is acknowledged by the processor, the interrupt logic creates an input to the module's vector generation circuit, which reflects the line needing service and the type of service needed (Receive/Transmit). The vector generation circuits then generate a vector based upon vector switch settings which causes the processor to jump to the vector location for the peripheral device service routine.

2.2.3 Break Logic

During normal operation, the UART checks each received character for the proper number of stop bits. It does this by testing for a marking condition at the appropriate bit time. If a spacing condition is found instead, the UART sets the framing error flag (FE). The BREAK signal is a continuous spacing condition, and it is interpreted by the UART as a data character that is missing stop bit(s). The UART, therefore, responds to the BREAK signal by asserting FE. If Line 0 jumper E44-E43 is installed and E44-E45 is removed, FE will cause BDCOKH to be asserted, signaling the system to execute a power-up boot procedure (provided proper processor power-up mode is selected).

If jumper E44-E43 is removed and E44-E45 is installed, FE will cause BHALT L to be asserted. This signals the computer to halt when BREAK is received. See Table 2-5 for BREAK jumper configurations.

OPTION	E44-343	E44-345
Halt on BREAK	X	O
Boot on BREAK	O	X
None	X	X

X = Out, O = In

TABLE 2-5: BREAK LOGIC JUMPERS

2.2.4 Reset Option

The SMF-V100 provides the option of clearing the UARTS on either assertion of power-up (BDCOK) or upon assertion of INIT by the processor. If jumper E50-E51 is installed and jumper E52-E53 is removed, the UARTS will be cleared by INIT. If E52-E53 is installed and E50-E51 is removed, the UARTS are cleared by BDCOK.

It is preferable to use BDCOK to clear the UARTS in order to prevent loosing characters if the processor starts a transfer and then asserts BINIT L. Refer tp Table 2-6 for UART reset options.

OPTION	E50-E51	E52-E53
Reset on BDCOK	X	O
Reset on BINIT	O	X

X = Out, O = In

TABLE 2-6: UART RESET OPTIONS

2.2.5 Baud Rate Selection

Baud rates for each of the two channels are set independently via switch SW1 (Line 0) and switch SW2 (Line 1). Refer to Table 2-7 for baud rate switch settings.

BAUD RATE	SWITCH POSITIONS							
LINE 0 (SW1)——1	2	3	4	5	6	7	8
LINE 1 (SW2)——1	2	3	4	5	6	7	8
38.4K	O	X	X	X	X	X	X	X
19.2K	X	O	X	X	X	X	X	X
9600	X	X	O	X	X	X	X	X
4800	X	X	X	O	X	X	X	X
2400	X	X	X	X	O	X	X	X
1200	X	X	X	X	X	O	X	X
600	X	X	X	X	X	X	O	X
300	X	X	X	X	X	X	X	O

X = Off, O = On

TABLE 2-7: BAUD RATE SWITCH SETTINGS

2.2.6 Data Word Format

The data word format parameters are jumper selectable for individual lines. The number of data bits, the number of stop bits, and the mode of parity are determined as shown in Table 2-8.

JUMPERS LINE 0	JUMPERS LINE 1	NAME	DESCRIPTION
E1-E2	E11-E12	NPB	Enable/Disable Parity Out = Parity Disabled, In = Parity Enabled
E3-E4	E13-E14	NSB	Select 1 or 2 Stop Bits Out = 2 Stop Bits In = 1 Stop Bit
E5-E6	E15-E16	NB2	Select Number of Data Bits per Character NB2 / NB1 / # BITS IN* / IN / 5 BITS IN / OUT / 6 BITS
E7-E8	E17-E18	NB1	Select Number of Data Bits per Character NB2 / BN1 / # BITS OUT* / IN / 7 BITS OUT / OUT / 8 BITS

OUT = Even Parity, IN = Odd Parity

TABLE 2-8: DATA WORD PARAMETER JUMPERS
(FACTORY CONFIGURATION: PARITY DISABLED,
ONE STOP BIT, 8 CHARACTER BITS)

2.2.7 Serial Interface Selection

The SMF-V100 can interface with RS232C, RS-422, or RS-423 devices. The serial interface for each channel is independently jumper selectable as shown in Table 2-9.

JUMPERS LINE 0	JUMPERS LINE 1	RS-232C/423	RS-422
E21-E22	E27-E28	O	X
E22-E23	E28-E29	X	O
E24-E25	E30-E31	O	O
E25-E26	E31-E32	X	X

X = Out, O In

TABLE 2-9: SERIAL INTERFACE SELECTION
(FACTORY CONFIGURATION: RS-232C)

2.2.8 Interface Connector

The SMF-V100 uses 10-pin connectors for Line 0 and Line 1. Connector pin-out is the same as that of the DEC DLV11J. Refer to Table 2-10.

Figure 2-2 illustrates the connector pin assignment as viewed from the top of the board (serial line connector end), component side up.

I/O CONNECTOR PIN NUMBER	SIGNAL
1	UART CLK (16 x baud)
2	SIGNAL GND
3	Transmit Data
4*	Transmit Data -
5	SIGNAL GND
6	Indexing Key - No Pin
7	Receive Data -
8	Receive Data +
9	SIGNAL GND
10	+12VDC

*Grounded for EIA RS-423

TABLE 2-10: I/O PIN CONNECTOR

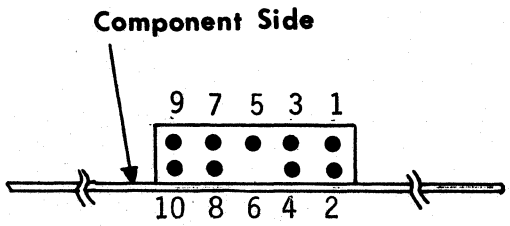

FIGURE 2-2: 10-PIN I/O CONNECTOR

2.2.9 Interrupt Priorities

Interrupt priorities within the SMF-V100 are structured as follows:

PRIORITY	REGISTER
4 (high)	CHO RBUF
3	CHI RBUF
2	CHO XBUF
1	CHI XBUF

TABLE 2-11: SMF-V100 INTERRUPT PRIORITIES

2.10 Line Time Clock

The SMF-V100 provides an on-board crystal controlled line frequency clock. The clock circuitry allows the option of supplying a line time clock from the on-board circuits, controlling the BEVENT L line when it is driven from a power supply LTC signal, or providing a clock from an external source.

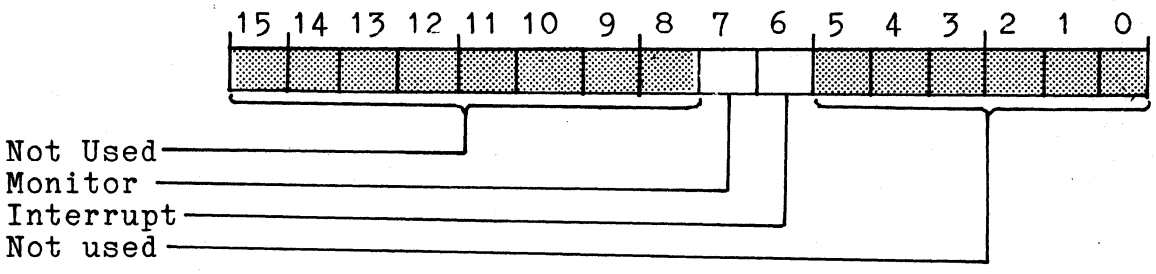

FIGURE 2-3: CLOCK CSR - 177546

BIT	DEFINITION	DESCRIPTION
7	MONITOR	Set by the line frequency clock signal OR INIT. Cleared by the program or INIT.
6	INTERRUPT ENABLE	When asserted (1), the BEVENT line is toggled to provide interrupts to the LSI-11. Read/Write. Cleared on power-up.

The SMF-V100 provides a Clock Register at location 177546. Bit 6, when asserted, enables clock interrupts. When bit 6 is asserted clock pulses appear on the BEVENT L line. The processor is then interrupted at the clock frequency.

When Clock Register, bit 6, is not asserted, interrupts are disabled and, depending upon jumper configuration, the SMF-V100 will either block the internal clock or will clamp the BEVENT L line low to prevent interrupts from the power supply LTC signal.

There are three cases to be considered when determining which clock option to use:

1. Power supply generates LTC signal on BEVENTL

   In this situation, jumper for external BEVENT (See Table 2-12). The SMF-V100 will control the interrupts to the processor via the Clock Register bit 6 by clamping the BEVENT line when interrupts are disabled (bit 6 not asserted). The Clock Register will be cleared upon power-up or INIT to disable interrupts.

2. No power supply LTC. Internal SMF-V100 clock to be used.

   In this situation, jumper the SMF-V100 for internal clock (see Table 2-12). The SMF-V100 will control the BEVENT line via bit 6 of the clock CSR.

3. No power supply LTC and external clock is to be used.

   In this situation, the SMF-V100 should be jumpered for External Clcok (See Table 2-12). The externally supplied clock must be connected from backplane AF1 of the slot occupied by the SMF-V100. The clock CSR will control pulses on the BEVENT line exactly as described previously.

11/73 11/23

JUMPER	INTERNAL CLOCK	EXTERNAL CLOCK	EXTERNAL BEVENT
E33-E34	IN	OUT	OUT
E35-E36	IN	IN	OUT
E37-E38	OUT	OUT	IN
E46-E47	IN	IN	OUT
E48-E49	OUT	IN	OUT

TABLE 2-12: CLOCK JUMPER OPTIONS

NOTE

In external BEVENT mode, the power supply LTC signal is also controlled via the front panel switch.

2.2.11 Bootstrap

The SMF-V100 provides a multi-device bootstrap for most standard DEC devices. This bootstrap routine is interactive with the console device and depends upon a 2-character mnemonic from the operator to determine the device to boot.

The bootstrap PROM occupies two separate address regions in the I/O user page. Area 1 is 173000 through 173776, and area 2 is 164000 through 164776.

The bootstrap function can be disabled or selectively enabled by address region via switch SW3. Refer to Table 2-13 below.

BOOT FUNCTION	SW3-1	SW3-10
Disable Boot	ON	ON
Enable 173000-173776	OFF	ON
Enable 164000-164776	ON	OFF
Enable All	OFF	OFF

TABLE 2-13: BOOT ENABLE/DISABLE SWITCH SW3

The SMF-V100 can accommodate two bootstrap PROMs in U34 and U33. The standard PROM in location U34 includes devices listed in Table 2-14. Location U33 is reserved for an additional device PROM. To enable the additional PROM, set SW3-1 and SW3-10 both OFF (Enable All from Table 2-13).

DEVICE	MNEMONIC	UNIT
RXV11 Floppy (Single Density)	DX	0,1
RXV21 Floppy (Dual Density)	DY	0,1
RKV11 Cartridge Disk	DK	0-8
RL01, RL02 Cartridge Disk	DL	0-4
RK611, RK711 Cartridge Disk	DM	0-8
RP11 Disk Pack System	DP	0-8

TABLE 2-14: DEVICES SUPPORTED BY BOOTSTRAP

The bootstrap program is entered upon power-up if the processor is properly jumpered. The boot program can also be initiated by starting at location 173000 under ODT. Be sure RUN switch is enabled on the front panel.

After the bootstrap program is started an asterisk (*) will prompt the console for a 2- or 3-character mnemonic, followed by a carriage return (CR).

NOTE

If the SMF-V100 boot program is to be used, be sure that no other bootstrap device is enabled in the system. Also, if a controller resident boot is used, be sure to disable the SMF-V100 boot.

2.2.12 Installation in Backplane

After the SMF-V100 has been properly configured, plug the module into the appropriate Q bus slot of any standard backplane. Since the SMF-V100 is an interrupting device, be certain the continuity of the BIAKI and BIAKO from the CPU to the SMF-V100 exists.

Table 2-15 describes the Q bus pins used by the SMF-V100.

CONNECTOR A		CONNECTOR B	
AA1	NOT USED	BA1	BDCOK H
AB1	NOT USED	BB1	BPOK H
AC1	NOT USED	BC1	NOT USED
AD1	NOT USED	BD1	NOT USED
AE1	NOT USED	BE1	NOT USED
AF1	EXT CLK IN	BF1	NOT USED
AH1	NOT USED	BH1	NOT USED
AJ1	GND	BJ1	NOT USED
AK1	NOT USED	BK1	NOT USED
AL1	NOT USED	BL1	NOT USED
AM1	GND	BM1	GND
AN1	NOT USED	BN1	NOT USED
AP1	BHALT L	BP1	NOT USED
AR1	NOT USED	BR1	BEVENT L
AS1	NOT USED	BS1	NOT USED
AT1	GND	BT1	GND
AU1	NOT USED	BU1	NOT USED
AV1	NOT USED	BV1	5VDC
AA2	5VDC	BA2	5VDC
AB2	NOT USED	BB2	NOT USED
AC2	GND	BC2	GND
AD2	12VDC	BD2	NOT USED
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	NOT USED	BK2	BDAL6 L
AL2	BIRQL	BL2	BDAL7 L
AM2	BIAKL L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDALO L	BU2	BDAL14 L
AV2	BDALI L	BV2	BDAL15 L

TABLE 2-15: SMF-V100 BUS SIGNALS AND PIN ASSIGNMENTS

2.3 CABLES

Cables to mate with the 2 x 5 pin SMF-V100 connector are available from Sigma Information Systems. The standard cable is compatible with the DEC VT100.

When building a cable for the SMF-V100, consider the following:

A) The receivers have differential inputs. For RS-232C or RS-423, RECEIVE DATA - (Pin 7 on 2 x 5 pin connector) must be tied to signal ground (Pins 2, 5 or 9) in order to maintain proper EIA levels. RS-422 is balanced and uses both RECEIVE DATA+ and RECEIVE DATA -.

B) To directly connect to a local EIA RS-232C terminal, it is necessary to use a null modem. To build the null modem into the cable, switch RECEIVE DATA (Pin 2) with TRANSMIT DATA (Pin 3) on the RS-232C connector.

C) To mate to the SMF-V100 connector block, the following parts are required:

CABLE RECEPTACLE	AMP P/N 87456-9
CLIP CONTACTS	AMP P/N 87124-1
KEY PIN (PIN 6)	AMP P/N 87179-1

D) To mate to a VT100 or compatible terminal, the following parts are needed:

RS-232C CONNECTOR	AMP P/N 205207-1
CRIMP TERMINAL	AMP P/N 66504-4
STRAIN RELIEF COVER	AMP P/N 206472-1
4-CONDUCTOR CABLE	ALPHA P/N 5004.

The cable wire list for a null modem cable switchable for interconnection from a SMF-V100 to a VT100 compatible terminal is as illustrated in Figure 2-4 and defined in Table 2-16.

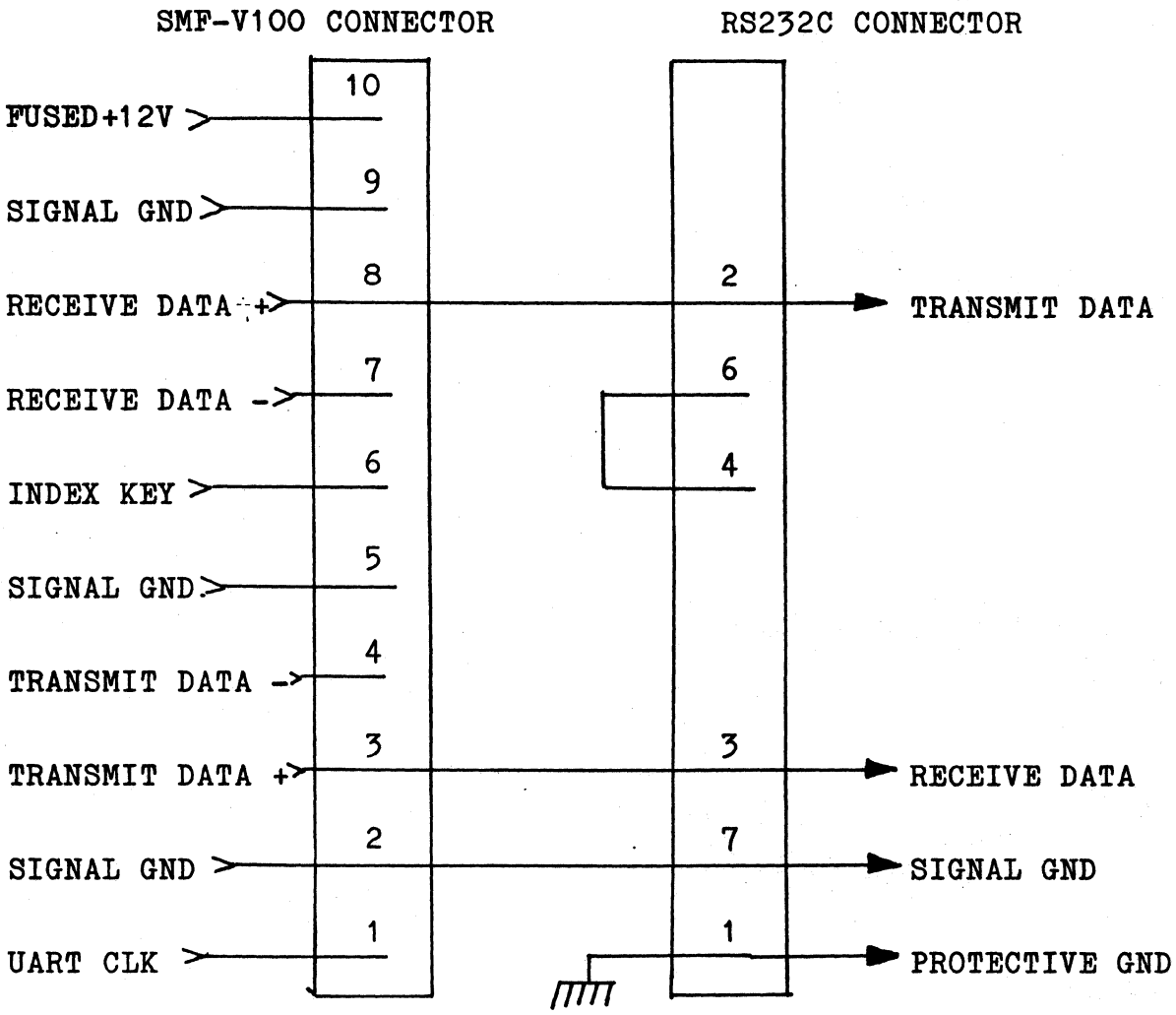

FIGURE 2-4: SMF-V100 RS-232C CONNECTIONS

PIN NO.	SIGNAL
1	UART CLOCK IN OR OUT (16 X BAUD RATE, CMOS)
2	SIGNAL GND
3	TRANSMIT DATA +
4	TRANSMIT DATA -
5	SIGNAL GND
6	INDEX KEY - NO PIN
7	RECEIVE DATA -
8	RECEIVE DATA +
9	SIGNAL GND
10	FUSED 12VDC FOR 20mA DLV11KA

TABLE 2-16: SMF-V100 RS-232C PIN DEFINITIONS

Section 3
Functional Description

3.0 GENERAL INFORMATION

The following is a functional description of the registers contained in the SMF-V100 multifunction board.

3.1 REGISTER DESCRIPTION

The SMF-V100 has four registers for each serial line, plus one register for the clock. The bootstrap addresses are each addressable in the I/O page.

3.1.1 Serial Line Registers

Each serial port has four device registers as follows:

17XXX0	RCSR	Receiver Control/Status Register
17XXX2	RBUF	Receiver Buffer
17XXX4	XCSR	Transmitter Control/Status Register
17XXX6	XBUF	Transmitter Buffer

If channel 0 is assigned as the console, the register assignment is as follows:

RCSR = 177560
RBUF = 177562
XCSR = 177564
XBUF = 177566

The serial line register description are shown in Figure 3-1 through 3-4.

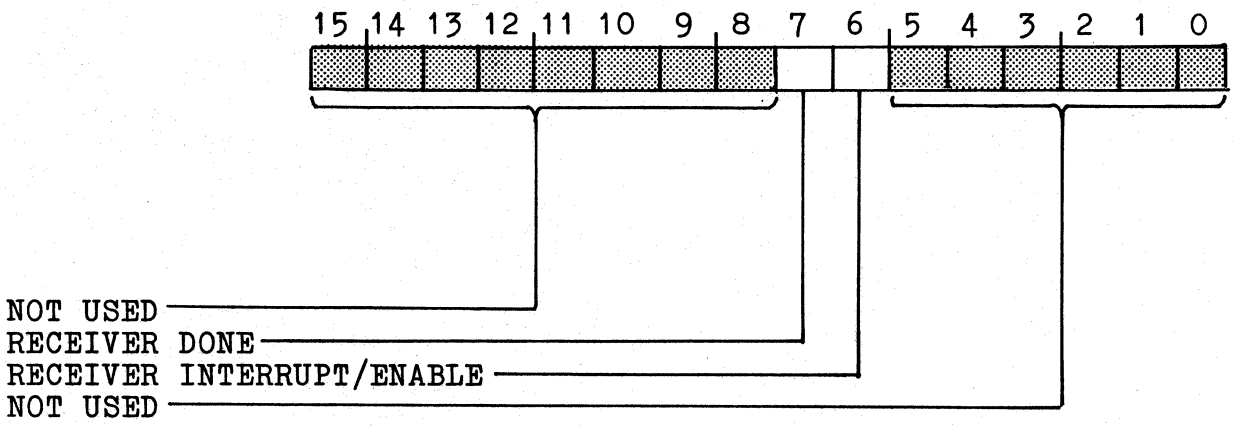

FIGURE 3-1: RCSR (17XXXO) REGISTER FORMAT

BIT	DESCRIPTION
15-8	NOT USED. On Read = 0.
7	RECEIVER DONE. Read Only. Set when an entire character has been received and is ready for input to the processor. If Receiver Interrupt Enable (bit 6) is set, setting Receiver Done will start an interrupt sequence. Cleared when RBUF is read, or by INIT.
6	RECEIVER INTERRUPT ENABLE. Read/Write. Set under program control to enable Done (bit 7) to initiate an interrupt sequence. Cleared by INIT or program control.
5-0	NOT USED. On Read = 0.

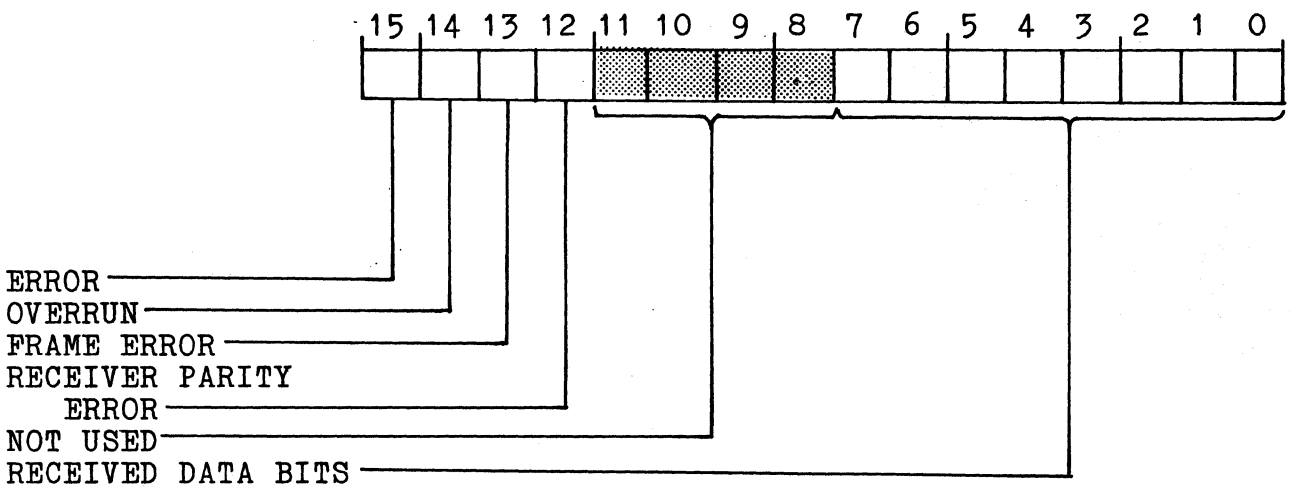

FIGURE 3-2: RBUF (17XXX2) REGISTER FORMAT

BIT	DESCRIPTION
15	ERROR. Read Only. Set whenever bit 14, 13 or 12 is set. Cleared by INIT.
14	OVERRUN. Read Only. Set when previous character has not completely been read (RCSR bit 7 not cleared) prior to receiving a new character. Cleared by INIT.
13	FRAME ERROR. Read Only. Set when no valid stop bit is present for the character being received. Cleared by INIT.
12	RECEIVER PARITY ERROR. Read Only. Set when the received parity does not agree with the expected parity. Always 0 if the line is configured for no parity. Cleared by INIT.
11-8	NOT USED. On Read = 0
7-0	RECEIVED DATA BITS. Read Only.

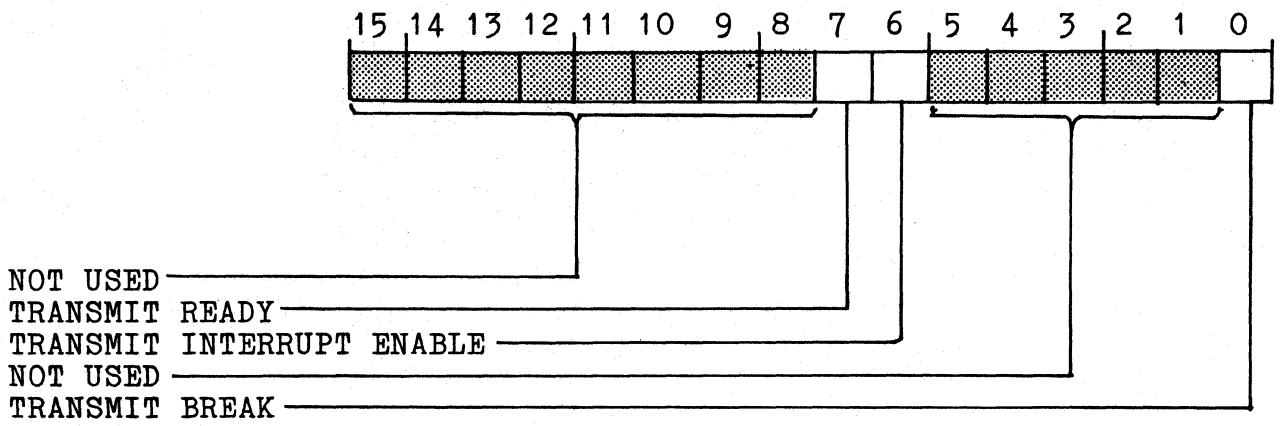

FIGURE 3-3: XCSR (17XXX4) REGISTER FORMAT

BIT	DESCRIPTION
15-8	NOT USED. Read as 0
7	TRANSMIT READY. Read Only. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during power-up sequence or during a Reset instruction.
6	TRANSMIT INTERRUPT ENABLE. Read/Write. Set under program control when it is desired to generate a transmitter interrupt request (transmitter ready to accept a character for transmission). Cleared under program control, during power-up sequence or Reset instruction.
5-1	NOT USED. Read as 0.
0	TRANSMIT BREAK. Read/Write. Set or Reset under program control. When set, a continuous space level is transmitted; however, bits 6 and 7 will still operate, allowing software timing on Break. When not set, normal character transmission can occur. Cleared by INIT.

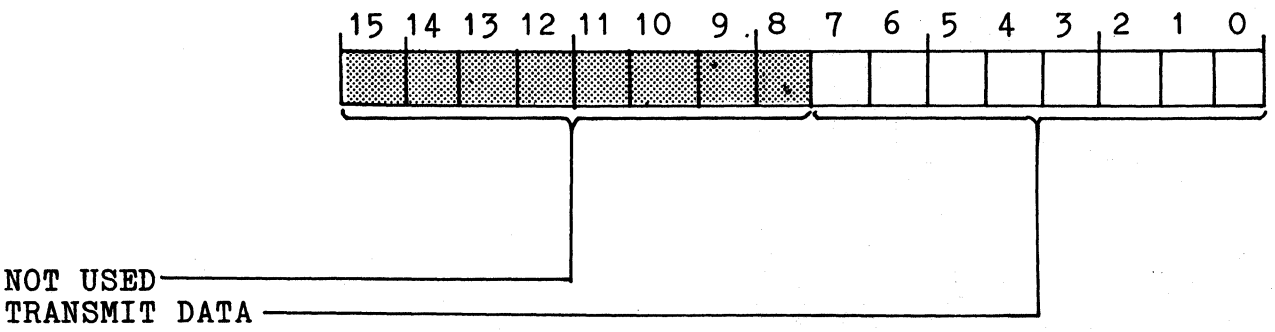

FIGURE 3-4: XBUF (17XXX6) REGISTER FORMAT

BIT	DESCRIPTION
15-18	NOT USED. Read as 0.
7-0	TRANSMIT DATA. Write Only. (On Read = 0.) 5 to 8 bit data is right justified. Loaded under program control for serial transmission.

3.1.2 Clock Register

The SMF-V100 Clock Register works in conjunction with the Q bus BEVENT L line (BR1). Both LSI-11 and LSI-11/23 (when jumpered to acknowledge BEVENT) are interrupted by a high to low transition of BEVENT. When interrupted, the processor vectors to the standard clock vector (100 octal) for service. No external interrupt is required from the SMF-V100.

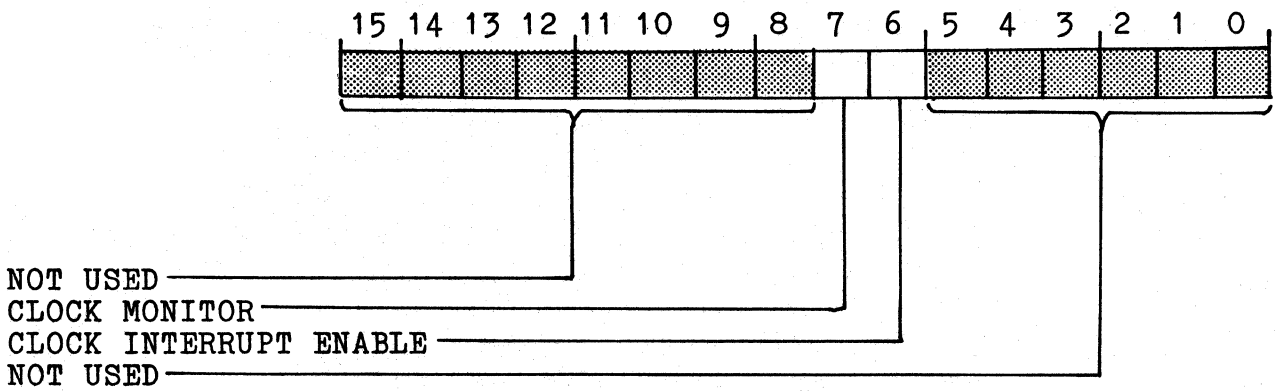

FIGURE 3-5; CSR (177546) CLOCK REGISTER FORMAT

BIT	DESCRIPTION
15-8	NOT USED. On Read = 0.
7	CLOCK MONITOR. Read/Write. Set by BEVENT transition. Can be cleared but not set. Cleared by the program, INIT, or power-up sequence.
6	INTERRUPT ENABLE. Read/Write. When cleared, BEVENT is clamped to prevent transition. When enabled, BEVENT is permitted to toggle. Cleared by INIT or power-up sequence.
5-0	NOT USED. On Read = 0

3.3 ASYNCHRONOUS TRANSMISSION FORMAT

In asynchronous transmission, data characters are transmitted in the format shown in Figure 3-6.

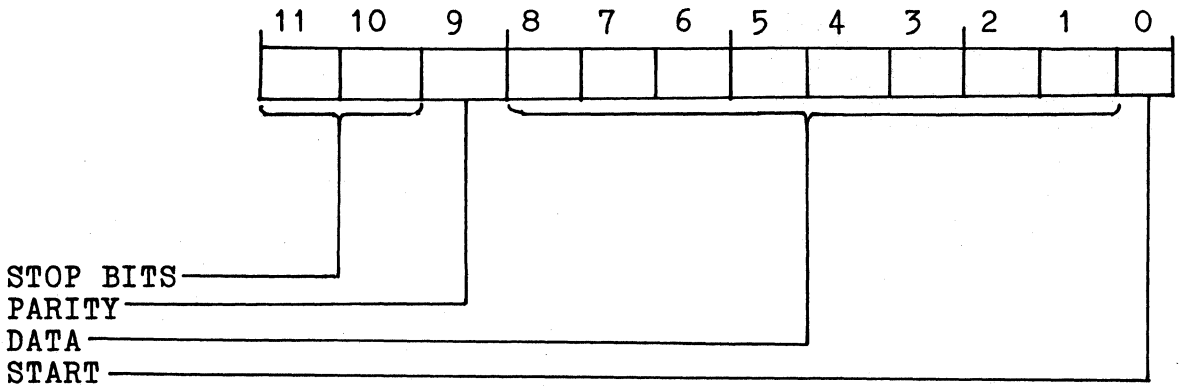

FIGURE 3-6: ASYNCHRONOUS TRANSMISSION FORMAT

BIT	DESCRIPTION
11-10	STOP BITS. Stop bits can be configured for either one or two Stop bits. When the first Stop bit is received, the UART shifts the data in parallel from the receiver shift register to the SMF-V100 parallel buffer register (RBUF). All Start, Stop and Parity bits are removed from the character. The receiver asserts Don (RCSR bit 7) and all data and error bits become valid.
9	PARITY. Parity can be configured for Odd, Even, or None. If the device is configured for no parity, the Stop bits follow immediately after the data bits.
8-1	DATA BITS. From 5 to 8 bits of data (depending upon predetermined character format) can be transmitted. Data is shifted in by the UART so the least significant bit is stored in the lowest bit position in the UART shift register.
0	START BIT. Detected by the UART as mark-to-space transition, causing the UART to begin loading the character into its shift register.

Technical Bulletin

NUMBER	PRODUCT: SMF-V100	RELEASED BY	PAGE 1
TB111	MODIFICATION FOR LSI-11/73 OPERATION	R. OSBORNE	2/19/85

Sigma's SMF-V100 multifunction module requires modification for operation in LSI-11/73 systems. The LSI-11/73 has an on-board clock, and the SMF-V100 clock must be disabled.

Using the figure below, disable the clock on the SMF-V100 module by installing a wire from U35 pin 1 to U35 pin 18.