TITLE SA1000 FIXED DISK DRIVE INTERFACE

1.0 INTRODUCTION

This specification describes the requirements of the physical and electrical interface with the SA1000 Disk Drive. The physical interface section specifies the mechanical requirements as well as lists recommended parts. The electrical interface is concerned with functional as well as timing relationship required of each I/O pin.

2.0 PHYSICAL INTERFACE

The electrical interface between the SA1000 and the host system is via four connectors: The first connector (J1) provides control signals for the drive: the second connector (J2) provides for radial connection of read/write data signals; the third connector (J5) provides for DC power; and the fourth connector (J4) provides for AC power and frame ground. Refer the figure 4A for connector locations.

2.1 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge connector. The dimensions for this connector are shown in figure 1. The pins are numbered 1 through 50 with the even pins located on the component side of the PCB and odd pins located on the non component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the AC connector and is labeled. A KEY SLOT is provided between pins 4 and 6. The recommended mating connector for P1 is scotchflex ribbon connector P/N 3415-0001 or Amp twin leaf printed circuit connector P/N 1-583717-1 utilizing Amp contacts P/N 1-583616-1.

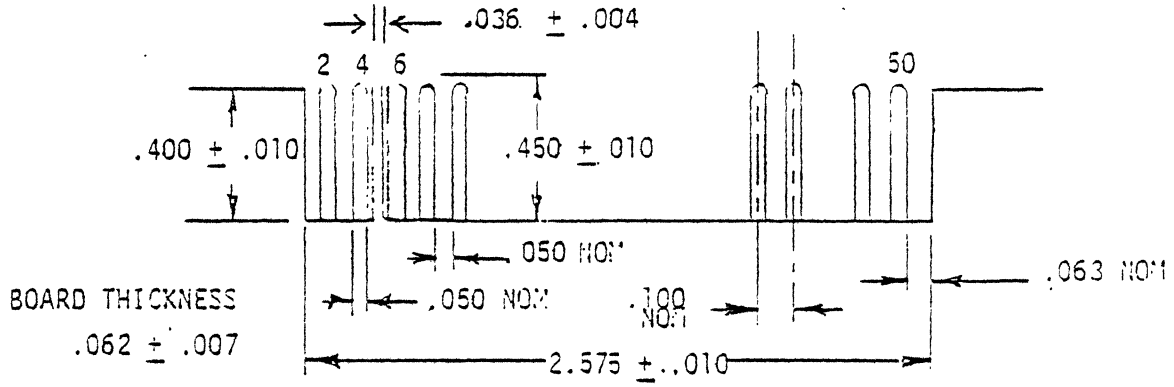


FIGURE 1 J1 CONNECTOR DIMENSIONS

2.2 J2/P2 CONNECTOR

Connection to J2 is through a 20 pin PCB edge connector. The dimensions for the connector are shown in figure 2. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is scotchflex ribbon connector P/N 3461-0001 or AMP P/N 583717-1 with AMP contacts P/N 1-583616-1. A KEY SLOT is provided between pins 4 and 6.

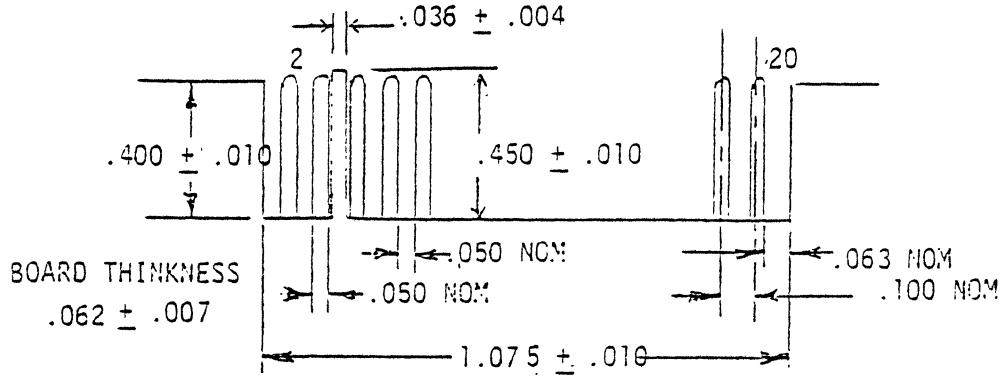
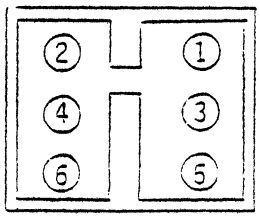


FIGURE 2 J2 CONNECTOR DIMENSIONS

2.3 J5/P5 CONNECTOR

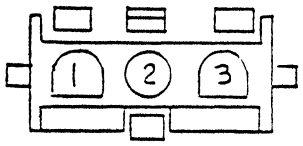
DC power connector (J5) is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0 mounted on the solder side of the PCB. The recommended mating connector (P5) is AMP P/N 1-480270 utilizing AMP pins P/N 60619-1. J5 pins are labeled on J5 connector.



J5 CONNECTOR (AS SEEN ON DRIVE PCB FROM SOLDER SIDE)

2.4 J4/P4 CONNECTOR

AC power and frame ground is interfaced through a 3 pin connector. The pin housing (J4) is mounted in the drive and is AMP P/N 1-480701-0 with pins AMP P/N 350687-1 and 350654-1 (gnd pin). The recommended mating connector (P4) is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.



J4 CONNECTOR (AS SEEN FROM BACK OF DRIVE)

The disk drive is shipped with DC ground (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor. If the system configuration requires the separation of these grounds, remove the ground strap.

3.0 INTERFACE LINES & PIN ASSIGNMENTS

The interface of the drive can be divided into three categories: Signal, DC power, and AC power. Tables I, II and III define the pin assignments for these interface lines. Tables IV and V show the recommended cable types and the grounding configurations at the drive and at the host systems. Those signal pins marked SPARE are uncommitted. They may be used as alternate pins to carry some SA1000 interface signals if the user prefers to do his own modification. Those signal pins marked NA are uncommitted at the SA1000, but are assigned in the SA850/851. Therefore, these pins should not be used as alternate I/O signal pins if a controller having an SA850/851 interface is used. A 4-drive subsystem is shown in Figure 4B.

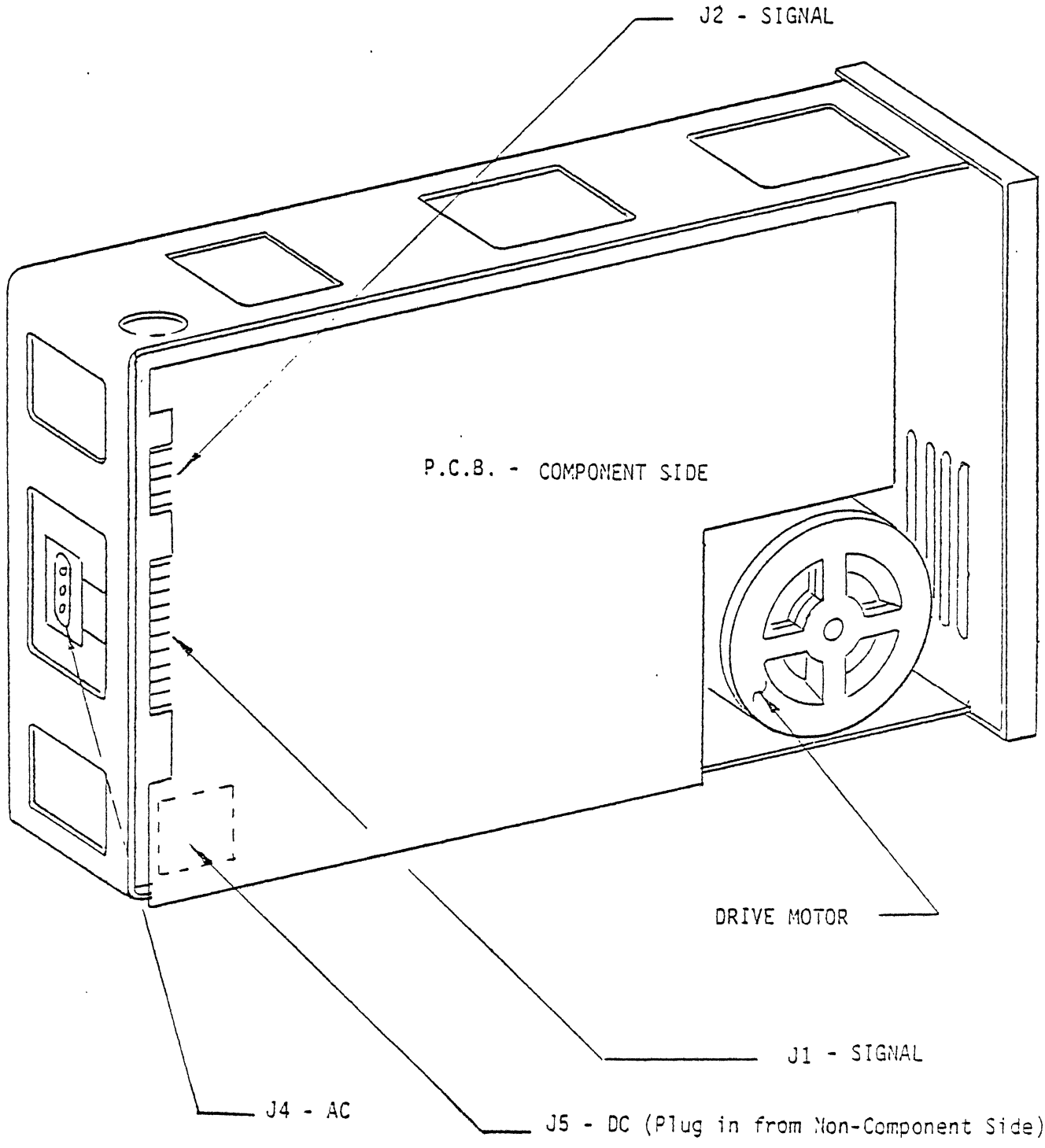


FIGURE 4A INTERFACE CONNECTOR PHYSICAL LOCATION

TABEL IA - J1/P1 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-REDUCED WRITE CURRENT
3	4	SPARE
5	6	SPARE
7	8	-SEEK COMPLETE
9	10	NA
11	12	NA
13	14	-HEAD SELECT 2^0
15	16	NA
17	18	-HEAD SELECT 2^1
19	20	-INDEX
21	22	-READY
23	24	NA
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN
35	36	-STEP
37	38	NA
39	40	-WRITE GATE
41	42	-TRACK ØØØ
43	44	-WRITE FAULT
45	46	NA
47	48	NA
49	50	NA

TABLE IB J2/P2 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	- DRIVE SELECTED
4	3	SPARE
6	5	SPARE
	7	SPARE
8		GND
	9	+ 2BYTE CLK
	10	- 2BYTE CLK
11		GND
12		GND
	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
15		GND
16		GND
	17	+ MFM READ DATA
	18	- MFM READ DATA
19		GND
20		GND

VOLTAGE		GROUND	
PIN 1	+24 VOLTS DC	PIN 2	+24 VOLT RETURN
PIN 4	-7 TO -16 (-5 OPT) VOLTS	PIN 3	-7 TO -16 (-5 OPT) VOLT RETURN
PIN 5	+5 VOLTS	PIN 6	+5 VOLT RETURN

TABLE II

P5 - DC CONNECTOR PIN ASSIGNMENTS

PIN 1	MOTOR POWER "A"
PIN 2	FRAME GROUND
PIN 3	MOTOR POWER "B"

TABLE III

P4 - AC CONNECTOR PIN ASSIGNMENTS

TITLE SA1000 INTERFACE SPECIFICATION

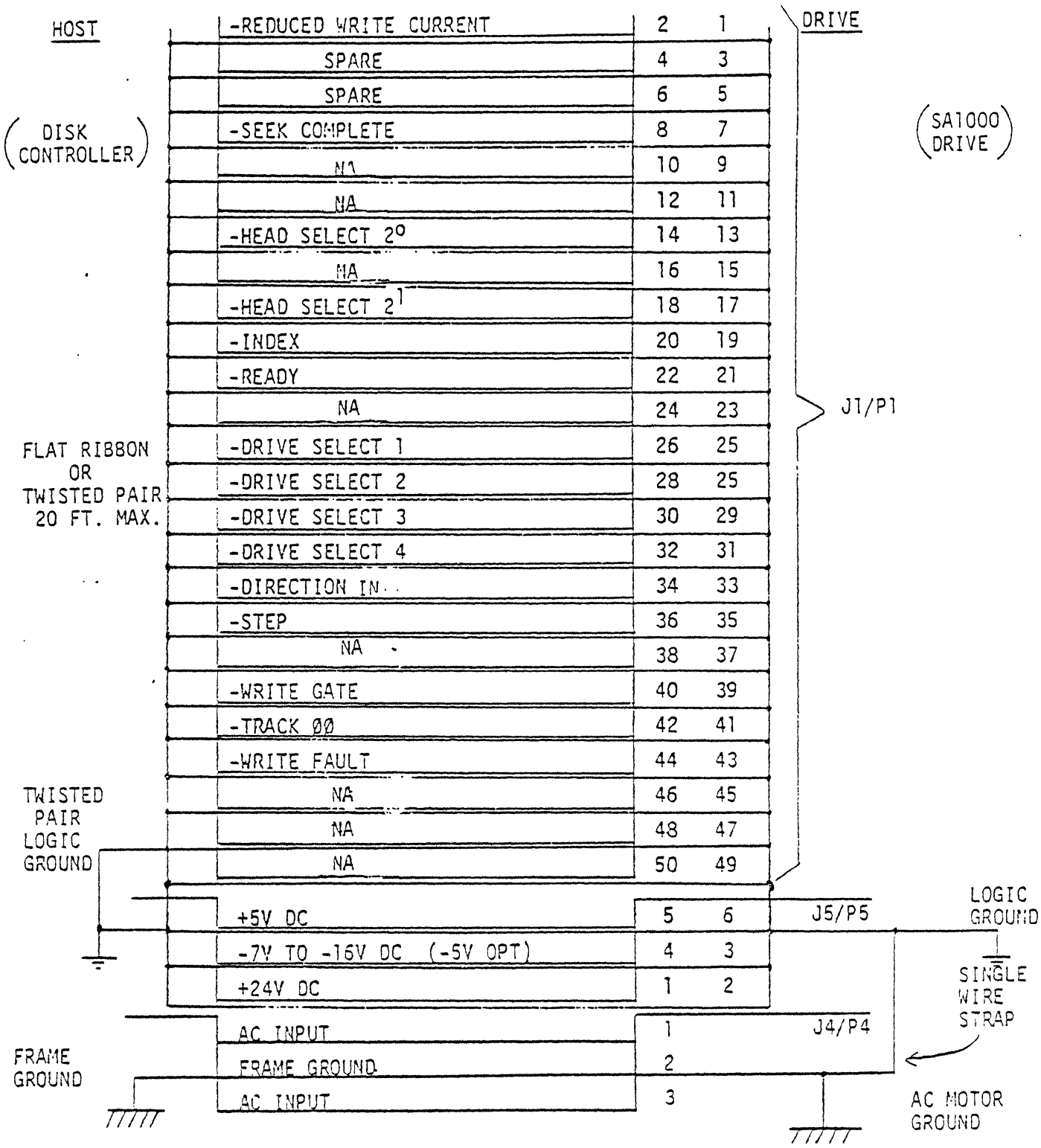


TABLE IV SINGLE DRIVE SYSTEM - DATA CABLE FROM DATA SEPARATOR TO P2/J2 NOT SHOWN

TITLE SA1000 INTERFACE SPECIFICATION

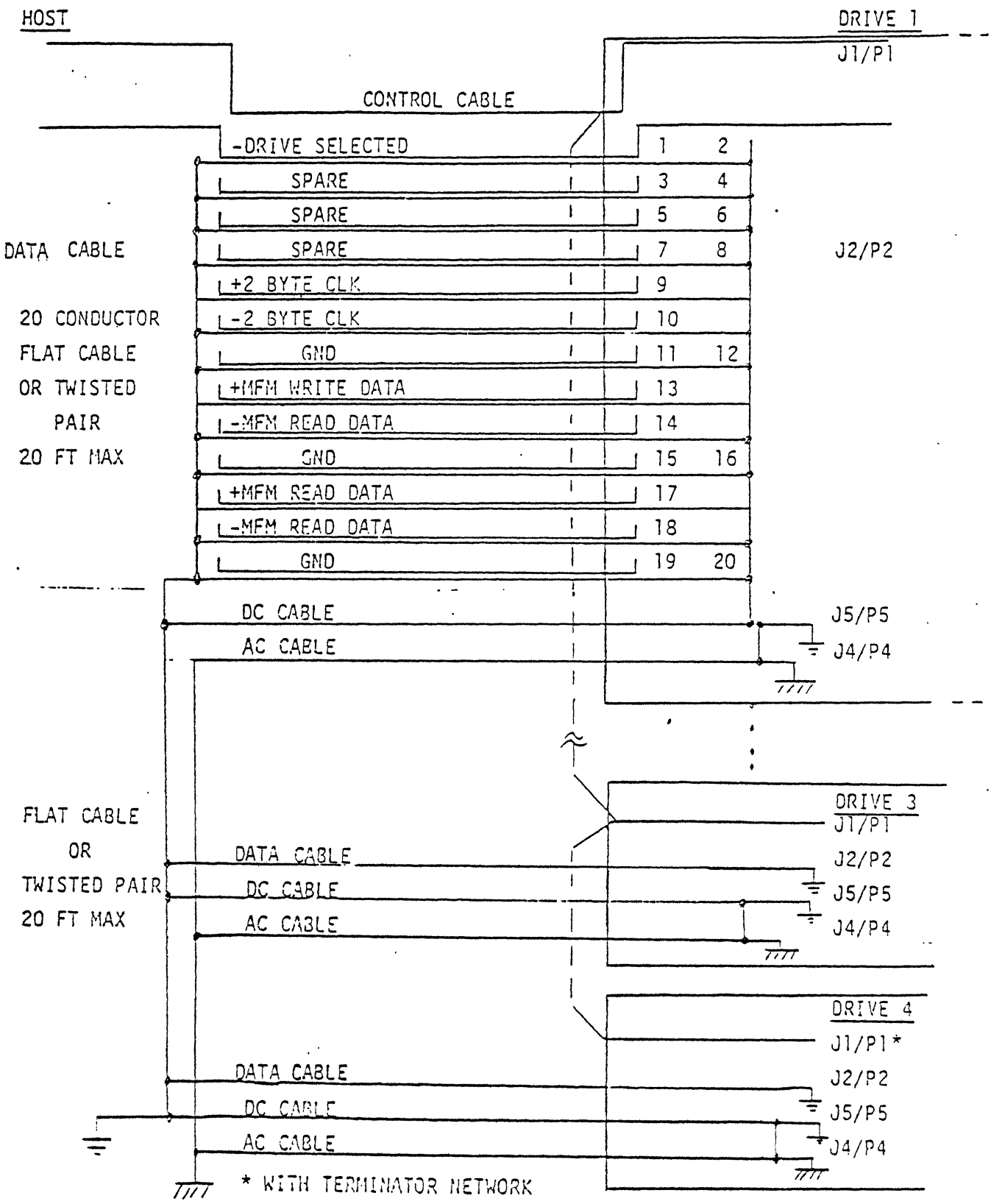
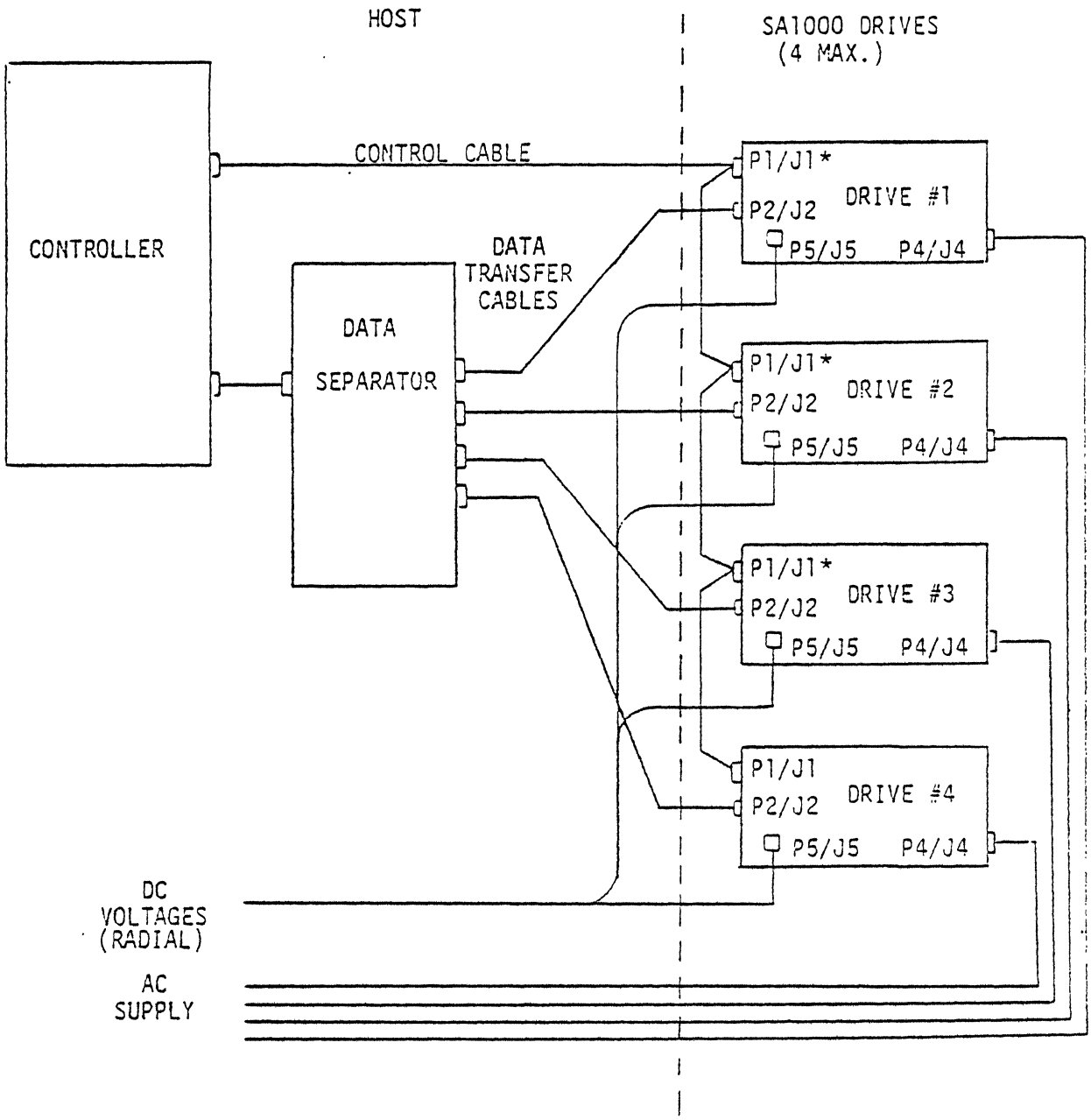


TABLE V INTERFACE CONNECTION - MULTIPLE DRIVE SYSTEM



* TERMINATOR NETWORK REMOVED.

FIGURE 48. TYPICAL CONNECTION - 4 DRIVE SYSTEM

4.0 SIGNAL INTERFACE

The signal interface consists of two categories: Control, and data transfer. All control lines are TTL in nature and either provide signals to the drive (input) or provide signals to the host (output) via interface connector J1/P1. The data transfer signals are differential in nature. They provide data and clocking, either to or from the drive, via the J2/P2 Connector.

4.1 CONTROL INPUT LINES

The control input signals are of two types: Those intended to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are STEP, DIRECTION, HEAD SELECT 2^0 and 2^1, WRITE GATE and REDUCED WRITE CURRENT. The signal which is intended to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to figure 6 for the recommended circuit.

True = 0.0 V DC to 0.4 V DC @ Iin = 40 MA (Max)

False = 2.5 V DC to 5.25 V DC @ Iin = 0 MA (Open)

4.1.1 DRIVE SELECT 1 THRU 4

DRIVE SELECT when true logically connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time and will allow the drive to respond to input signals and gate outputs.

Trace options DS1, DS2, DS3 and DS4 are used to select which drive select input line will activate the interface for a unique drive. The DRIVE SELECT input is terminated as shown in figure 6.

4.1.2 DIRECTION IN

This signal defines direction of motion of the R/W head when the STEP line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the STEP line the R/W head will move away from the center of the disk.

Conversely, if this input is shorted to ground or a logical zero level is applied, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the R/W head will move towards the center of the disk.

A 220/330 Ω resistor pack allows line termination.

4.1.3 STEP

This interface line is a control signal which causes the R/W head to move with the direction of motion defined by the DIRECTION IN line

The access motion is initiated at each logical zero to logical one transition or the trailing edge of this signal pulse. Any change in the DIRECTION IN line must be made at least 100ns before the leading edge of the step pulse.

There are two modes of operation of stepping the R/W heads. The normal mode and the buffered mode.

A 220/330 Ω resistor pack allows line termination.

4.1.3.1 NORMAL STEP MODE

In this mode of operation the R/W head will move at the rate of the incoming step pulses. The minimum time between successive steps is 1.5ms. The minimum pulse width is 300 ns. See figure 5A for normal step mode timing.

4.1.3.2 BUFFERED STEP MODE

In this mode of operation the step pulses are received at a high rate and buffered into a counter. After the last pulse the R/W head will then begin stepping the appropriate number of cylinders and Seek Complete (see section 4.2.5) will go true after the R/W head settles at the cylinder. This mode of operation is automatically selected when the time between step pulses is $\leq$ 200 µsec.

Once the step pulses have been sent to the drive, the Drive Select line may be dropped and a different drive selected. The minimum time after the last step pulse before Drive Select can be dropped is 100 ns.

The minimum time between steps is 300 ns with a pulse width of 300 ns minimum. The maximum time between steps is 200 µs. Refer to figure 5B for Buffered Step Mode Timing.

NOTE: Step pulses with periods between 200 µs and 1.5 ms are not allowed. Seek accurracy is not guaranteed if this restriction is violated.

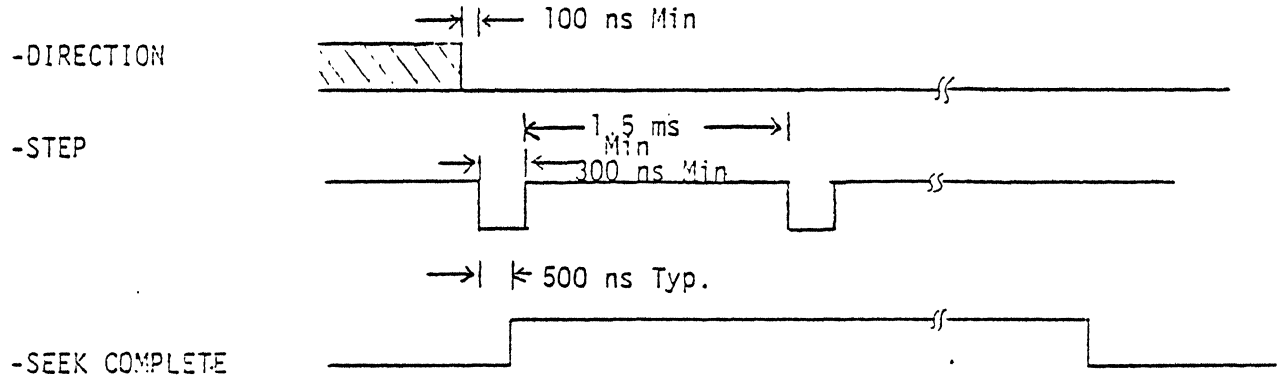


FIGURE 5A. NORMAL STEP MODE TIMING

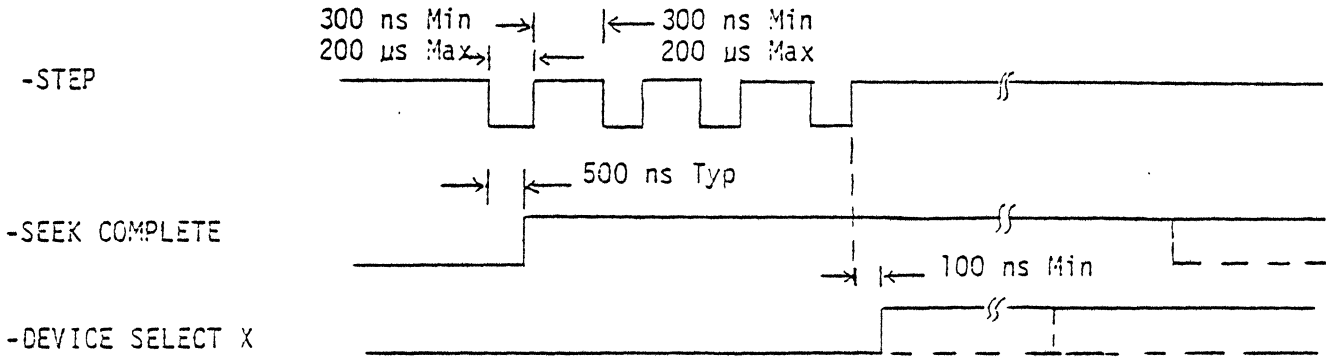


FIGURE 5B. BUFFERED STEP MODE TIMING

4.1.4 HEAD SELECT 2^0 & 2^1

These two lines provide for the selection of each individual read/write heads in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered Ø thru 3. When all HEAD SELECT lines are false head Ø will be selected. Table VI shows the HEAD SELECT sequence and model variations for the HEAD SELECT lines. See figure 11 for timing considerations.

A 220/330Ω resistor pack allows for termination on each line.

HEAD SELECT LINE 2	1	HEAD# SELECTED SA1002	HEAD# SELECTED SA1004
0	0	0	0
0	1	1	1
1	0	-	2
1	1	-	3

TABLE VI HEAD SELECT (0 = False, 1 = True)

4.1.5 WRITE GATE

The active state of this signal, or logical zero level, enables write data to be written on the disk. The inactive state of this signal, or logical one level, enables data to be transferred from the drive. Also, the inactive state of this signal enables the STEP pulses to step the R/W actuator.

A 220/330 resistor pack allows for termination on each line.

4.1.6 REDUCED WRITE CURRENT

This line, when active together with WRITE GATE, causes the write chain to write on the disk with a lower write current. It is re-recommended that this line be set true when writing is to be performed on cylinders 128 through 255, and be set false when writing is to be performed on cylinders 0 through 127.

A 220/330Ω resistor pack allows for line termination.

4.2 OUTPUT LINES

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at logical zero or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in logical one or false state the driver transistor is off and the collector cutoff current is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective DRIVE SELECTED line.

Figure 6 shows the recommended control signal driver/receiver combination.

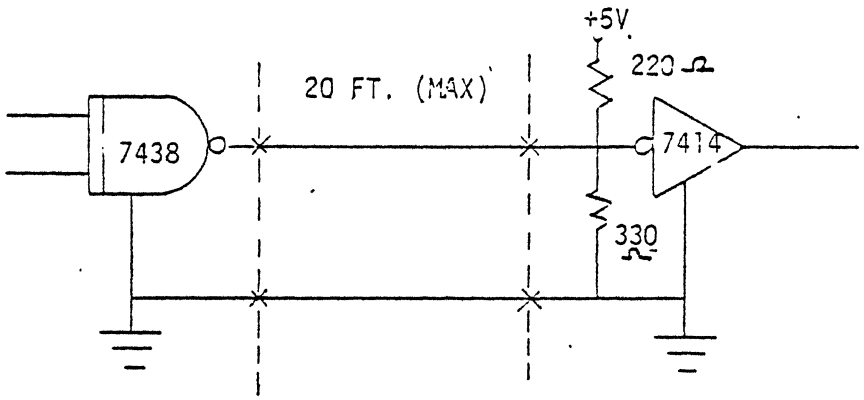


FIGURE 6

CONTROL SIGNAL DRIVER/RECEIVER COMBINATION

4.2.1 TRACK ØØØ

This interface signal indicates a true state only when drive's R/W heads are positioned at track zero (the outermost data track) and the access circuitry is driving current through phase one of the stepper motor. This signal is a logical one level, or false state, when the selected drive's R/W head is not at track zero.

4.2.2 INDEX

This interface signal is provided by the drive once each revolution (19.2 ms) to indicate the beginning of the track. Normally, this signal is a logical one level and makes the transition to the logical zero level for a period of approximately 10 µs once each revolution. The timing of this signal is shown in figure 7.

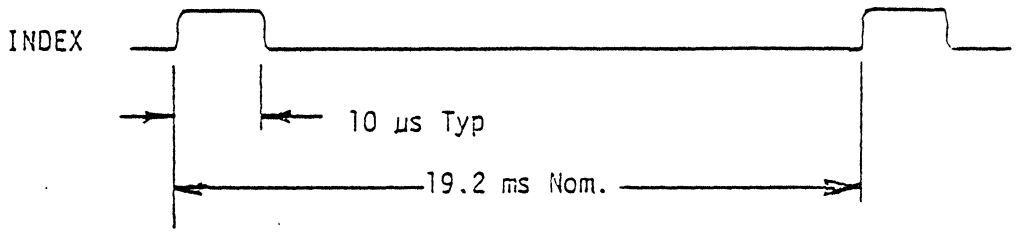


FIGURE 7

INDEX TIMING

4.2.3 READY

This interface signal, when true together with SEEK COMPLETE, indicates that the drive is ready to read, write or seek and that the signals are valid. When this line is false all writing on the disk and seeking is inhibited at the drive.

READY will be true after the drive is 95 ± 2% up to speed.

The typical time for READY to become true after power on is 20 seconds.

4.2.4 WRITE FAULT

This signal is provided by the drive and is used to indicate that a condition exists at the drive that caused improper writing on the disk. When this line goes true, further writing is inhibited at the drive until the condition no longer exists AND that the DRIVE SELECT X line for that particular drive made inactive for at least 500 ns to reset the fault detection circuit

There are two FAULT conditions detected and latched. They are:

(1) WRITE CURRENT in the head without WRITE GATE active.

(2) Multiple HEADS selected.

4.2.5 SEEK COMPLETE

This line will go true when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when SEEK COMPLETE is false.

SEEK COMPLETE will go false in two cases:

(i) a recalibration sequence is initiated (by drive logic) at power on because R/W heads are not over track zero.

(ii) 500 ns (typ.) after the leading edge of a step pulse (or the first of a series of step pulses).

SEEK COMPLETE is gated with DRIVE SELECT. See Figure 5B

4.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Three pairs of balanced signals are used for data transfer in a standard drive: MFM WRITE DATA, MFM READ DATA, and 2 BYTE CLK. Figure 8 illustrates the driver/receiver combination used in the SA1000 drive for DATA TRANSFER signals.

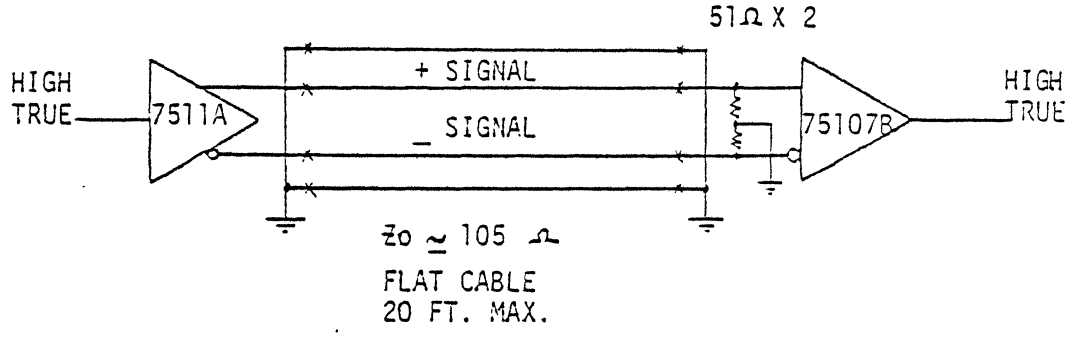


FIGURE 8
DATA LINE DRIVER/RECEIVER

(Positive Logic)

4.3.1 MFM WRITE DATA

This is a differential pair that defines the transitions to be written on the track. The transtion of + MFM WRITE DATA line going more positive than the - MFM WRITE DATA line will cause a flux reversal on the track provided WRITE GATE is active. This signal must be driven to an inactive state (+ MFM WRITE DATA more negative than - MFM WRITE DATA) by the host system when in a read mode. Figure 9 shows the timing for MFM WRITE DATA as required at the interface. The actual occurrence of the flux reversals may differ due to write pre-compensation.

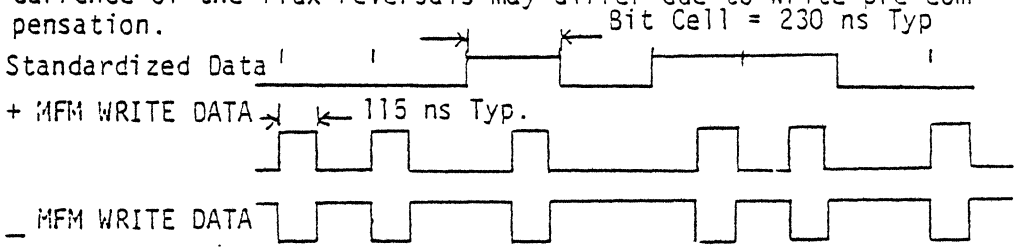


FIGURE 9 MFM WRITE DATA TIMING

4.3.2 MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. The transition of the + MFM READ DATA line going more positive than the - MFM READ DATA line represents a flux reversal on the track of the selected head while READ GATE is active. The timing for MFM READ DATA is given in Figure 10.

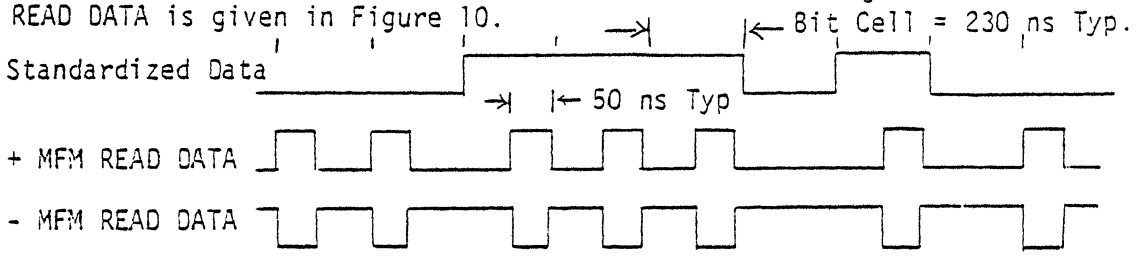


FIGURE 10 MFM READ DATA TIMING

4.3.3 2 BYTE CLK

This is a differential pair of clock signals having a 50% (nominal) duty cycle and a 3.6866 µs ± .1% period. The frequency of this clock is exactly 1/16 times the bit frequency for the standardized write data. Phase relationship between 2 BYTE CLK and MFM WRITE DATA need not be maintained by the host for the SA1000 inferface.

4.4 SELECT STATUS

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driven as shown in Figure 6. This signal will go active only when the drive is programmed as drive X (X = 1,2,3, and 4) by proper placement of the shorting plug at the vicinity of J1, and that the DRIVE SELECT X line at J1/P1 is activated by the host system.

5.0 GENERAL TIMING REQUIREMENTS

The timing diagram as shown in figure 11 shows the necessary sequence of events with associated timing restrictions for proper operation.

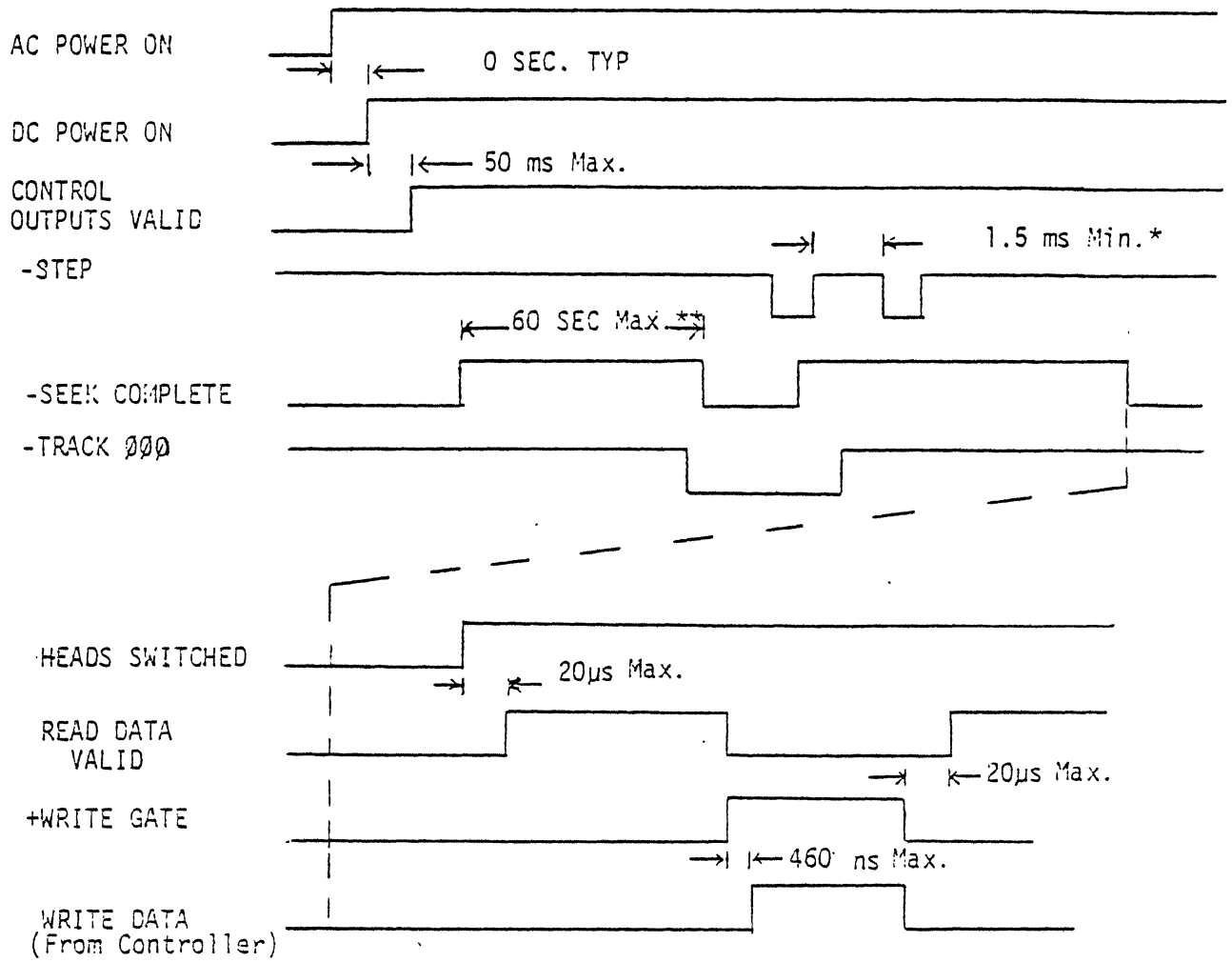
6.0 POWER INTERFACE

The drive requires both AC and DC power for operation. The AC power is used for the drive motor and the DC power is used for the electronics and the stepper motor.

6.1 AC POWER

	60 HZ		50 HZ	
CONN P4	110V (STANDARD)	208/230V	100V	220V
1 2 3	90-127V FRAME GND 90-127V RTN	180-253V FRAME GND 180-253V	90-127V FRAME GND 90-127V RETURN	180-253V FRAME GND 180-253V
MAX INRUSH CURRENT (3 SEC)	4.0A	TBS	TBS	TBS
MAX RUN CURRENT	1.0A	0.5A	1.1A	0.6A
FREQ TOL	± 0.5 HZ		± 0.5 HZ	

TABLE VIII
AC POWER REQUIREMENTS



* FOR NORMAL STEP MODE

** TIME FOR RECALIBRATION IS DEPENDENT ON POSITION OF R/W HEADS AT AC AND DC POWER ON.

FIGURE 11

GENERAL/CONTROL TIMING REQUIREMENTS

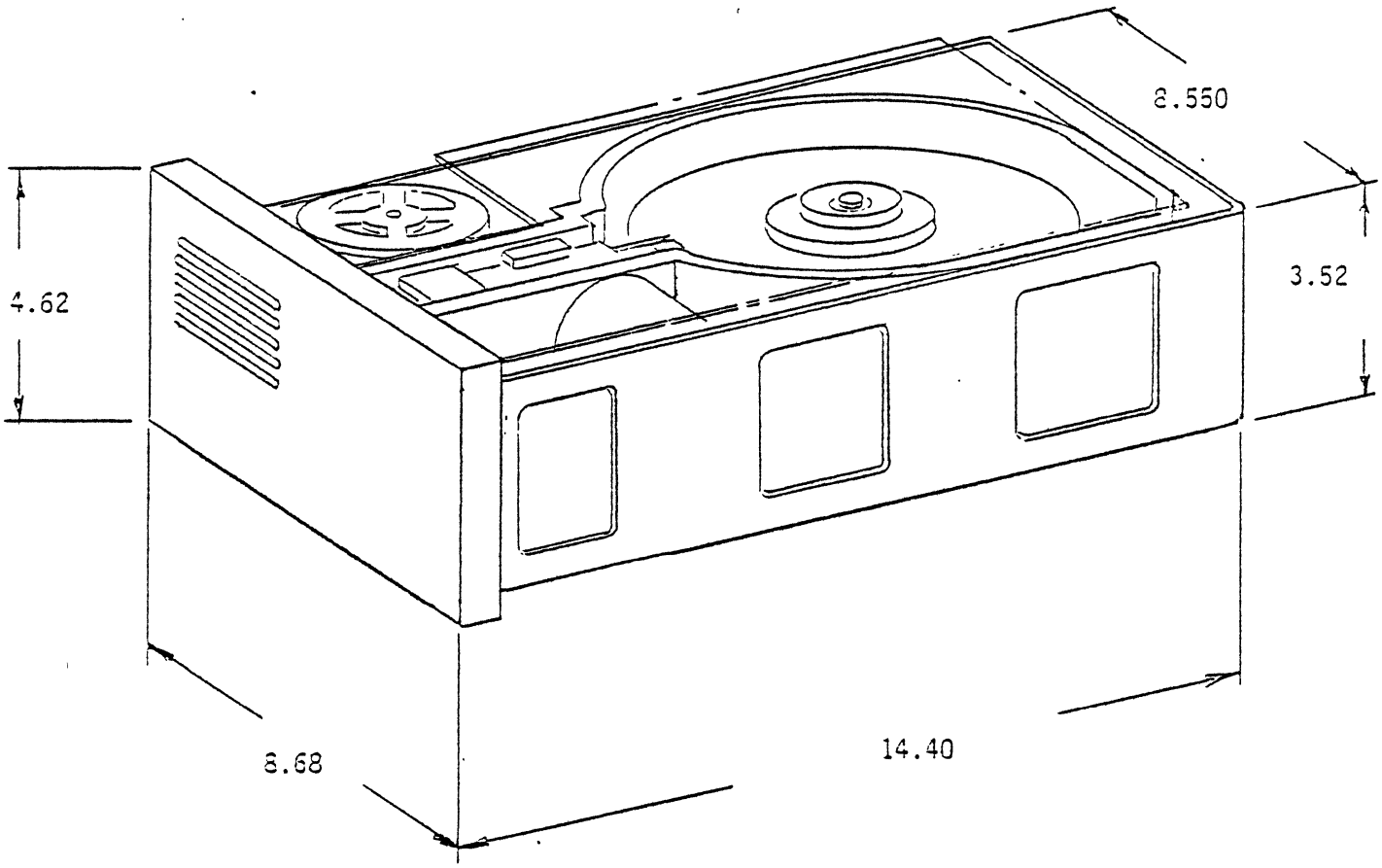
6.2 DC POWER

DC power to the drive is via P5/J5. The three required voltages are as follows:

DC VOLTAGE	CURRENT			
	STEADY STATE		STEPPING	
	MAX.	TYP	MAX.	TYP
+24 ± 2.4V 1V. P-P Max Ripple	0.25A	0.20A	3.3A	2.8A
+5 ± 0.25V 50mV P-P Max Ripple	4.1A	3.6A	4.1A	3.6A
-7 TO -16V (-5 ± 0.25V OPT) 50mV P-P Max Ripple	0.25A	0.20A	0.25A	0.20A

7.0 PHYSICAL OUTLINE

The mechainical outline of the SA1000 is given in Figures 12 and 13.



All dimensions in inches.

FIGURE 12 SA1000 MECHANICAL OUTLINE
GENERAL PERPECTIVE

All dimensions in inches

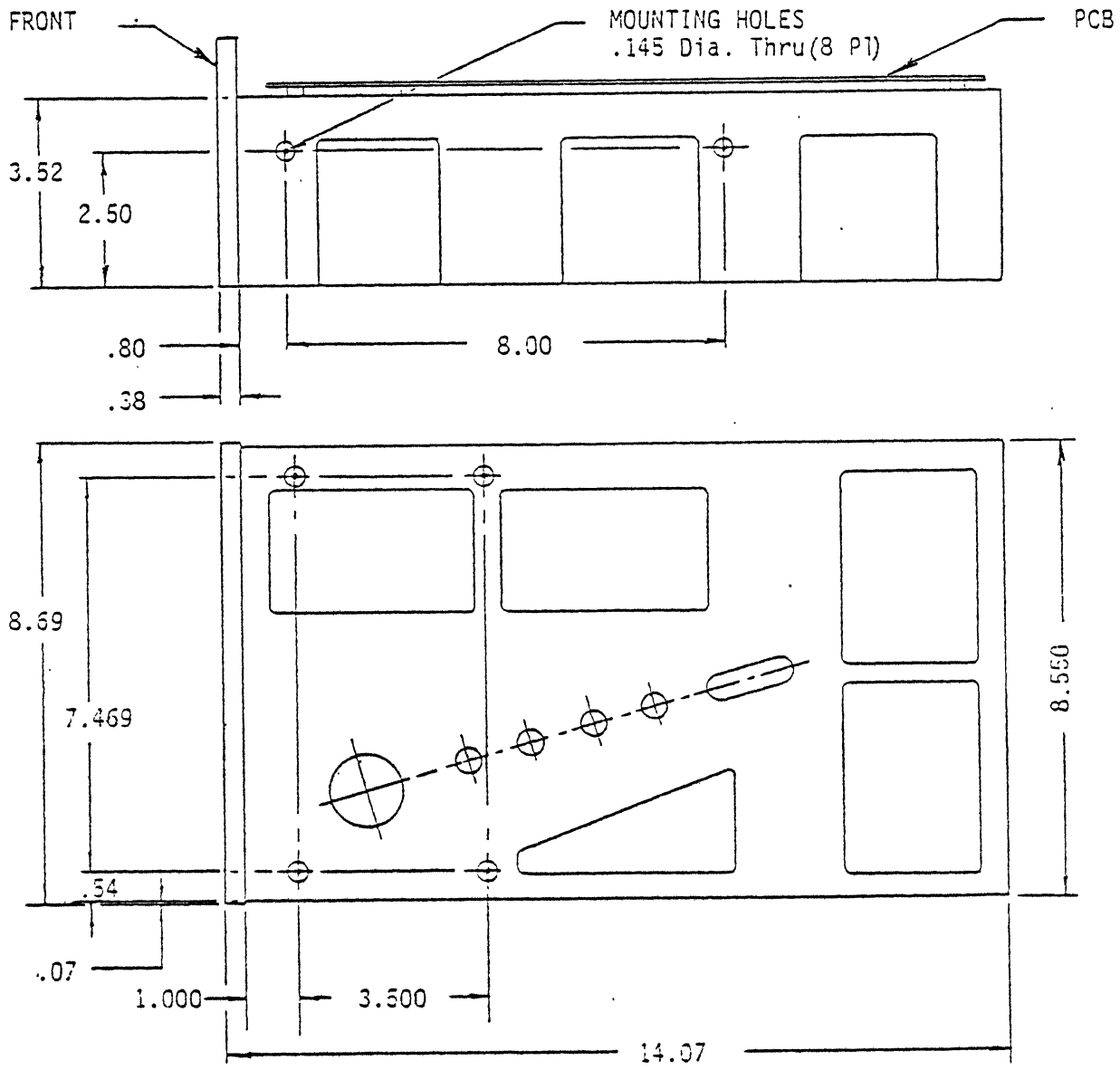


FIGURE 13 SA1000 MECHANICAL OUTLINE
BOTTOM AND SIDE VIEW