INDY ELAN GRAPHICS - GR4 BOARD

(Fab # 034-8234-002 REV. A)

ATTENTION!! THERE ARE SOME REFERENCE DESIGNATORS ON THE SILKSCREEN THAT ARE PLACE INCORRECTLY ON THIS BOARD.
PLEASE SEE PAGE 8 FOR DETAILS.

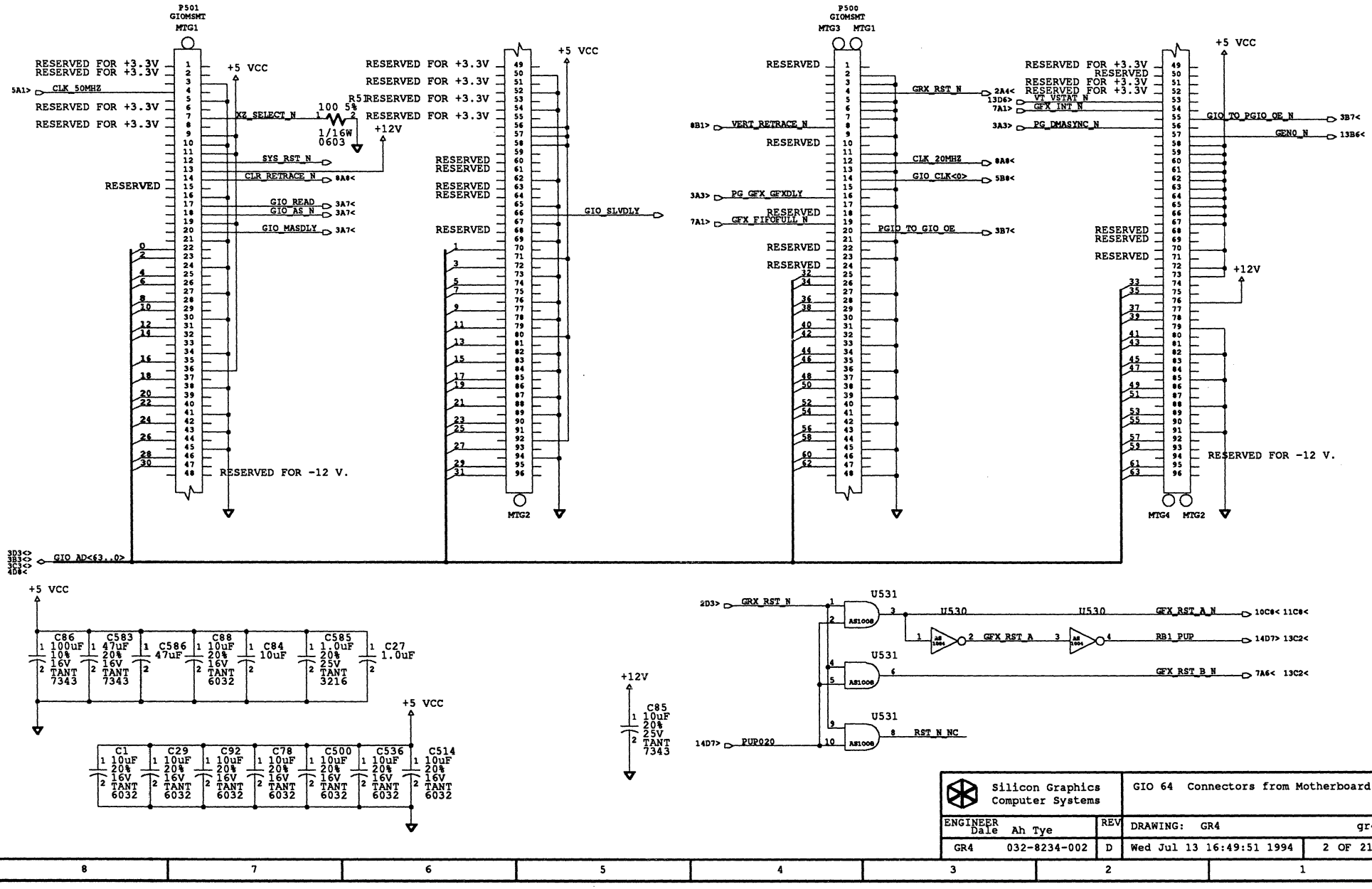
SCHEMATIC #032-8234-002 REV D

Silicon Graphics Computer Systems - Digital Sight & Sound

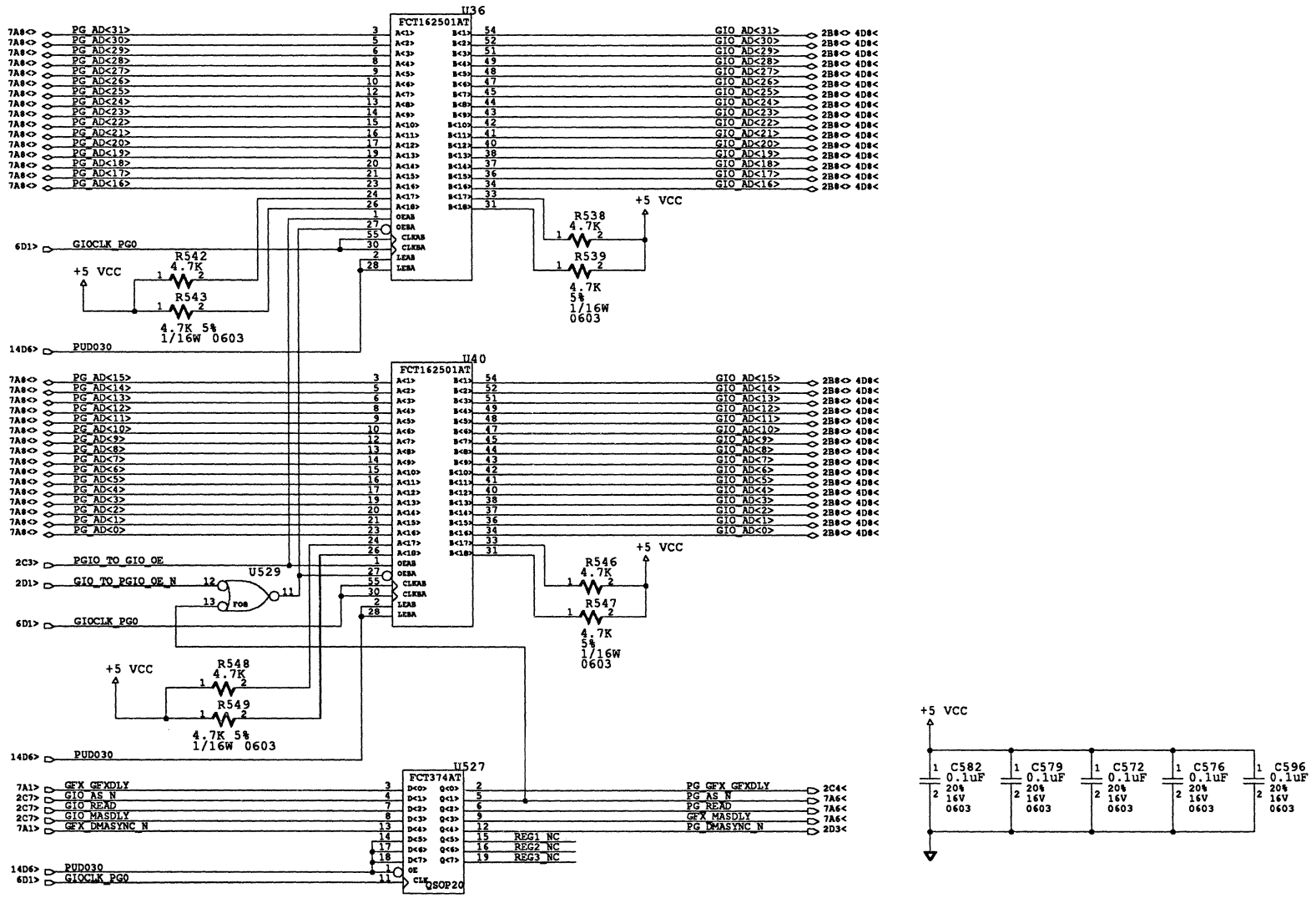
APPROVALS	DATE
DRW Dale Ah Tye	07/13/94
CHK	
RLS	
RLS	

GR4

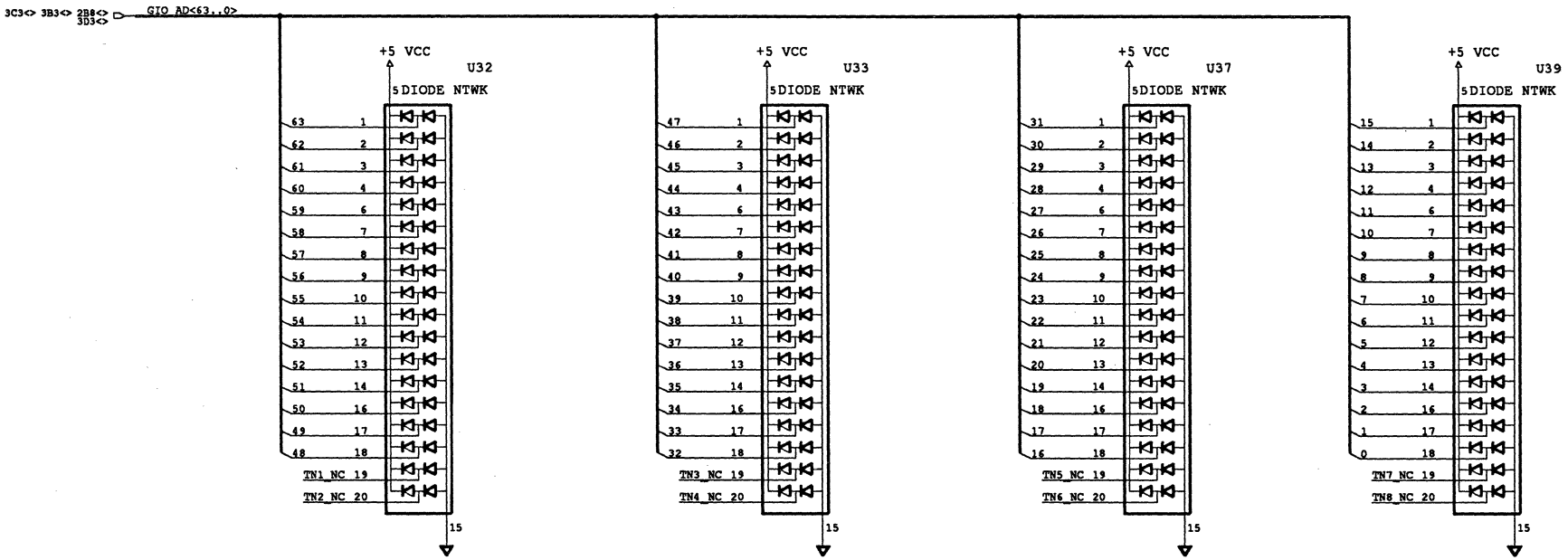
	REV	DATE	SHEET
032-8234-002	D	July 13, 1994	1 OF 21



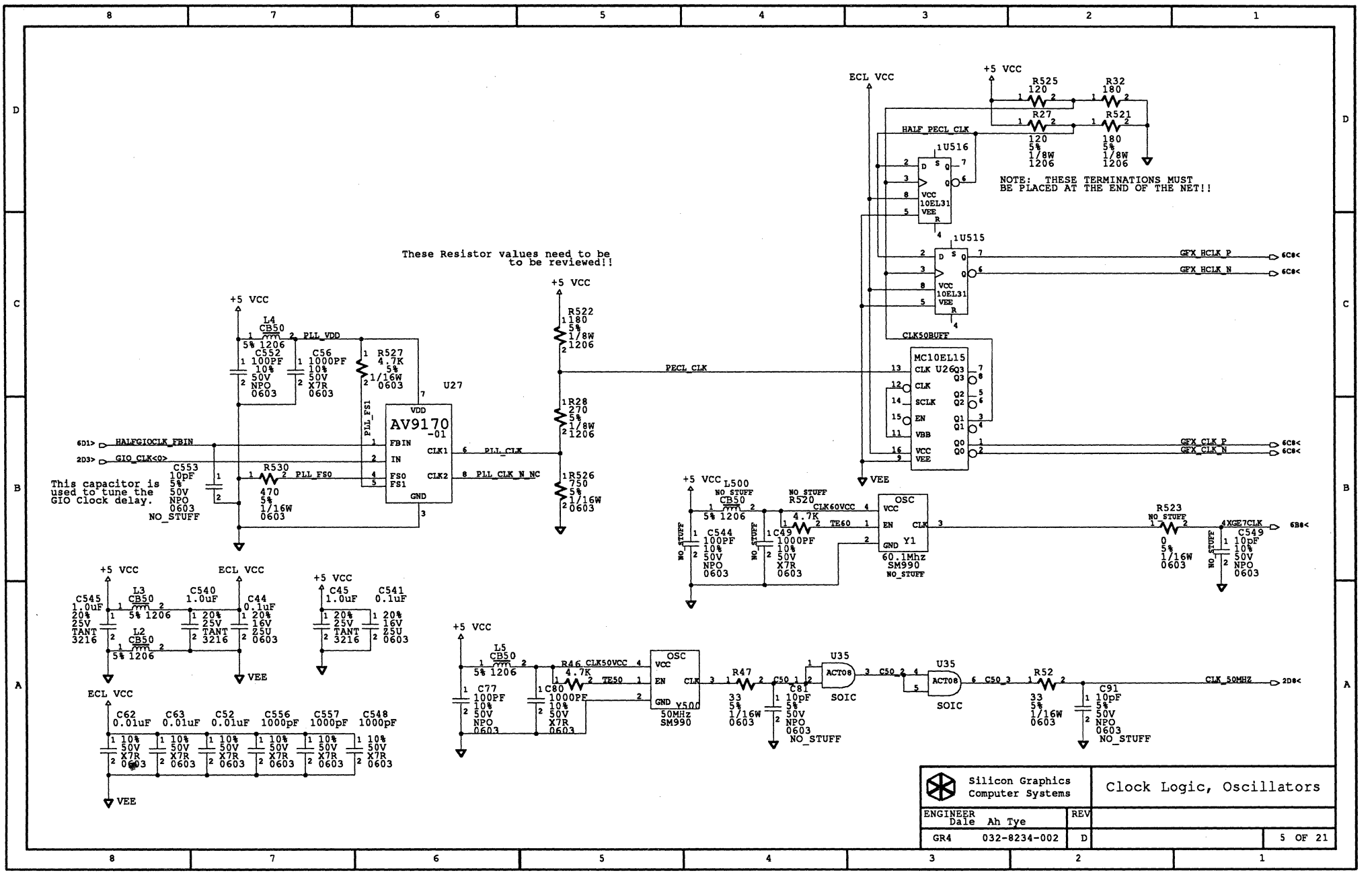
Silicon Graphics Computer Systems		GIO 64 Connectors from Motherboard	
ENGINEER Dale Ah Tye	REV	DRAWING: GR4	gr4
GR4 032-8234-002	D	Wed Jul 13 16:49:51 1994	2 OF 21



Silicon Graphics Computer Systems		Pipeline Registers	
ENGINEER Dale Ah Tye	REV	DRAWING: GR4	gr4
GR4 032-8234-002	D	Wed Jul 13 16:50:36 1994	3 OF 21



Silicon Graphics Computer Systems			GIO 64 clamp diodes
ENGINEER Dale Ah Tye		REV	DRAWING: GR4 gr4
GR4	032-8234-002	D	Wed Jul 13 16:51:01 1994 — 4 OF 21


These Resistor values need to be to be reviewed!!
NOTE: THESE TERMINATIONS MUST BE PLACED AT THE END OF THE NET!!
This capacitor is used to tune the GIO Clock delay.
AV9170 -01
MC10EL15
10EL31
OSC
60.1Mhz SM990
50MHz SM990
NO_STUFF
SOIC
Silicon Graphics Computer Systems
Clock Logic, Oscillators
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
D
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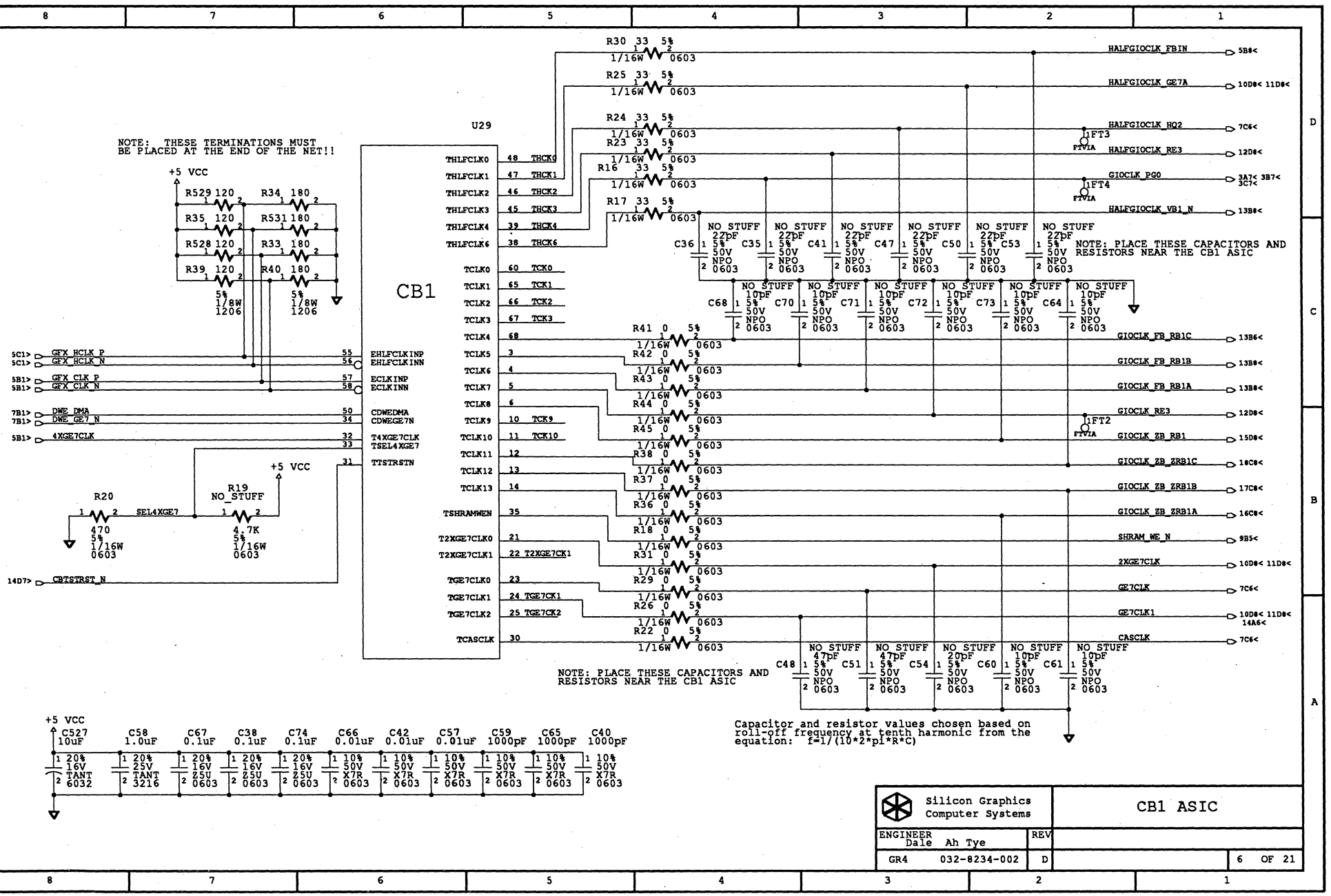
NOTE: THESE TERMINATIONS MUST BE PLACED AT THE END OF THE NET!!
+5 VCC
R529 120 5% 1/8W 1206
R34 180 5% 1/8W 1206
R35 120
R531 180
R528 120
R33 180
R39 120
R40 180
U29
CB1
THLFCLK0 48 THCK0
THLFCLK1 47 THCK1
THLFCLK2 46 THCK2
THLFCLK3 45 THCK3
THLFCLK4 39 THCK4
THLFCLK6 38 THCK6
TCLK0 60 TCK0
TCLK1 65 TCK1
TCLK2 66 TCK2
TCLK3 67 TCK3
TCLK4 68
TCLK5 3
TCLK6 4
TCLK7 5
TCLK8 6
TCLK9 10 TCK9
TCLK10 11 TCK10
TCLK11 12
TCLK12 13
TCLK13 14
TSHRAMWEN 35
T2XGE7CLK0 21
T2XGE7CLK1 22 T2XGE7CK1
TGE7CLK0 23
TGE7CLK1 24 TGE7CK1
TGE7CLK2 25 TGE7CK2
TCASCLK 30
EHLFCLKINP 55
EHLFCLKINN 56
ECLKINP 57
ECLKINN 58
CDWEDMA 50
CDWEGE7N 34
T4XGE7CLK 32
TSEL4XGE7 33
TTSTRSTN 31
5C1> GFX_HCLK_P
5C1> GFX_HCLK_N
5B1> GFX_CLK_P
5B1> GFX_CLK_N
7B1> DWE_DMA
7B1> DWE_GE7_N
5B1> 4XGE7CLK
14D7> CBTSTRST_N
R20 470 5% 1/16W 0603
R19 NO_STUFF 4.7K 5% 1/16W 0603
SEL4XGE7
R30 33 5% 1/16W 0603
R25 33 5% 1/16W 0603
R24 33 5% 1/16W 0603
R23 33 5% 1/16W 0603
R16 33 5% 1/16W 0603
R17 33 5% 1/16W 0603
R41 0 5% 1/16W 0603
R42 0 5% 1/16W 0603
R43 0 5% 1/16W 0603
R44 0 5% 1/16W 0603
R45 0 5% 1/16W 0603
R38 0 5% 1/16W 0603
R37 0 5% 1/16W 0603
R36 0 5% 1/16W 0603
R18 0 5% 1/16W 0603
R31 0 5% 1/16W 0603
R29 0 5% 1/16W 0603
R26 0 5% 1/16W 0603
R22 0 5% 1/16W 0603
NO STUFF 22pF 5% 50V NPO 0603
C36 C35 C41 C47 C50 C53
NOTE: PLACE THESE CAPACITORS AND RESISTORS NEAR THE CB1 ASIC
NO STUFF 10pF 5% 50V NPO 0603
C68 C70 C71 C72 C73 C64
NO STUFF 47pF 5% 50V NPO 0603
C48 C51 C54
NO STUFF 20pF 5% 50V NPO 0603
C60
NO STUFF 10pF 5% 50V NPO 0603
C61
NOTE: PLACE THESE CAPACITORS AND RESISTORS NEAR THE CB1 ASIC
1FT3 FTV1A
1FT4 FTV1A
1FT2 FTV1A
HALFGIOCLK_FBIN 5B8<
HALFGIOCLK_GE7A 10D8< 11D8<
HALFGIOCLK_HQ2 7C6<
HALFGIOCLK_RE3 12D8<
GIOCLK_PG0 3A7< 3B7< 3C7<
HALFGIOCLK_VB1_N 13B8<
GIOCLK_FB_RB1C 13B6<
GIOCLK_FB_RB1B 13B8<
GIOCLK_FB_RB1A 13B8<
GIOCLK_RE3 12D8<
GIOCLK_ZB_RB1 15D8<
GIOCLK_ZB_ZRB1C 18C8<
GIOCLK_ZB_ZRB1B 17C8<
GIOCLK_ZB_ZRB1A 16C8<
SHRAM_WE_N 9B5<
2XGE7CLK 10D8< 11D8<
GE7CLK 7C6<
GE7CLK1 10D8< 11D8< 14A6<
CASCLK 7C6<
+5 VCC
C527 10uF 20% 16V TANT 6032
C58 1.0uF 20% 25V TANT 3216
C67 0.1uF 20% 16V Z5U 0603
C38 0.1uF 20% 16V Z5U 0603
C74 0.1uF 20% 16V Z5U 0603
C66 0.01uF 10% 50V X7R 0603
C42 0.01uF 10% 50V X7R 0603
C57 0.01uF 10% 50V X7R 0603
C59 1000pF 10% 50V X7R 0603
C65 1000pF 10% 50V X7R 0603
C40 1000pF 10% 50V X7R 0603
Capacitor and resistor values chosen based on roll-off frequency at tenth harmonic from the equation: f=1/(10*2*pi*R*C)
Silicon Graphics Computer Systems
CB1 ASIC
ENGINEER Dale Ah Tye
REV
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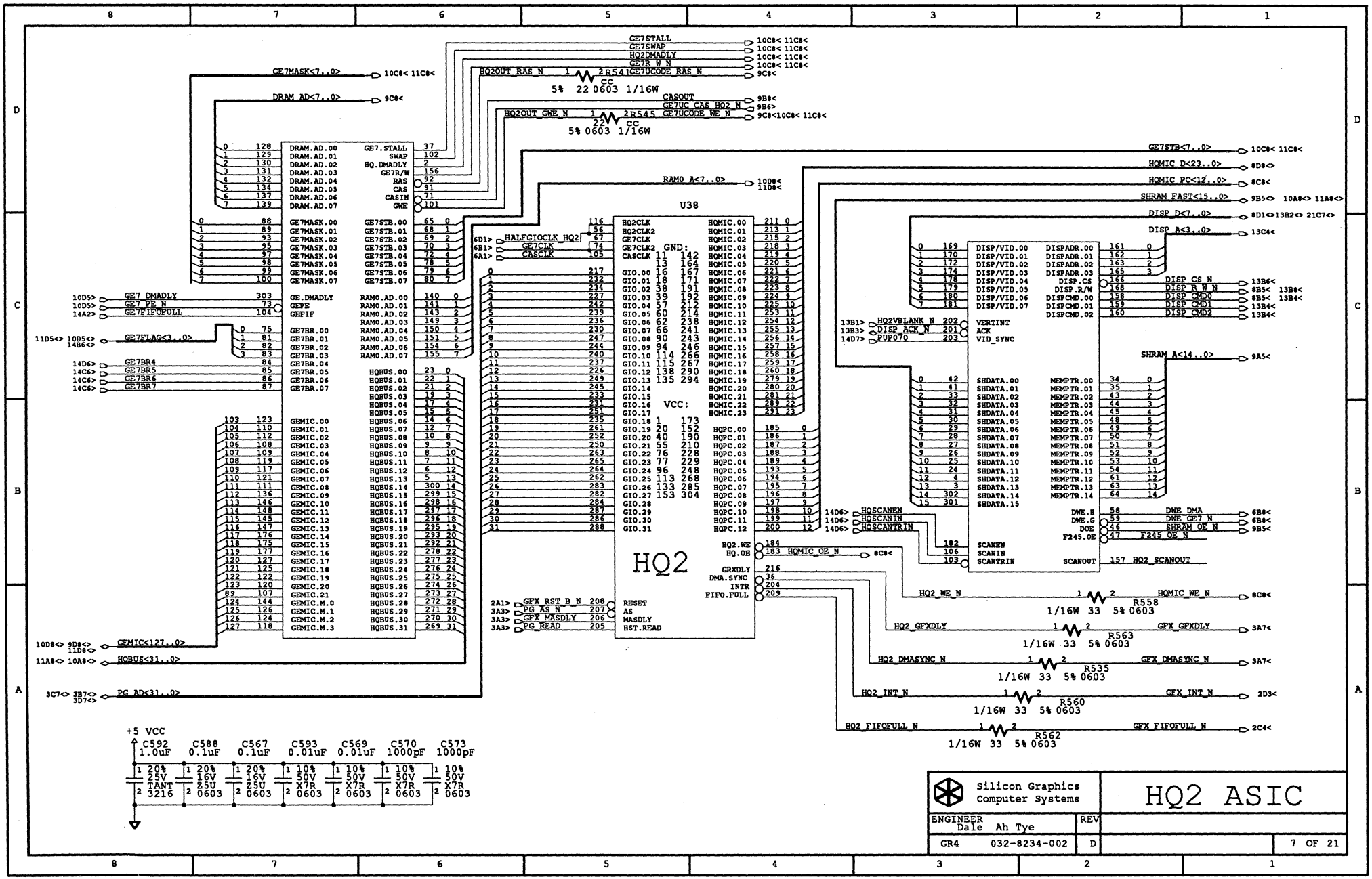
HQ2
U38
GE7STALL
GE7SWAP
HQ2DMADLY
GE7R/W N
HQ2OUT_RAS_N
2R541 22 CC 5% 0603 1/16W
GE7UCODE_RAS_N
CASOUT
GE7UC_CAS_HQ2_N
HQ2OUT_GWE_N
2R545 22 CC 5% 0603 1/16W
GE7UCODE_WE_N
GE7MASK<7..0>
DRAM_AD<7..0>
RAM0_A<7..0>
GE7STB<7..0>
HQMIC_D<23..0>
HQMIC_PC<12..0>
SHRAM_FAST<15..0>
DISP_D<7..0>
DISP_A<3..0>
SHRAM_A<14..0>
GE7_DMADLY
GE7_PE_N
GE7FIFOFULL
GE7FLAG<3..0>
GE7BR4
GE7BR5
GE7BR6
GE7BR7
HALFGIOCLK_HQ2
GE7CLK
CASCLK
GFX_RST_B_N
PG_AS_N
GFX_MASDLY
PG_READ
GEMIC<127..0>
HQBUS<31..0>
PG_AD<31..0>
HQ2VBLANK_N
DISP_ACK_N
PUP070
VERTINT
ACK
VID_SYNC
HQSCANEN
HQSCANIN
HQSCANTRIN
SCANEN
SCANIN
SCANTRIN
SCANOUT
HQ2_SCANOUT
HQ2.WE
HQ.OE
HQMIC_OE_N
GRXDLY
DMA.SYNC
INTR
FIFO.FULL
RESET
AS
MASDLY
BST.READ
HQ2_WE_N
HQMIC_WE_N
R558 1/16W 33 5% 0603
HQ2_GFXDLY
GFX_GFXDLY
R563 1/16W 33 5% 0603
HQ2_DMASYNC_N
GFX_DMASYNC_N
R535 1/16W 33 5% 0603
HQ2_INT_N
GFX_INT_N
R560 1/16W 33 5% 0603
HQ2_FIFOFULL_N
GFX_FIFOFULL_N
R562 1/16W 33 5% 0603
+5 VCC
C592 1.0uF 20% 25V TANT 3216
C588 0.1uF 20% 16V Z5U 0603
C567 0.1uF 20% 16V Z5U 0603
C593 0.01uF 10% 50V X7R 0603
C569 0.01uF 10% 50V X7R 0603
C570 1000pF 10% 50V X7R 0603
C573 1000pF 10% 50V X7R 0603
Silicon Graphics Computer Systems
HQ2 ASIC
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
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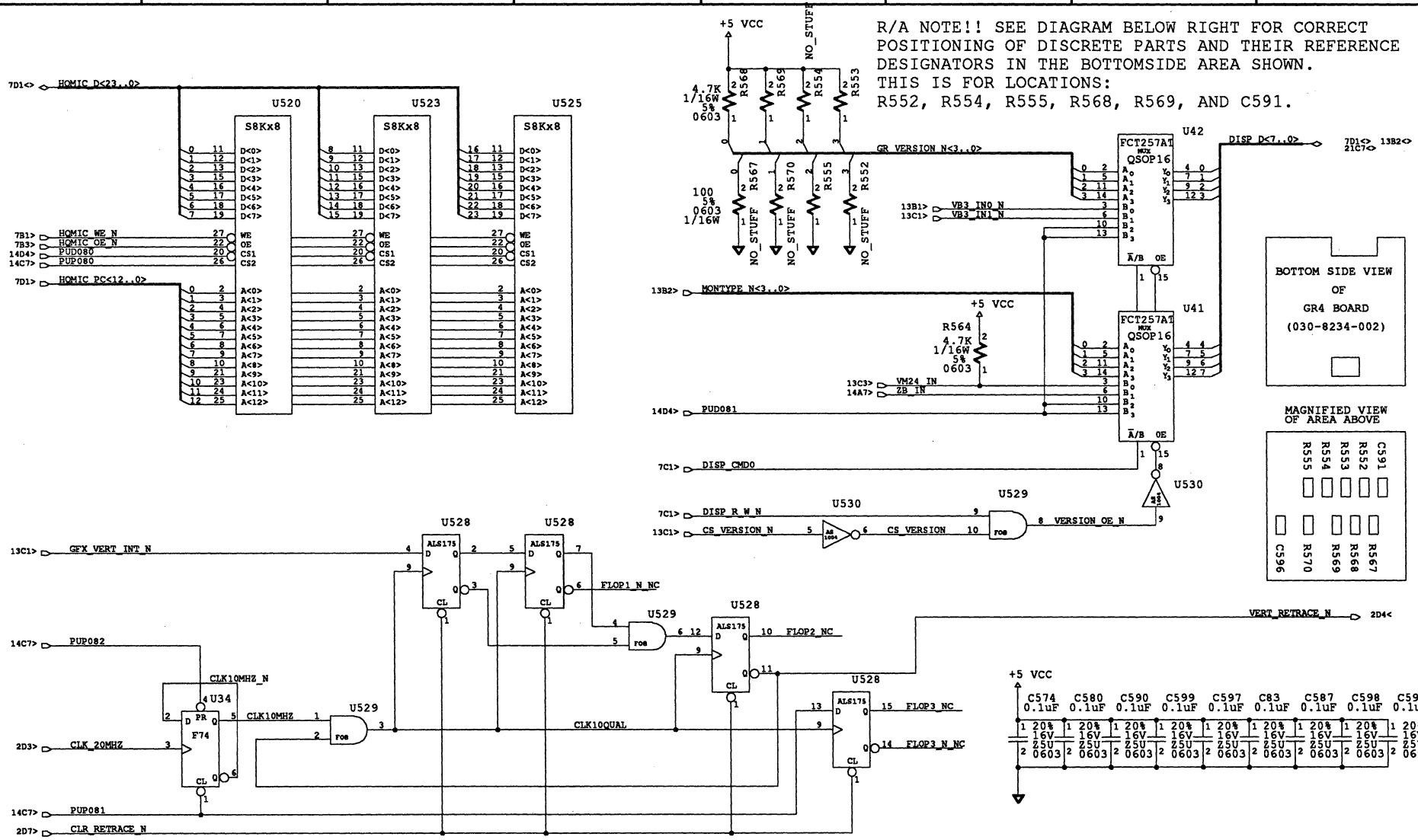
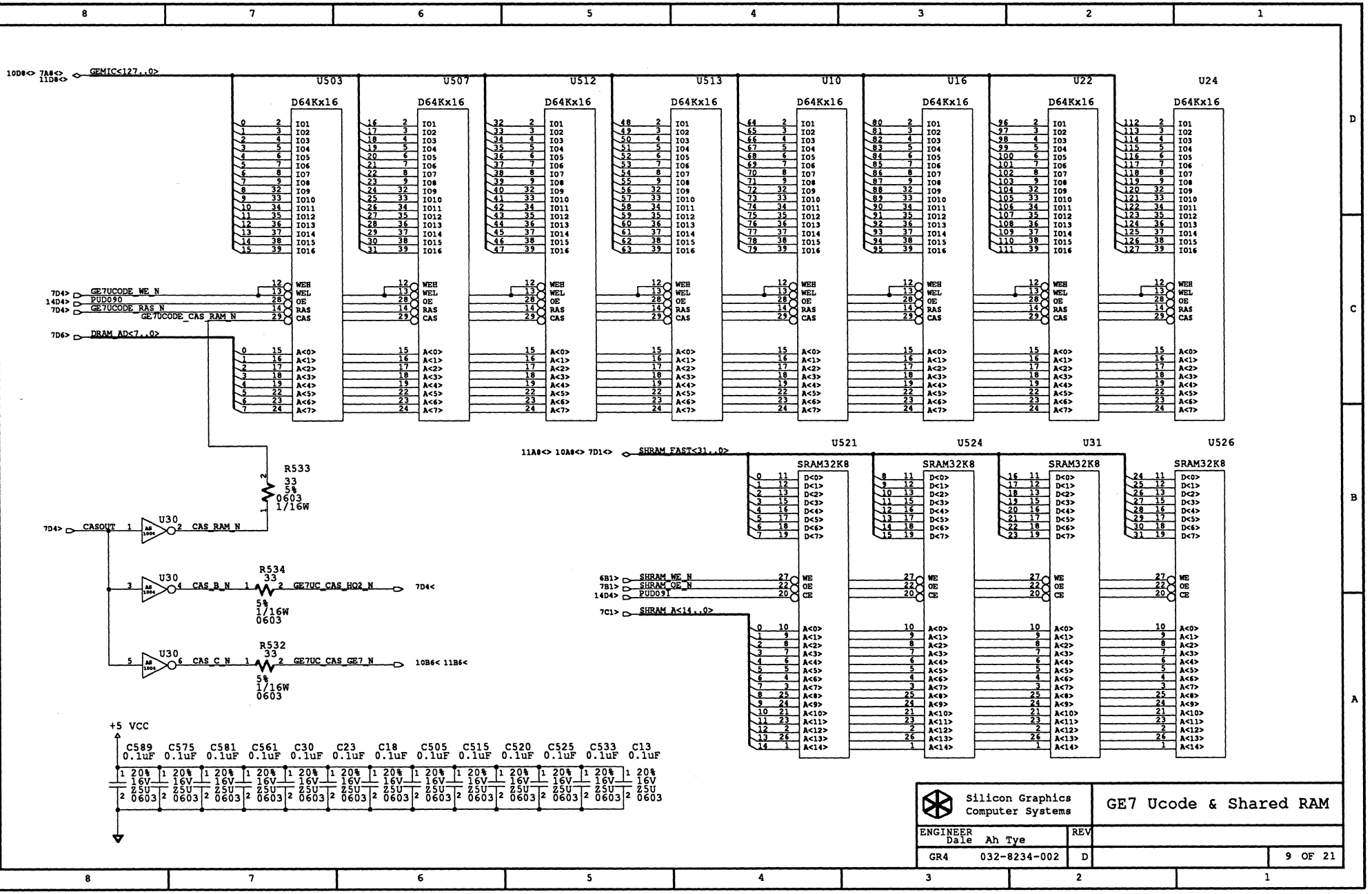
R/A NOTE!! SEE DIAGRAM BELOW RIGHT FOR CORRECT POSITIONING OF DISCRETE PARTS AND THEIR REFERENCE DESIGNATORS IN THE BOTTOMSIDE AREA SHOWN.
THIS IS FOR LOCATIONS:
R552, R554, R555, R568, R569, AND C591.



Silicon Graphics Computer Systems	HQ2 UCODE, VERSION, AND INTERRUPT EDGE TO LEVEL CONVERSION	
ENGINEER Dale Ah Tye	REV	
GR4 032-8234-002	D	8 OF 21


GEMIC<127..0>
U503
U507
U512
U513
U10
U16
U22
U24
D64Kx16
GE7UCODE_WE_N
PUD090
GE7UCODE_RAS_N
GE7UCODE_CAS_RAM_N
DRAM_AD<7..0>
R533
33
5%
0603
1/16W
U30
CASOUT
CAS_RAM_N
R534
CAS_B_N
GE7UC_CAS_HQ2_N
R532
CAS_C_N
GE7UC_CAS_GE7_N
+5 VCC
C589 C575 C581 C561 C30 C23 C18 C505 C515 C520 C525 C533 C13
0.1uF
SHRAM_FAST<31..0>
U521
U524
U31
U526
SRAM32K8
SHRAM_WE_N
SHRAM_OE_N
PUD091
SHRAM_A<14..0>
Silicon Graphics
Computer Systems
GE7 Ucode & Shared RAM
ENGINEER
Dale Ah Tye
REV
GR4
032-8234-002
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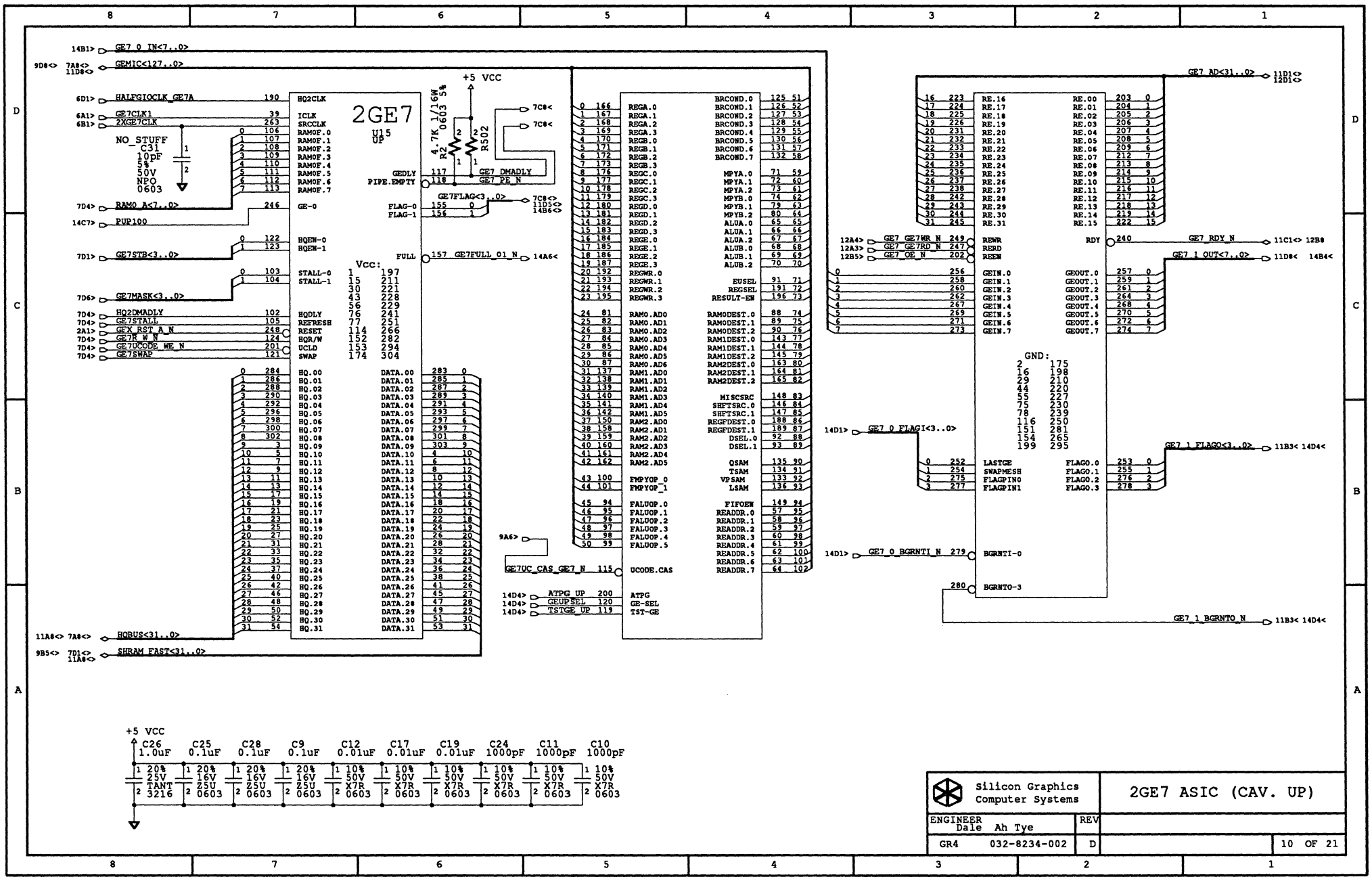
2GE7
U15
UP
Vcc:
+5 VCC
NO_STUFF
C31
10pF
5%
50V
NPO
0603
4.7K 1/16W 5%
R2
0603
R502
GE7 0 IN<7..0>
GEMIC<127..0>
HALFGIOCLK_GE7A
GE7CLK1
2XGE7CLK
RAM0_A<7..0>
PUP100
GE7STB<3..0>
GE7MASK<3..0>
HQ2DMADLY
GE7STALL
GFX_RST_A_N
GE7R_W_N
GE7UCODE_WE_N
GE7SWAP
HOBUS<31..0>
SHRAM_FAST<31..0>
GE7UC_CAS_GE7_N
GE7 DMADLY
GE7 PE_N
GE7FLAG<3..0>
GE7FULL_01_N
GE7 AD<31..0>
GE7 GE7WR_N
GE7 GE7RD_N
GE7 OE_N
GE7 RDY_N
GE7 1 OUT<7..0>
GE7 0 FLAGI<3..0>
GE7 1 FLAGO<3..0>
GE7 0 BGRNTI_N
GE7 1 BGRNTO_N
GND:
+5 VCC
C26 1.0uF
C25 0.1uF
C28 0.1uF
C9 0.1uF
C12 0.01uF
C17 0.01uF
C19 0.01uF
C24 1000pF
C11 1000pF
C10 1000pF
Silicon Graphics Computer Systems
2GE7 ASIC (CAV. UP)
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
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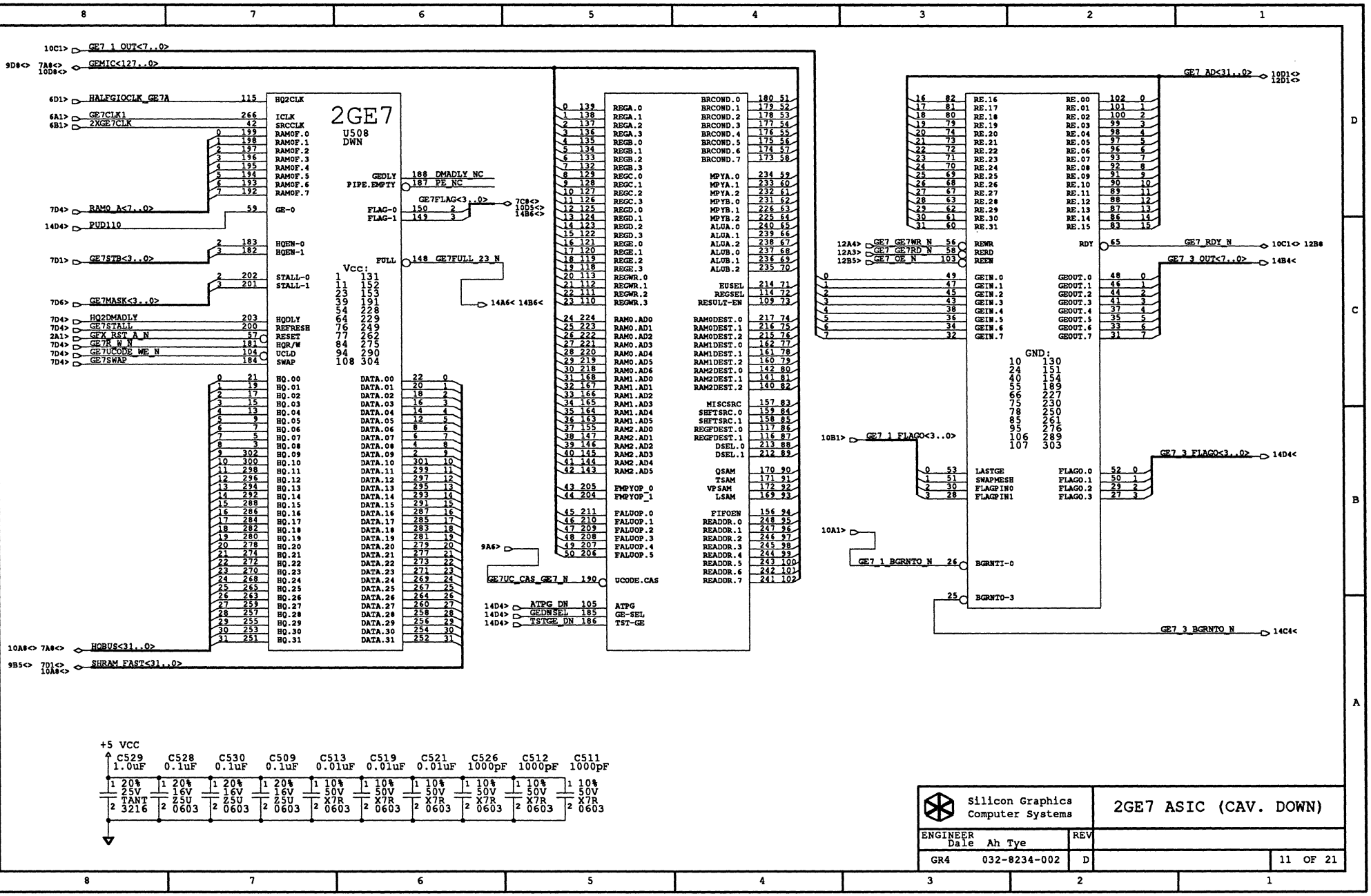
2GE7
U508
DWN
Vcc:
GND:
HQ2CLK
ICLK
SRCCLK
RAMOF.0
RAMOF.1
RAMOF.2
RAMOF.3
RAMOF.4
RAMOF.5
RAMOF.6
RAMOF.7
GE-0
HQEN-0
HQEN-1
STALL-0
STALL-1
HQDLY
REFRESH
RESET
HQR/W
UCLD
SWAP
HQ.00
HQ.01
HQ.02
HQ.03
HQ.04
HQ.05
HQ.06
HQ.07
HQ.08
HQ.09
HQ.10
HQ.11
HQ.12
HQ.13
HQ.14
HQ.15
HQ.16
HQ.17
HQ.18
HQ.19
HQ.20
HQ.21
HQ.22
HQ.23
HQ.24
HQ.25
HQ.26
HQ.27
HQ.28
HQ.29
HQ.30
HQ.31
GEDLY
PIPE.EMPTY
FLAG-0
FLAG-1
FULL
DATA.00
DATA.01
DATA.02
DATA.03
DATA.04
DATA.05
DATA.06
DATA.07
DATA.08
DATA.09
DATA.10
DATA.11
DATA.12
DATA.13
DATA.14
DATA.15
DATA.16
DATA.17
DATA.18
DATA.19
DATA.20
DATA.21
DATA.22
DATA.23
DATA.24
DATA.25
DATA.26
DATA.27
DATA.28
DATA.29
DATA.30
DATA.31
REGA.0
REGA.1
REGA.2
REGA.3
REGB.0
REGB.1
REGB.2
REGB.3
REGC.0
REGC.1
REGC.2
REGC.3
REGD.0
REGD.1
REGD.2
REGD.3
REGE.0
REGE.1
REGE.2
REGE.3
REGWR.0
REGWR.1
REGWR.2
REGWR.3
RAM0.AD0
RAM0.AD1
RAM0.AD2
RAM0.AD3
RAM0.AD4
RAM0.AD5
RAM0.AD6
RAM1.AD0
RAM1.AD1
RAM1.AD2
RAM1.AD3
RAM1.AD4
RAM1.AD5
RAM2.AD0
RAM2.AD1
RAM2.AD2
RAM2.AD3
RAM2.AD4
RAM2.AD5
FMPYOP_0
FMPYOP_1
FALUOP.0
FALUOP.1
FALUOP.2
FALUOP.3
FALUOP.4
FALUOP.5
UCODE.CAS
ATPG
GE-SEL
TST-GE
BRCOND.0
BRCOND.1
BRCOND.2
BRCOND.3
BRCOND.4
BRCOND.5
BRCOND.6
BRCOND.7
MPYA.0
MPYA.1
MPYA.2
MPYB.0
MPYB.1
MPYB.2
ALUA.0
ALUA.1
ALUA.2
ALUB.0
ALUB.1
ALUB.2
EUSEL
REGSEL
RESULT-EN
RAM0DEST.0
RAM0DEST.1
RAM0DEST.2
RAM1DEST.0
RAM1DEST.1
RAM1DEST.2
RAM2DEST.0
RAM2DEST.1
RAM2DEST.2
MISCSRC
SHFTSRC.0
SHFTSRC.1
REGFDEST.0
REGFDEST.1
DSEL.0
DSEL.1
QSAM
TSAM
VPSAM
LSAM
FIFOEN
READDR.0
READDR.1
READDR.2
READDR.3
READDR.4
READDR.5
READDR.6
READDR.7
RE.16
RE.17
RE.18
RE.19
RE.20
RE.21
RE.22
RE.23
RE.24
RE.25
RE.26
RE.27
RE.28
RE.29
RE.30
RE.31
RE.00
RE.01
RE.02
RE.03
RE.04
RE.05
RE.06
RE.07
RE.08
RE.09
RE.10
RE.11
RE.12
RE.13
RE.14
RE.15
REWR
RERD
REEN
RDY
GEIN.0
GEIN.1
GEIN.2
GEIN.3
GEIN.4
GEIN.5
GEIN.6
GEIN.7
GEOUT.0
GEOUT.1
GEOUT.2
GEOUT.3
GEOUT.4
GEOUT.5
GEOUT.6
GEOUT.7
LASTGE
SWAPMESH
FLAGPIN0
FLAGPIN1
FLAGO.0
FLAGO.1
FLAGO.2
FLAGO.3
BGRNTI-0
BGRNTO-3
10C1> GE7_1_OUT<7..0>
9D8<> 7A8<> 10D8<> GEMIC<127..0>
6D1> HALFGIOCLK_GE7A
6A1> GE7CLK1
6B1> 2XGE7CLK
7D4> RAM0_A<7..0>
14D4> PUD110
7D1> GE7STB<3..0>
7D6> GE7MASK<3..0>
7D4> HQ2DMADLY
7D4> GE7STALL
2A1> GFX_RST_A_N
7D4> GE7E_W_N
7D4> GE7UCODE_WE_N
7D4> GE7SWAP
10A8<> 7A8<> HOBUS<31..0>
9B5<> 7D1<> 10A8<> SHRAM_FAST<31..0>
7C8<> 10D5<> 14B6<> GE7FLAG<3..0>
14A6< 14B6< GE7FULL_23_N
9A6>
GE7UC_CAS_GE7_N
14D4> ATPG_DN
14D4> GEDNSEL
14D4> TSTGE_DN
GE7_AD<31..0> 10D1<> 12D1<>
12A4> GE7_GE7WR_N
12A3> GE7_GE7RD_N
12B5> GE7_OE_N
GE7_RDY_N 10C1<> 12B8
GE7_3_OUT<7..0> 14B4<
10B1> GE7_1_FLAGO<3..0>
GE7_3_FLAGO<3..02> 14D4<
10A1>
GE7_1_BGRNTO_N
GE7_3_BGRNTO_N 14C4<
+5 VCC
C529 1.0uF TANT 3216
C528 0.1uF 0603
C530 0.1uF 0603
C509 0.1uF 0603
C513 0.01uF 0603
C519 0.01uF 0603
C521 0.01uF 0603
C526 1000pF 0603
C512 1000pF 0603
C511 1000pF 0603
Silicon Graphics Computer Systems
2GE7 ASIC (CAV. DOWN)
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002 D
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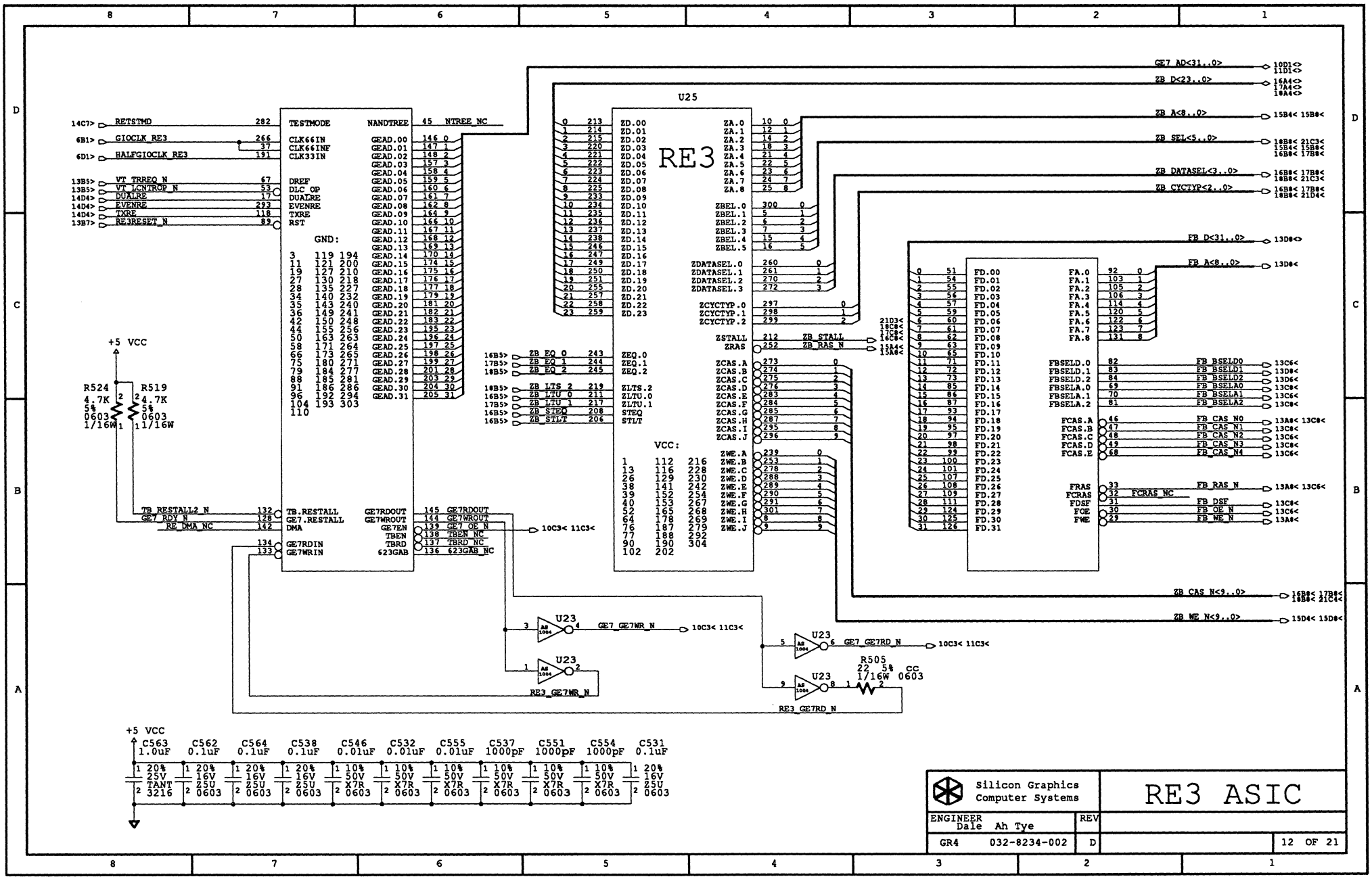
RE3
U25
TESTMODE
NANDTREE
GND:
RETSTMD
GIOCLK_RE3
HALFGIOCLK_RE3
VT_TRREQ_N
VT_LCNTROP_N
DUALRE
EVENRE
TXRE
RE3RESET_N
CLK66IN
CLK66INF
CLK33IN
DREF
DLC_OP
DUALRE
EVENRE
TXRE
RST
GEAD.00
GEAD.01
GEAD.02
GEAD.03
GEAD.04
GEAD.05
GEAD.06
GEAD.07
GEAD.08
GEAD.09
GEAD.10
GEAD.11
GEAD.12
GEAD.13
GEAD.14
GEAD.15
GEAD.16
GEAD.17
GEAD.18
GEAD.19
GEAD.20
GEAD.21
GEAD.22
GEAD.23
GEAD.24
GEAD.25
GEAD.26
GEAD.27
GEAD.28
GEAD.29
GEAD.30
GEAD.31
NTREE_NC
ZD.00
ZD.01
ZD.02
ZD.03
ZD.04
ZD.05
ZD.06
ZD.07
ZD.08
ZD.09
ZD.10
ZD.11
ZD.12
ZD.13
ZD.14
ZD.15
ZD.16
ZD.17
ZD.18
ZD.19
ZD.20
ZD.21
ZD.22
ZD.23
ZA.0
ZA.1
ZA.2
ZA.3
ZA.4
ZA.5
ZA.6
ZA.7
ZA.8
ZBEL.0
ZBEL.1
ZBEL.2
ZBEL.3
ZBEL.4
ZBEL.5
ZDATASEL.0
ZDATASEL.1
ZDATASEL.2
ZDATASEL.3
ZCYCTYP.0
ZCYCTYP.1
ZCYCTYP.2
ZSTALL
ZRAS
ZEQ.0
ZEQ.1
ZEQ.2
ZLTS.2
ZLTU.0
ZLTU.1
STEQ
STLT
ZCAS.A
ZCAS.B
ZCAS.C
ZCAS.D
ZCAS.E
ZCAS.F
ZCAS.G
ZCAS.H
ZCAS.I
ZCAS.J
ZWE.A
ZWE.B
ZWE.C
ZWE.D
ZWE.E
ZWE.F
ZWE.G
ZWE.H
ZWE.I
ZWE.J
VCC:
FD.00
FD.01
FD.02
FD.03
FD.04
FD.05
FD.06
FD.07
FD.08
FD.09
FD.10
FD.11
FD.12
FD.13
FD.14
FD.15
FD.16
FD.17
FD.18
FD.19
FD.20
FD.21
FD.22
FD.23
FD.24
FD.25
FD.26
FD.27
FD.28
FD.29
FD.30
FD.31
FA.0
FA.1
FA.2
FA.3
FA.4
FA.5
FA.6
FA.7
FA.8
FBSELD.0
FBSELD.1
FBSELD.2
FBSELA.0
FBSELA.1
FBSELA.2
FCAS.A
FCAS.B
FCAS.C
FCAS.D
FCAS.E
FRAS
FCRAS
FDSF
FOE
FWE
GE7RDOUT
GE7WROUT
GE7EN
TBEN
TBRD
623GAB
GE7RDIN
GE7WRIN
TB.RESTALL
GE7.RESTALL
DMA
TB_RESTALL2_N
GE7_RDY_N
RE_DMA_NC
GE7_AD<31..0>
ZB_D<23..0>
ZB_A<8..0>
ZB_SEL<5..0>
ZB_DATASEL<3..0>
ZB_CYCTYP<2..0>
FB_D<31..0>
FB_A<8..0>
ZB_CAS_N<9..0>
ZB_WE_N<9..0>
ZB_EQ_0
ZB_EQ_1
ZB_EQ_2
ZB_LTS_2
ZB_LTU_0
ZB_LTU_1
ZB_STEQ
ZB_STLT
ZB_STALL
ZB_RAS_N
FB_BSELD0
FB_BSELD1
FB_BSELD2
FB_BSELA0
FB_BSELA1
FB_BSELA2
FB_CAS_N0
FB_CAS_N1
FB_CAS_N2
FB_CAS_N3
FB_CAS_N4
FB_RAS_N
FCRAS_NC
FB_DSF
FB_OE_N
FB_WE_N
GE7_GE7WR_N
GE7_GE7RD_N
RE3_GE7WR_N
RE3_GE7RD_N
+5 VCC
R524
4.7K 5% 0603 1/16W
R519
4.7K 5% 0603 1/16W
R505
22 5% CC 1/16W 0603
C563 1.0uF 20% 25V TANT 3216
C562 0.1uF 20% 16V Z5U 0603
C564 0.1uF 20% 16V Z5U 0603
C538 0.1uF 20% 16V Z5U 0603
C546 0.01uF 10% 50V X7R 0603
C532 0.01uF 10% 50V X7R 0603
C555 0.01uF 10% 50V X7R 0603
C537 1000pF 10% 50V X7R 0603
C551 1000pF 10% 50V X7R 0603
C554 1000pF 10% 50V X7R 0603
C531 0.1uF 20% 16V Z5U 0603
Silicon Graphics Computer Systems
RE3 ASIC
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
D
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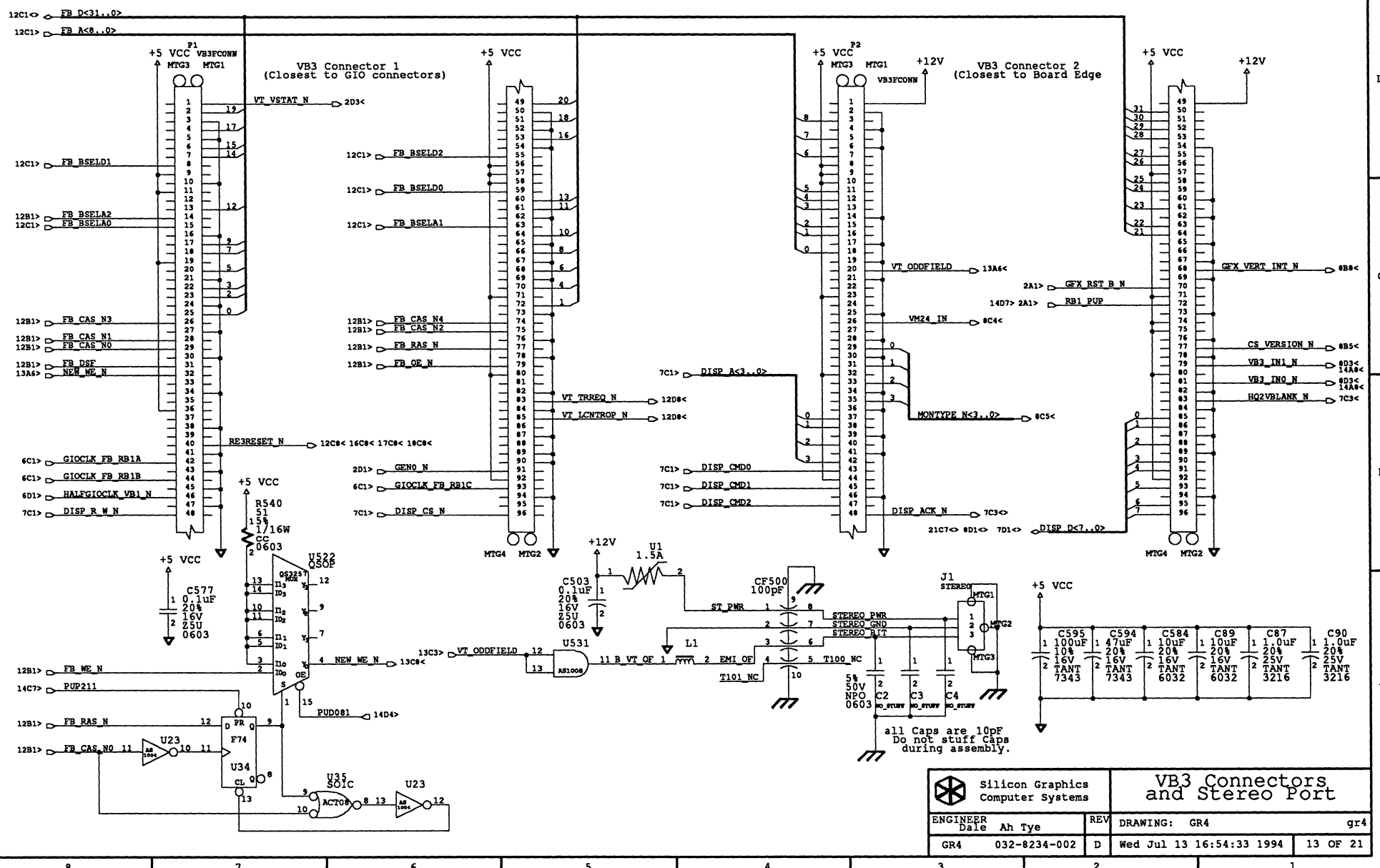
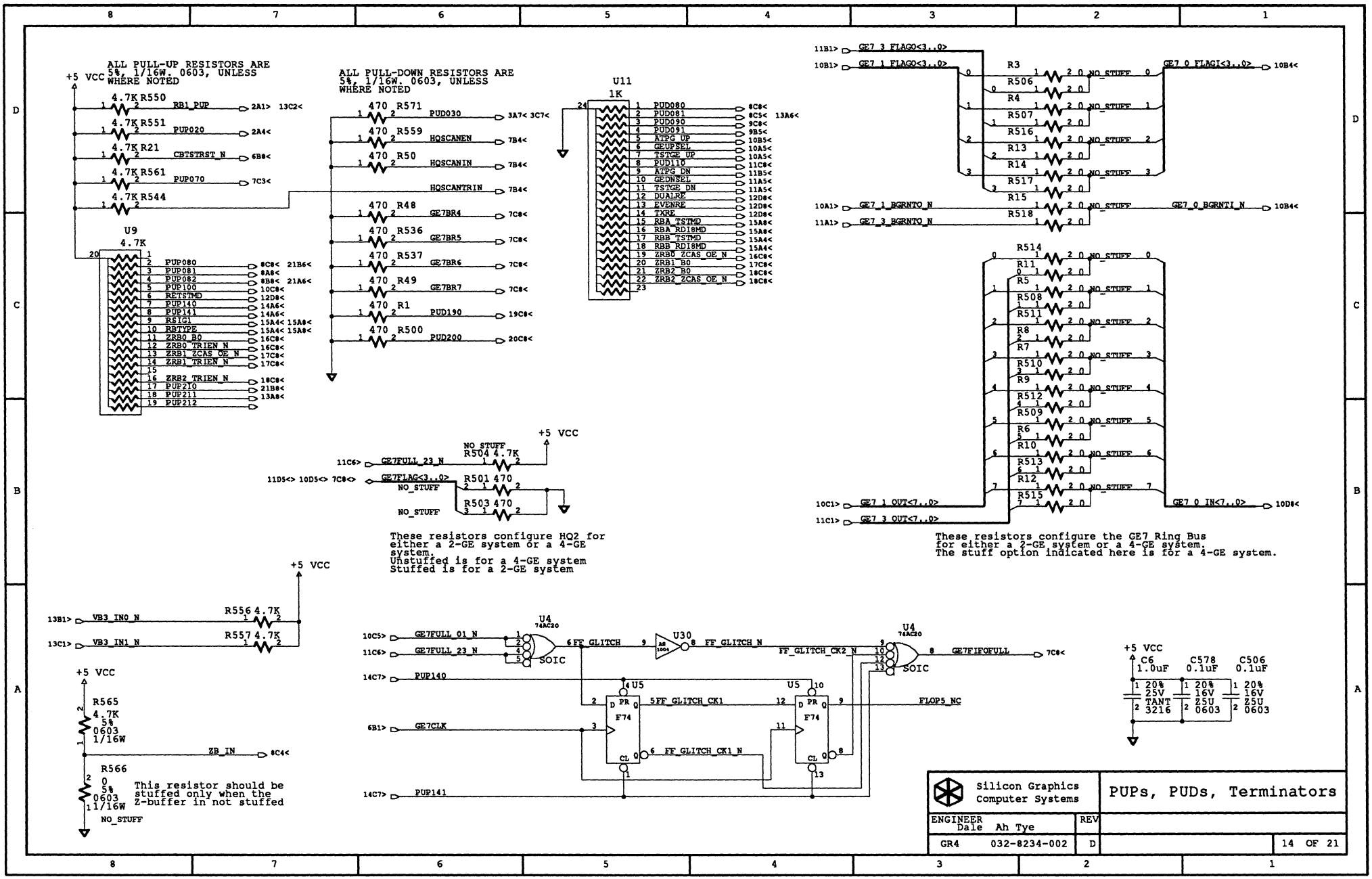


Silicon Graphics Computer Systems		VB3 Connectors and Stereo Port	
ENGINEER Dale Ah Tye	REV	DRAWING: GR4	gr4
GR4 032-8234-002	D	Wed Jul 13 16:54:33 1994	13 OF 21


ALL PULL-UP RESISTORS ARE 5%, 1/16W, 0603, UNLESS WHERE NOTED
+5 VCC
4.7K R550 RB1_PUP 2A1> 13C2<
4.7K R551 PUP020 2A4<
4.7K R21 CBTSTRST_N 6B8<
4.7K R561 PUP070 7C3<
4.7K R544
U9 4.7K
PUP080 8C8< 21B6<
PUP081 8A8<
PUP082 8B8< 21A6<
PUP100 10C8<
RETSTMD 12D8<
PUP140 14A6<
PUP141 14A6<
RSIG1 15A4< 15A8<
RBTYPE 15A4< 15A8<
ZRB0_B0 16C8<
ZRB0_TRIEN_N 16C8<
ZRB1_ZCAS_OE_N 17C8<
ZRB1_TRIEN_N 17C8<
ZRB2_TRIEN_N 18C8<
PUP210 21B8<
PUP211 13A8<
PUP212
ALL PULL-DOWN RESISTORS ARE 5%, 1/16W, 0603, UNLESS WHERE NOTED
470 R571 PUD030 3A7< 3C7<
470 R559 HQSCANEN 7B4<
470 R50 HQSCANIN 7B4<
HQSCANTRIN 7B4<
470 R48 GE7BR4 7C8<
470 R536 GE7BR5 7C8<
470 R537 GE7BR6 7C8<
470 R49 GE7BR7 7C8<
470 R1 PUD190 19C8<
470 R500 PUD200 20C8<
U11 1K
PUD080 8C8<
PUD081 8C5< 13A6<
PUD090 9C8<
PUD091 9B5<
ATPG_UP 10B5<
GEUPSEL 10A5<
TSTGE_UP 10A5<
PUD110 11C8<
ATPG_DN 11B5<
GEDNSEL 11A5<
TSTGE_DN 11A5<
DUALRE 12D8<
EVENRE 12D8<
TXRE 12D8<
RBA_TSTMD 15A8<
RBA_RDI8MD 15A8<
RBB_TSTMD 15A4<
RBB_RDI8MD 15A4<
ZRB0_ZCAS_OE_N 16C8<
ZRB1_B0 17C8<
ZRB2_B0 18C8<
ZRB2_ZCAS_OE_N 18C8<
11B1> GE7_3_FLAGO<3..0>
10B1> GE7_1_FLAGO<3..0>
R3 R506 R4 R507 R516 R13 R14 R517 R15 R518
NO_STUFF
GE7_0_FLAGI<3..0> 10B4<
10A1> GE7_1_BGRNTO_N
11A1> GE7_3_BGRNTO_N
GE7_0_BGRNTI_N 10B4<
R514 R11 R5 R508 R511 R8 R7 R510 R9 R512 R509 R6 R10 R513 R12 R515
10C1> GE7_1_OUT<7..0>
11C1> GE7_3_OUT<7..0>
GE7_0_IN<7..0> 10D8<
These resistors configure the GE7 Ring Bus for either a 2-GE system or a 4-GE system. The stuff option indicated here is for a 4-GE system.
+5 VCC
11C6> GE7FULL_23_N
11D5<> 10D5<> 7C8<> GE7FLAG<3..0>
R504 4.7K
R501 470
R503 470
NO_STUFF
These resistors configure HQ2 for either a 2-GE system or a 4-GE system.
Unstuffed is for a 4-GE system
Stuffed is for a 2-GE system
13B1> VB3_IN0_N
13C1> VB3_IN1_N
R556 4.7K
R557 4.7K
R565 4.7K 5% 0603 1/16W
ZB_IN 8C4<
R566 0 5% 0603 1/16W
This resistor should be stuffed only when the Z-buffer in not stuffed
NO_STUFF
U4 74AC20 SOIC
10C5> GE7FULL_01_N
11C6> GE7FULL_23_N
6FF_GLITCH
U30
FF_GLITCH_N
FF_GLITCH_CK2_N
GE7F1FOFULL 7C8<
14C7> PUP140
U5 F74
5FF_GLITCH_CK1
FLOP5_NC
6B1> GE7CLK
FF_GLITCH_CK1_N
14C7> PUP141
C6 1.0uF 20% 25V TANT 3216
C578 0.1uF 20% 16V Z5U 0603
C506 0.1uF 20% 16V Z5U 0603
Silicon Graphics Computer Systems
PUPs, PUDs, Terminators
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
D
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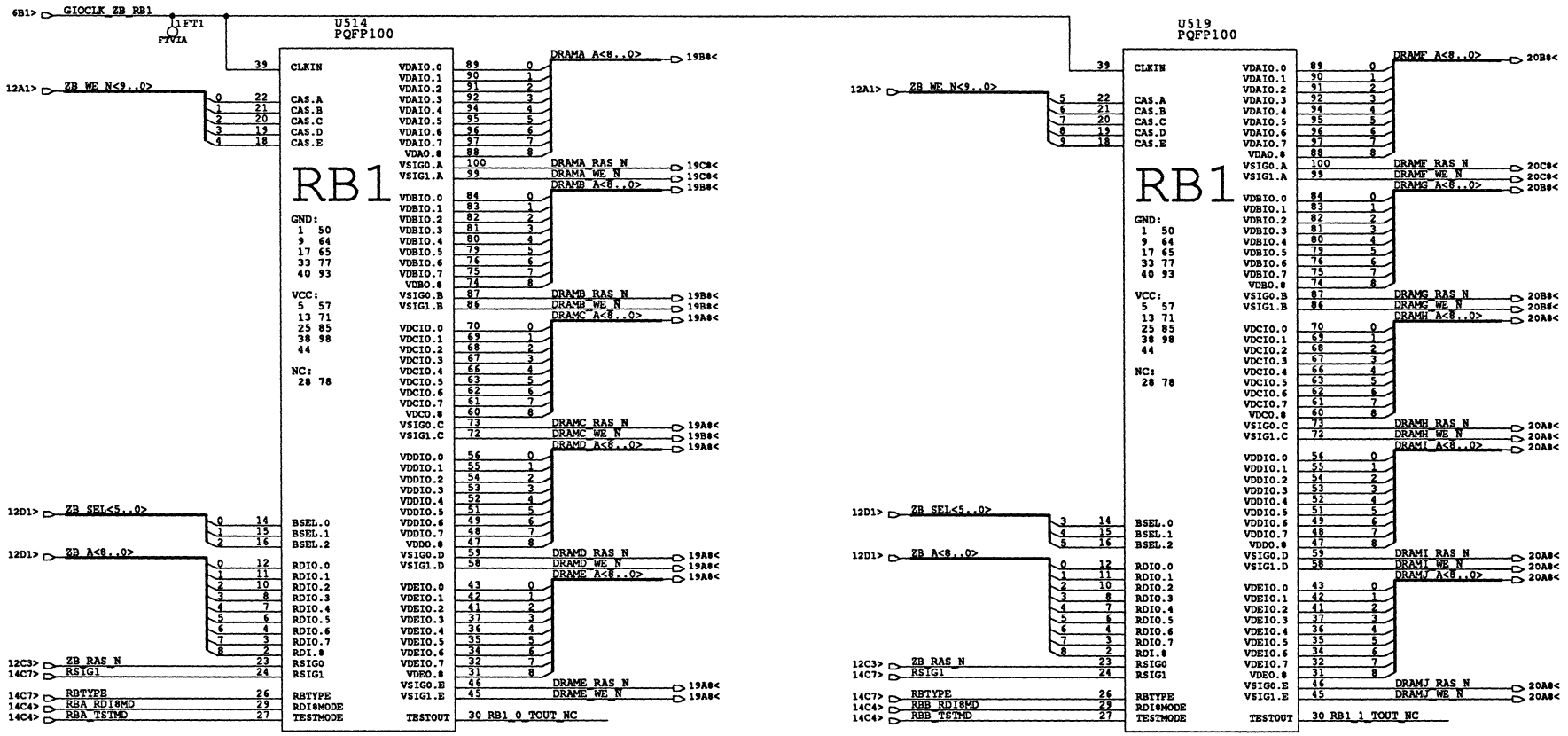
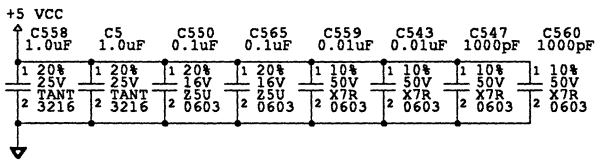
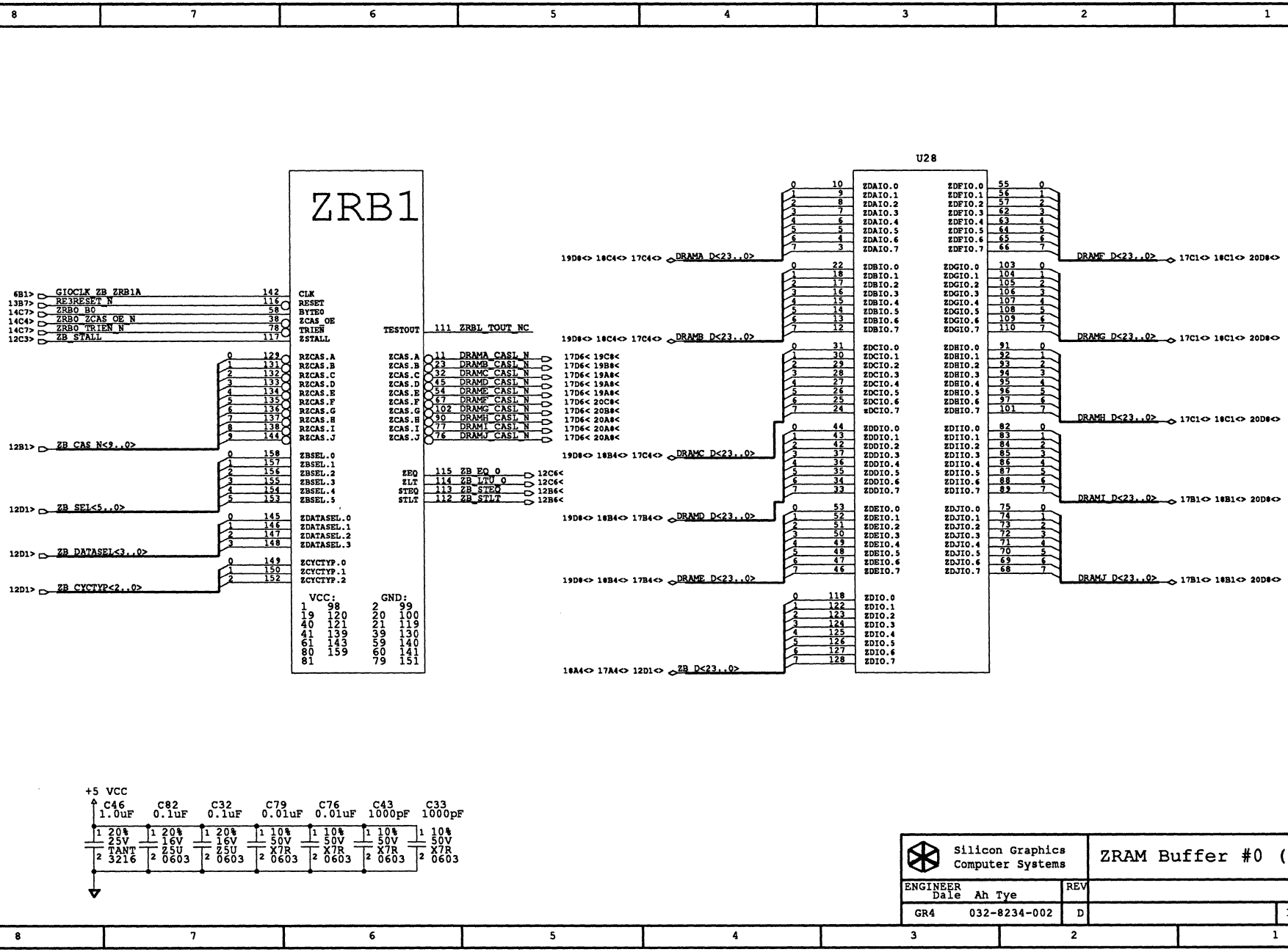
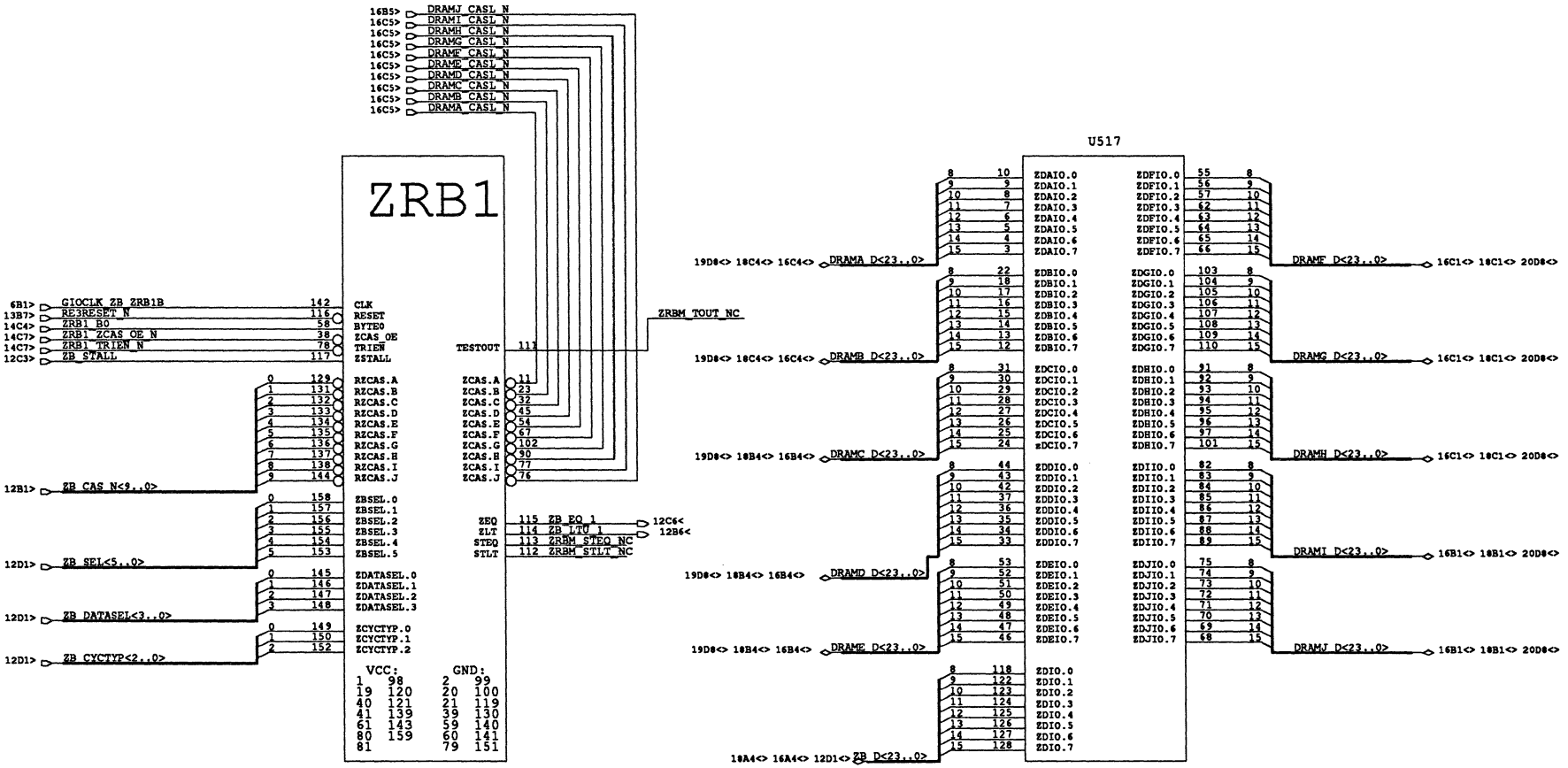




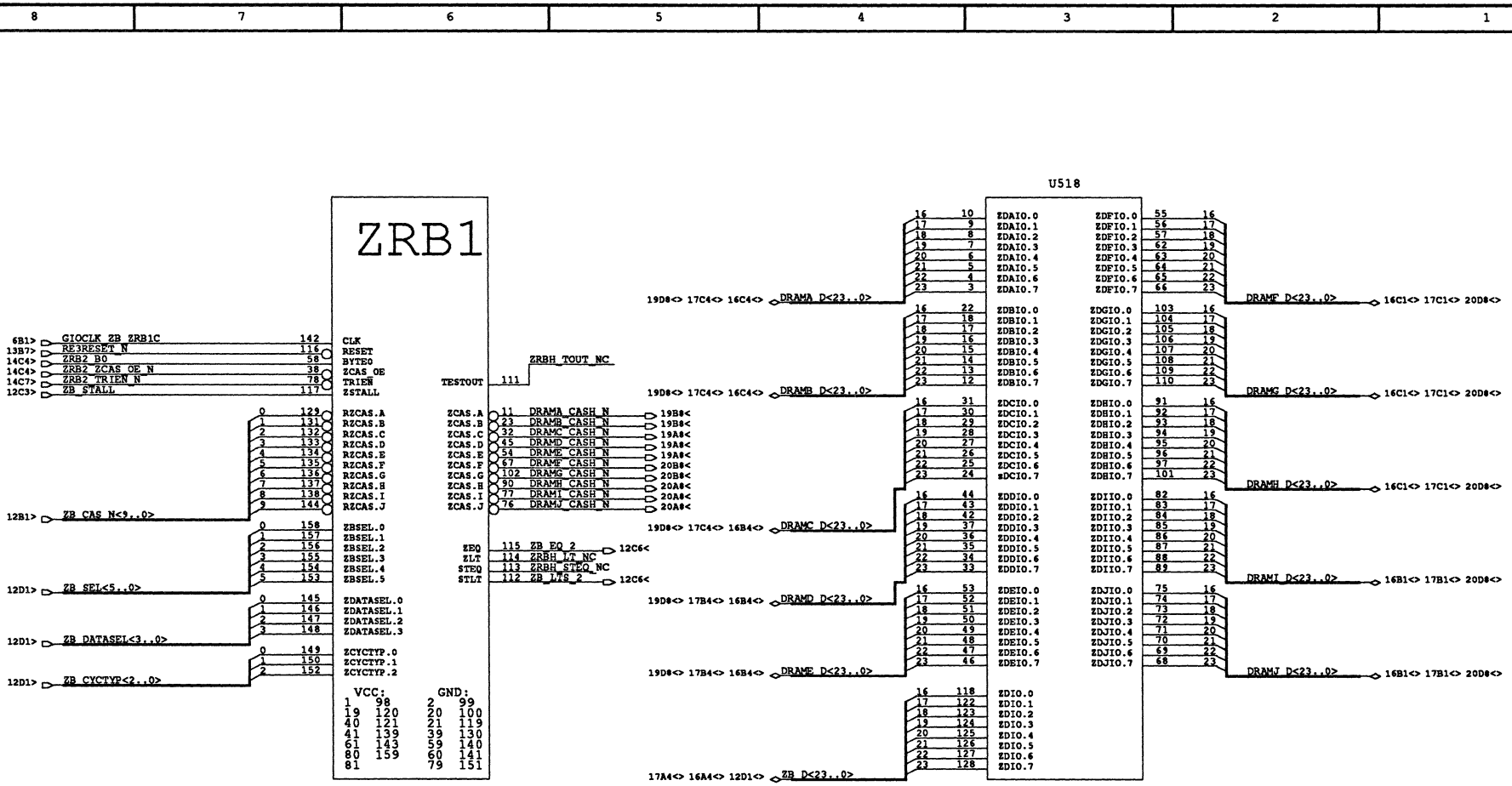
Silicon Graphics Computer Systems		RB1s for Z Buffer Memory	
ENGINEER Dale Ah Tye	REV		
GR4 032-8234-002	D		15 OF 21



Silicon Graphics Computer Systems	ZRAM Buffer #0 (ZRB1)	
ENGINEER Dale Ah Tye	REV	
GR4 032-8234-002	D	16 OF 21



Silicon Graphics Computer Systems	ZRAM Buffer #1 (ZRB1)
ENGINEER Dale Ah Tye	REV
GR4 032-8234-002	D
	17 OF 21


ZRB1
U518
GIOCLK_ZB_ZRB1C
RE3RESET_N
ZRB2_B0
ZRB2_ZCAS_OE_N
ZRB2_TRIEN_N
ZB_STALL
CLK
RESET
BYTE0
ZCAS_OE
TRIEN
ZSTALL
TESTOUT
ZRBH_TOUT_NC
ZB_CAS_N<9..0>
ZB_SEL<5..0>
ZB_DATASEL<3..0>
ZB_CYCTYP<2..0>
RZCAS.A
RZCAS.B
RZCAS.C
RZCAS.D
RZCAS.E
RZCAS.F
RZCAS.G
RZCAS.H
RZCAS.I
RZCAS.J
ZBSEL.0
ZBSEL.1
ZBSEL.2
ZBSEL.3
ZBSEL.4
ZBSEL.5
ZDATASEL.0
ZDATASEL.1
ZDATASEL.2
ZDATASEL.3
ZCYCTYP.0
ZCYCTYP.1
ZCYCTYP.2
VCC:
GND:
ZCAS.A
ZCAS.B
ZCAS.C
ZCAS.D
ZCAS.E
ZCAS.F
ZCAS.G
ZCAS.H
ZCAS.I
ZCAS.J
DRAMA_CASH_N
DRAMB_CASH_N
DRAMC_CASH_N
DRAMD_CASH_N
DRAME_CASH_N
DRAMF_CASH_N
DRAMG_CASH_N
DRAMH_CASH_N
DRAMI_CASH_N
DRAMJ_CASH_N
ZEQ
ZLT
STEQ
STLT
ZB_EQ_2
ZRBH_LT_NC
ZRBH_STEQ_NC
ZB_LTS_2
ZDAIO.0
ZDAIO.1
ZDAIO.2
ZDAIO.3
ZDAIO.4
ZDAIO.5
ZDAIO.6
ZDAIO.7
ZDBIO.0
ZDBIO.1
ZDBIO.2
ZDBIO.3
ZDBIO.4
ZDBIO.5
ZDBIO.6
ZDBIO.7
ZDCIO.0
ZDCIO.1
ZDCIO.2
ZDCIO.3
ZDCIO.4
ZDCIO.5
ZDCIO.6
ZDCIO.7
ZDDIO.0
ZDDIO.1
ZDDIO.2
ZDDIO.3
ZDDIO.4
ZDDIO.5
ZDDIO.6
ZDDIO.7
ZDEIO.0
ZDEIO.1
ZDEIO.2
ZDEIO.3
ZDEIO.4
ZDEIO.5
ZDEIO.6
ZDEIO.7
ZDIO.0
ZDIO.1
ZDIO.2
ZDIO.3
ZDIO.4
ZDIO.5
ZDIO.6
ZDIO.7
ZDFIO.0
ZDFIO.1
ZDFIO.2
ZDFIO.3
ZDFIO.4
ZDFIO.5
ZDFIO.6
ZDFIO.7
ZDGIO.0
ZDGIO.1
ZDGIO.2
ZDGIO.3
ZDGIO.4
ZDGIO.5
ZDGIO.6
ZDGIO.7
ZDHIO.0
ZDHIO.1
ZDHIO.2
ZDHIO.3
ZDHIO.4
ZDHIO.5
ZDHIO.6
ZDHIO.7
ZDIIO.0
ZDIIO.1
ZDIIO.2
ZDIIO.3
ZDIIO.4
ZDIIO.5
ZDIIO.6
ZDIIO.7
ZDJIO.0
ZDJIO.1
ZDJIO.2
ZDJIO.3
ZDJIO.4
ZDJIO.5
ZDJIO.6
ZDJIO.7
DRAMA D<23..0>
DRAMB D<23..0>
DRAMC D<23..0>
DRAMD D<23..0>
DRAME D<23..0>
DRAMF D<23..0>
DRAMG D<23..0>
DRAMH D<23..0>
DRAMI D<23..0>
DRAMJ D<23..0>
ZB D<23..0>
+5 VCC
C542 1.0uF
C571 0.1uF
C34 0.1uF
C568 0.01uF
C566 0.01uF
C539 1000pF
C535 1000pF
Silicon Graphics Computer Systems
ZRAM Buffer #2 (ZRB1)
ENGINEER Dale Ah Tye
REV
GR4 032-8234-002
D
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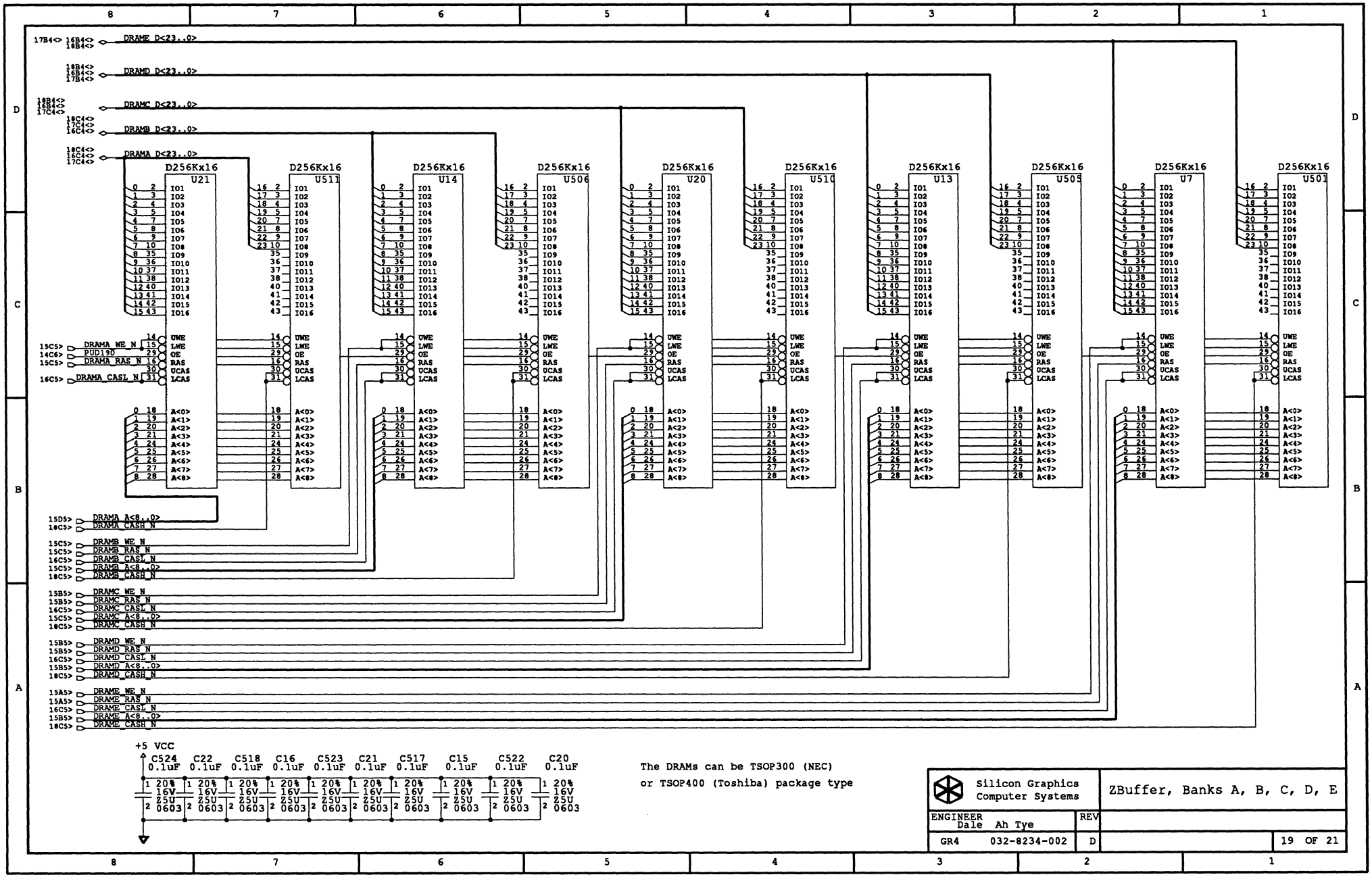
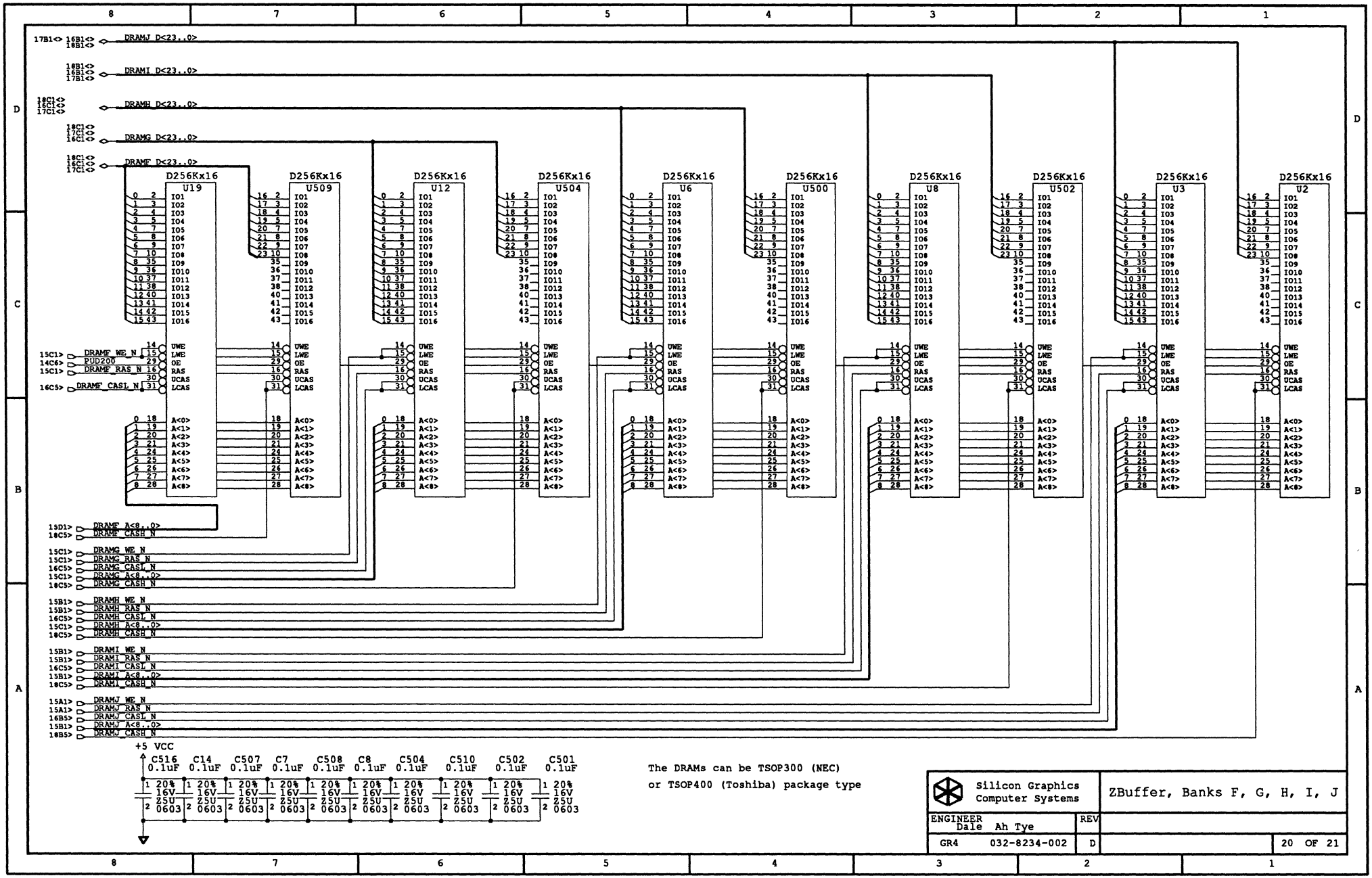


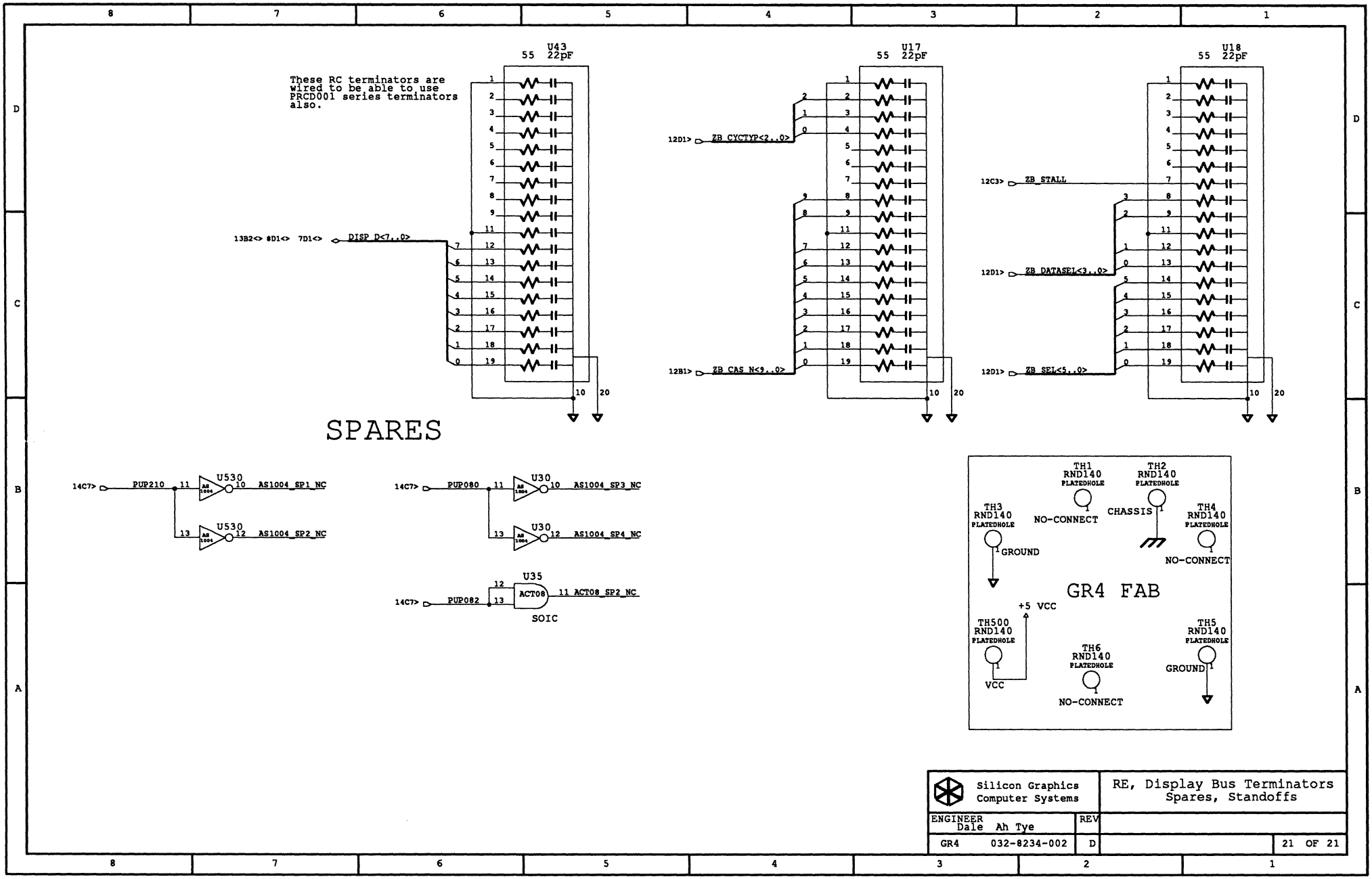
The DRAMs can be TSOP300 (NEC)
or TSOP400 (Toshiba) package type

Silicon Graphics Computer Systems			ZBuffer, Banks A, B, C, D, E
ENGINEER Dale Ah Tye		REV	
GR4	032-8234-002	D	19 OF 21



The DRAMs can be TSOP300 (NEC)
or TSOP400 (Toshiba) package type

Silicon Graphics Computer Systems			ZBuffer, Banks F, G, H, I, J
ENGINEER Dale Ah Tye		REV	
GR4	032-8234-002	D	20 OF 21



Silicon Graphics Computer Systems		RE, Display Bus Terminators Spares, Standoffs
ENGINEER Dale Ah Tye	REV	
GR4 032-8234-002	D	21 OF 21