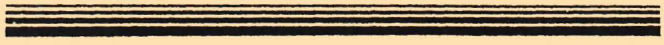
SCCS-85



user's manual

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PREFACE

To use the SCCS-85 to its fullest, especially when hardware reconfiguration is being made, it is strongly recommended that the user obtain a copy of the "8080/8085 User's Manual" from Intel. This manual contains detailed information on all chips used on the SCCS-85 (except standard TTL parts). Also on the recommended reading list is the "8080/8085 Assembly Language Progamming Manual" which will be useful when writing assembly language routines and programs.

1.0 INTRODUCTION

The SCCS-85 is a versatile 8085-based microcomputer system residing on a single 4.5 by 7.0 inch PC board. It may be used by itself as a powerful control computer in a variety of control applications such as peripheral I/O controllers, programmable device controllers, and the like. Or, with the addition of a keyboard, video interface and monitor it may serve as a complete microcomputer for the hobbyist, with capabilities for easy expansion as the need dictates.

By extending the SCCS-85's bus to additional cards, memory capacity can be extended to a full 65K bytes, additional I/O devices may be added as needed, the bus may be buffered to permit additional bus loading, etc.

Flexibility was the prime design goal of the SCCS-85. The card is designed so that for a particular application only those chips required need be installed. For example, in applications which do not require the 4-channel DMA controller, the two chips comprising the DMA GROUP are simply omitted from the board. If, at a later date, it is decided to add the DMA capability one need only cut two traces on the underside of the board and install the chips.

Furthermore, extensive provisions have been made in the PC board to permit configuring the I/O devices in the way which best suits an application. For example, a group of wrap-posts are provided which allow any combination of two interrupts from the SERIAL GROUP and the PIO GROUP to be combined into a single interrupt line to the 8085, thus allowing these devices to operate in various modes of interrupt-driven and/or polled I/O.

While the SCCS-85 has extensive provisions for reconfiguring the components to suit an application the PC board has also been etched so that with no modifications at all, the board is already configured to operate as a small computer communicating via RS-232 with a terminal. With no modifications, the board provides the necessary hardware to implement a real-time clock, programmable signal generator, and the like.

Lastly, the SCCS-85 has been designed with the user's pocketbook in mind. All chips used on the SCCS-85 are easily obtainable and at modest costs. I/O as well as the system bus connectors are inexpensive, easily-obtained A P Products

jumper headers. These are available in either straight or right-angle configurations, and either male or female. This allows connections to be made with ribbon cables, by plugging into other boards, or even wire-wrapping to individual pins. And only those connectors actually needed have to be installed.

FEATURES

The SCCS-85 CPU is divided into seven functional groups: the CPU group, ROM group, RAM group, SERIAL I/O group, PARALLEL I/O group, TIMER group, and DMA group. While some groups, like the CPU, RAM, and ROM group are mandatory and must be present on any SCCS-85, the remaining groups are optional and need only be present on the board if the application requires it.

Following is a description of the features of each group, suggested applications, and user-definable options for that group.

** CPU GROUP. Ths SCCS-85 is based on the Intel 8085 CPU chip. This MPU was chosen because of its extensive provisions for interrupts, MPU support, and ease of interfacing with a very low chip count, plus its widespead software support at present time. The address bus is fully demultiplexed and the control signals have been decoded into individual memory-read, memory-write, I/O-read, I/O-write, and interrupt-acknowledge signals to make expansion easy.

Very flexible interrupt facilities are available. The normal 8080-type interrupt/interrupt-acknowledge protocol can be used by external peripherals which can place the RESTART instruction on the bus. Another, easier to use facility includes three separate RST lines, each of which can directly interrupt the CPU causing the CPU to jump to one of three different locations in memory, with NO other hardware required. One of these lines may be used by the TIMER group to interrupt the CPU at equal time intervals, after programmable delays, etc. Another is available for using the serial and/or parallel interfaces in interrupt mode. The third is left available on the bus for user purposes. A final interrupt line, similar to the RST lines, is the TRAP line, which causes an immediate "panic" jump to a location in memory for such purposes as power-fail sequences, hardware errors, etc.

The 8085 also provides a 1-bit intput and 1-bit output port. Two 8085 instructions allow the bits to read, and set or reset.

The 8085 may run at speeds up to 3 MHz, but if the TIMER group is present a maximum of 2 MHz is recommended, allowing the timer clock to be derived from the CPU clock. Alternativly, the timer clock may be supplied independently, allowing the 8085 to run at 3MHz, so long as sufficiently fast RAM and ROM are used. The maximum allowable memory access time is 1.5 times the CPU clock period. For example, for an 8085 running at 3MHz the CPU clock period is 333 ns, so the memory access time is 500ns. RAMs used in a 3 MHz system, then, must have an access time less that 500ns.

When power is applied to the SCCS-85 the CPU is automatically reset, and begins execution at memory location 0000h. Space is avialable on the PC board for a manual reset pushbutton, plus a signal on the bus may be pulled low to reset the CPU. A RESET line coming FROM the CPU is available for resetting other devices.

** ROM group. The SCCS-85 has room for 2K or 4K of PROM. As etched, the board accepts two 2708 EPROMs, giving 2K of ROM. If more ROM is desired pads and traces on the board are organized so that it may be reconfigured to accept two 2716 EPROMs, giving 4K of ROM.

Memory locations 0000h through 0FFFh are reserved for the on-board ROM. This constitutes the first 4K of memory. At least one ROM is required for operation of the SCCS-85, located at 0000 where execution begins when the system is powered-up.

If 2708 ROMs are used, a +12 and -5 volt supply will be needed. If the serial interface group is used along with the RS-232 drivers +12 and -12 volts will be required for them, so a 5V zener diode and resistor are provided on the board to derive the -5V from the -12V supply. If the new +5V-only 2716s are used instead, no supplies will be required for the ROMs except the normal +5V supply.

** RAM group. Up to 4K of RAM may be intstalled on the SCCS-85, in increments of 1K bytes. Each 1K block of RAM consists of a pair of 2114 1K x 4 static rams; one for the upper and one for the lower four bits of each byte. RAM addresses range from 1000h to 1FFFh, the second 4K block of memory.

Other memory-related points: ROM and RAM together occupy the first 8K of memory. The memory is fully decoded, meaning that this 8K block does not "appear" at any other memory locations within the 65K byte address space. This makes it possible to expand the SCCS-85 memory on additional boards. To make external memory decoding easy the SCCS-85 generates a MEMSEL signal on the expansion bus which indicates if a memory location currently being read or written is within the first 8K block of memory.

** TIMER group. In many control applications events occuring in real time must be monitored and/or controlled. A simple real-time clock required that the CPU be interrupted at a constant rate. Other applications may require that the time interval between two events be measured, pulses of a particular length or signals of a particular frequency be generated. The TIMER group, using an Intel 8253 peripheral timer chip, provides a flexible means of performing these and other tasks.

The 8253 contains three separate, identical 16-bit counters. Each counter may be programmed by software to operate in one of six different modes. Mode 0 allows the CPU to command the timer to interrupt the CPU after a programmed delay. Mode 1 is a programmable one-shot for generating pulses of programmable length. Mode 2 allows pulses to be generated at a programmable rate, while mode 3 generates a square wave of programmable frequency. Mode 4 produces a single pulse after a programmable delay. Mode 5 allows a hardware trigger input to initiate a programmable delay after which a single pulse is produced.

Each counter may be read at any time to ascertain the contents of the counter. Thus, if the timer's clock input is supplied externally the result is a hardware event counter which the software can read and modify at any time. Furthermore, even if the timer's clock inputs are supplied on board, an individual enable input for each is available to allow external hardware to enable counting.

As configured, one timer's output is connected to the RST7.5 input of the 8085. Thus, the output of the timer is used to interrupt the CPU at a programmable rate, after a programmable delay, etc. Another timer's output serves as the baud rate generator for the serial interface group, thus allowing a fully-programmable baud rate for serial I/O. The third timer's output is available for external use at connector J3.

If other configurations are desired jumpers in P1 may be changed to allow each timer's clock and enable input and each timer's output to be connected as desired.

** PIO group. An Intel 8255 parallel I/O interface chip provides 24 lines of parallel I/O for user applications. The chip is programmable in several different modes including 24 lines of basic input/output, one or two strobed 8-bit I/O ports with handshaking and interrupt control lines, strobed bi-directional 8-bit bus with 5 control lines and interrupts, or combinations of the above. The SCCS-85 allows the PIO group to be handled under programmed control, interrupt control, or a combination of the two.

All 24 I/O lines plus GND and +5V are available at connector J2.

** SERIAL I/O group. The Intel 8251 USART chip provides a programmable choice of synchronous or asynchronous I/O. Synchronous serial I/O is useful for such applications as using the SCCS-85 as an intelligent tape controller where data is recorded as a combination of both clock and data. The 8251 can be commanded to search for the sync byte/s which precede the data, as in IBM's bi-sync format.

A more common application is using the 8251 as a serial I/O port connected to a terminal or another computer. For these applications RS-232 drivers and receivers are provided on the SCCS-85 for the transmit and receive data lines, plus the modem-control lines $\overline{CTS}$, $\overline{RTS}$, $\overline{DTR}$, and $\overline{DSR}$. As configured, the modem control inputs $\overline{DSR}$ and $\overline{CTS}$ inputs are disabled, as most terminals do not support them. They may be easily enabled for use on modems by simply cutting two option traces on the board.

Using the timer group as the baud rate generator, baud rates from less than one bit per second to 9600 may be programed. If a 3.5795 MHz crystal (color-burst) is used on the SCCS-85 baud rates of 19,200 and 38,400 are also available.

Since the RS-232 lines usually use a standard 25-pin D (delta) connector, special provisions have been made on the SCCS-85 PC board for mounting one of these connectors very easily. The most readily available 25-pin D connectors are the type with the solder-cup pins. By apparent coincidence the two rows of pins on these connectors are 1/16th inch apart, just the thickness of the SCCS-85 PC board. Taking advantage of this fact, wide PC traces extend to the extreme edge of the board in a pattern that exactly aligns with the pins on a 25-pin D connector. Thus, a connector may

be slipped onto the edge of the PC board and its pins soldered directly to the PC traces, thereby wiring the connector with the standard pinout and rigidly mounting it.

If the D connector must be mounted external to the PC board, connector J6a is provided. Since D connectors are available which crimp directly to a 25-pin ribbon cable which in turn crimps to a standard female ribbon cable connector, the pinout of J6a is such that the result is a correctly wired D connector.

** DMA group. Some applications require that blocks of data be rapidly transferred directly from memory to a peripheral and vice-versa. Examples include disks and CRT controller chips such as the Intel 8275. For these applications the DMA group with its 8257 provides four separate channels of DMA (direct memory access) for supporting up to four DMA peripherals. Having the DMA controller on the SCCS-85 board makes it as easy to add a DMA peripheral device to the system as a non-DMA peripheral.

All DMA request and grant lines, as well as the terminal count line (indicating when a DMA transfer is complete), are available at connector J5.

OTHER FEATURES:

** The PC board is designed to be mounted in one of two methods. As supplied, the SCCS-85 board is 4.5 x 7.0 inches. Four mounting holes are provided near the corners for mounting the board, adding rubber feet, or mounting a protective plexiglas cover above and/or below the board for protection. In addition, four large pads are provided for connecting a power supply cable directly to the board.

In applications where the system is to be expanded with a mother board, 1/4-inch is sheared from each end of the board. Now, a right-angle AP connector is installed in the bus connector location and the board can be perpendicularly-plugged into a mating AP female connector on a mother board, which now supplies the power to the board through the bus.

** Consideration has been given to making the board as easy to assemble as possible. The PC board is rather dense, yet nearly all conductors-between-IC-pins are on the top side of the board to minimize the possibility of solder bridges. Pin 1 of each IC is identified on the top and bottom sides of the board, and all holes are plated-through. Both sides of the board have a solder mask, and the top is silk-screened with a component placement "road-map".

** For making more extensive modifications to the SCCS-85 a spare 16-pin IC pattern is provided. This allows an additional IC to be mounted on the board and used for any desired purpose.

PARTS LIST

CPU GROUP & MISC. (mandatory)

U1	8085 CPU	
U2	74LS373	8-bit tri-state latch
U3	74LS257	demultiplexor
U4,U19	74LS138	decoder
U17	74LS54	quad AOI gate
U18	74LS02	quad nor gate
R1	1K	resistor
R2	75 ohm 1	watt (see ROM GROUP assembly directions)
R3	1K	resistor
C1,C2	20pF	ceramic disk capacitor
C3,C4	100uF	tantalum capacitor
C5-C8	1uF	tantalum capacitor
D1	1N4733	5V zener diode, 1 watt
D2	1N4001	diode
X1		crystal 3.57 (color burst) or 4 MHz (see text)
SW1	SPST N.O.	pushbutton switch (optional) reset switch
J1		50-pin connector J1 (see text)

ROM GROUP (mandatory)

U5,U6 2708 (or 2716 if board altered)
NOTE: U5 is optional

RAM GROUP (1K mandatory, other 3K optional)

U7-U14 2114,2114L, etc. 1K x 4 static ram, 450ns or less
- 300ns 2114L chips highly-recommended
U10,U14 - 1st 1K of RAM
U9, U13 - 2nd 1K of RAM
U8, U12 - 3rd 1K of RAM
U7, U11 - 4th 1K of RAM

TIMER GROUP (optional)

U20 8253 Intel 3-channel timer chip
J3 or J4 10-pin connector J3 or 40-pin connector J4

PIO GROUP (optional)

U21 8255 Intel programmable peripheral interface
J2 or J4 26-pin connector for J2 or 40-pin connector
for J4

POWER SUPPLY

Board requires +5V regulated plus or minus 5%; if 3-voltage EPROMS or RS-232 options are used, also requires plus and minus 12V at 150 ma. regulated to 10%. Five-volt supply current is typically 1.25 A for fully-populated SCCS-85.

SERIAL I/O GROUP (optional)

U22	8251	Intel USART
U23	1488	quad RS-232 line driver
U24	1489	quad RS-232 line receiver
J6a or J6b		26-pin connector J6a or 25-pin delta connector for J6b

DMA GROUP (optional)

U16	8257	Intel 4-channel DMA controller
U15	74LS373	8-bit tri-state latch
J5		10-pin connector J5

NOTE: Because of the high component density of the SCCS-85 PC board successful assembly requires some degree of expertise in the soldering of many very small connections. A low-wattage pencil-type soldering iron and fine rosin-core solder is a must! If you feel that your expertise or equipment are not up to the task and cannot enlist the help of a friend, please do us both a favor and return the board for a refund.

PRELIMINARY COMMENTS ON ASSEMBLY

It is advised when assembling and bringing up an SCCS-85 system for the first time that the board be assembled in the minimum configuration with no hardware reconfigurations made. This means installing the CPU group, one 2708 with the SCCS-85 Monitor, 1K bytes of RAM, the Timer Group, and Serial Group with RS-232 interface. This will simplify debugging the system should it become necessary.

Note that by simply installing the above components and making no other changes the SCCS-85 can be connected to a terminal and be operated with its operating system.

Before beginning assembly it is a good idea to inspect the board for any flaws in manufacturing. They are much easier to find now than after the board is assembled, and IF NO SOLDERING HAS BEEN DONE ON THE BOARD a defective board may be returned for replacement. Look for shorted or broken traces by holding the board up to a bright light.

It is generally recommended that sockets be used for all ICs on the board to facilitate replacememt should it ever become necessary. However, some applications requiring very high tolerance to vibration or corrosive and/or dirty environments may be best served by first testing and burning-in chips, then soldering them directly to the board. In all cases sockets will probably be used for the proms, and all sockets should be of a high quality. A recommended type (sold by James Electronics) have pins which contact the FLAT SIDE of the IC pins over a broad surface area, and plugging & unplugging the IC seems to result in less damage to the IC socket than the TI low-profile sockets which contact the ragged EDGES of the IC pins. Gold-plated IC sockets are probably a good idea in hostile environments though not absolutely necessary in most other applications.

When installing IC sockets, be sure to note that the pin-1 designation on the socket (most have them) is oriented properly on the PC board.

In other critical applications where the board may be subject to repeated flexing (such as plugging into and out of a mother board) a further precaution is sometimes taken to insure the integrity of through-plated holes. After all components have been soldered in place (IC sockets, etc.) all remaining feed-through holes are filled with a small amount of solder. This can be done from the bottom side of the board, although a bit of practice is recommended to judge how much solder to put in each hole where you can't see the other side. In general, filling the feed-throughs is not needed, although it doesn't take very long to do and may enhance one's peace of mind.

It is probably best that sockets not be installed where options are being omitted (e.g. U15 and U16 when the DMA option is not installed). If the option is later installed a new socket installed then would be preferable to one which has been accumulating dirt and corrosion for a period of time.

After the board has been assembled but before the ICs are installed, you may want to de-flux the bottom side of the board. This is probably only a cosmetic improvement and is not recommended unless ALL feed-through holes have been filled. Even then, extreme caution must be exercised to prevent the defluxing solution from getting into the IC sockets on the top side, a virtual disaster since when it evaporates it will leave a small film of flux on the pins.

The remainder of the assembly is categorized into functional groups.

CPU GROUP

The CPU group is mandatory.

STEP 1:

Install:

☐ C3,C4	100uF tantalum capacitor. OBSERVE POLARITY!
☐ R1,R3	1K ohm, 1/4 watt resistor
☐ D2	1N4001 diode or equiv. OBSERVE POLARITY
☐ SW1	momentary contact N.O. pushbutton switch for RESET

STEP 2:

It is recommended that the 8085 clock be crystal controlled. It is mandatory that a crystal be used IF:

1. The 8253 timer chip (U20) is installed and requires that it's input clock (which comes from the CPU) be accurate.
2. The 8251 USART chip (U22) is installed and its clock is derived from the 8253 timer chip (standard) or derived directly from the CPU clk signal CLK (see option under SERIAL I/O GROUP).

The 8085 itself may be run at speeds up to 3MHz (using a 6MHz crystal) but care must be taken that at speeds higher than 2MHz the other components on the board will also be able to run that fast. Standard Intel parts will meet specs up to 3MHz with 300ns RAMs and EPROMs, but one may have little information on parts from second-source manufacturers, so it may prove less of a problem to limit yourself to 2MHz. Furthermore, while the 8253 timer chip can handle bus accesses at 3MHz its clock input (which comes from the CPU clock on the SCCS-85) is limited to 2MHz, so running the CPU faster than that would require that the timer chip be supplied with its own clock.

It is therefore recommended that the CPU be run at 2MHz or slower.

To provide a crystal controlled clock, install:

☐ X1	3.5795 (color burst) or 4 MHz crystal
☐ C1,C2	20pF ceramic capacitors

NOTE: On the prototype it was found that with some 8085 chips the crystal clock would not consistently power-up correctly at the proper frequency. It appears this problem can be eliminated by omitting C1.

If maintaining a precise CPU clock frequency is not required, and substantial drift of frequency is not objectionable, the expense of the crystal may be eliminated by installing

- ☐ install 10K resistor in place of X1
- ☐ install 20pF capacitor in C1
- ☐ omit C2

This information is from Intel literature and has not been tested as yet. The above values will cause the 8085 to run at approx. 3 MHz; somewhat faster that the 2 MHz rate obtained with a 4 MHz crystal. Note that using this technique of driving the 8085 clock will required that any serial communications chips have their own crystal-controlled clock, hence it is felt that this option has little to recommend it.

STEP 3:

Install:

- ☐ 40-pin IC socket for U1
- ☐ 20-pin IC socket for U2
- ☐ 16-pin sockets for U3, U19 respectively
- ☐ 14-pin sockets for U17, U18 respectively

--->> NOTE: DO NOT INSTALL ICs IN SOCKETS AT THIS TIME <<---

Install:

☐ C5, C6, C7, C8	1uF 35V tantalum capacitors. Do not substitute non-tantalum capacitors! OBSERVE POLARITY!
☐ P3	6-pin double-row header (optional - see section on INTERRUPTS under HARDWARE ENGINEERING)

This completes assembly of the CPU group.

ROM GROUP

One 2708 or 2716 EPROM is required (U6). The second (U5) is optional. BOTH ROMs must be either 2708s or 2716s; no mixing possible.

As etched, the SCCS-85 board will accept one or two 2708 EPROMs. Alternatively, one of two options may be chosen: one or two 5V only (Intel) 2716 EPROMs; or one or two three-voltage 2716 EPROMs.

2708 EPROM installation

To utilize 2708 EPROMs, for which the board has been etched, do the following:

STEP 1:

Install:

- ☐ 24-pin IC socket for U6 (mandatory)
- ☐ 24-pin IC socket for U5 (optional - install if two proms will be used)

☐ 16-pin IC socket for U4

--->> DO NOT INSTALL ICS IN SOCKETS AT THIS TIME <<---

NOTE: It is recommended that high-reliability sockets be used for U6 and U5 since they will be inserted and removed often. Better still would be zero insertion force sockets.

Step 2:

Install:

☐ R2 75 ohm 1 watt resistor (see note below)
☐ D1 5.1 volt 1 watt zener diode (1N4733)

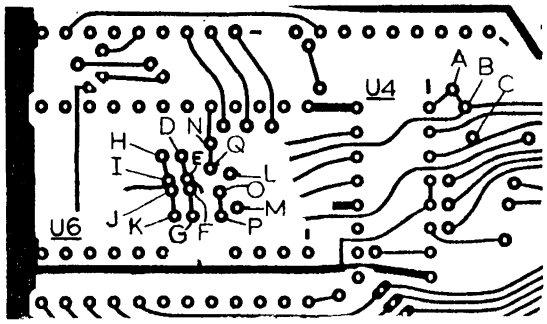
NOTE: If you will never use more than one EPROM you may substitute a 120 ohm 1/2 watt resistor for R2. Alternatively, if you can guarantee that the total current draw from both EPROMs on the -5V supply is 60 ma or less then you may substitute a 100 ohm 1/2 watt resistor for R2.

This completes assembly of the 2708 ROM GROUP.

Three-voltage 2716 EPROM installation

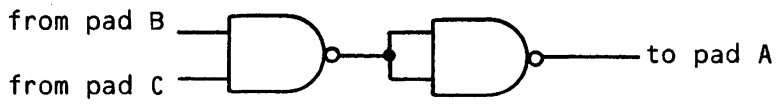
To utilize 2716 EPROMs which require +5, -5, and +12V supplies (e.g. TMS2716, Motorola 2716, etc.) perform the following modifications and assembly. (Refer to dwng. no. 2 of schematics.)

Step 1 On the bottom side of the board find the area of the PC pattern near U4 and U6 shown at right. In this figure, three pads near pin 1 of U4 have been labelled A, B, and C. Cut the trace between pads A and B.



Step 2 Install a 74LS00 IC in the SPARE IC pattern on the board. Be sure to connect +5V and GND to the chip using the conveniently located traces on the bottom side of the board.

Step 3 Using short lengths of wire-wrap wire use two of the gates in the 74LS00 chip to add the following circuit to the board:



Step 4 On the bottom side of the PC board find the area under U6 shown above. In the figure above pads have been labelled D through Q. Cut the trace between pads O and P. Also cut the trace between pads N and Q. Jumper pads N, L, and P together.

Step 5 Cut the trace between pads H and I. Also cut the trace between pads J and K. Jumper pad H to Q. Also jumper pad K to M.

Step 6 Install IC sockets for U4, U5, and U6 exactly as in Step 1 under "2708 EPROM installation" above. DO NOT INSTALL IC CHIPS YET.

Step 7 Install D1 and R2 exactly as in Step 2 under "2708 EPROM installation" above.

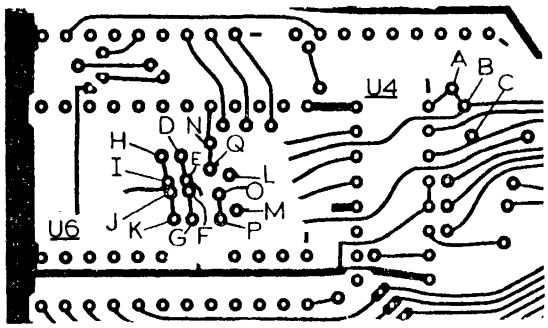
This completes the assembly of the three-voltage 2716 EPROM option.

Single-voltage 2716 EPROM installation

To utilize single-voltage (5V-only) 2716 EPROMs such as the Intel 2716 perform the following modifications and assembly:

Step 1 Perform steps 1 through 3 under "Three-voltage 2716 EPROM installation" above.

Step 2 The figure at right shows the PC board area under IC U6. In the figure pads have been labelled D through Q. Cut the trace between pads D and E. Also cut the trace between pads F and G. Jumper pads D, G, and L together.

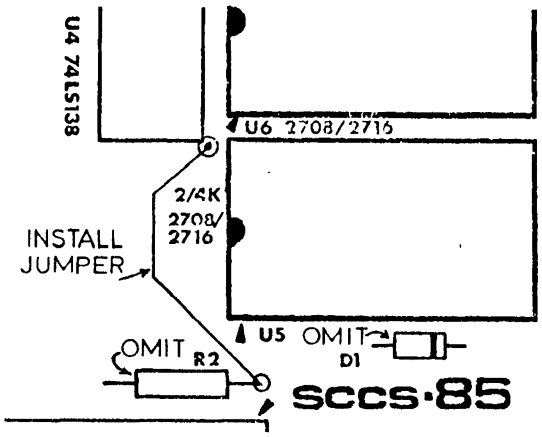


Step 3 Cut the trace between pads O and P. Jumper pads P and M together.

Step 4 Install IC sockets for ICs U4, U5, and U6 exactly as in step 1 under "2708 EPROM installation" above. DO NOT INSTALL CHIPS YET.

Step 5 DO NOT install R2 or D1. Instead, on the top side of the PC board install a jumper from the pad for R2 which is closest to pin 1 of J1, to the pad circled in white near pin 9 of IC U4. See figure at right.

This completes installation of the single-voltage EPROM option.



RAM GROUP

The SCCS-85 board can support up to 4K bytes of on-board RAM. The RAM is made up of 2114 static RAMs which are organized as 1K by 4 bits wide, thus allowing RAM to be expanded in increments of 1K bytes.

For an SCCS-85 running at 2 MHz (with 4 MHz crystal) RAMs with 450ns access times are satisfactory. For faster CPU clock rates, e.g. 3MHz, 300ns RAMs will be needed, and are recommended for good reliability margins. In all cases low-power RAMs are not absolutely necessary, but are highly recommended, as they not only reduce power consumption of the board, but also generate less noise.

RAM GROUP INSTALLATION:

For 1K bytes of RAM, install

- ☐ 18-pin IC socket for U10
- ☐ 18-pin IC socket for U14

--->> NOTE: DO NOT INSTALL ICs IN SOCKETS AT THIS TIME <<---

For 2K bytes of RAM, also install

- ☐ 18-pin IC socket for U9
- ☐ 18-pin IC socket for U13

For 3K bytes of RAM, also install

- ☐ 18-pin IC socket for U8
- ☐ 18-pin IC socket for U12

For 4K bytes of RAM, also install

- ☐ 18-pin IC socket for U7
- ☐ 18-pin IC socket for U11

This completes assembly of the RAM group.

TIMER GROUP

The timer group is optional.

As wired the 8253 timer receives its clock signal from the CPU clock. Since the maximum clock frequency for the 8253 is 2MHz using the 8253 will require that the CPU clock not be faster than 2MHz. If it is then the timer group will have to be slightly reconfigured to allow input of a separate clock signal. For details on this see the section on Hardware Engineering.

Timer Group Installation

Install:

- ☐ 24-pin IC socket for U20

If extensive reconfiguration is anticipated (see Hardware Engineering) install:

- ☐ 16-pin double-row header in P1

If connections to the timer group must be made from off-board, install:

- ☐ 10-pin double-row header in J3 or, alternatively,
  40-pin double-row header in J4 (see section on Connectors)

This completes assembly of the timer group. See Hardware Engineering section for suggestions on reconfiguring timer group.

PARALLEL I/O GROUP

The parallel I/O group is optional.

To add the parallel I/O group install:

- ☐ 40-pin IC socket for U21

--->> WARNING <<---

When installing the socket for U21, the PIO chip, and when installing the chip itself, note that pin 1 of this chip will be oriented in the opposite direction from nearly all other chips. Plugging the PIO chip in backwards would likely destroy it!

Install:

- ☐ 26-pin double-row header in J2 or, alternatively, 40-pin double-row header in J4 (see section on Connectors)

This completes assembly of the Parallel I/O Group.

SERIAL I/O GROUP

This group is optional.

The serial I/O group consists of the 8251 serial communications IC, and optional RS-232 driver and receiver chips.

As configured, the 8251 USART receives its baud rate clock from the timer group. This allows the baud rates to be fully software-controllable, as well as minimizing chip count. Thus, as configured, installing the serial I/O group will necessitate that the timer group be present. If desired, however, the 8251 USART may be supplied separately. See Hardware Engineering.

The 8251 USART may also operate in a synchronous rather than asynchronous mode. This would be used, for example, if the SCCS-85 were a dedicated digital mag. tape drive controller. The serial data to and from the USART would be interfaced to the tape head, requiring different driver chips than the 1488/1489 duo used here. Most likely then, U23 and U24 would be omitted and connections made directly to appropriate pads. Since the vast majority of users will use the serial port for normal RS-232 communications with terminals and the like, a detailed discussion of other configurations is beyond the scope of this manual.

To add the serial I/O group install:

- ☐ 28-pin socket for U22
- ☐ 14-pin sockets for U23, U24 (if being used)

If the RS-232 signals will be taken off-board through a ribbon cable, install:

- ☐ 26-pin double-row header for J6a

If the RS-232 cable is to plug directly onto the PC board, install:

- ☐ 25-pin female Delta, or "D" connector. (See mounting instructions in section on Connectors.)

This completes assembly of the Serial I/O Group.

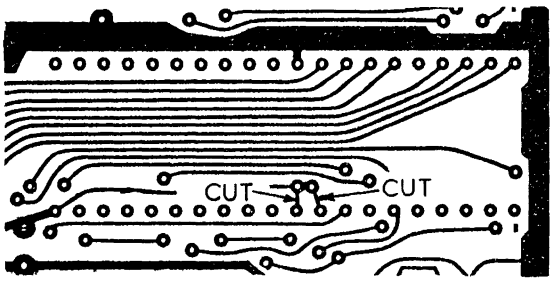
DMA GROUP

The DMA group is optional.

The on-board DMA group, when installed, allows external I/O peripherals to be as easily designed for DMA operation as the more common program-controlled technique.

To add the DMA group, perform the following modifications and assembly:

Step 1 On the bottom side of the PC board find the area under U16 shown at right. Extending from pins 9 and 10 of U16 are two short traces connecting both to another pair of connected pads. Cut these two short traces as shown to enable the DMA group.



NOTE: If the DMA option is later removed (chips U15 and U16 removed) these traces MUST be re-installed or the SCCS-85 will not operate.

Step 2

Install:

- ☐ 40-pin IC socket for U16
- ☐ 20-pin IC socket for U15

DO NOT INSTALL CHIPS YET

WARNING: Some 8085 chips with early date codes have a bug in them which prevents correct DMA operation. The symptoms are that a DMA cycle may affect the flags in the 8085 flag register. The DMA transfer itself operates correctly, but the program being executed at the time will have unpredictable results.

This completes assembly of the DMA Group.

FINAL ASSEMBLY

The assembly of the SCCS-85 is now nearly finished.

If interrupts from either the 8251 USART or the 8255 parallel I/O chip are to be used, install:

- [] 12-pin double-row header in P2

For directions on configuring P2 for interrupts see section on Interrupts in Hardware Engineering.

If the SCCS-85 bus is to be extended to other cards, install:

- ☐ 50-pin double-row header in J1

For suggestions on different connector options, see section on Connectors.

If the SCCS-85 will be receiving its power through the provided pads near the lower edge of the board, install:

- ☐ 4-conductor power cable for +5, +12, -12, and GND. Connect to indicated pads.

Before installing the ICs apply power to the board. With a VOM meter check for the following voltages:

- ☐ 0V at pin 20 of U1
- ☐ 5V at pin 40 of U1

If 2708 or 3-voltage 2716 EPROMS are being used, check for

- ☐ -5V at pin 21 of U6
- ☐ +12V at pin 19 of U6

If 5V-only EPROMs are being used, check for

- ☐ +5V at pin 21 of U6

If the RS-232 driver is being used, check for

- ☐ +12V at pin 14 of U23
- ☐ -12V at pin 1 of U23

IF THE ABOVE VOLTAGES ARE NOT ALL CORRECT DO NOT PROCEED UNTIL THE SOURCE OF THE PROBLEM IS FOUND AND CORRECTED!

With all other assembly completed and any reconfigurations made, install the ICs in their proper sockets. Be absolutely sure that the IC is properly oriented with respect to pin 1, ESPECIALLY IC U21, which is reversed relative to the others. Pin 1 is indicated by a white arrow on the silkscreened top of the board. It is also indicated by a "half-moon" in each silkscreened IC locator box.

This completes assembly of the SCCS-85 board! If an EPROM containing the SCCS-85 monitor is being used refer to the manual for the monitor for a simple program which can be entered into the SCCS-85 for demonstration purposes.

3. HARDWARE ENGINEERING

This chapter contains suggestions for reconfiguring various component groups on the SCCS-85 to fit your particular application.

CPU CLOCK RATE

The 8085 CPU may be operated at clock rates up to 3MHz, although other restrictions may make 2MHz a more practical upper limit. Since this selection must be made at time of assembly it is covered fully in the CPU GROUP section of chapter 2, ASSEMBLY.

ROM SELECTION

The SCCS-85 is etched to accept 2708 EPROMs without alteration. However, with a minimum of patching either single-supply or triple-supply 2716 EPROMs may be used, thereby doubling the ROM capacity of the board.

Like the CPU CLOCK RATE, the ROM SELECTION is best done at time of assembly. However, the change to 2716 EPROMs can be made even after all parts have been installed. For directions on making the reconfiguration see the ROM GROUP section of chapter 2, ASSEMBLY.

RAM OPTIONS

In order for the 8085 to have access to a stack at least 1K bytes of RAM will have to be installed on the SCCS-85. Since it is most likely that users expanding their RAM will want to do so into successively higher memory locations, then the following table for RAM expansion should be followed:

For 1K bytes of RAM, locations 1000H to 13FFH, use RAMs U10 and U14.

For 2K bytes of RAM, locations 1000H to 17FFH, use RAMs U9, U10, U13, and U14.

For 3K bytes of RAM, locations 1000H to 1BFFH, use RAMs U8, U9, U10, U12, U13, and U14.

For 4K bytes of RAM, locations 1000H to 1FFFH, use RAMs U7 through U14.

TIMER GROUP OPTIONS

The TIMER GROUP is probably one of the most versatile components of the SCCS-85. Much of the SCCS-85's flexibility in adapting to dedicated control applications stems from the power of the TIMER GROUP. Since the 8253 timer contains three completely independent and identical timer/counters, and each can be individually programmed to operate in one of six modes of pulse generation, square-wave generation, delay timing, event counting, and the like, nearly endless applications can be easily accommodated.

Each of the three timer/counters in the 8253 has its own clock input, gate input, and output line. The clock input provides the events (level transitions) which the chip's counters count, while the gate input allows the clock input to be enabled or disabled. Depending on the mode the timer has been programmed with, the output will then provide the appropriate signal such as a continuous square wave of programmable frequency, a pulse train of programmable rate, a single pulse of programmable length, a single pulse at the end of a programmable delay, and so on.

The flexibility of the 8253 itself is enhanced by the SCCS-85's provisions for supplying the clock and gate inputs from different sources, as well routing the outputs to various places for use.

Nearly all of the clock, gate, and output signals for the 8253 are routed through the double-row connector pattern P1. Throughout this discussion refer to dwng. no. 4 of the schematics (Timer Group, I/O address decoder). Here it can be seen that nearly all of the 8253 clock, gate, and output pins are connected to the side of P1 closest to the 8253 chip itself (both on the schematic and on the PC board as well). The various signal sources and output destinations are connected to the other side of P1. Thus, most all hardware configurations for the three timers can be made by proper connections between these two rows of pins.

In keeping with the design philosophy of the SCCS-85 the timer group comes pre-configured in a logical structure so that with no modifications the timer group will function in a way that will suit many applications. Looking on the bottom side of the PC board between the two rows of pins of P1 can be seen the seven traces which define this configuration, and which can easily be cut later if reconfiguration is desired. Following is a discussion of that configuration along with suggested applications.

Timer 0

Looking at the schematic it can be seen that timer 0 is configured to receive its clock from the 2MHz CPU clock. This signal passes from pin 15 to pin 16 of P1 as shown by the dotted line on the schematic. If a different source for CLK0 is desired the trace between pins 15 and 16 would be cut, and the new clock connected to pin 16. The gate for timer 0 passes through pins 11 and 12 to Vcc, hence it is enabled all the time. The output for timer 0 passes through pins 13 and 14 to pad B, which is connected by cuttable traces to pads A and C. Pad A leads to connector J3 pin 3, while pad C is the RST7.5 interrupt input to the 8085. Thus, as configured, timer 0 may serve two different purposes. In the first, the 8085 program would enable the RST7.5 interrupt input and the output of timer 0 would then interrupt the 8085 on each rising edge of the output. Hence, with the six possible modes timer 0 can be used in, the CPU can be interrupted: 1. at a constant rate (real time clock); 2. after a programmed delay; 3. at the end of a programmed delay initiated by either a software or hardware trigger. The second use of timer 0 would be to simply provide its output at connector J3 pin 3. RST7.5 interrupts should then be masked in the 8085.

Timer 1

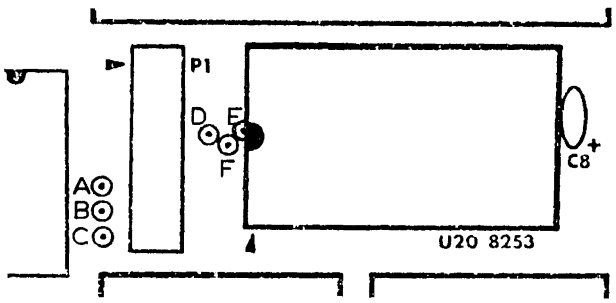
As configured timer 1 also gets the 2MHz CPU clock, though it comes through pads D-E rather than through P1. The gate for timer 1 is permanently tied TRUE. The output of timer 1 passes through pins 7-8 of P1 then on to the SERIAL I/O group where it serves as the baud rate clock for the USART chip. This allows the baud rate to be fully programmable by software. For suggestions on progamming timer 1 for various standard baud rates see chapter 4 on Software Engineering.

Timer 2

As configured timer 2 receives the 2MHz CPU clock through pins 1-2 of P1. Its gate is tied TRUE through pins 5-6. The output of timer 2 is connected, through pins 3-4 of P1, to connector J3 pin 2 for whatever use is desired. An example might be to buffer the output through a transistor to drive a small loudspeaker for generating beeps, tunes, and the like.

RECONFIGURATION

Reconfiguration will generally involve cutting one or more traces under P1, or possibly at pad groups A-B-C or D-E-F. (Shown at right.) If changes will be made at P1 it is suggested that a 16-pin double-row header be installed at P1. This will allow connections to be easily and reliably made by wire-wrapping to the pins on this header.



At this point possible reconfigurations should be apparent. If it is desired to supply any of the timers with clocks other than the CPU clock, one need only cut the appropriate trace under P1 (or trace D-E in the case of timer 1) and connect the desired clock. Note that if the clock is originating off the board, pin 1 of J3 has been conveniently routed to pin 9 of P1 for the user to connect to whatever he pleases.

If very long timing periods are desired, a seperate low-frequency clock can be supplied to a timer. Alternatively, two timers may be cascaded by connecting the output of one to the clock of another. The first timer would then be programmed to operate as a rate generator (a divide by N circuit) to supply a programmable frequency to the next.

It should be noted that the clocks need not be continuous square wave signals. The timers themselves merely count falling transitions on the clock inputs. Thus, if a clock is supplied externally from a device which produces a pulse in coincidence with some event, then the timer can serve as an event counter. The 8253 will allow the count register to be read by the program at any time to determine the current count of events. Or, with the various modes the timer may be programmed into, such things as "interrupt after N events", "interrupt after N events following a hardware strobe on the gate input", "interrupt every N events", etc. are easy to implement.

Since the use of the timers can involve interrupts, see also the discussion of interrupts in chapters 3 and 4.

INTERRUPTS

The 8085 has extensive provisions for using interrupts. As on the 8080A the 8085 has an INTR line which may be pulled high to initiate an interrupt sequence. On the first machine cycle of the next instruction the $\overline{\text{INTA}}$ (interrupt acknowledge) signal will be sent, informing the interrupting device that it should place its interrupt vector on the bus, after which the 8085 will call to one of eight memory locations.

For purposes of using interrupts from peripherals on the SCCS-85 board, (e.g.the 8251, 8253, or 8255) the 8085 also provides another mechanism for generating interrupts. Three inputs to the 8085 chip, the RST5.5, RST6.5, and RST7.5 inputs, will each cause an interrupt vector to a specific memory location when pulled high, WITH NO OTHER HARDWARE NECESSARY. Furthermore, two of these inputs, the RST5.5 and RST6.5 are LEVEL SENSITIVE, meaning that an interrupt will be maintained as long as the input is held high. This is used for things like a USART which provides a RECEIVE BUFFER FULL signal which can be used to interrupt the 8085 when a character is received. Here, the interrupt is held until it is serviced by the software which reads the received character, thereby resetting the flag and the interrupt request.

The other input, the RST7.5 input, is EDGE sensitive meaning that if the input is pulled high and held there indefinitely, only ONE interrupt will be recognized - it is the low-to-high transition which generates the interrupt. To generate another interrupt the input must go low then go high again. This input is useful for things like making a real time clock. A square wave of desired frequency is simply tied to the RST7.5 input, then on each rising edge an interrupt will be generated.

Provisions have been made on the SCCS-85 for configuring RST interrupts in any desired fashion. As manufactured two of the interrupt inputs, the RST7.5 and RST6.5 inputs have been pre-configured in a way which should be adequate in most applications. This configuration is described below, along with suggestions for re-configuring for other applications.

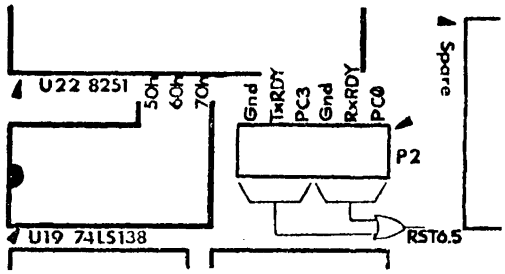
RST7.5

As described above under TIMER GROUP the RST7.5 input is connected to the output of timer 0. Thus with no alterations this timer can be used for such things as "interrupt at an N Hz frequency (real time clock)", "interrupt after N clock cycles (programmable delay)", or in general, interrupt according to some programmable time function.

If it is desired to use the RST7.5 interrupt input for some other purpose this can be done in different ways. For example, if the interrupt will be supplied from some other point on the PC board, cut the trace between pads B and C shown above, and connect the signal to pad C. (Refer also to dwng. no. 4 of the schematics.)

If the interrupt signal will be supplied from off the board, cutting the trace between pins 13 and 14 of P1 will leave the RST7.5 input connected to connector J3 pin 3.

RST6.5



Referring to dwng. no. 5 of the schematics it can be seen that an INTERRUPT SELECTOR GROUP has been provided to allow two interrupt signals to be OR-ed together to generate the RST6.5 interrupt input. Selecting two of four possible signals can be done at the double-row header P2. (See figure at right.) The four signals are RxRDY and TxRDY from the 8251 USART and PC0 and PC3 from the 8255 PIO chip. Also present at P2 are two grounded pins, allowing one or both of the interrupt inputs to be tied inactive. Note on the schematic the dotted lines indicating that the PC board is etched with both interrupt inputs grounded. Hence, to allow one or two of the four interrupt signals it will be necessary to cut one or both of the traces 5-6 or 11-12 under P2 and connect the desired interrupt signal to pads 2-4-6 and/or pads 8-10-12.

Of course it is also possible to use interrupt signals other than the four mentioned above. Just cut trace 5-6 or 11-12 and connect the desired interrupt signal to pads 2-4-6 or 8-10-12 as above.

OTHER INTERRUPTS

Three other interrupt inputs to the 8085 are available for user purposes. These are RST5.5, INTR, and TRAP. All three of these signals pass through double-row header P3 where, as pre-configured, these inputs are all tied low by short traces on the bottom side of the PC board under P3. (See dwng. no. 1 of the schematics.) These three inputs are available on the bus at J1 for connection to other boards in the system, but this by no means rules out using any of them on the board. Just cut the trace under P3 to enable the desired input, and connect the interrupt signal to pad 2, 4, or 6, depending on the interrupt desired.

Note when using the INTR input that the bus on the SCCS-85 DOES NOT float to the high level. This means that the "trick" used on some systems of letting the floating bus put a RST 7 instruction on the bus will not work.

SERIAL I/O

In nearly all applications the SERIAL I/O group, when used, will be used for RS-232 communications with other devices.

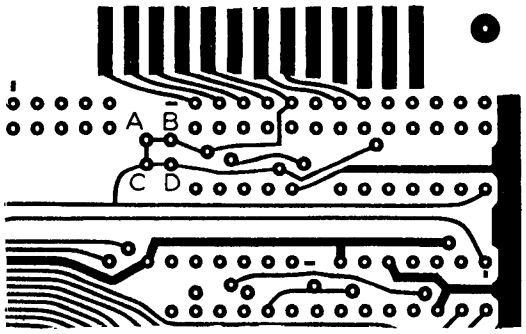
Some devices, modems in particular, make use of a number of device-control and handshaking signals in the RS-232 definition, so the SCCS-85 has been designed to support these signals. Such signals include REQUEST-TO-SEND, DATA-TERMINAL-READY, DATA-SET-READY, and CLEAR-TO-SEND. Two of these are inputs while two are outputs.

The two outputs, $\overline{DTR}$ and $\overline{RTS}$ are GENERAL PURPOSE 1-BIT OUTPUT PORTs and as such can be used for any purpose the user desires, such as powering-up a printer, etc.

Of the two inputs, one is a GENERAL PURPOSE 1-BIT INPUT PORT, the $\overline{DSR}$. Its status can be read at any time by the CPU and has no effect on the transmission or reception of data.

The other input, $\overline{CTS}$ is a clear-to-send input which must be low (TRUE) to enable the 8251 transmitter. Transmission will stop on the next character if this pin goes high.

Since not all devices will support the $\overline{DSR}$ and $\overline{CTS}$ inputs, the SCCS-85 has these two inputs tied TRUE on the RS-232 side of the 1489 receiver chip. (See dwng. no. 6 of the schematics.) If your device supports either of these signals be sure to cut the appropriate traces on the bottom side of the board to enable the input. The trace between pads A-B (shown at right) must be cut to enable $\overline{CTS}$, while C-D must be cut to enable $\overline{DSR}$.



Two options exist for connecting the external device to the PC board. These options are covered in the section on CONNECTORS below.

It is possible to supply the 8251 with a baud rate clock other that from the timer group. This is most easily done by cutting the trace between pins 7 and 8 of P1, then connecting the new clock signal to pin 7 of P1.

No provisions have been made for supporting a current-loop interface on the SCCS-85.

SOD, SID LINES ON 8085

The 8085 chip itself provides a 1-bit input and 1-bit output port, called SID (serial-in data) and SOD (serial-out data) respectively.

These lines are present on connector J3, pins 7 and 8 for user purposes. Refer to the 8080/8085 Assembly Language Reference Manual and 8085 User's Manual for information on reading and setting these lines.

BUS EXTENSION

The SCCS-85 on-card bus is available at connector J1 for expansion to other boards.

Chapter 5 contains a Bus Signal Definition table which describes each of the signals on J1.

For the most part, the signals on the bus are unbuffered, direct connections to the 8085 and other chips. Hence, care must be taken when expanding the system to other cards that the bus loading be kept below minimums.

The Connector Signal Definition table indicates which lines are buffered.

With all address and data lines on the bus being driven by MOS chips, and also being listened to by MOS chips, two aspects of bus-loading must be considered when extending the bus.

The first aspect is current-drive capability. The 8085 address and data lines can sink up to 2ma of current and still maintain an output-low voltage less than 0.45V. Connecting other MOS chips to the address and data lines add an insignificant current load (less than 10uA) to the bus, hence they need not be considered when checking bus current loading.

On the other hand, connecting TTL to the bus (e.g. for I/O address decoding) adds a significant current load to the bus. Since all TTL on the SCCS-85 is LS, the current load per TTL input is a max. of about .36 ma for a low input. Hence, an unbuffered MOS address or data line can support at most five LS TTL loads.

The other aspect of bus loading which must be considered is capacitance-loading. The timing specs for the 8085 chip are given assuming a 150pF load on the signal outputs. For loads between 150pF and 300pF timing specs are to be derated by +0.30ns per pF. In other words, if we load the bus to 300pF we must derate the timing specs by 45ns. In high bus-load systems, the advantages of running the CPU at 2MHz rather than 3MHz is apparent.

The Intel specs for the MOS peripheral chips (e.g. 8251, 8253, etc.) quote that an input to the chip has a max. capacitance of 10pF, while a bi-directional data pin has a max. capacitance of 20pF. LS TTL inputs also have an input capacitance of about 5 pF, but since more than five LS TTL chips will overload the current drive of the bus, the total capacitance of the TTL loads on the bus can be overlooked in most cases.

Based on the above and armed with the data sheets for the chips on your particular SCCS-85 you can add up the bus loading for the various signals and establish how much more any bus extension dare load the bus. To give some idea of what you might come up with, the following table shows the loading on the upper 8 address lines, the lower 8 address lines, and the data bus for a FULLY POPULATED SCCS-85:

A8-A15	A0-A7	D0-D7
65pF, 1 TTL	110pF, 1 TTL	134pF, 1 TTL

Above it can be seen that for the user with some options missing on his system, quite a bit of "headroom" exists for expanding the bus without overdoing the loading.

CONNECTORS

The SCCS-85 provides a convenient and flexible system for making connections between the board and the outside world. Connectors J1 through J6a are each a double-row of plated-through holes spaced on 0.100 inch centers in patterns of from 10 to 50 holes.

These patterns can support a wide variety of connector hardware which is not only versatile, but inexpensive as well. Some of the possiblilties are outlined below.

No connections at all

The connector system used has advantages even where no connections at all are made to a connector. The connector pattern is very inexpensive to produce on a PC board, and requires no special tooling, gold-plating, and the like. You don't have to pay extra for something you may not even use!

Just one or two connections

If only one or two connections need to be made, a piece of wire can simply be soldered directly to the proper hole in the pattern without damaging its future use with a regular connector.

With ribbon cables

When a ribbon cable is to be connected to a pattern, it is recommended that a "double-row jumper header" made by AP Products be installed in the connector. These are double rows of pins bound together in the proper spacing by a plastic header. The header is simply inserted into the pattern and soldered on the bottom. Then a ribbon cable with a female connector on the end may be simply plugged onto the header.

These double-row headers come in two varieties; straight and right-angle. The straight variety will serve best on the I/O connectors J2 through J6a where a ribbon cable extending to a single destination will be plugged.

The right-angle type are very useful for "daisy-chaining" the bus connector J1 to several boards. For example, to make an economical "mother-board" for extending the bus to three other cards, 50-pin right-angle headers would be installed in connector J1 of all cards. Then, four 50-pin female ribbon cable connectors would be installed equidistantly along a length of 50-conductor ribbon cable. Finally, each of the four boards would be plugged onto this cable.

Plugging boards directly into other boards

AP Products also makes double-row FEMALE headers which will solder directly into the connector patterns on the board. This provides two ways in which boards may be plugged directly into other boards.

For example if a right-angle header is installed in connector J1 and a female header installed in another PC board, then the SCCS-85 can be plugged perpendicularly into the "mother-board".

Or, if it is known that the SCCS-85 will extended to only one other board then one may solder a female header in the connector on the TOP side of the peripheral board, and a male header installed on the BOTTOM side of the SCCS-85. Then the two boards may be easily plugged together in a "sandwitch" configuration. This technique will be recommended for the up-coming CRT interface card, when using the SCCS-85 as a dedicated smart terminal.

CONNECTOR J2, J3, and J4

According to the silk-screen legend on the board, J4 is the combination of connectors J2 and J3.

J3 is mainly associated with inputs and outputs for the Timer Group, while J2 provides access to the PIO group. If the signals from J2 and those from J3 are destined to different places, then a 26-pin header should be installed in J2 and a 10-pin header installed in J3. Then, separate ribbon cables may be plugged into these connectors.

If, on the other hand, both the timer and PIO signals will be cabled to the same destination, then a single 40-pin header may be installed in J4. A single 40-conductor ribbon cable will then be sufficient for the interconnection.

The Connector Pin Assignment table in chapter 5 gives the signal assignments for connectors J2 through J4.

SERIAL CONNECTOR J6b

One last connector deserves mentioning, that being the RS-232 connector J6b. Provisions have been made for installing an easy-to-get DB-25S "D" connector directly on the SCCS-85 board. Once installed, this connector is already wired in the RS-232 standard configuration.

On the PC board note that connector J6b appears to be a set of edge-finger contacts. In fact, the positioning of these fingers on the top and bottom of the board exactly coincide with that of the pins on a DB-25S connector. Further, the two rows of pins on the connector are separated by 1/16th inch, just the thickness of the SCCS-85 board. This means that the connector may be slipped onto the edge of the board with the row of 13 pins on the bottom side and the row of 12 pins on the top side. Sliding the connector along the edge of the board, eventually the pins will line-up with the edge fingers. Once positioned, simply solder each of the pins on the connector to the finger directly beneath it. Not only is the connector now correctly wired, but rigidly mounted as well!

ADDITIONAL I/O SELECT LINES

If the user is adding additional peripheral chips on another board he may find it convenient to use one or more of the unused outputs of the ON-BOARD I/O ADDRESS DECODER to perform the chip-select function. (Refer to dwng. no. 4 of the schematics.)

These pads are located between U19 and U22 on the PC board labelled 50h, 60h, and 70h.

> WARNING: There is an error on the silkscreen on the SCCS-85 PC board - the pads between U19 and U22 labelled 50h, 60h, and 70h should be labelled 40h, 50h, and 60h respectively.

These pads each go low anytime the lower 8 bits of the address bus equal the indicated value through the next 15 higher addresses. For example, the pad labelled 50h will go low anytime the address bus contains XX50h through XX5Fh where XX indicates that the upper 8 bits are arbitrary. (This makes no

difference during I/O cycles since the 8085 places the I/O address on BOTH the upper AND lower 8 bits of the address bus.)

It is important to note that the peripheral using these I/O address select signals must qualify them with either the $\overline{IOR}$ or $\overline{IOW}$ control signal. This is because these outputs will go low when MEMORY locations with addresses in the proper range are being accessed. It is a convention that Intel peripheral chips qualify their chip-select inputs with the $\overline{IOR}$ and $\overline{IOW}$ signals.

4. SOFTWARE ENGINEERING

This chapter contains hardware-related software information; such things as the I/O addresses of the various peripheral chips, interrupt vector addresses, programming the timer chip to provide standard baud rates for the 8251 USART, etc.

POWER-UP INFORMATION

When power is first applied to the 8085 the reset circuitry will reset the 8085 automatically, after which the 8085 will immediately begin executing at loc. 0000 in memory. Therefore, there must be some program there to execute. That is why at least one EPROM must be installed in U6. At loc. 0000 in your software should be the initialization routine needed for your particular hardware. For example, if the timer chip is used to provide the baudrate clock for the USART, then the timer chip must be initialized to operate timer 1 in the correct mode and divide by the proper number for the desired baud rate. Then the USART must be initialized for the desired mode of operation.

If interrupts are being used, the 8085 interrupt mask must be initialized to enable the desired interrupts.

The stack pointer must be set to point to the top of your available RAM. Etc., etc.

Note also that this same reset sequence takes place any time the manual reset pushbutton SW1 is closed.

RAM

As mentioned under hardware engineering, RAM starts at 1000H and goes up to 13FF for 1K bytes, 17FF for 2K bytes, 1BFF for 3K bytes, and 1FFF for 4K bytes.

PERIPHERAL CHIP I/O ADDRESSES

There are four peripherals on a fully-populated SCCS-85. These are the 8253 timer, 8255 PIO, 8251 USART, and 8257 DMA. The following table gives the I/O addresses for each of the registers within the chip:

DEVICE	ADDRESS	READ OPRATION	WRITE OPERATION
8251 USART	00h	Rec. Data Reg.	Trans. Data Reg.
	01h	Status Reg.	Control Reg.
8255 PIO	10h	Read Port A	Write Port A
	11h	Read Port B	Write Port B
	12h	Read Port C	Write Port C
	13h	ILLEGAL	Write Control Reg.

8253 TIMER	20h	Rd. Counter 0	Wrt. Counter 0
	21h	Rd. Counter 1	Wrt. Counter 1
	22h	Rd. Counter 2	Wrt. Counter 2
	23h	ILLEGAL	Write Mode reg.
8257 DMA	30h	Read/write chan. 0 DMA address	
	31h	Read/write chan. 0 Terminal Count reg.	
	32h	Read/write chan. 1 DMA address	
	33h	Read/write chan. 1 Terminal Count reg.	
	34h	Read/write chan. 2 DMA address	
	35h	Read/write chan. 2 Terminal Count reg.	
	36h	Read/write chan. 3 DMA address	
	37h	Read/write chan. 3 Terminal Count reg.	
	38h	Read Status Reg.	Write Mode Reg.

I/O Addresses 80h and higher are available for user definition

INITIALIZATION OF TIMER AND USART FOR SERIAL I/O

If you are using the 8253 timer and 8251 USART in the configuration the board is manufactured in, then the following 8085 assembly code may be used to initialize both for serial I/O at the buad rate of your choice:

```
;************************************************************
; code to initialize 8253 timer and 8251 USART for serial I/O on
; SCCS-85 board.

; first initialize timer chip to generate 16X baudrate for USART
        mvi     a,76h   ;program timer 1 for mode 3, expect 2 bytes
        out     23h
        mvi     a,lobaud ;send lower byte of baudrate divisor to timer
        out     21h
        mvi     a,hibaud ;send upper byte of baudrate divisor
        out     21h

;next initialize USART
        mvi     a,82h   ;force usart to expect command word
        out     01h
        mvi     a,40h   ;now make usart expect mode word
        out     01h
        mvi     a,4eh   ;mode byte - baud clock is 16X
        out     01h
        mvi     a,27h   ;command byte
        out     01h

; initialization complete!
;************************************************************
```

In the code above there are two bytes, lobaud and hibaud, which the user must determine to select the desired baudrate. The table below gives the proper divisor value for each of the standard baudrates, and for two different CPU clock crystals. To use this divisor value, convert it into hexadecimal. Then the upper two hex digits are "hibaud" and the lower two digits are "lobaud".

Baud Rate	Divisor, with 3.58MHz crystal, (1.79MHz CPU clk)	Divisor, with 4.00MHz crystal (2MHz CPU clk)
38,400	3	not possible
19,200	6	not possible
9600	12	13
4800	23	26
2400	47	52
1200	93	104
600	186	208
300	373	417
150	746	833
110	1017	1136
75	1491	1667

INTERRUPTS

As configured the SCCS-85 makes use of the RST7.5 and RST6.5 interrupt inputs on the 8085.

When a RST7.5 interrupt occurs, the equivalent of a CALL instruction to loc. 003Ch is executed. At this point the user should store a JMP instruction to the service routine for that particular interrupt. Don't forget to preserve the contents of the registers and re-enable interrupts before returning to the interrupted program.

Similarly, when a RST6.5 interrupt occurs, the equivalent of a CALL to loc. 0034h is executed.

CONNECTOR PIN ASSIGNMENTS

J1 - Expansion bus

1	GND	2	GND
3	A1	4	A0
5	A3	6	A2
7	A5	8	A4
9	A7	10	A6
11	A9	12	A8
13	A15	14	A14
15	A13	16	A12
17	A11	18	A10
19	MEMSEL	20	(not used)
21	+12V	22	-12V
23	$\overline{IOR}$	24	$\overline{MEMR}$
25	$\overline{MEMW}$	26	$\overline{IOW}$
27	D6	28	D7
29	D4	30	D5
31	D2	32	D3
33	D0	34	D1
35	$\overline{INTA}$	36	AEN
37	S1	38	S0
39	INTR	40	RST5.5
41	IO/$\overline{M}$	42	TRAP
43	(user defined)	44	ALE
45	READY	46	CLK
47	RESET OUT	48	$\overline{RESET\ IN}$
49	+5V	50	+5V

J2 - PIO

1	PA4	2	PA3
3	PA5	4	PA2
5	PA6	6	PA1
7	PA7	8	PA0
9	+5V	10	GND
11	PC6	12	PC7
13	PC4	14	PC5
15	PC1	16	PC0
17	PC3	18	PC2
19	PB7	20	PB0
21	PB6	22	PB1
23	PB5	24	PB2
25	PB4	26	PB3

J3 - TIMER

1	user defined	2	OUT2
3	RST7.5	4	$\overline{CLK}$
5	user defined	6	user defined
7	SID	8	SOD
9	user defined	10	user defined

J4 - PIO/TIMER

1	PA4	2	PA3
3	PA5	4	PA2
5	PA6	6	PA1
7	PA7	8	PA0
9	+5V	10	GND
11	PC6	12	PC7
13	PC4	14	PC5
15	PC1	16	PC0
17	PC3	18	PC2
19	PB7	20	PB0
21	PB6	22	PB1
23	PB5	24	PB2
25	PB4	26	PB3
27	(not used)	28	(not used)
29	(not used)	30	(not used)
31	user defined	32	OUT2
33	RST7.5	34	$\overline{CLK}$
35	user defined	36	user defined
37	SID	38	SOD
39	user defined	40	user defined

J5 - DMA

1	DRQ1	2	DRQ0
3	DRQ3	4	DRQ2
5	$\overline{DACK0}$	6	$\overline{DACK1}$
7	$\overline{DACK2}$	8	$\overline{DACK3}$
9	GND	10	TC

J6b - RS-232 Delta connector		J6a - RS-232 double-row header	
1	GND	1	GND
2	$\overline{\text{Transmit data}}$	3	$\overline{\text{Transmit data}}$
3	$\overline{\text{Receive data}}$	5	$\overline{\text{Receive data}}$
4	Request to send (output)	7	Request to send
5	Clear to Send (input)	9	Clear to send
7	GND	13	GND
8	Data Set Ready (input)	15	Data Set Ready
20	Data Terminal Ready (output)	14	Data Terminal Ready

NOTE: Connectors J2 and J3 are positioned such that together they may be considered a single 40-pin connector J4, or used individually.

BUS SIGNAL DEFINITIONS

GND — Logic ground for SCCS-85

A0 - A15 — (Output) Address lines 0 through 15. These are positive true signals. Lower eight bits are valid from the falling edge of ALE to end of machine cycle, and are buffered EXCEPT DURING A DMA CYCLE. (See data sheets on 8257 DMA controller. Upper eight bits are also valid from the falling edge of ALE to end of cycle but are not buffered.

D0 - D7 — Bi-directional positive-true data bus. During write cycles data on bus is valid during trailing edge of $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ pulse. During read cycles, data must be valid on trailing edge of $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse. The data bus is not buffered.

$\overline{\text{IOR}}$ — (Output) $\overline{\text{I/O READ}}$ control signal. Low-going pulse during which selected peripheral should enable its tri-state bus drivers and place data on bus. Data must be valid on the trailing (rising) edge of pulse. Buffered by LS TTL gate.

$\overline{\text{IOW}}$ — (Output) $\overline{\text{I/O WRITE}}$ control signal. Low-going pulse used by peripherals to strobe data on bus into peripheral register. Latching should occur on trailing (rising) edge of pulse. Buffered by LS TTL gate.

$\overline{\text{MEMR}}$ — (Output) $\overline{\text{MEMORY READ}}$ control signal. Low-going pulse during which selected memory device should place its data on the bus. Data must be valid on the trailing (rising) esge of pulse. Buffered by LS TTL gate.

$\overline{\text{MEMW}}$ — (Output) $\overline{\text{MEMORY WRITE}}$ control signal. Low-going pulse used by memory devices to enable the writing of the data currently on the bus into the selected memory location. Buffered by LS TTL gate.

AEN — (Output) ADDRESS ENABLE signal used only during DMA cycles. Otherwise remains low. Positive-true signal which indicates that the address currently on the address bus is that provided by the DMA controller during a DMA transfer cycle. Unbuffered, has same timing and specs as pin by same name on 8257 DMA controller.

S0, S1 — (Output) Machine-cycle status bits output by 8085. Same timing specs and definitions as pins by same name on 8085. Not buffered.

IO/$\overline{M}$ — (Output) Indicates if the current READ or WRITE is to memory or I/O. Same timing and specs as pin by same name on 8085. Not buffered.

ALE — (Output) Positive going pulse used to latch the lower eight address bits and the status bits S0 and S1. Latches should be a level-triggered type. Not buffered.

CLK — (Output) Square wave of half the frequency of the crystal used to clock the 8085. Same timing as the pin by same name on 8085. Not buffered.

READY — (Input) This input is used by a slow peripheral or memory to insert wait states into a machine cycle. Has pullup resistor, so may be left unconnected, or several devices may drive the input through open-collector gates.

$\overline{\text{RESET IN}}$ — (Input) When pulled low the program counter is reset to 0 and the INTE flip-flop and HLDA flip-flop are reset. May be momentarily grounded with pushbutton switch to effect a manual reset.

RESET OUT — (Output) Positive-true signal that indicates the CPU is being reset. May be used as a system reset. Not buffered.

INTR — (Input) Positive-true input which initiates an interrupt to the 8085. Same definition and restrictions as pin by same name on 8085.

$\overline{\text{INTA}}$ — (Output) Is used instead of (and has the same timing as) the $\overline{\text{MEMR}}$ during the next instruction cycle after the INTR has been accepted. Has same timing and specs as pin by same name on 8085. Not buffered.

TRAP — (Input) Input which causes a non-maskable interrupt. Control transfers to location 0024h in memory. Same timing and specs as pin by same name on 8085.

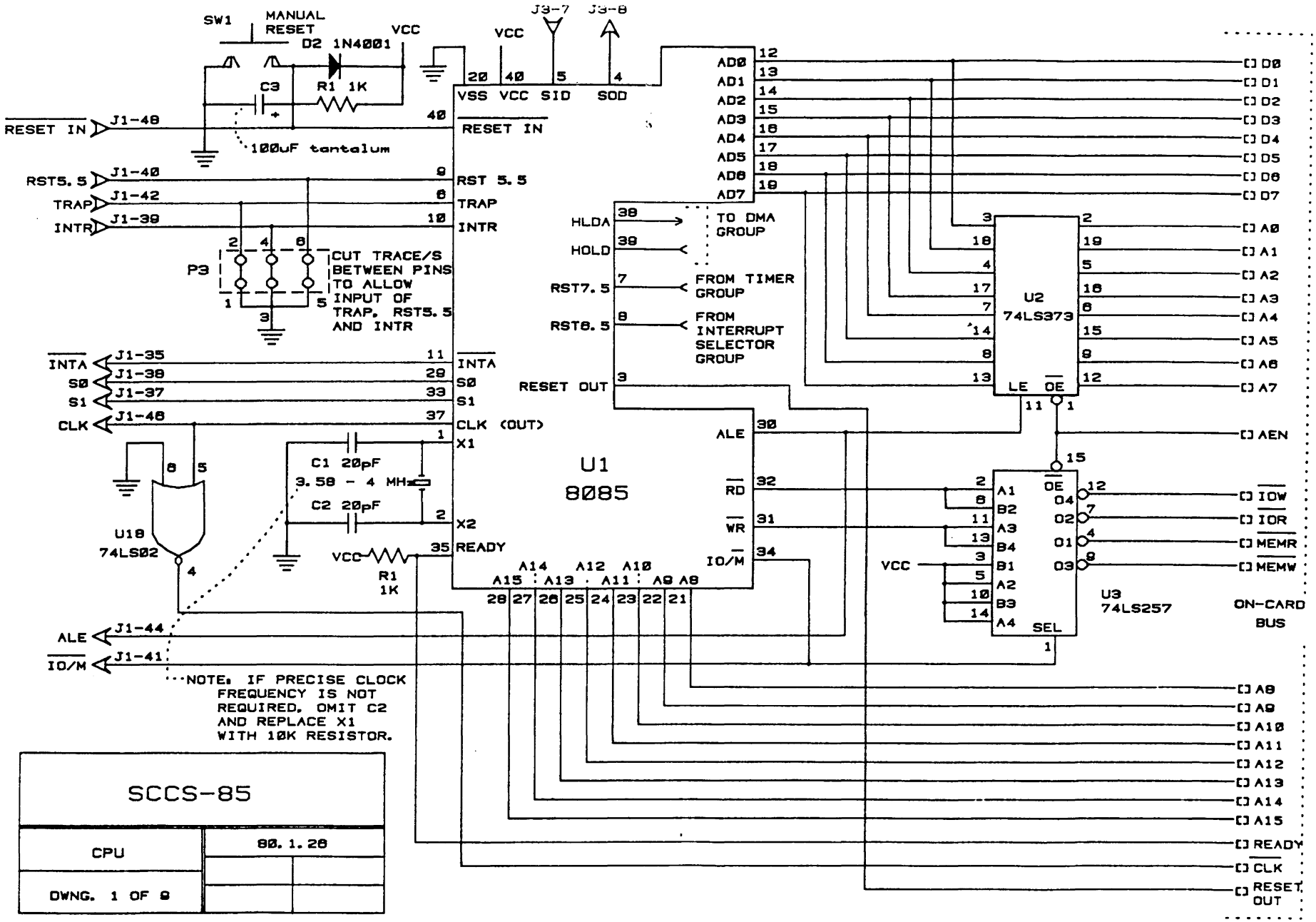
RST5.5 — (Input) Has same input timing as INTR but causes a RESTART to automatically be inserted. Control is transferred to loc. 002Ch. Maskable.

MEMSEL — (Output) Positive-true signal which indicates that the address currently on the bus is within the first 8K bytes of memory space. Is useful in systems with memory expanded onto additional cards to determine if the memory selected is on the SCCS-85 card. Buffered by LS TTL gate.

+12V, -12V — Power supply inputs to SCCS-85 board. Requirements are regulation to plus or minus 10% with currents up to 150 ma. If the SCCS-85

uses 5V-only EPROMS and the RS-232 driver chip is not used, these supplies may be omitted.

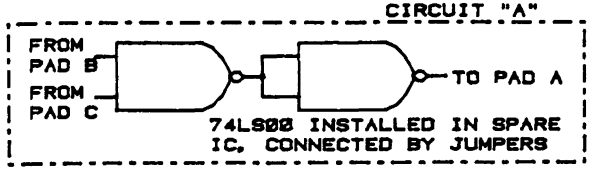
+5V — Logic supply to all chips. Must be regulated to plus or minus 5% and capable of 1.5 A for a fully-populated SCCS-85.

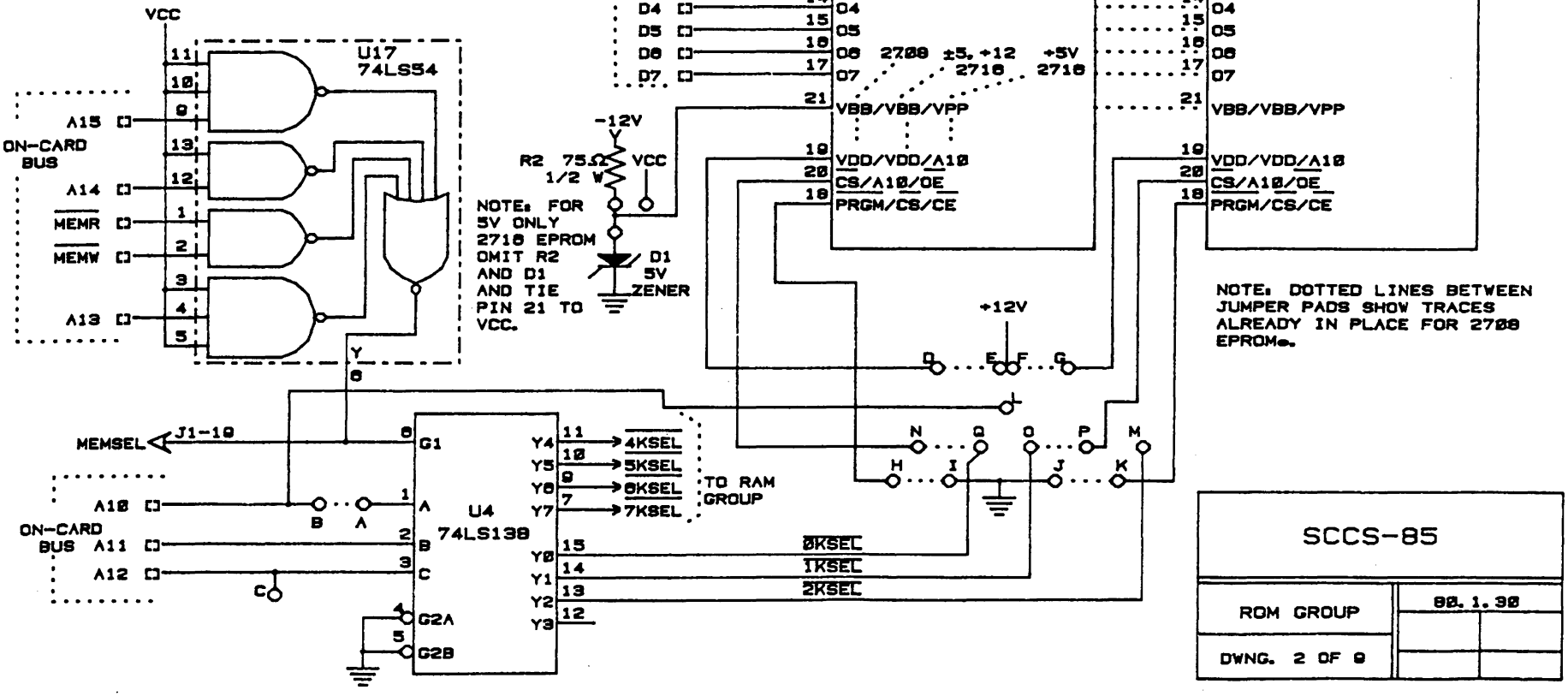


SCCS-85	
CPU	80.1.28
DWNG. 1 OF 8	

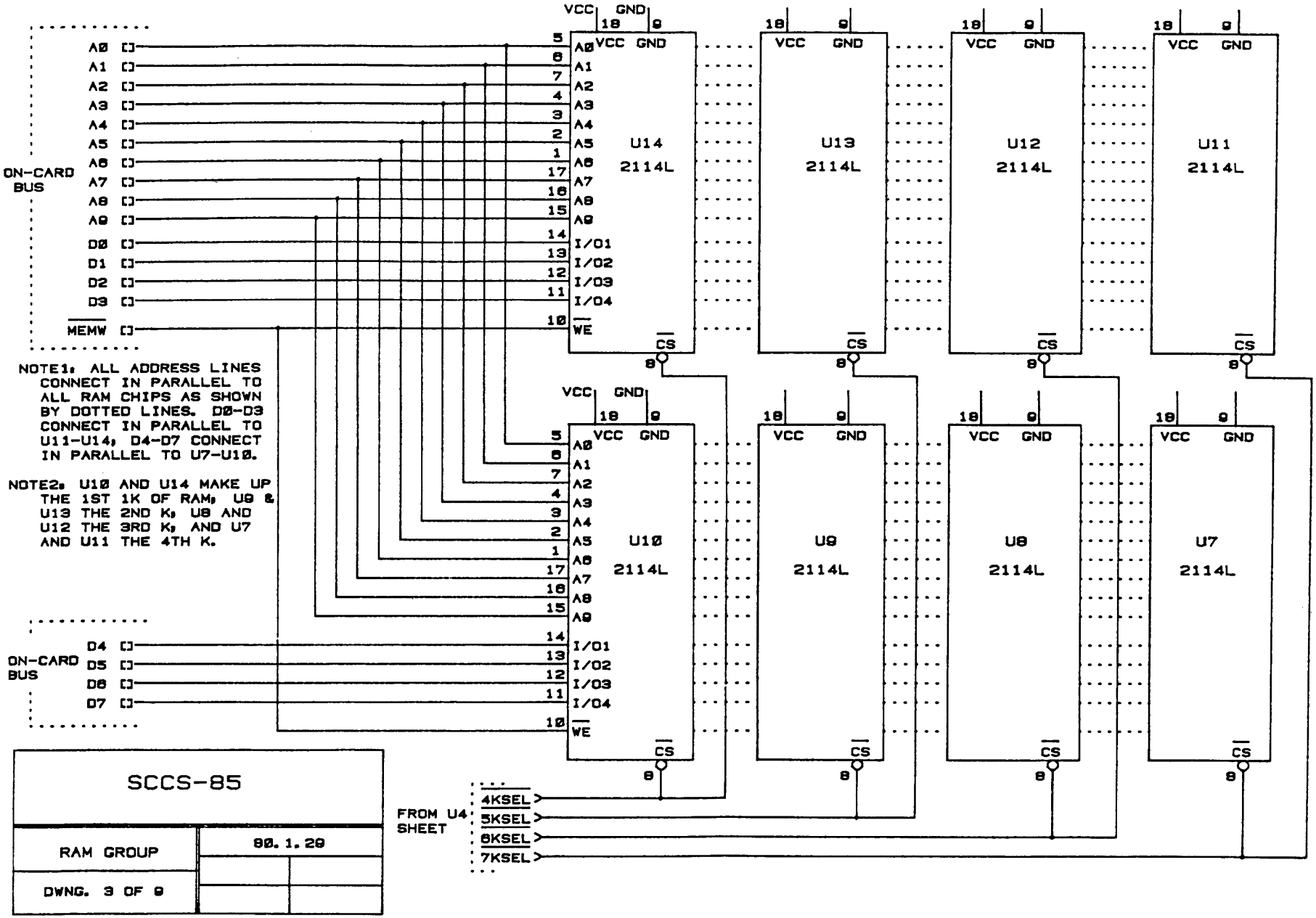
	CUT TRACES:	JUMPER PADS
2708	NONE	NONE
+5, -5, +12V 2716	N-Q, O-P, H-I, J-K, A-B	N-L-P, H-Q, K-M INSTALL CIRCUIT "A"
+5V ONLY 2716	D-E, F-G, O-P, A-B	D-L-G, P-M INSTALL CIRCUIT "A"

CIRCUIT "A"





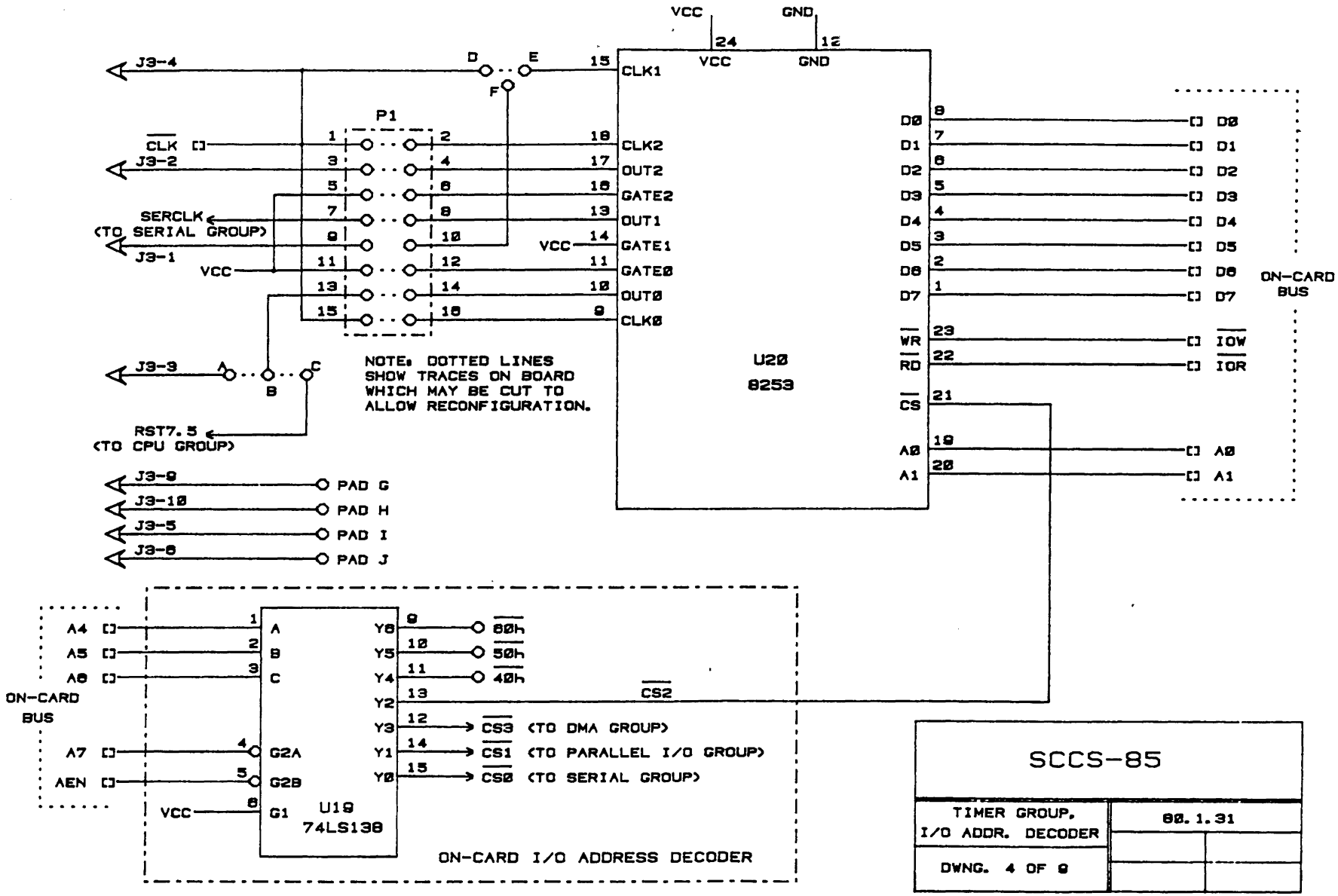
SCCS-85	
ROM GROUP	80.1.30
DWNG. 2 OF 9	

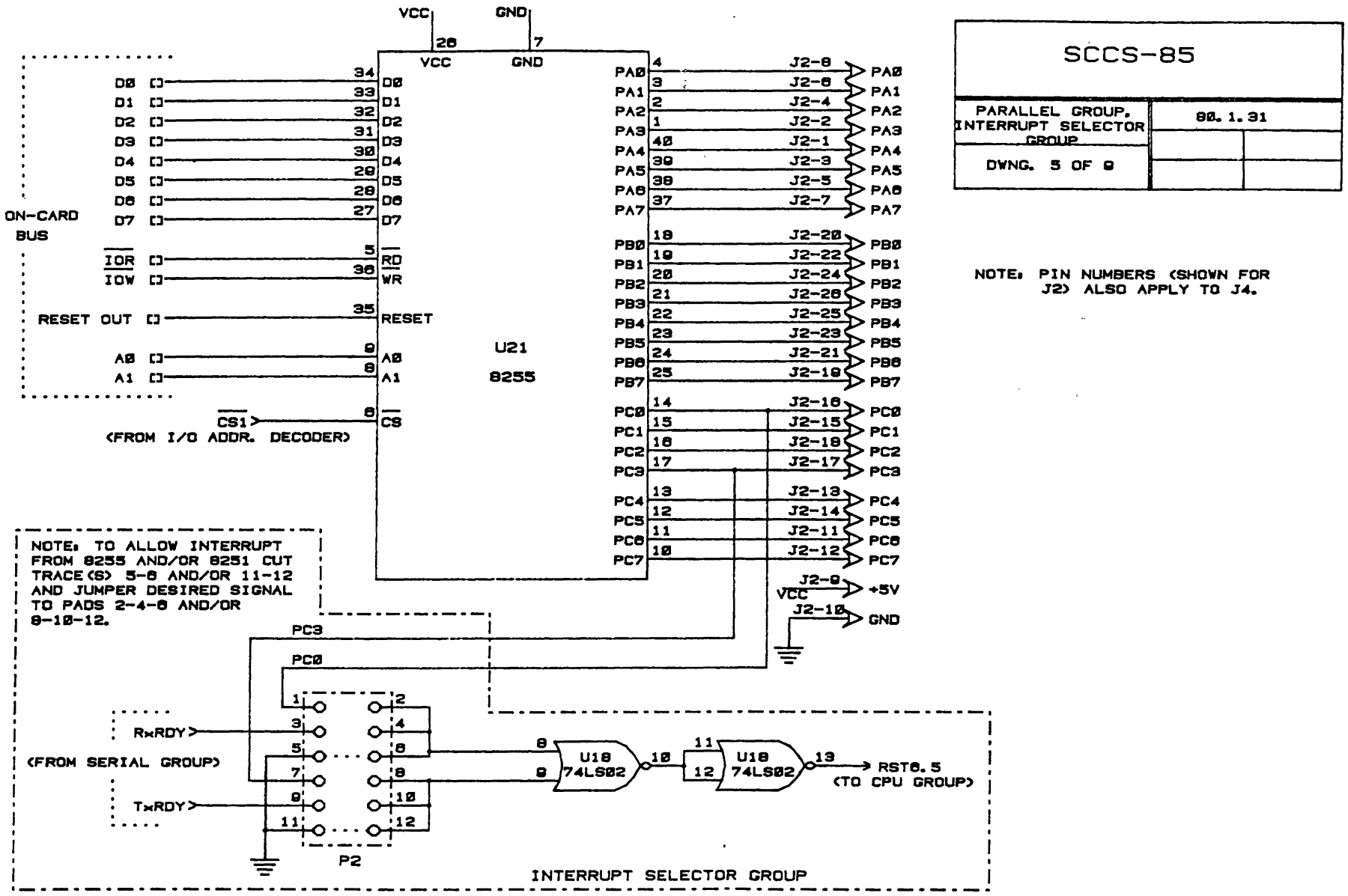


NOTE1: ALL ADDRESS LINES CONNECT IN PARALLEL TO ALL RAM CHIPS AS SHOWN BY DOTTED LINES. D0-D3 CONNECT IN PARALLEL TO U11-U14, D4-D7 CONNECT IN PARALLEL TO U7-U10.

NOTE2: U10 AND U14 MAKE UP THE 1ST 1K OF RAM, U9 & U13 THE 2ND K, U8 AND U12 THE 3RD K, AND U7 AND U11 THE 4TH K.

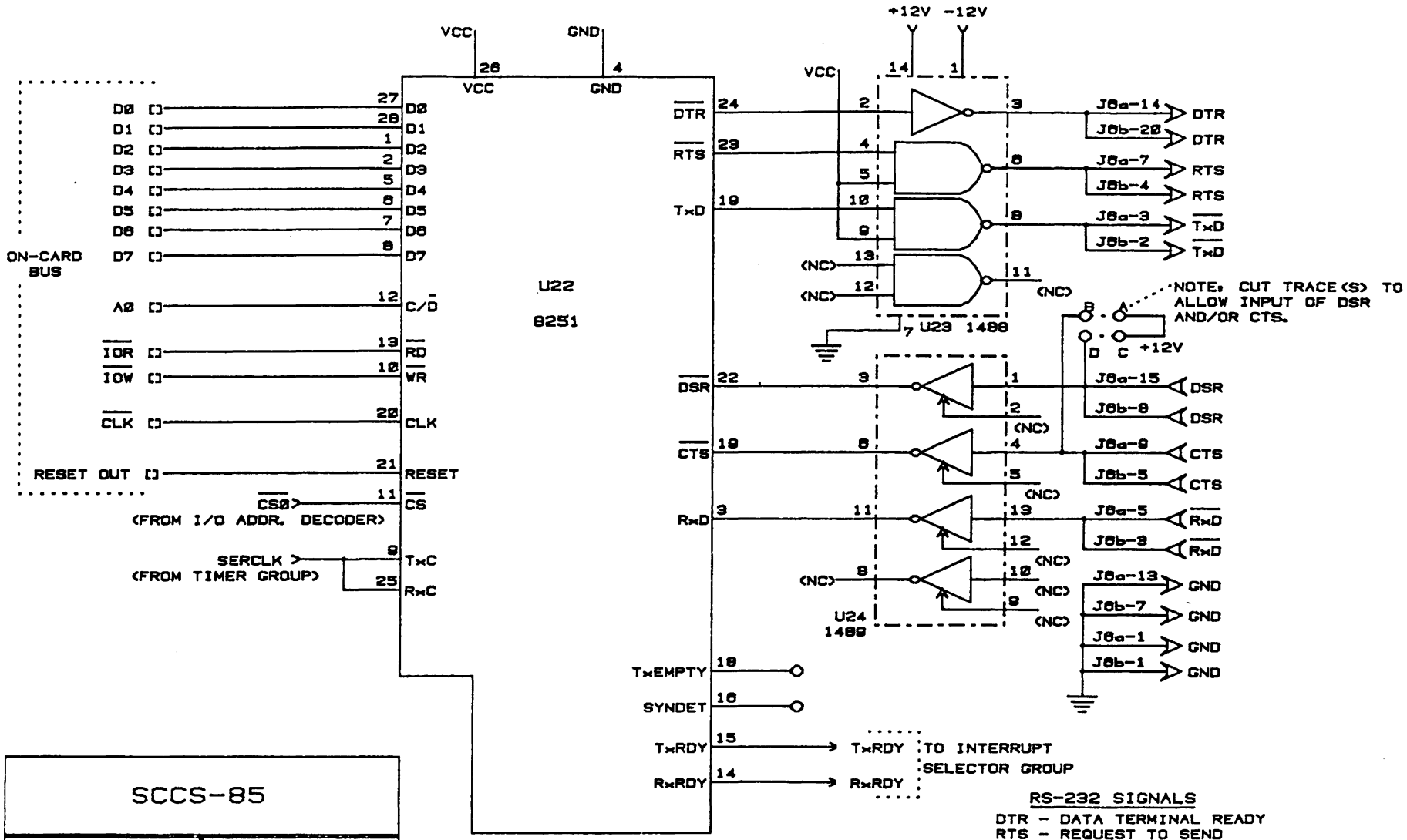
SCCS-85		
RAM GROUP	80.1.29	
DWNG. 3 OF 9		


VCC
GND
24
12
VCC
GND
J3-4
D
E
F
15
CLK1
P1
CLK
J3-2
SERCLK
(TO SERIAL GROUP)
J3-1
VCC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
18
17
16
13
14
11
10
9
CLK2
OUT2
GATE2
OUT1
GATE1
GATE0
OUT0
CLK0
J3-3
A
B
C
RST7.5
(TO CPU GROUP)
NOTE: DOTTED LINES SHOW TRACES ON BOARD WHICH MAY BE CUT TO ALLOW RECONFIGURATION.
U20
8253
D0
D1
D2
D3
D4
D5
D6
D7
WR
RD
CS
A0
A1
8
7
6
5
4
3
2
1
23
22
21
19
20
ON-CARD BUS
IOW
IOR
J3-9
J3-10
J3-5
J3-6
PAD G
PAD H
PAD I
PAD J
A4
A5
A6
A7
AEN
ON-CARD BUS
A
B
C
G2A
G2B
G1
U19
74LS138
VCC
Y6
Y5
Y4
Y2
Y3
Y1
Y0
9
10
11
13
12
14
15
80h
50h
40h
CS2
CS3 (TO DMA GROUP)
CS1 (TO PARALLEL I/O GROUP)
CS0 (TO SERIAL GROUP)
ON-CARD I/O ADDRESS DECODER
SCCS-85
TIMER GROUP, I/O ADDR. DECODER
00.1.31
DWNG. 4 OF 9



SCCS-85		
PARALLEL GROUP, INTERRUPT SELECTOR GROUP	80. 1. 31	
DWNG. 5 OF 8		

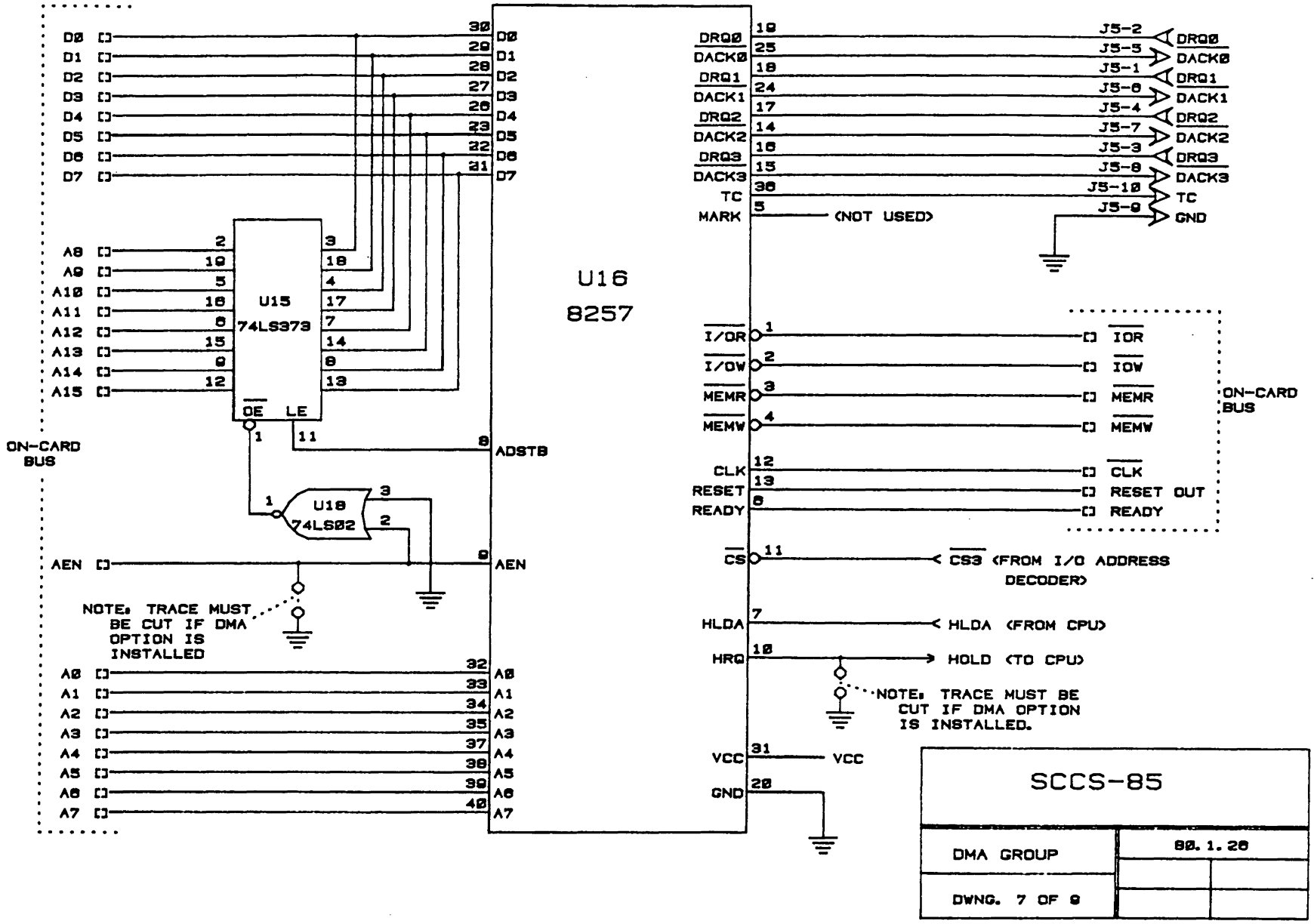
NOTE: PIN NUMBERS (SHOWN FOR J2) ALSO APPLY TO J4.

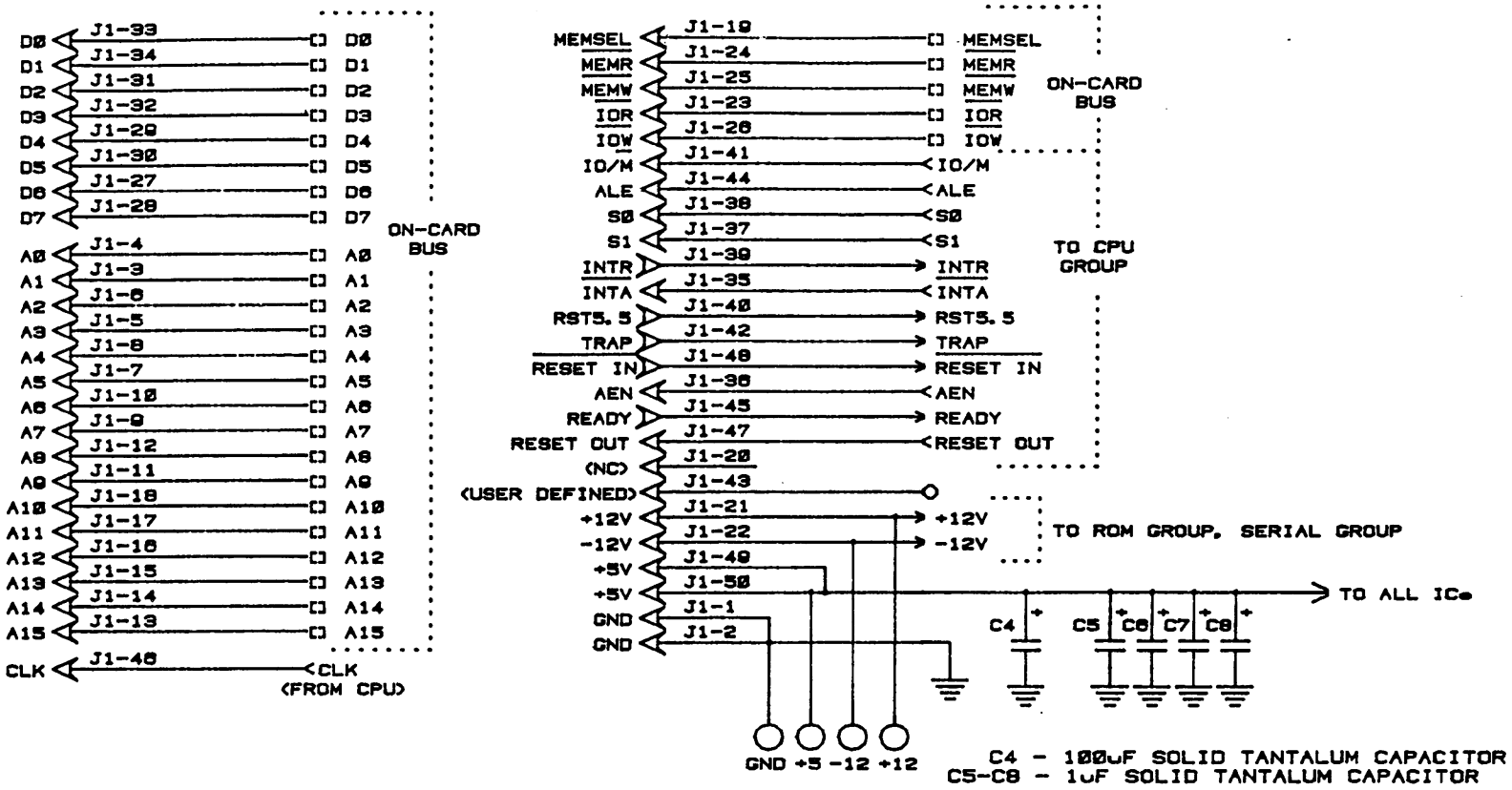


SCCS-85		
SERIAL GROUP	80.1.31	
DWNG. 6 OF 9		

RS-232 SIGNALS

DTR - DATA TERMINAL READY
RTS - REQUEST TO SEND
TxD - TRANSMIT DATA
DSR - DATA SET READY
CTS - CLEAR TO SEND
RxD - RECEIVED DATA

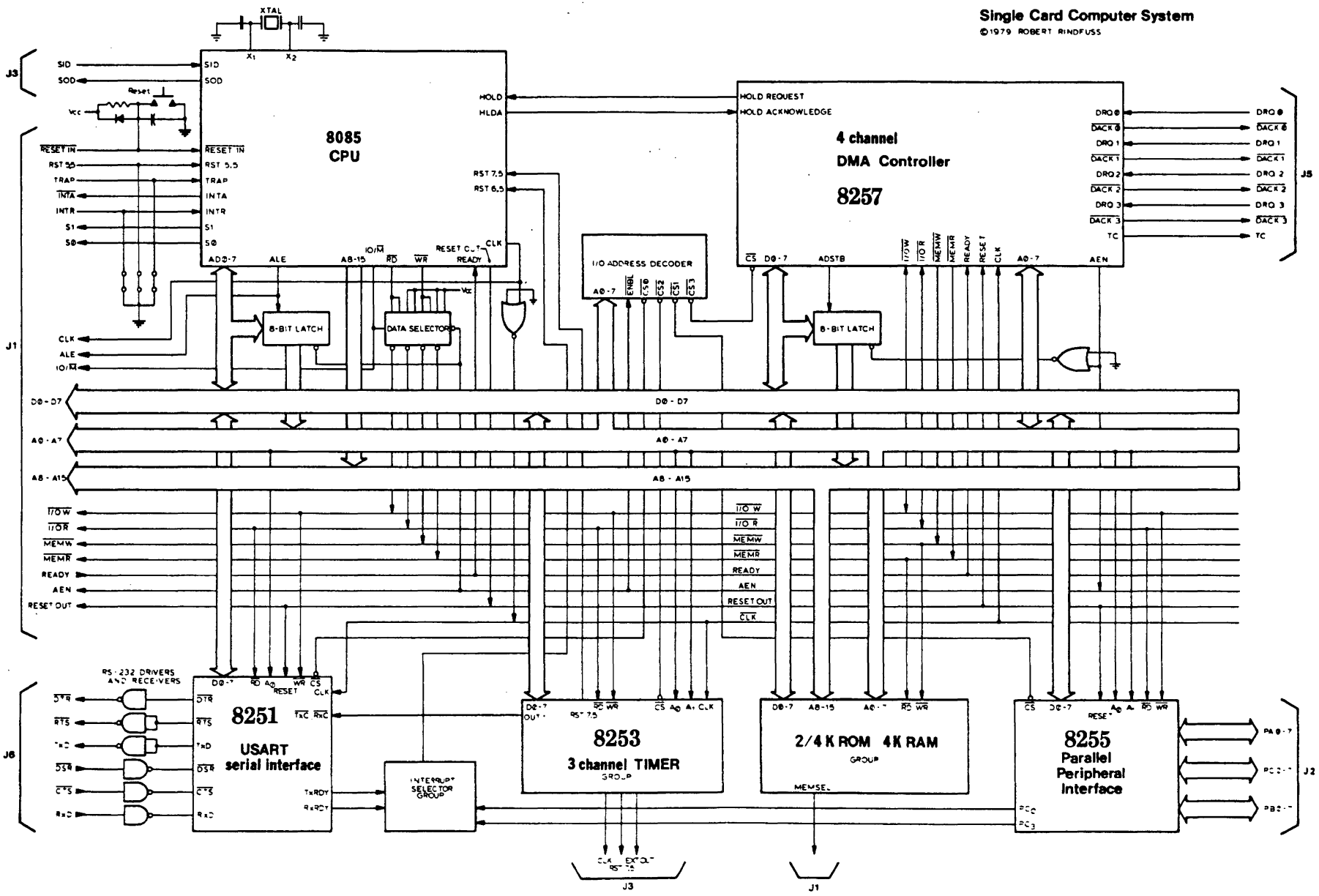

U16
8257
U15
74LS373
U18
74LS02
ON-CARD BUS
D0
D1
D2
D3
D4
D5
D6
D7
A8
A9
A10
A11
A12
A13
A14
A15
OE
LE
ADSTB
AEN
NOTE: TRACE MUST BE CUT IF DMA OPTION IS INSTALLED
A0
A1
A2
A3
A4
A5
A6
A7
DRQ0
DACK0
DRQ1
DACK1
DRQ2
DACK2
DRQ3
DACK3
TC
MARK
(NOT USED)
J5-2
J5-5
J5-1
J5-6
J5-4
J5-7
J5-3
J5-8
J5-10
J5-9
GND
I/OR
I/OW
MEMR
MEMW
IOR
IOW
MEMR
MEMW
CLK
RESET
READY
RESET OUT
CS
CS3 (FROM I/O ADDRESS DECODER)
HLDA
HLDA (FROM CPU)
HRQ
HOLD (TO CPU)
NOTE: TRACE MUST BE CUT IF DMA OPTION IS INSTALLED.
VCC
SCCS-85
DMA GROUP
80.1.26
DWNG. 7 OF 9



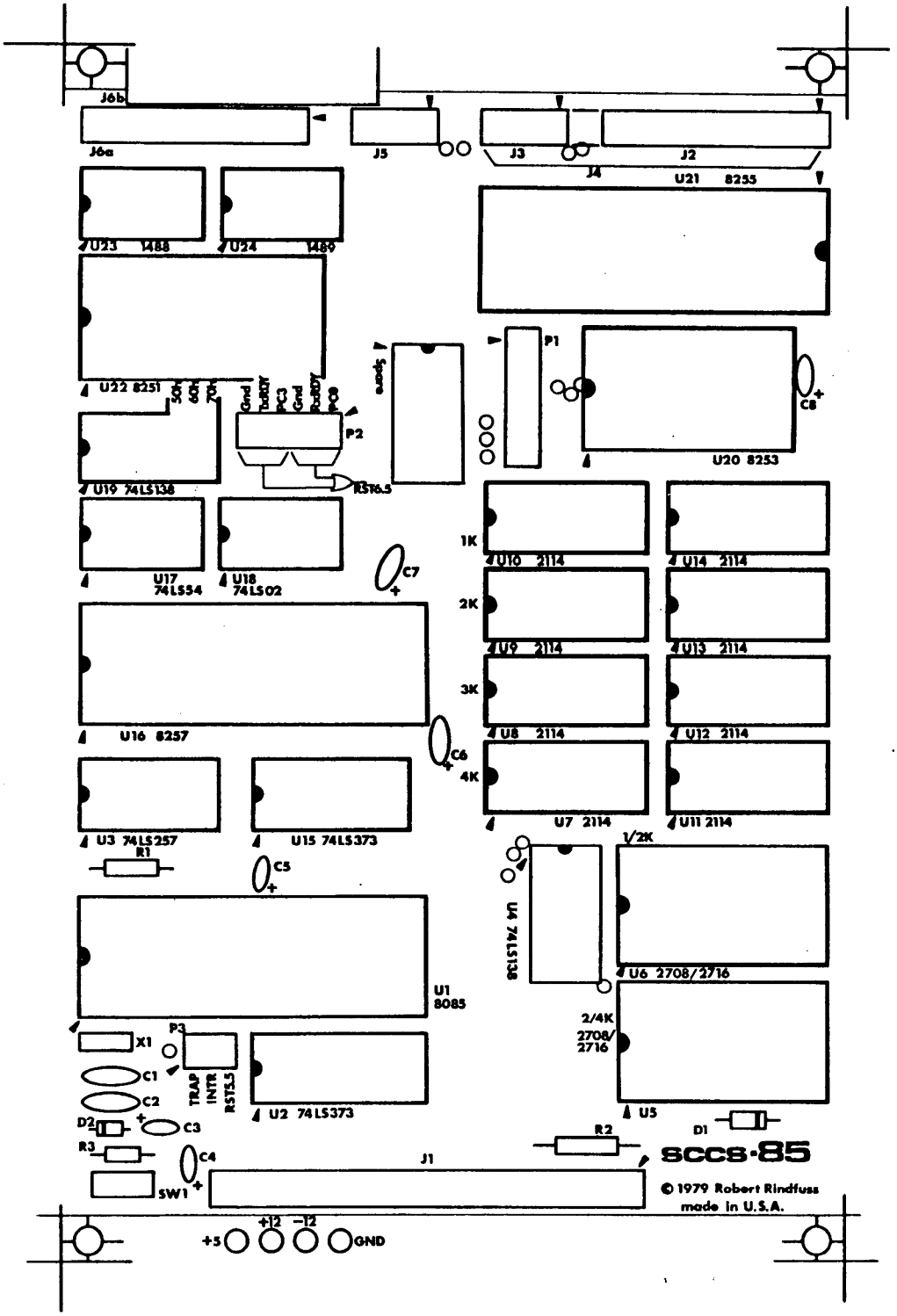
SCCS-85		
BUS CONNECTOR, POWER SUPPLY	80.2.1	
DWNG. 8 OF 9		

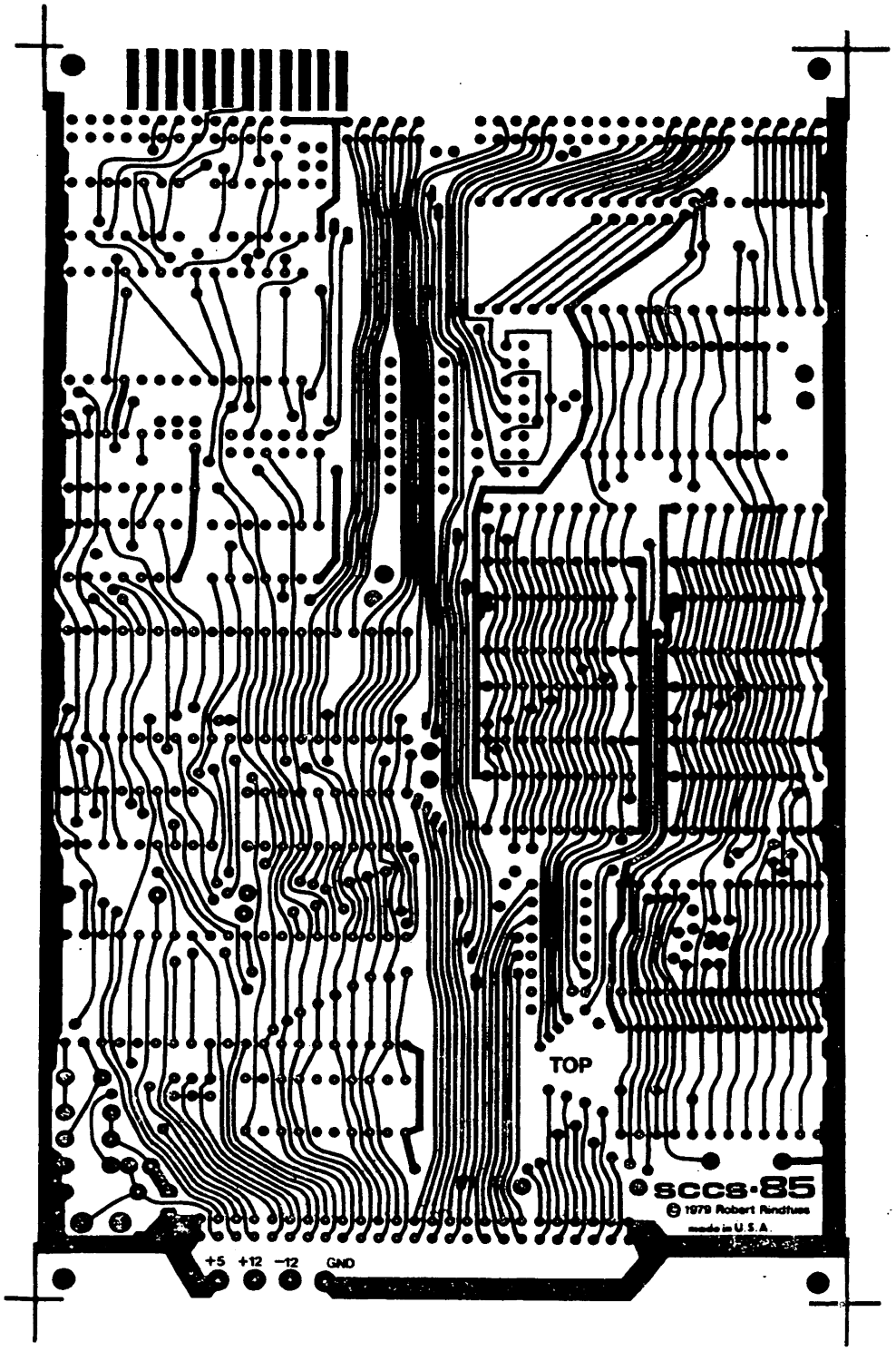
SCCS-85

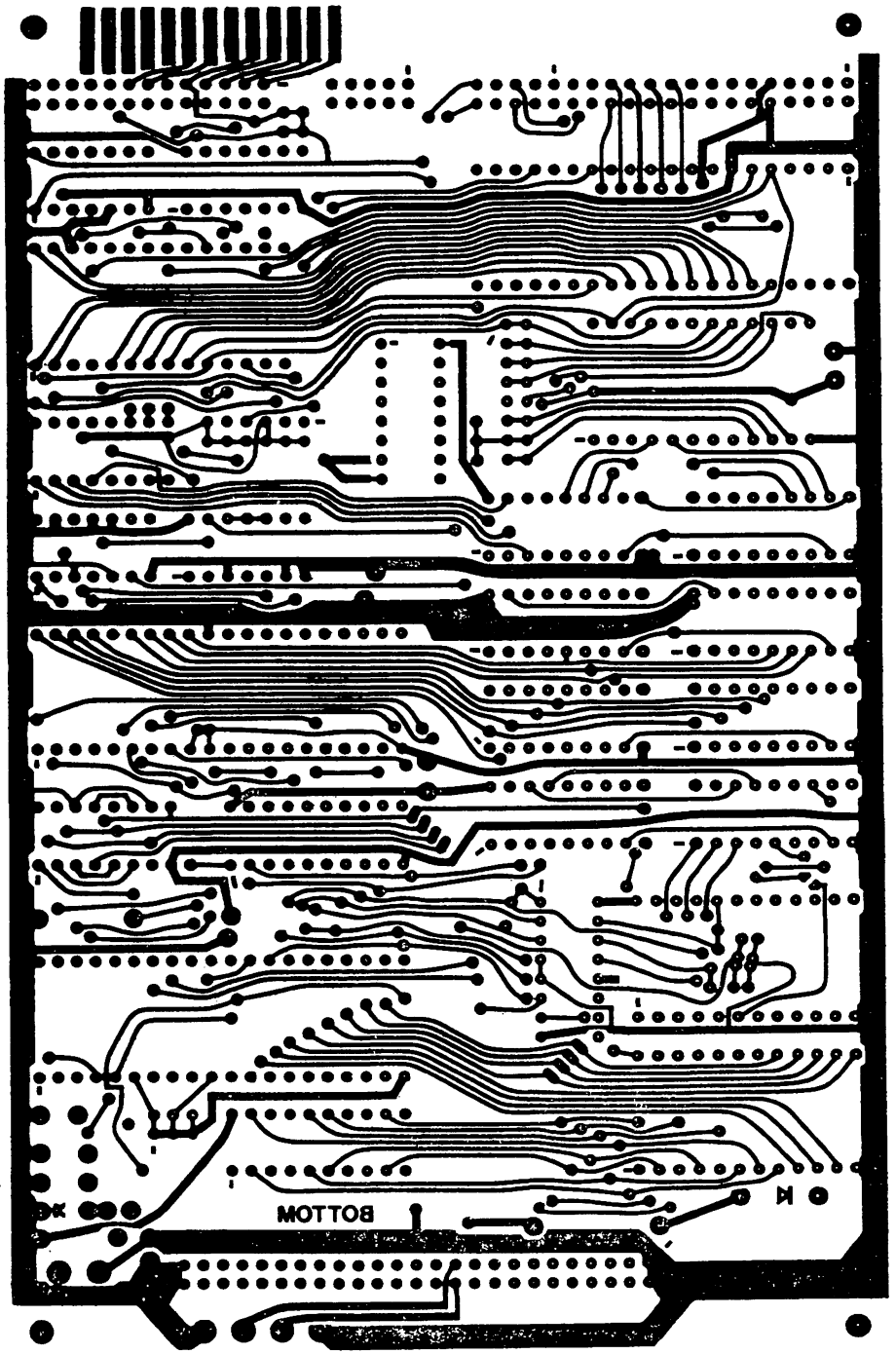
Single Card Computer System



DWNG. 9 OF 9


J6b
J6a
J5
J3
J4
J2
U21 8255
U23 1488
U24 1489
U22 8251
P1
C8
U20 8253
P2
RST6.5
U19 74LS138
U17 74LS54
U18 74LS02
C7
1K
U10 2114
U14 2114
2K
U9 2114
U13 2114
3K
U8 2114
U12 2114
4K
U7 2114
U11 2114
U16 8257
C6
U3 74LS257
U15 74LS373
R1
C5
1/2K
U4 74LS138
U6 2708/2716
U1 8085
2/4K 2708/2716
X1
P3
C1
C2
TRAP
INTR
RST5.5
U2 74LS373
U5
D2
C3
D1
R3
C4
R2
J1
SW1
SCCS-85
© 1979 Robert Rindfuss
made in U.S.A.
+5
+12
-12
GND


TOP
sccs-85
© 1979 Robert Rindfuss
made in U.S.A.
+5 +12 −12 GND


BOTTOM