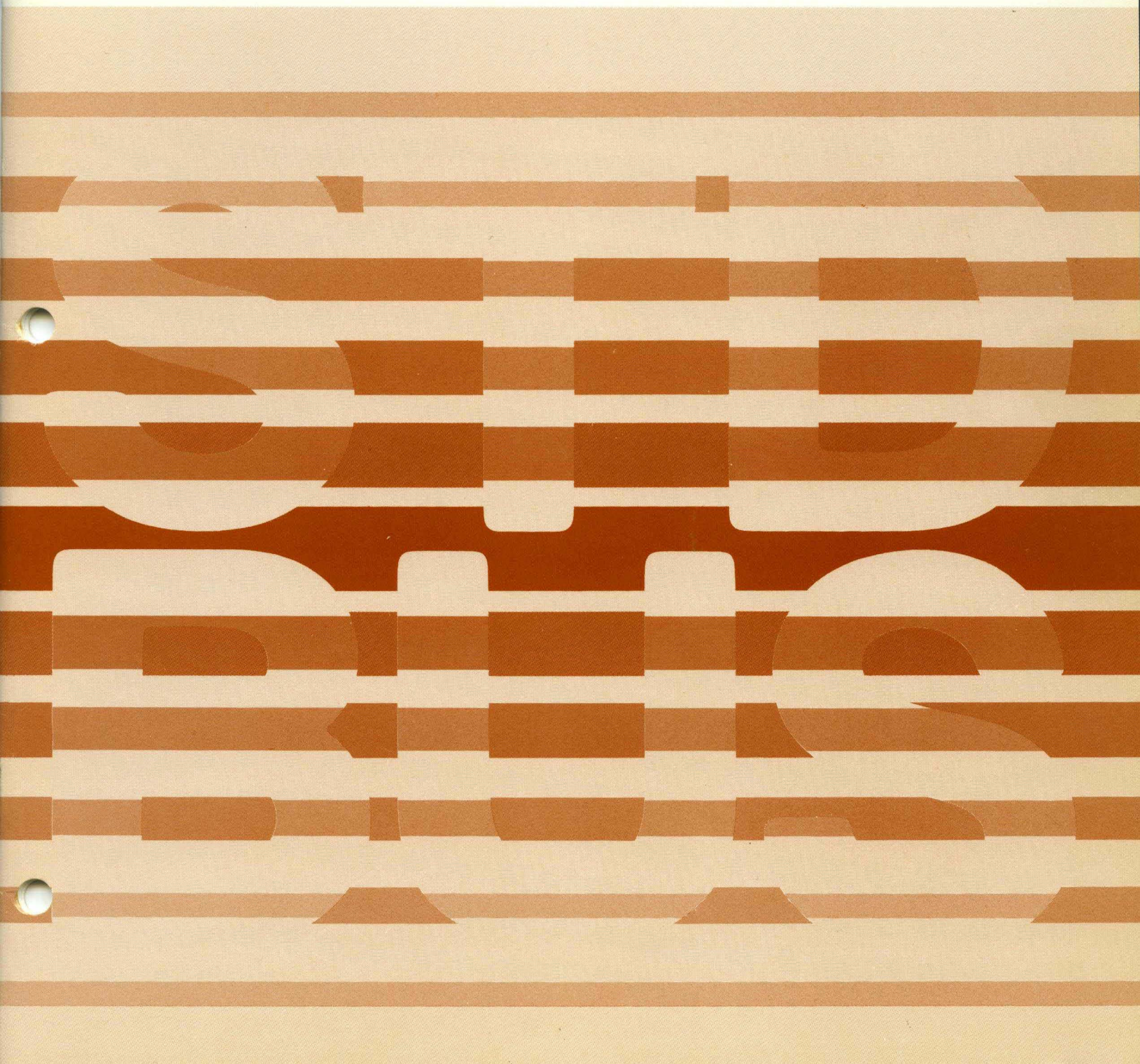
PRO-LOG
CORPORATION

STD 7000

7604
TTL I/O Card
USER'S MANUAL



7604
TTL I/O Card
USER'S MANUAL

PRELIMINARY

PRO-LOG
CORPORATION

9/81

7604 TTL I/O CARD USER'S MANUAL

TABLE OF CONTENTS

7000

7604
TTL I/O CARD

TTL INPUT/OUTPUT CARD

This card provides 8 ports of which any number can be input or output ports or output ports with readback (64 I/O lines total).

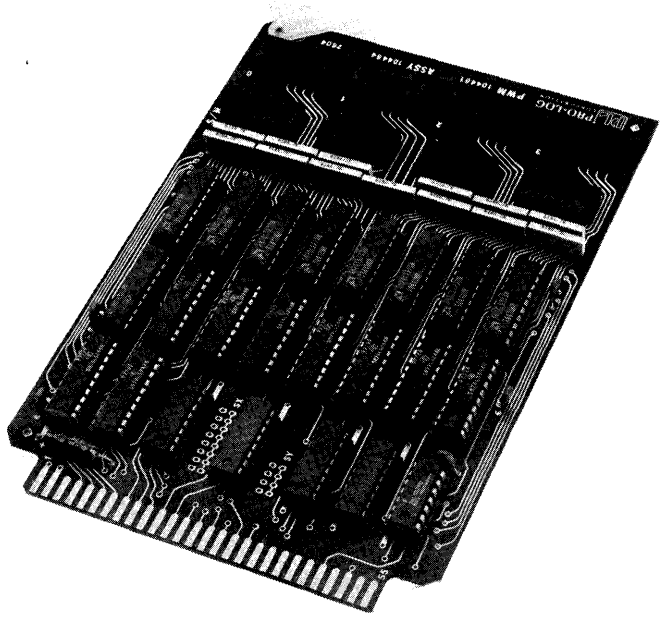
The ports are accessed at 16-pin DIP sockets on the card.

The output lines are TTL compatible with the ability to drive 16 low power Schottky TTL Loads each (4 TTL loads). A reset line is available to clear all output ports simultaneously.

The input lines are TTL compatible with an input rating of 4 low-power Schottky loads.

The ports are configured as input or output ports simply by removing the unused IC associated with that port. If the input buffer is retained, output port data may be read back into the Processor.

The 7604 decodes eight address lines with provisions for expansion and memory mapping. An on-card jumper system allows users to establish the eight consecutive port addresses occupied by the 7604.



FEATURES

- **8 Ports configurable as input or output or output with readback**
- **User selectable port address (256 port field)**
- **Outputs Drive 16 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **All IC's socketed**
- **Single +5V operation**

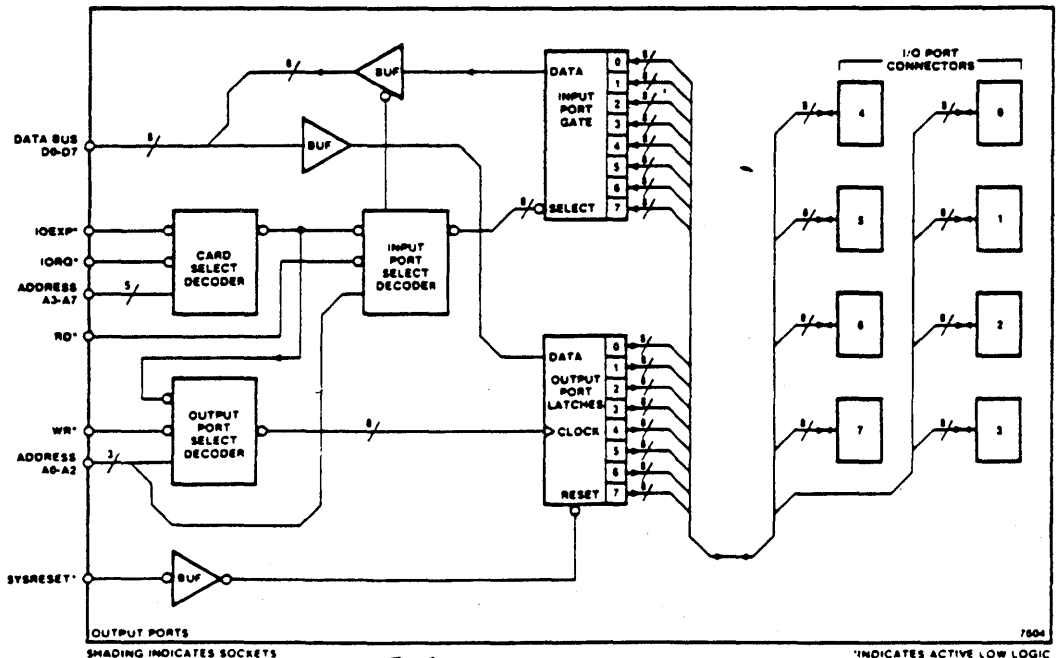


FIGURE 1

2. FUNCTIONAL

The 7604 is shipped fully populated. The card is customized (to A input and B output ports such that A + B = 8 ports) by removing the unused input buffer or output port latch according to the following table.

	OUTPUT PORTS	INPUT PORTS
PORT NO.	IC NUMBER	IC NUMBER
Port 0	U17	U9
Port 1	U19	U11
Port 2	U21	U13
Port 3	U23	U15
Port 4	U16	U8
Port 5	U18	U10
Port 6	U20	U12
Port 7	U22	U14

Leaving the input buffer in at output ports allows the Processor to read back the output port data to check for noise alteration or to use the output port as a data register.

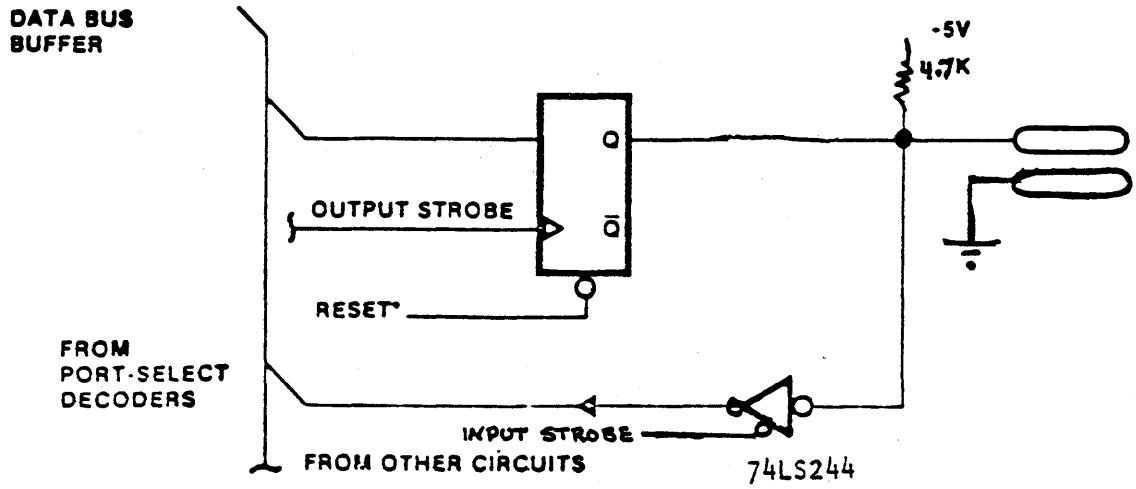
The 7604 provides 64 alternating data and ground lines. These signal lines can be up to 10 feet (3.05m) long with proper electrical considerations. When writing to an eight bit output port the data bus data is latched in the output port. The output data will remain latched in that state until it is written to with new data or the SYSRESET* signal clears the port. When reading from an 8-bit input port the state of the port lines at the time of the read is transferred to the data bus.

RESET

The SYSRESET line clears all eight output ports to zero simultaneously. On system power-up the SYSRESET signal clears the output ports.

GENERAL PURPOSE INTERFACE

The 7604 is useful as a general purpose TTL interface card. If flat cable or twisted pair discrete wire cable assemblies are used, the ground-signal-ground of the I/O connectors minimizes crosstalk between inter-system signal lines in electrically noisy environments.



TYPICAL I/O CIRCUIT

FIGURE 2

3. **Card Address Mapping**

The 7604 Card is selected by a decoded combination of address lines A3-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U3 and U4 (see diagram). The 7604 is shipped mapped at Hex Port Address 00. To map the 7604 anywhere in the hexadecimal address range 00 to FF, change the decoder outputs connected to SX and SY.

Port Addresses

Address lines A0, A1 and A2 select one of eight Port addresses. One input port and one output port reside at each address. The RD* and WR* inputs control the input gating and output latch functions.

4. ADDRESS DECODER OPERATION

Refer to the schematic, Document #104483.

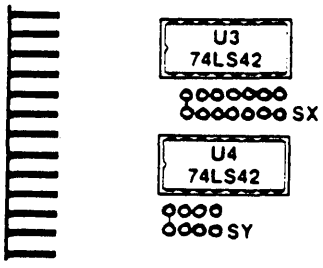
The 7605 uses four cascaded 74LS42 decoders (U3, U4, U5 and U6) to decode address lines A0-A7. These decoders are enabled only when IORQ* and IOEXP* are active. Address lines A0, A1, A2 and the WR* signal are used to gate the select strobes from U6 that control the output ports. Address lines A0, A1, A2 and the RD* signal are used to gate the select strobes from U5 that control the input ports.

CHANGING THE 7604's PORT ADDRESS

Refer to the Assembly diagram, Document #104484.

Locate decoders U3 and U4 (74LS42) adjacent to the STD BUS edge connector. Each decoder device has a dual row of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U3 and U4.

The decoder jumper pads numbered as shown in Figure 3 are adjacent to the decoder chips on the 7604. Also shown are the jumpers (at X0 and Y0) which produce hexadecimal port addresses 00, 01, 02 thru 07, the selections made when the card is shipped.



Card Address Selection

FIGURE 3

The I/O address mapping and jumper selection table for eight addresses per card shows where to place jumper straps to obtain any eight sequential port addresses in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the vertical axis, and the least significant hex digit on the horizontal axis. For example, port addresses 00, 01, 02 thru 07 are obtained by connecting jumpers at X0 and Y0.

The only restriction that applies in address selection for the 7604 is that the lower of the eight port addresses (00 as shipped) must occur only at every eighth possible address; for example, the sequence 01, 02, 03 thru 08 is not allowed by the decoder.

The pad matrices adjacent to U3 and U4 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0								X0 Y1								X AND Y
1	X0 Y2								X0 Y3								
2	X1 Y0								X1 Y1								
3	X1 Y2								X1 Y3								
4	X2 Y0								X2 Y1								
5	X2 Y2								X2 Y3								
6	X3 Y0								X3 Y1								
7	X3 Y2								X3 Y3								
8	X4 Y0								X4 Y1								
9	X4 Y2								X4 Y3								
A	X5 Y0								X5 Y1								
B	X5 Y2								X5 Y3								
C	X6 Y0								X6 Y1								
D	X6 Y2								X6 Y3								
E	X7 Y0								X7 Y1								
F	X7 Y2								X7 Y3								

I/O Address Mapping And Jumper Selection Tables For 8 Addresses Per Card

FIGURE 4

5. 7604 CARD ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity ①	5		95	0	95	%RH

① Non-condensing

6. ELECTRICAL SPECIFICATIONS

7604 GENERAL PURPOSE TTL I/O CARD ELECTRICAL TEST SPECIFICATION

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C

USER WORST CASE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

For Input Port

PARAMETER ⚠1		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.7	V
	Hysteresis (VT+ — VT-)	0.2	0.4		V
for Input current each port line represents 4 LSTTL loads					

For Output Port

PARAMETER ⚠2		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage ⚠3	2.7	3.5		V
V_{OL}	Low level output voltage ⚠4		0.35	0.5	V
Each output can drive 16 LSTTL loads *					

* 1 LSTTL load - 0.4mA

STD BUS ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

PARAMETER		MIN	TYP	MAX	UNITS
I_{CC}	SUPPLY CURRENT		450	700	mA
	STD BUS INPUT LOAD	See Figure 6			
	STD BUS OUTPUT DRIVE	See Figure 6			

⚠1 Input characteristics with output chip removed.

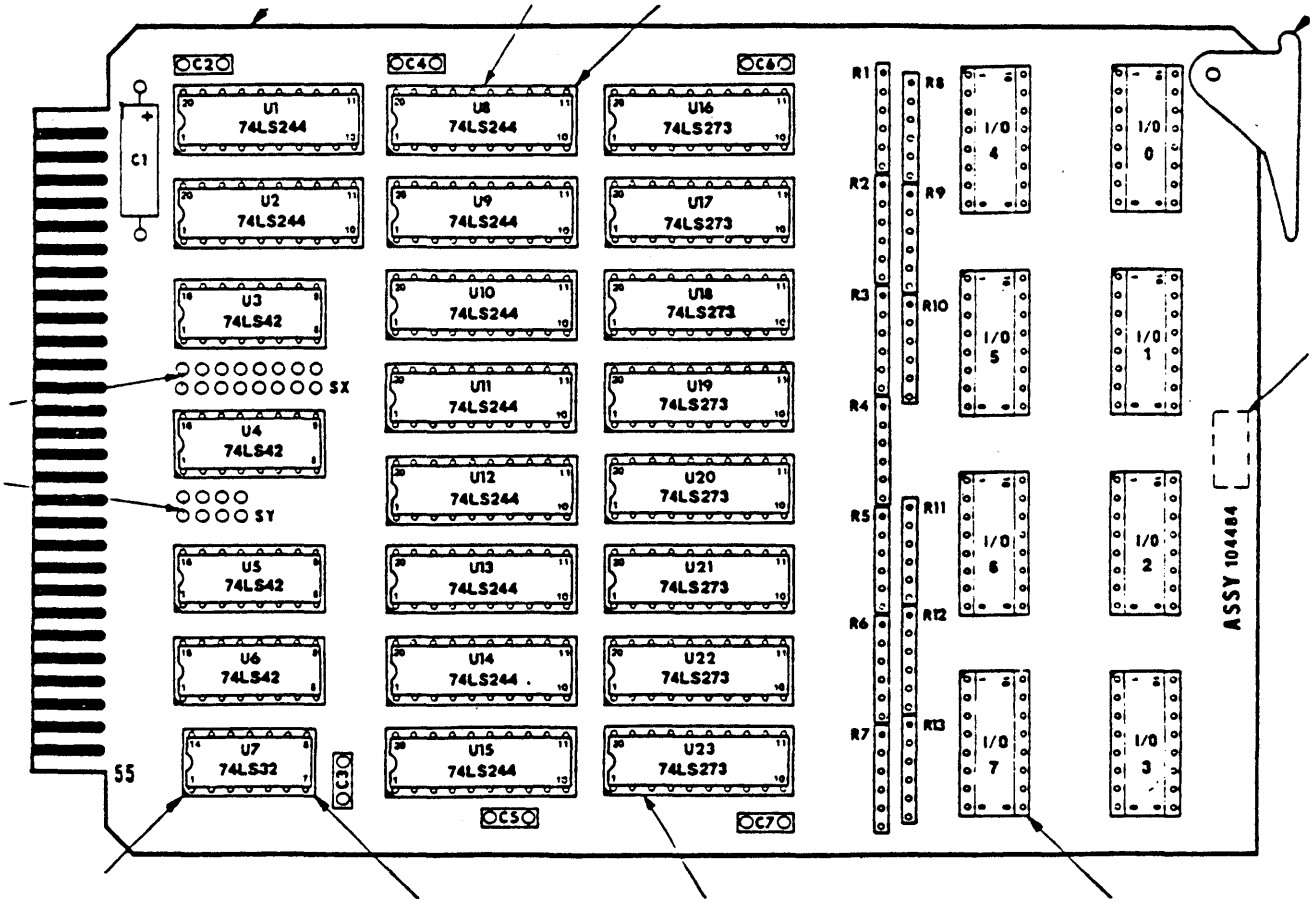
⚠2 Output characteristics with input chip installed.

⚠3 V_{CC} = 4.5V I_{OL} = 8mA

⚠4 V_{CC} = 4.5V I_{OH} = 400μA

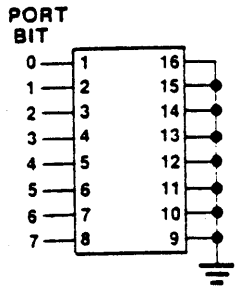
7. MECHANICAL

. Meets all STD BUS general mechanical specifications
. May require one additional card slot width for ribbon cable access to ports (connector dependent).
. Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley Catalog No. 609-M165H or equivalent.



7604 ASSEMBLY

FIGURE 5



Input/Output Port Socket

STD/7604 EDGE CONNECTOR PIN LIST								
PIN NUMBER					PIN NUMBER			
OUTPUT (DRIVE)							OUTPUT (DRIVE)	
INPUT (LOADING)							INPUT (LOADING)	
MNEMONIC								MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS	
GROUND	GND		4	3		GND	GROUND	
-5V			6	5			-5V	
D7	1	60	8	7	60	1	D3	
D6	1	60	10	9	60	1	D2	
D5	1	60	12	11	60	1	D1	
D4	1	60	14	13	60	1	D0	
A15			16	15		1	A7	
A14			18	17		1	A6	
A13			20	19		1	A5	
A12			22	21		1	A4	
A11			24	23		1	A3	
A10			26	25		2	A2	
A9			28	27		2	A1	
A8			30	29		2	A0	
RD*	1		32	31		1	WR*	
MEMRQ*			34	33		1	IORQ*	
MEMEX*			36	35		1	IOEXP*	
MCSYNC*			38	37			REFRESH*	
STATUS 0*			40	39			STATUS 1*	
BUSRQ*			42	41			BUSAK*	
INTRQ*			44	43			INTAK*	
NMIRQ*			46	45			WAITRQ*	
PBRESET*			48	47		1	SYSRESET*	
CNTRL*			50	49			CLOCK*	
PC1	IN		52	51	OUT		PC0	
AUX GND			54	53			AUX GND	
AUX -V			56	55			AUX +V	

*Designates Active Low Level Logic

Edge Connector Pin List

FIGURE 6

- Address, Data and Control Busses meet all STD BUS general electrical specifications except A0, A1 and A2 which are 2 LSTTL loads each.

8. 7604 OPERATING SUBROUTINE MODULES

This section provides flow diagrams and subroutines to operate your 7604 card. These may be used intact, or used as models to construct subroutines for a specific application.

The subroutines are written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7604 port addresses used are the address jumper selections made when the 7604 is shipped.

To use these subroutines in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility.

The flow diagrams presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7604 operation without reference to a particular microprocessor.

The (check bits) subroutine will compare the present input port status with the port status from the last time that the port was read.

To use the routine the HL pointer must point to a place in memory where port status is stored. Also, the port must be read into the accumulator before calling the routine.

Upon return from the routine the location that the HL pointer was previously set will contain new port status. Plus the next four locations will contain change status.

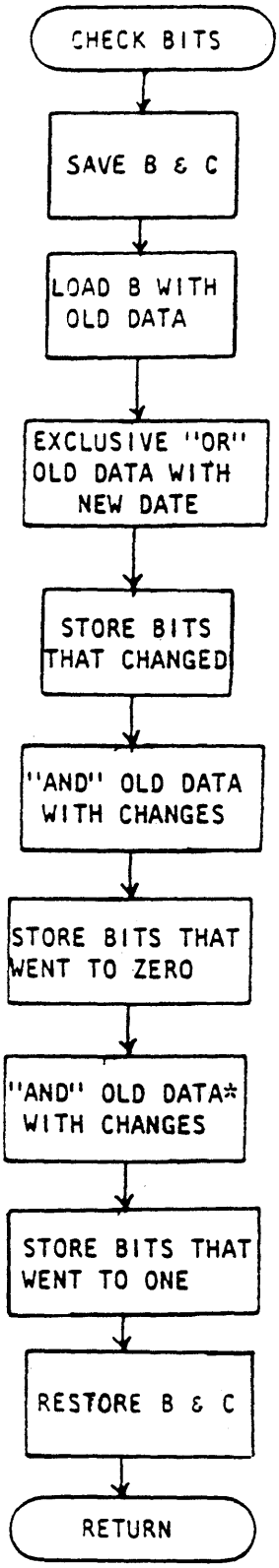
Uses Registers A, H and L

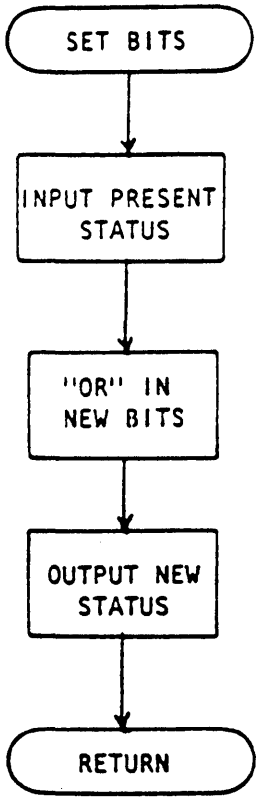
M	XX New Data	←Location HL was set to
M+1	XX Old Data	
M+2	XX Changes	
M+3	XX Bits to Zero	
M+4	XX Bits to One	

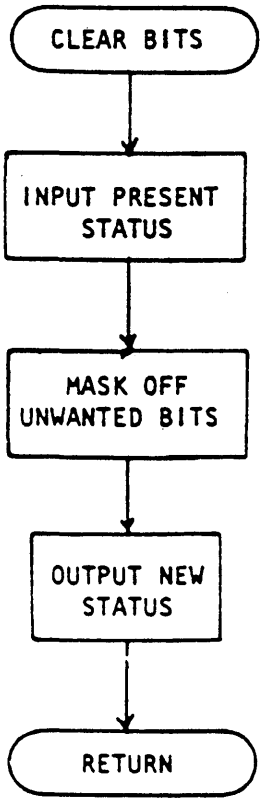
Memory after Return

The (set bit) routine can set a bit or bits on an output port. To use the routine load the accumulator with the bits that should be changed.
(Input chip must be installed)

The (clear bit) routine can clear a bit or bits on an output port. To use the routine load the accumulator with the bits that should be changed.
(Input chip must be installed)


CHECK BITS
SAVE B & C
LOAD B WITH OLD DATA
EXCLUSIVE "OR" OLD DATA WITH NEW DATE
STORE BITS THAT CHANGED
"AND" OLD DATA WITH CHANGES
STORE BITS THAT WENT TO ZERO
"AND" OLD DATA* WITH CHANGES
STORE BITS THAT WENT TO ONE
RESTORE B & C
RETURN


SET BITS
INPUT PRESENT STATUS
"OR" IN NEW BITS
OUTPUT NEW STATUS
RETURN


CLEAR BITS
INPUT PRESENT STATUS
MASK OFF UNWANTED BITS
OUTPUT NEW STATUS
RETURN

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
	0			LDPI	HL	← Set Pointer
	1			—	XX	
	2			—	XX	
	3			IPA		← Input New Data
	4			—	XX	
	5	C5	(Check Bits)	PSP	BC	← Save Contence of Regs B and C
	6	46		LDB	M(HL)	← Put OLD Data in B
	7	77		STAN	(HL)	← Store New Data
	8	23		ICP	(HL)	← Store OLD Data in Next Location
	9	70		STBN	(HL)	
	A	A8		XRA	B	← OLD ⊕ NEW = CHANGES
	B	23		ICP	HL	← Store CHANGES in Next Location
	C	77		STAN	(HL)	
	D	4F		LDC	A	← Put Changes in C
	E	78		LDA	B	← Put OLD DATA IN A
	F	A1		ANA	C	← OLD • CHANGES = Bits to Zero
	0	23		ICP	HL	← Store Bits to Zero in Next Location
	1	77		STAN	(HL)	
	2	78		LDA	B	← Compliment OLD DATA
	3	2F		CMA		
	4	A1		ANA	C	← $\overline{OLD}$ • CHANGES = Bits to ONE
	5	23		ICP	HL	← Store Bits to ONE in Next Location
	6	77		STAN	(HL)	
	7	C1		PLP	BC	← Restore Contence of Reg B and C
	8	C9		RTS	UN	← Return from Subroutine
	9					USES REGS A and Pointer HL
	A					
	B					
	C					
	D					
	E					
	F					

00001111 OLD
⊕ 01010101 NEW
01011010 CHANGES

00001111 OLD
• 01011010 CHANGES
00001010 Bits to Zero

11110000 $\overline{OLD}$
• 01011010 CHANGES
01010000 Bits to ONE

RAM MEMORY AFTER Return (USES 5 locations)	XX NEW DATA	M
	XX OLD DATA	M+1
	XX CHANGES	M+2
	XX Bits to Zero	M+3
	XX Bits to ONE	M+4

100665 A 5A 13 EF 10

100001 2/77

PRO-LOG CORPORATION

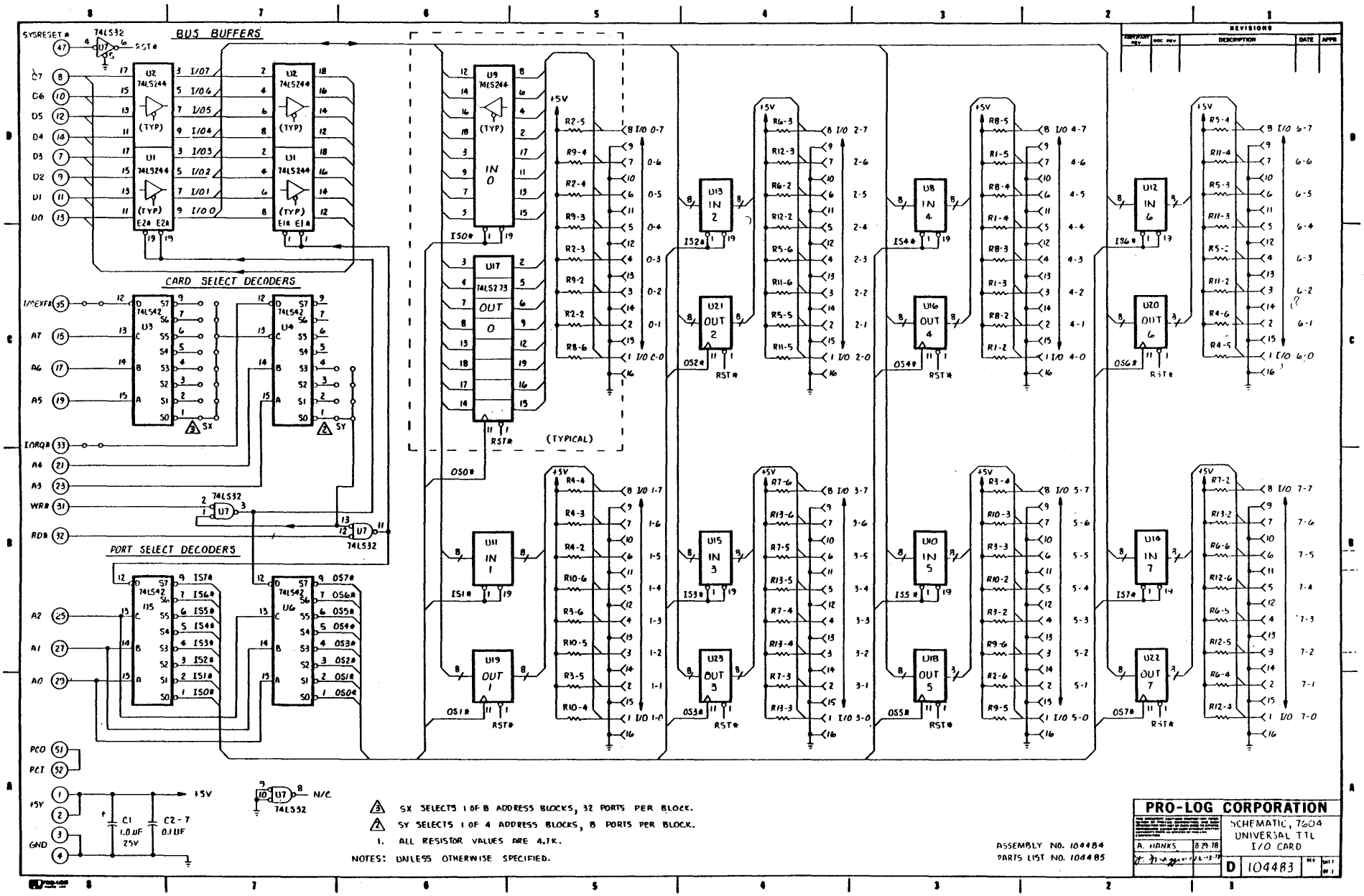
PROGRAM ASSEMBLY FORM

TITLE 7604 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	0			LDAI		Load A with Bit(s) to be set
	1			-	XX	
	2	47	(Set BIT)	LDB	A	← Save Bits in B
	3	DB		IPA		Input Port Status
	4	XX		-	XX	
	5	B0		ORA	B	← OR in New Bits
	6	D3		OPA		Output New Port Status
	7	XX		-	XX	
	8	C9		RTS		
	9					
	A					
	B					
	C					
	D					
	E					
	F					
	0			LDAI		Load A with Bit(s) to be cleared
	1			-	XX	
	2	2F	(clear Bit)	CMA		Compliment Bits and Put in B
	3	47		LDB	A	
	4	DB		IPA		Input Port Status
	5	XX		-	XX	
	6	A0		ANA	B	← Mask off Bits
	7	D3		OPA		Output New Port Status
	8	XX		-	XX	
	9	C9		RTS		
	A					
	B					
	C					
	D					
	E					
	F					

106665 A

5/14 6/16



3 SX SELECTS 1 OF 8 ADDRESS BLOCKS, 32 PORTS PER BLOCK.

4 SY SELECTS 1 OF 4 ADDRESS BLOCKS, 8 PORTS PER BLOCK.

1. ALL RESISTOR VALUES ARE 4.7K.

NOTES: UNLESS OTHERWISE SPECIFIED.

ASSEMBLY NO. 104484
PARTS LIST NO. 104485

REVISIONS				
ASSY/PART REV	DOC REV	DESCRIPTION	DATE	APPR
	A	ADDED ITEM 25 ADDED NOTES ... ADDED TABLE I PER ... PCN 162	[illegible]	[illegible]
	B	REVISED PER PCN 0888	[illegible]	[illegible]

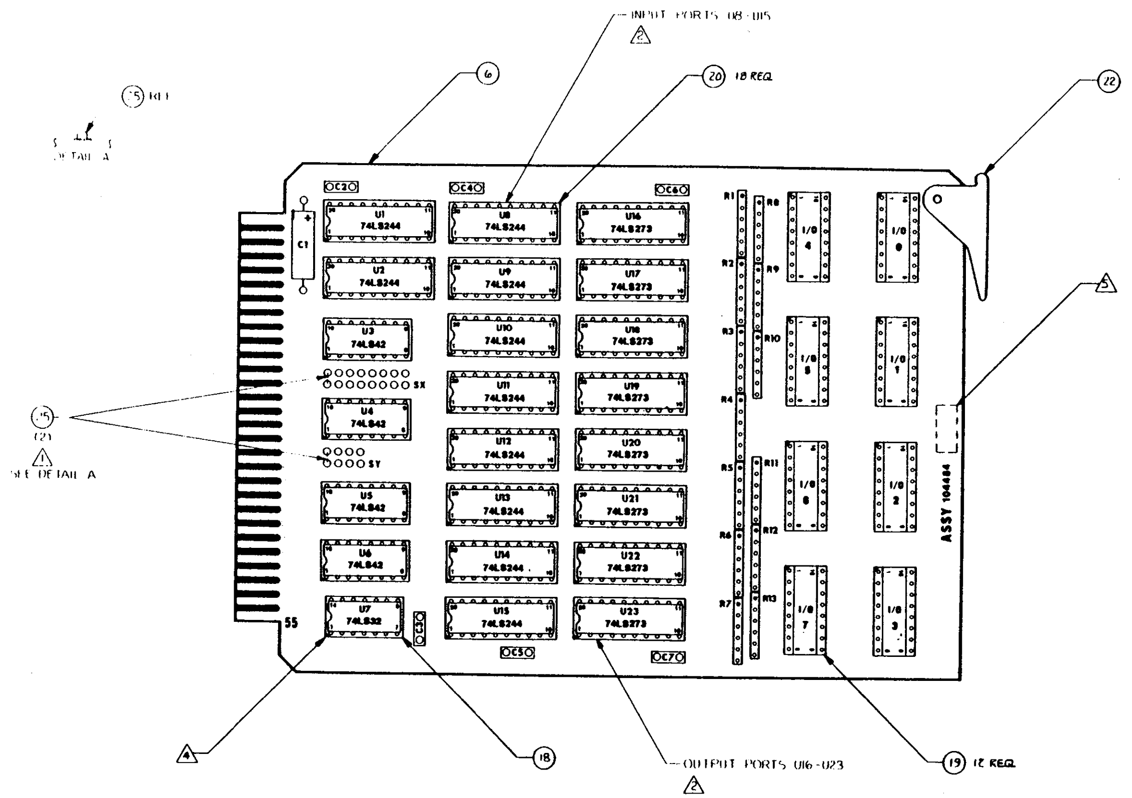


TABLE I	
TO USE INPUT PORTS NO.	REMOVE OUTPUT LATCH 74LS273
0	U17
1	U19
2	U21
3	U23
4	U16
5	U18
6	U20
7	U22

6 REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND MAY NOT APPEAR ON ACTUAL PART

5 IDENTIFY WITH ASSY REV LETTER USING RUBBER STAMP

4 DENOTES PIN NO. 1 OF IC'S (TYP)

3 BOARD TO CONFORM WITH ASSY PROCEDURES AS1004

2 TO CONFIGURE AS INPUT PORTS REMOVE ICs PER TABLE I. WHEN USED AS AN OUTPUT 74LS244s MAY BE LEFT IN.

1 MAPPED TO PORT 00.

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC NO. 104483
PARTS LIST NO. 104485

ITEM	DESCRIPTION	REF. DESIGNATION
11	4.7K NETWORK	R1 - R13
10		
9	0.1 µF, 50V	C2 - C7
8	1.0 µF, 25V	C1
7		
6	104482	PWB

PRO-LOG CORPORATION

ASSEMBLY, 7604 UNIVERSAL TTL I/O CARD

A. HANKS	9-19-78
[illegible signature]	12-13-78

SIZE	DWG NO.	REV	SHEET
D	104484	B	SHT 1 OF 1

USER'S MANUAL

2411 Garden Road
Monterey, California 93940
Telephone: (408) 372-4593
TWX: 910-360-7082

106665B 600 9/81