OB68K/VME1

VME/68000 SINGLE BOARD COMPUTER

REFERENCE MANUAL

OMNIBYTE™

245 WEST ROOSEVELT ROAD • WEST CHICAGO, ILLINOIS 60185

FAX (708) 231-7042 • PHONE (708) 231-6880

A Look At Today . . . A Vision of Tomorrow.

MAY, 1990
REVISION E1

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OMNIBYTE CORPORATION * 245 West Roosevelt Road * West Chicago, Illinois 60185

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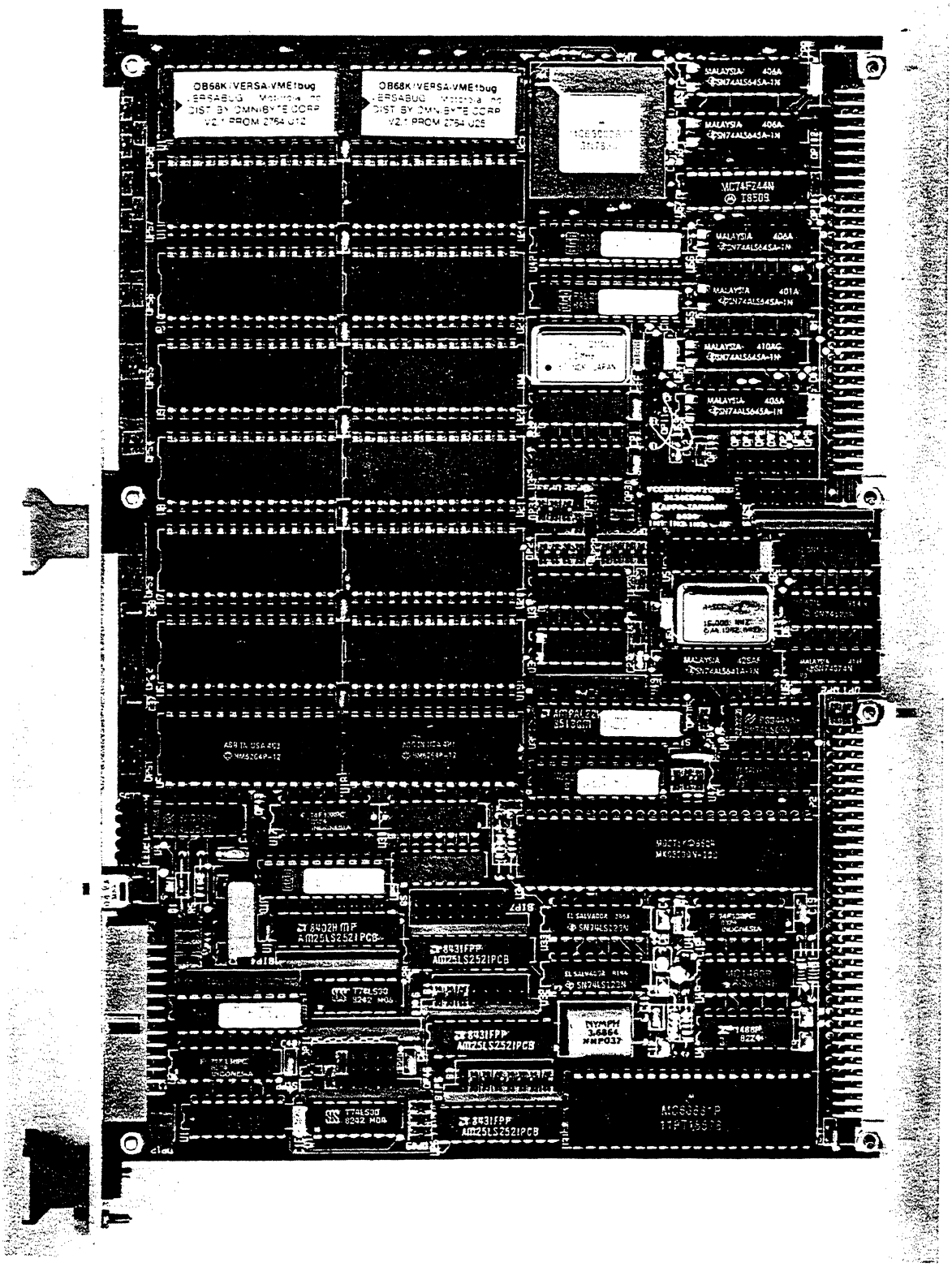
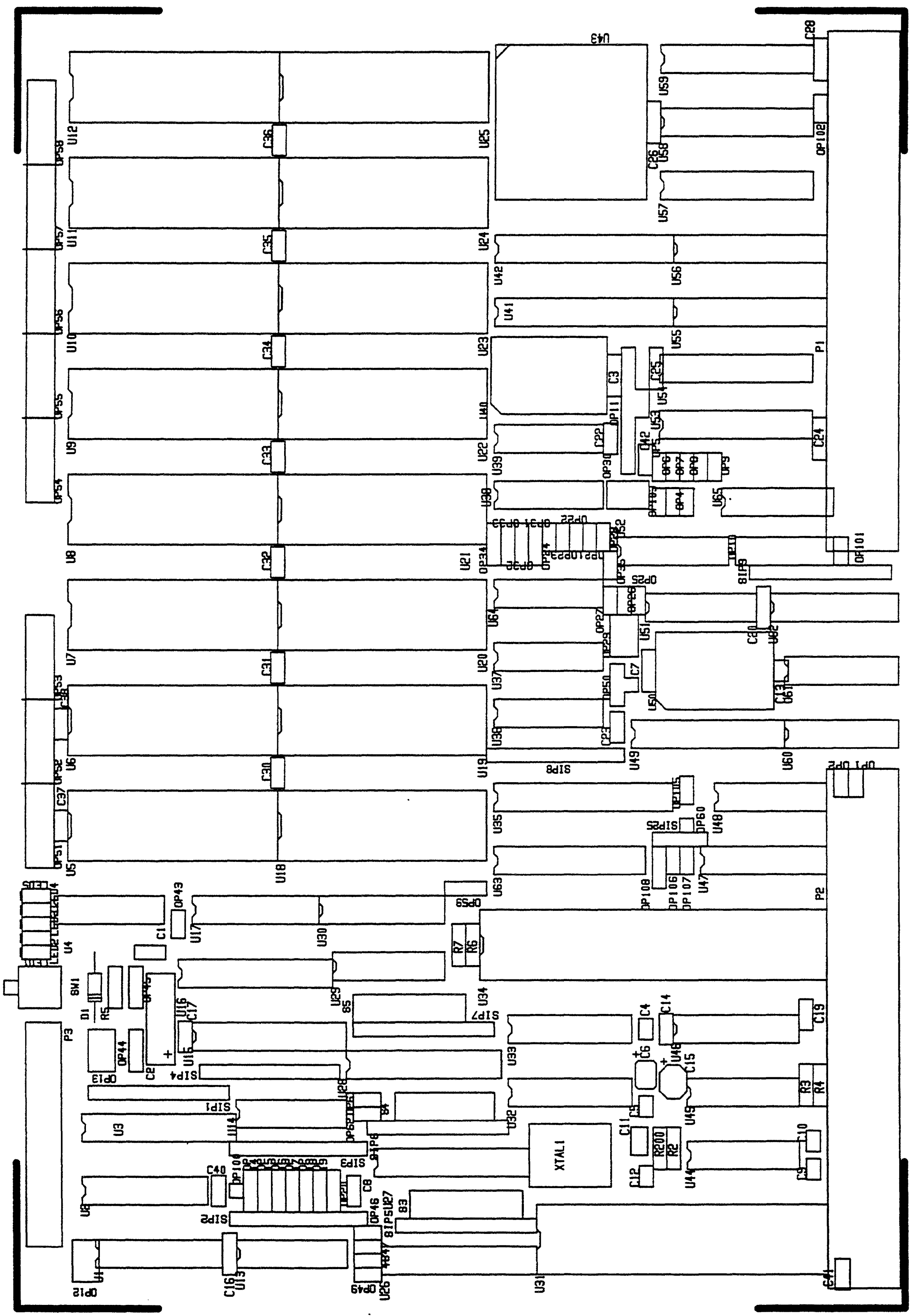


PHOTOGRAPH OF THE OB68K/VME1
FIGURE 1.0



OB68K/VME1 PARTS LOCATION DIAGRAM
FIGURE 1.1

1.0 INTRODUCTION/INSTALLATION

1.1 Introduction

This chapter provides the unpacking, inspection and configuration instructions for the OB68K/VME1 Single Board Computer.

1.2 Unpacking Instructions

"NOTE"

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT, REQUEST THAT CARRIER'S AGENT BE PRESENT WHILE THE ITEMS ARE BEING UNPACKED AND INSPECTED.

Unpack the OB68K/VME1 Single Board Computer from its shipping carton. Save the packing material for storing and reshipping the items in case this becomes necessary.

1.3 Inspection

The OB68K/VME1 Single Board Computer should be inspected upon receipt for broken, damaged, or missing parts, and for physical damage to the printed circuit board or connectors.

1.4 Factory Standard Configuration

The OB68K/VME1 Single Board Computer may be used in several configurations. Prior to inserting the OB68K/VME1 in a system, care should be taken to install the proper jumper options where necessary for your system configuration. Refer to the Figure 4.0 for physical locations of these jumpers on the OB68K/VME1. Included below is standard configuration information.

The OB68K/VME1 is shipped in a configuration that allows it to be operated as the system controller in Slot 1 of a standard VMEbus chassis. Factory standard jumper configurations are indicated by dashed lines on the electrical schematic diagrams shown in Section 10. The function of each jumper group is described in detail in Section 4.

The OB68K/VME1 is configured at the factory to operate in the following way:

a) Bus Controller Functions

The System Clock (SYSCLK) and SYSRESET line are driven by this board. On-board power-on reset is enabled and the bus error jumper is installed so that bus error exception processing

will be executed, if a bus error is encountered. The BERR watchdog timer is connected to the bus. All four bus arbitration levels are enabled and this computer board uses level 3, the highest priority.

b) Interrupts

No interrupts are connected.

c) On-Board Memory

The OB68K/VME1 is configured at the factory to use 8K byte RAM chips and 16K byte PROM chips. The base address of the RAM and ROM are $000000 and $F80000, respectively. One hundred and twelve Kbytes of RAM space extends from $000000 through $1BFFFF, and 64K bytes of ROM space begins at $F80000 and ends at $F9FFFF. The RAM DTACK is preset at 160nS appropriate for 150nS RAM chips, while the ROM DTACK is preset at 320nS appropriate for 300nS ROM chips.

d) I/O Addressing

The 64K byte block of physical address from $FF0000 through $FFFFFF is decoded for I/O address space. On-board I/O facilities occupy the upper 256 bytes of this space ($FFFF00-$FFFFFF) and the remainder ($FF0000-$FFFEFF) defaults to off-board I/O space that is accessed from the VMEbus as a short I/O access (Address Modifier 4 low).

e) Serial I/O Ports

Both On-Board serial I/O ports are configured to drive RS232C terminals. Two handshake lines are provided for each port; the RTS output and the CTS input.

Please note that the above is the configuration of the OB68K/VME1 as shipped from the factory and it does not preclude setting up the board in a different configuration, if desired. Factory standard configuration is compatible with Omnibyte's optional PROM-based terminal monitor/debugger program that provides the functionality of Motorola's VERSAbug program.

JUMPER GROUP	CONFIGURATION	FUNCTION
OP1	INSTALLED	OB68K/VME1 Drives SYSRESET
OP2	INSTALLED	Bus Error (BERR) to 68000 Enabled
OP3-9	REMOVED	No Interrupts Connected
OP10	REMOVED	No Onboard Interrupts Connected
OP11	1-10, 2-8	RAM/ROM DTACK, 160 nS RAM; 320 nS ROM
OP12	1-4,2-5,3-6	Onboard IACK Priority 1-PIACK,2-TIACK,3-IACKN
OP13	1-4,2-5,3-6	Onboard IRQ Priority 1-PIRQ, 2-TIRQ, 3-INTRN
OP14-20	REMOVED	No Interrupts Connected
OP21-24	INSTALLED	Bus Grant Lines Enabled (SYSTEM CONTROLLER)
OP25-28	INSTALLED	Bus Request Lines Enabled (SYSTEM CONTROLLER)
OP29	3-6	Bus Request Level 3 for this Board
OP30	4-6	Bus Grant Level 3 for this Board
OP31	1-2	BG3OUT Enabled
OP32-34	2-3	BG0OUT,BG1OUT,BG2OUT Disabled
OP35	REMOVED	Release On Request (ROR) Enabled
OP43	REMOVED	8K Byte RAM Parts
OP44	1-2	27128 PROM Parts
OP45	2-3	27128 PROM Parts
OP46-48	INSTALLED	128K Byte ROM Block Selected
OP49	REMOVED	128K Byte RAM Block Selected
OP50	1-2	128K Byte RAM Block Selected
OP51-57	7-8, 11-12	RAM Pair 0 to 6 Set for 8K Type Static RAMS
OP58	8-9, 4-10 6-12	ROM Pair 0 Set for 27128 Type EPROMS
OP59	2-3	Push Button/Power On Circuitry Drives Reset
OP60	REMOVED	68230 PC4
OP61	INSTALLED	128K Byte RAM Block Selected
OP62	INSTALLED	128K Byte RAM Block Selected
OP100	REMOVED	On-Board BVIACK
OP101	INSTALLED	SYSCLK Driven by OB68K/VME1
OP102	INSTALLED	BCLR TO VMEbus Driven by OB68K/VME1
OP103	INSTALLED	BUS ERROR from VMEbus Enabled
OP105	REMOVED	Round Robin Arbitration Enabled
OP106	INSTALLED	OB68K/VME1 Drives BBUSY
OP107	INSTALLED	Arbiter Reset by SYSRESET
OP108	2-3	Factory Set
S3	See Figure 4.8	RAM Base Address = $00
S4	See Figure 4.8	ROM Base Address = $F8 (LS-->MS)
S5	ALL REMOVED	I/O Base Address = $FF

FACTORY STANDARD OPTION CONFIGURATION
TABLE 1.4

2.0 OVERVIEW OF THE COMPUTER BOARD

This section describes the major features of the OB68K/VME1. A block diagram of this single board computer is shown in Figure 2.0.

2.1 Summary of Features

The OB68K/VME1 computer board provides the following features:

a. MC68000 16/32 bit processor.
b. Two asynchronous RS-232C serial ports (68681).
c. VMEbus compatible (REVISION C.1).
d. Full four level bus arbiter.
e. Interrupt handler for all seven interrupt levels.
f. On-Board BERR timeout.
g. Separate VMEbus BERR watchdog timer.
h. Power-on/pushbutton/software generated SYSRESET.
i. 12.5 MHz operation standard.
j. 16 MHz SYSCLK.
k. Sixteen Universal JEDEC 28-Pin RAM/ROM sockets.
l. Up to 1M bytes ROM/448K byte RAM onboard
m. Software programmable baud rates.
n. (2) parallel I/O ports & (1) 24-bit timer circuit (68230).
o. 16 Megabyte (24-bit) direct memory addressing.
p. Optional VME1bug terminal monitor/debugger program.
q. Two year limited warranty.

2.2 Specifications

Listed below are the specifications for dimensions, environment, power and compliance for the OB68K/VME1.

2.2.1 Power Requirements

The computer board receives its power through the VME bus backplane. Typical power requirements are as follows:

+5 VDC $\pm$ 5%	2.5 A. Max (1.75 A Typ.)
+12 VDC $\pm$ 5%	50 mA Max (20 mA Typ.)
-12 VDC $\pm$ 5%	50 mA Max (20 mA Typ.)

Note: Single 5 volt operation is possible with the OB68K/VME1 if the serial ports are not used.

2.2.2 OB68K/VME1 Compliance

This section lists the VMEbus compliance and options for the OB68K/VME1 computer.

Master Data Transfer Options:
A24:D16
TOUT = 1 millesecond (STAT)

Address Modifier Options:
Any One of 29,2D,39,3A,3D,3E (DYN)

Arbiter Options:
Any One of PRI, OR RRS (STAT)

Requester Options:
Any One of R(0),R(1),R(2),R(3) (STAT)
Any One of ROR Release on Request
RWD Release When Done

Interrupt Handler Options:
Any of IH(X-Y) (STAT)
where; $1 < X < 7$ and $X < Y < 7$

Interrupter Options:
None

Physical configuration Options:
NEXP Non-expanded Bus, Double VMEbus Board

2.2.3 Environmental

Temperature:	0 to 65 degrees C (operating)
	-15 to +85 degrees C (storage)
Humidity:	0 to 90% (non-condensing)

2.2.4 Physical

The OB68K/VME1 is a standard VME Double Height printed circuit board format. The PC board is made of a glass epoxy fire retardant (94-V0) material. All critical IC's are socketed. See Figure 2.2.4 for exact dimensions of the board.

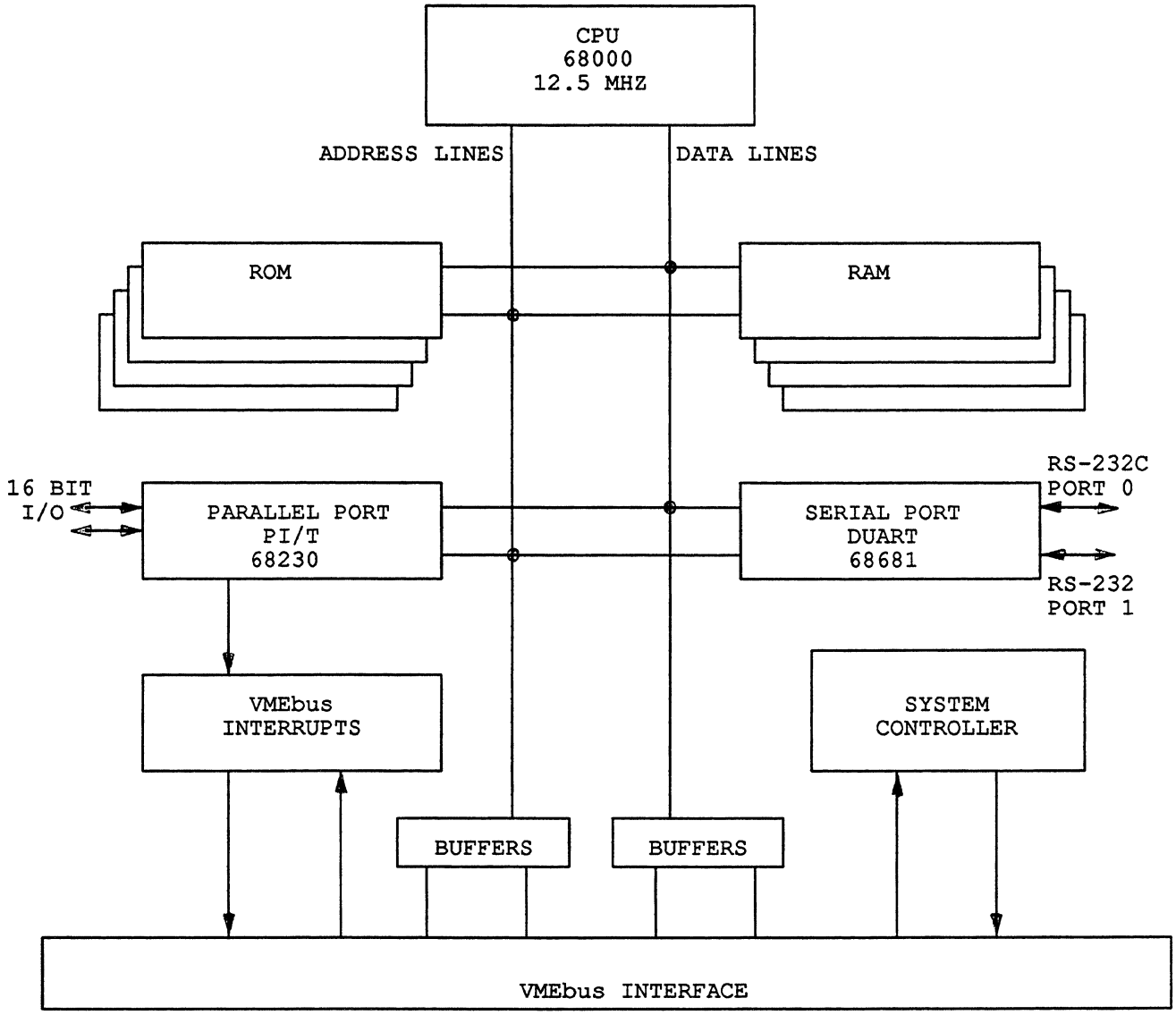
Dimensions:	9.17in. (23.3cm) X 6.29in.(16.0cm) X 0.062in.(0.16cm). Component height: <.550 in.
PC Board:	94-V0 material, fire retardant 6 sec @ 530 degrees F. Multilayer.

2.3 OB68K/VME1 Access Time Information

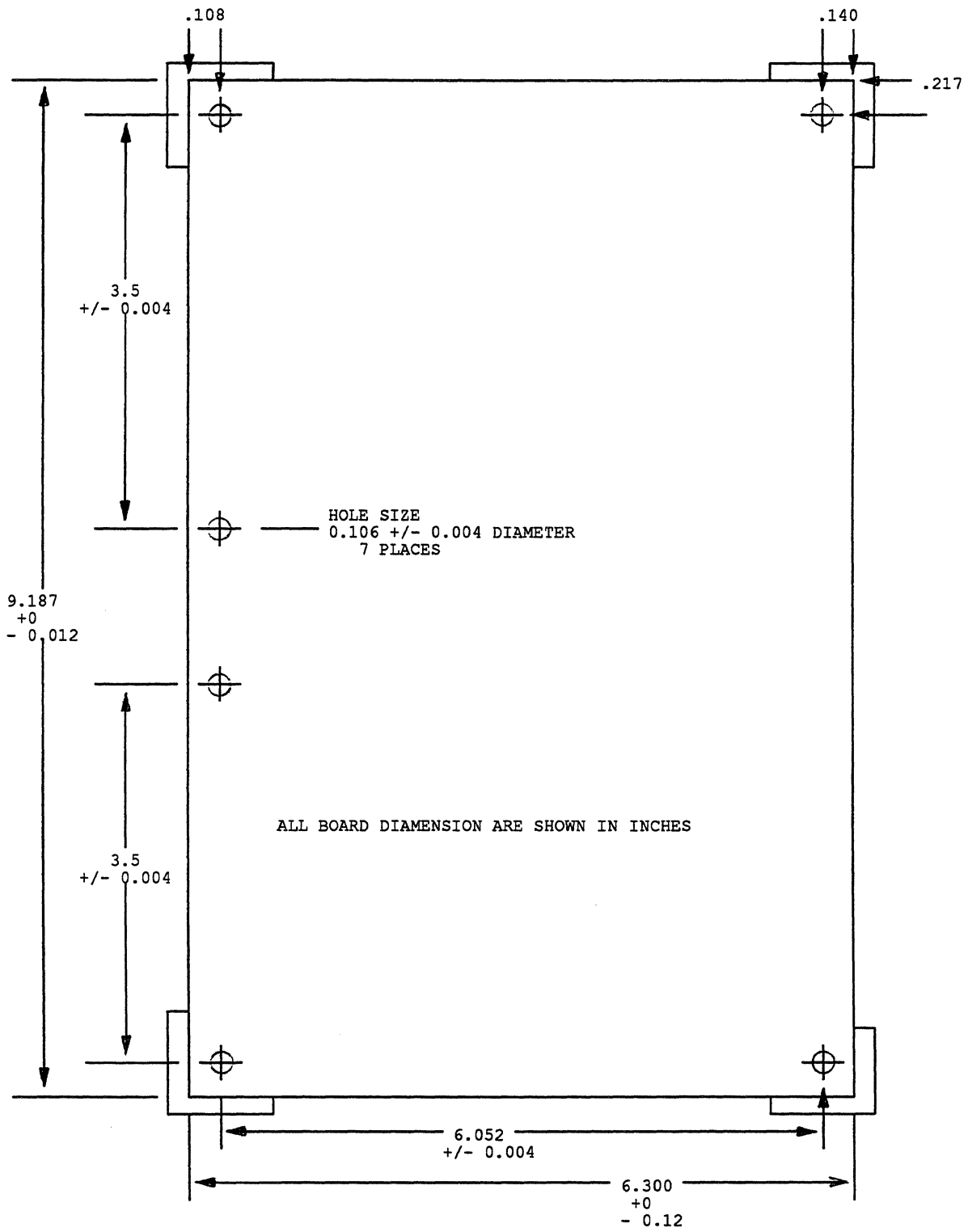
Listed below are access/cycle times for the various on-board devices, as well as off-board memory and I/O. Please note that many factors contribute to the timing and access times for off-board memory and I/O. Listed below are minimum access times achievable with the OB68K/VME1.

ACCESS/CYCLE	TIME (nS)	COMMENTS
On-Board RAM Cycle Time	320-1040	User Selectable.
On-Board ROM Cycle Time	320-1040	User Selectable.
VMEbus Cycle Time Memory or I/O	560 400	Release When Done. Release On Request. Data Strobe connected to DTACK. READ or WRITE. Round Robin or Parallel Arbitration.
68681 DUART Cycle Time	720-880	Clock asynchronous with processor
68230 PI/T Cycle Time	560-640	Clock asynchronous with processor

NOTE: All Access and Cycle times with 12.5 MHz processor speed.



BLOCK DIAGRAM
FIGURE 2.0



OB68K/VME1 BOARD DIMENSIONS
FIGURE 2.2.4

3.0 GENERAL DESCRIPTION OF OB68K/VME1

The OB68K/VME1 is a single board microcomputer designed to conform to the VMEbus specification (REVISION C.1).

3.1 VMEbus

The VMEbus is a high performance microcomputer system bus designed by the 68000 manufacturers. The bus defines the mechanical, electrical and protocol characteristics for devices that are components of a closely coupled computer system. VMEbus proponents are seeking an IEEE bus standard for this microcomputer bus. The working group for this project has been assigned the number P1014. The VMEbus allows byte, word, and longword transfers of data between modules in the system using the backplane interconnection paths. A full 32-bit addressing space is supported although short (16-bit) and standard (24-bit) addressing modes are also allowed, these being defined through the use of address modifier bits on a cycle by cycle basis. Four separate, daisy chained, bus priority levels allow the backplane to be shared by many masters that are granted the use of the bus by a centralized arbiter circuit. It is recommended that the user become familiar with the VMEbus specification.

3.2 Design Goals for the OB68K/VME1

The VMEbus specification accommodates a wide range of system designs that vary from very small and simple to extremely large and complex. Therefore, it is appropriate to describe the overall design goals of the OB68K/VME1.

The OB68K/VME1 is a straight forward, single board microcomputer design that is simple enough to operate stand-alone and flexible enough to operate in large multimaster systems. As a single board computer, it includes the CPU, RAM, ROM, two RS232C serial ports and two 8-bit parallel I/O ports - everything necessary to operate as a microcomputer.

In addition to the microcomputer capability, the OB68K/VME1 is also a full VMEbus controller and may operate in Slot 1 of the backplane. The OB68K/VME1 provides the 4-level bus arbiter functions, interrupt handling for up to seven levels, the SYSCLK, the BERR timeout, and power-on, pushbutton and program controlled SYSRESET. Thus, the OB68K/VME1 is a powerful VMEbus engine.

The OB68K/VME1 is optimized for use in high performance process control environments. A 12.5 MHz CPU is standard and no-wait-state operation is achieved for on-board memory access. Eight pairs of byte-wide memory sockets can be used for either PROM or static RAM chips. Using 512K bit PROMs, up to 1024K bytes of program storage is available, so most programs can reside on-board.

3.3 Serial Interface

Two asynchronous serial ports are implemented using a 68681 dual universal asynchronous receiver/transmitter (DUART). This is a single chip MOS LSI communications device that includes such advanced features as programmable baud rates, auto-echo option, four-byte FIFO buffer for each receiver and local/remote loopback. Baud rates of 50 to 38.4K baud are individually programmable for the transmit and receive channels of each serial port. Two handshake lines, CTS input and RTS output, are available for each of the two serial ports. All serial I/O lines are RS-232C compatible. The 68681 supports the vectored interrupt protocol of the 68000 family. Both the serial I/O ports are available on the user I/O pins of connector P2, and one port is also run to a connector on the front panel, for system diagnostic purposes.

3.4 Parallel Interface

A 68230 parallel I/O circuit on the OB68K/VME1 combines several binary I/O utilities into one interface chip. The 68230 also supports vectored interrupts.

Of the three bytes of parallel interface, port A and B are connected to the user I/O pins of connector P2 along with the H1 and H2 handshake lines. Port C is used for the parallel and timer interrupt request/interrupt acknowledge functions, and to interface to several status lines.

3.5 Timers

The 68230 contains a multipurpose 24-bit timer that may be configured to function as an interrupt source. Interrupts can be generated periodically, or one time only, following a programmed countdown. It can be used for elapsed time measurements or as a watchdog timer. A separate vectored interrupt capability is supported by timer interrupt and interrupt acknowledge lines on the 68230.The time base is the 8MHz 68230 CLK input prescaled by the internal 5-bit divider.

A second timer is included in the 68681. This is a 16-bit counter/timer that can be set and read by the processor.

3.6 Bus Arbitration

The VMEbus specification provides for a very fast centralized, four level, daisy chained, bus arbitration facility. The OB68K/VME1 fully supports the bus arbitration protocol. The OB68K/VME1 requests the use of the data transfer bus by interfacing to the bus request/grant lines on the backplane just as any other master on the bus. Thus this computer can operate at any of the four priority levels. For larger systems using more than one OB68K/VME1, the arbiter can be disabled by removing several jumpers. The master in Slot 1 must have the bus arbiter enabled and provide the bus arbitration for all masters in the system. This computer has the ability to retain its bus mastership for successive data transfers as long as no other masters request the use of the bus.

3.7 On-Board Memory

A large fraction of the OB68K/VME1 is dedicated to on-board memory space in the form of sixteen 28-pin memory sockets. Several sizes of PROM and static RAM chips can be used, but for any given configuration, all PROM chips must be the same size and all RAM chips must be the same size, but the RAM and PROM sizes need not be the same. The factory standard configuration is for 8K byte RAM chips and 16K byte PROM chips, although this selection is easily changed by the user.

3.8 Address Decoding and Memory Mapping

The address decoding on the OB68K/VME1 is determined by a combination of programmable logic array devices that cannot be changed and jumper options that set the base address of the on-board memory and I/O. Any address that does not lie within the space allocated for on-board resources, defaults automatically to a VMEbus memory access. Figure 6.1 is the factory standard memory map for the OB68K/VME1.

This map places a 128K byte RAM block at $000000 so that the exception vector table entries may be dynamically written by the processor. The 64K byte I/O block is at the very top of memory, $FF0000-$FFFFFF (This choice allows short addressing modes to be used when accessing I/O devices in the upper 32K bytes of memory). The 128K bytes of PROM space is located at $F80000-$FAFFFF. All other addresses are VMEbus memory.

3.9 Data Transfer Acknowledge and Bus Errors

The 68000 data transfers are asynchronous--A Data Transfer ACKnowledge (DTACK) signal is required to complete an access. For VMEbus cycles this signal is provided naturally by the transfer acknowledge signal of the bus. An on-board DTACK generator provides the required signal for ROM and RAM accesses. The DTACK delay is separately selectable for RAM and ROM to match the access time requirements of the installed memory devices.

In the event that unimplemented off-board memory is accessed, no DTACK will be generated. An on-board "watchdog" timer is included to detect a lack of response, and a pulse is generated that may be jumpered to the 68000 Bus Error input pin. A signal asserted on this pin will initiate bus error exception processing and a user-supplied routine may be executed to allow the system to analyze and report or recover from this condition.

Two watchdog timers are provided so that on-board and off-board BERR conditions may be treated differently. For an on-board bus error, only the local processor needs to be alerted. For an off-board bus error, the VMEbus BERR signal should be asserted. This is a controller function that is always monitoring the bus activity to detect any access cycle that exceeds the timer delay (1 millesecond).

Conditions that will cause a bus error are:

a) Access to off-board memory addresses that have no responding memory (not plugged in, or not working).

b) Access to off-board I/O addresses that have no responding device (not plugged in, or not working).

c) Access to an on-board I/O address that does not return a DTACK signal.

An access to an on-board memory address will not cause a bus error even if a memory chip is not installed. The 68000 family peripheral devices return their own DTACK signal so an access to a missing on-board device (68230, 68681) will result in a watchdog timer bus error.

3.10 Clocks

Several clock sources are included on the OB68K/VME1. This section describes each of them.

3.10.1 Processor Clock

A crystal oscillator that is divided by 2 provides the clock for the 68000 processor. This processor clock is also used as the time base for the RAM/ROM DTACK generator. Notice that other clock frequencies may be used by simply replacing the 25.0 MHz oscillator with a different frequency oscillator (i.e. 20MHZ, 16MHz, 12MHz). Please note that there will also be a shift in the RAM/ROM DTACK times.

3.10.2 Baud Rate Clock

The baud rate generator for the serial communication ports is internal to the 68681 DUART. A 3.68640 MHz crystal sets the frequency of the internal oscillator and the baud rate is selected under program control.

3.10.3 VMEbus SYSCLK

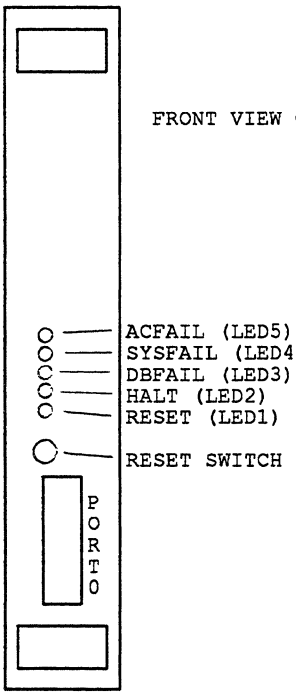
A 16 MHz clock is included for use as the VMEbus SYSCLK. Because only one card in a VMEbus system can assert this signal, a jumper is provided to remove it from the bus. With this jumper removed, the card uses the SYSCLK generated by another master in the VMEbus chassis.

3.11 Interrupts

The OB68K/VME1 supports the VMEbus Interrupt Handler Module functions for all seven interrupt levels. The 68000's three interrupt priority input lines IPL2, IPL1, and IPL0 are driven by a 74148 priority encoder. IRQn lines from the VMEbus backplane or a composite on-board interrupt request may be connected to 74148 input levels by the user. For each interrupt level, jumpers allow the choice of either vectored or non-vectored interrupt protocol. All on-board interrupts share a single interrupt level. Within the on-board level, the priority of the on-board sources is selectable. On-board devices will normally be selected to operate as vectored interrupts because each interrupting device supports the vectored protocol.

3.12 Status Indicators

Three LED status indicators are mounted on the front panel to show the status of the VMEbus ACFAIL and SYSFAIL signals along with a local BDFAIL signal. The ACFAIL signal is normally driven by the power monitor circuitry in the power supply. SYSFAIL may be driven by any module in the system that is capable of detecting faults. BDFAIL is a locally generated signal asserted by the 68000 using an output pin of port C on the 68230. In addition to turning on the LED indicator, BDFAIL also drives the SYSFAIL line. SYSFAIL and ACFAIL are connected to the 68230 input lines PC0 and PC1, and to the H3 and H4 handshake lines. The 68230 can be configured to allow either one or both lines to cause a parallel IRQ. Alternately, the PC0 and PC1 lines may be read as status without configuring for interrupts.



LED#	FUNCTION	COLOR
LED5	ACFAIL	YELLOW
LED4	SYSFAIL - VME1 driven by VMEbus	RED
LED3	BDFAIL - VME1 drives BDFAIL	RED
LED2	HALT	RED
LED1	RESET	YELLOW

INDICATOR LED IDENTIFICATION
TABLE 3.12

3.13 Restart Vector Accessing

When a power-on or manual reset of the processor occurs, the processor begins operation by accessing memory location zero, in Supervisory Program space, to load the restart vector and the Supervisor stack pointer. These two vectors must be stored in PROM because the contents of RAM are unknown at restart time.

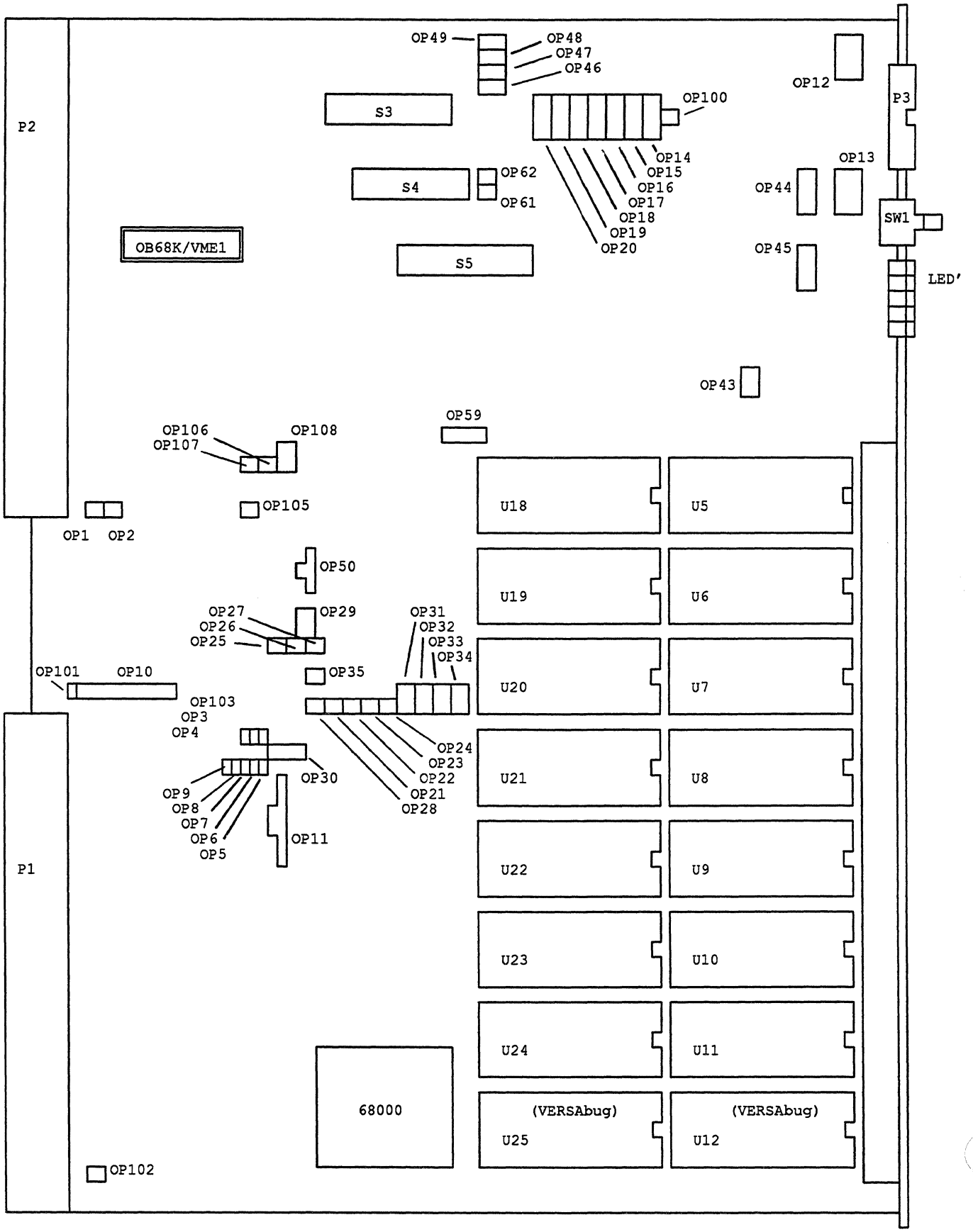
A shift register that is cleared by RESET generates a signal that causes the first four (Word) memory accesses, following RESET, to be unconditionally directed to location 0 through 7 of the PROM in memory socket pair zero. For this reason one pair of PROM chips must be installed in socket pair zero. The access to these PROM locations is independent of the switch selected location of ROM in the address map of the OB68K/VME1. For proper operation after restart, some memory must exist at location $000000 in order to have memory at the addresses where the processor expects to find exception vectors. This may be either RAM or PROM and can be in off-board memory. All other socket pairs may have either RAM or ROM installed. The Supervisor Stack Pointer must reside in locations 0 through 3, and the Program Counter must reside in locations 4 through 7.

4.0 USER DEFINABLE OPTIONS

This section describes the jumpers and options included on the board. Table 4.0 is a summary of all the user definable jumpers. The location of these jumpers are shown in Figure 4.0. Please note, in the diagrams that follow, the factory standard configuration is shown.

Jumper No.	No. of Pins	Function	SCHM PG #	PAGE #
OP1	2	SYSRESET controller/slave select	1	34
OP2	2	BERR to CPU (From onboard devices)	1	20
OP3-OP9	14	VMEbus IRQ1...IRQ7 to priority encoder	1	22-23
OP10	14	ON-BOARD IRQ priority select	1	22-24
OP11	11	RAM/ROM DTACK delay select	1	21
OP12	6	TIACK,PIACK,IACKN priority select	1	22-25
OP13	6	TIRQ,PIRQ,INTRN priority select	1	22-25
OP14-20	21	Auto Vector/Bus Vector interrupt select	2	22-23
OP21-24	8	BGnIN enable for 4 levels	1	27
OP25-28	8	BR enable for 4 levels	1	27
OP29	6	Bus Req. level for this CPU	1	30
OP30	6	Bus Grant level for this CPU	1	30
OP31-34	12	BGOUT disable for local access	1	31
OP35	2	Release on Request(ROR)/Release when Done(RWD)	1	29
OP43	2	RAM chip size select	2	37
OP44-45	6	ROM chip size select	2	37
OP46-48	6	ROM block 64,128,256,512K,1M select	2	38
OP49	2	RAM block 64,128K select	2	38
OP50	4	Upper/Lower RAM block select	2	38
OP51-58	10	Memory socket configuration jumpers; 8 pairs (ROM and RAM)	2	35-36
OP59	3	Power-on and Push Button RESET	1	34
OP60	1	68230 pin PC4	2	41
OP61-62	2	RAM block 256K,512K select	2	38
OP100	1	ON-BOARD Bus Vectored Interrupt ACK	2	22-24
OP101	2	SYSCLK to bus	1	29
OP102	2	BCLR to VMEbus	1	28
OP103	2	BERR to VMEbus	1	20
OP105	2	Round Robin/Parallel Arbitration	1	28
OP106	2	OB68K/VME1 Drives BBUSY to VMEbus	1	29
OP107	2	SYSRESET Drives Arbiter Reset	1	29
OP108	3	Factory Set	1	41
S3	16	RAM Base Address	2	39
S4	14	ROM Base Address	2	39
S5	16	I/O Base Address	2	39

USER DEFINABLE OPTIONS
TABLE 4.0



FIGUIRE 4.0 LOCATION OF JUMPER OPTIONS

4.1 Serial Port Configuration

The connections to the serial ports are fixed. Each of the two ports are interfaced with four signals plus ground: RXDATA, TXDATA, RTS and CTS. The CTS input is biased so that the channel is enabled unless it is pulled down by the off-board device. The baud rate is set under software control by storing the appropriate code in the clock select register for channels A and B (CSRA and CSRB). Bits 0-3 and 4-7 of these registers control the transmit and receive baud rates, respectively. The baud rates corresponding to the available choices for the 4- bit select values are given in Table 4.1. VME1bug, if used, sets the baud rate to 9600 at power-up and reset.

Value	(ACR bit 7=0)	(ACR bit 7=1)
0	50	75
1	110	110
2	134.5	134.5
3	200	150
4	300	300
5	600	600
6	1200	1200
7	1050	2000
8	2400	2400
9	4800	4800
A	7200	1800
B	9600	9600
C	38.4K	19.2K

BAUD RATE SELECTION VALUES
TABLE 4.1

4.1.1 VME1bug TERMINAL MONITOR/DEBUGGER PROGRAM

A terminal monitor/debugger program, VME1bug, is available from Omnibyte for use with your OB68K/VME1. This program is licensed from Motorola Inc. by Omnibyte and is provided as object code in two 16K (27128) PROMS.

VME1bug allows the usual terminal interaction features of display, modify, load and dump memory, run programs with breakpoints, and register display and modify. In addition VME1bug includes a HELP display, memory test, block fill, block move and one line assembler/disassembler capabilities.

4.2 Bus Error Jumpers (OP103, OP2)

When the OB68K/VME1 is a system controller (Slot 1), OP103 should be installed to drive the BERR signal on the VMEbus backplane. In the event a VMEbus transfer sequence fails to terminate within 100 microseconds, an on-board bus timeout circuit will drive the VMEbus BERR signal and terminate the transfer. Jumper OP103 connects the output of the timeout circuit to the backplane. If the OB68K/VME1 is in any other VMEbus Slot, then OP103 should be removed to avoid having two masters driving the BERR signal. See page 18, FIGUIRE 4.0 for the location of OP103.

Jumper OP2 connects both, the "On-Board Watchdog Timer" and the "VMEbus BERR" backplane signal, to an encoder that drives the BERR and HALT lines of the 68000. When OP2 is installed, BERR is enabled and if DTACK is not received from an addressed device, a bus error is generated and the processor will begin bus error exception processing. With OP2 removed, the address and data lines will be static and can be examined at leisure. This is a useful mode for debugging off- board system problems. This signal does not connect to the backplane. See page 18, FIGUIRE 4.0 for the location of OP2.

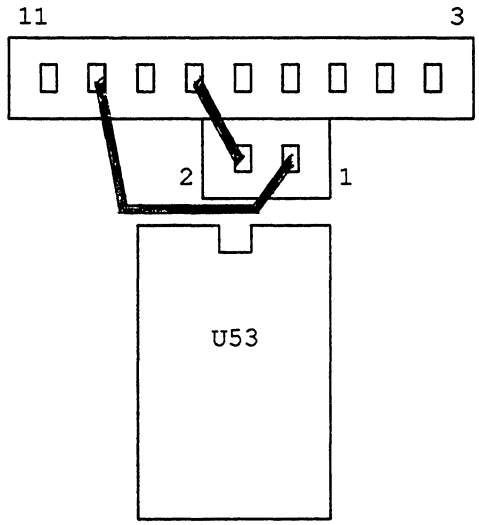
OP103	FUNCTION: BERR TO VMEbus
IN	INSTALLED ONLY when board is in Slot 1.
OUT	Removed when board is in any Slot but 1.

OP2	BUS ERROR (BERR) TO 68000
IN	BERR Watchdog timer circuitry enabled. (BERR to CPU)
OUT	Processor (68000) waits indefinitely for DTACK. NOTE: This is a useful mode for troubleshooting.

TABLE 4.2 BUS ERROR (BERR) OPTIONS

4.3 DTACK Select (OP11)

The DTACK signal is generated by the accessed device in all cases except for the on-board RAM and ROM. The DTACK for the on-board memory chips is selected from a shift register that is enabled during an access. The shift register is clocked at the processor frequency and the RAM and ROM DTACK delays are independently selectable in increments from the shift register outputs. The DTACK delays are shown below. The proper tap on the DTACK generator depends upon the access time of the installed memory chips. The factory standard setting is appropriate for 250ns ROM and 120ns RAM. The DTACK jumpers are shown in Figure 4.3 and the delay values are given in Table 4.3.



OP11 /DTACK OPTION	
1	RAM DELAY INPUT
2	ROM DELAY INPUT
3	U39-Q7
4	U39-Q6
5	U39-Q5
6	U39-Q4
7	U39-Q3
8	U39-Q2
9	U39-Q1
10	U39-Q0
11	NO DELAY

FACTORY STANDARD

RAM = 1 - 10
ROM = 2 - 8

RAM/ROM DTACK DELAY OPTIONS
FIGURE 4.3

P11-1(RAM) P11-2(ROM) CONNECT TO	MAXIMUM RAM/ROM ACCESS TIME 10.0 MHz	MAXIMUM RAM/ROM ACCESS TIME 12.5 MHz	MAXIMUM RAM/ROM ACCESS TIME 16.0 MHz	NO. OF WAIT STATES	NO. OF WAIT CYCLES
OP11-11	155nS	125nS	94nS	0	0
OP11-10	255nS	205nS	156nS	2	1
OP11-9	355nS	295nS	219nS	4	2
OP11-8	455nS	365nS	281nS	6	3
OP11-7	555nS	445nS	344nS	8	4
OP11-6	655nS	525nS	406nS	10	5
OP11-5	755nS	605nS	469nS	12	6
OP11-4	855nS	685nS	531nS	14	7
OP11-3	955nS	765nS	594nS	16	8

NOTE: The OB68K/VME1 may be run at a processor clock speeds of 10.0 MHz and 12.5 MHz. 16.0MHz operation is shown here for comparative and illustrative purposes only.

RAM/ROM DTACK DELAYS
TABLE 4.3

4.4 Interrupts (OP3-OP10, OP12-OP14)

The interrupt jumper groups for the OB68K/VME1 are shown on the subsequent pages. Jumper group OP3-OP9 are the inputs to the priority encoder that drive the Interrupt Priority Level (IPL) signals to the 68000 processor. Inputs to this priority encoder may be any combination of the seven VMEbus IRQ (OP3-OP9) lines or the (OBIRQ) ON-BOARD I/O Interrupt Request (OP10).

Individual ON-BOARD Interrupts connect to a separate priority encoder (OP13) which prioritizes the ON-BOARD requests and generates the composite ON-BOARD Interrupt Request (OBIRQ; OP10) signal. The ON-BOARD sources are TIRQ from the 68230 timer, PIRQ from the 68230 parallel handshake lines, and INTRN from the 68681 (DUART). Option OP100, returns the /IACK signal to ON-BOARD devices during Bus-Vectored Interrupts.

During the interrupt acknowledge cycle, the processor outputs the priority level being acknowledged on address lines A1-A3. These three lines are input to a one- of-eightdecoder, U2, and the decoded outputs are brought out to jumper group OP14-20;2. Each priority level can then be jumpered to be either a Bus-Vectored (OP14-20;1) or Auto-Vectored (OP14-20;3) interrupt. For any particular level, if a Bus-Vectored Interrupt is selected, the processor proceeds to read the vector number asserted on D7-D0 by the interrupting device. If the interrupting device does not support Bus-Vectored Interrupts, then an Auto-Vectored Interrupt should be selected for that level. Note that all interrupting devices connected to a particular level must respond in the same way.

Bus-Vectored and Auto-Vectored Interrupts cannot be mixed on the same level.

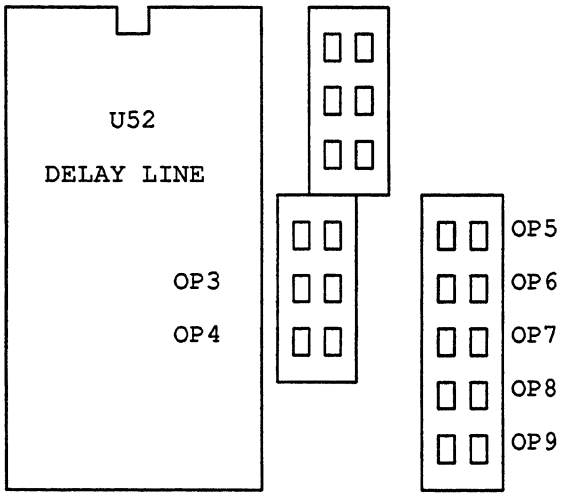
All ON-BOARD devices support Bus-Vectored Interrupts. Their relative priority is chosen by connecting the ON-BOARD sources to the input of a priority encoder, a PAL16R4 (U3) using jumper group OP13. The output from the PAL16R4 is input to a 74137 decoder that is latched and enabled by the ON-BOARD Interrupt Acknowledge signal (OP10). For Bus-Vectored Interrupts OP100 is connected to the appropriate interrupt level at option OP14-20;2, if Auto-Vectored interrupts are desired for the ON-BOARD devices, the appropriate interrupt level should be connected OP14- 20;2 to OP14-20;3. Outputs from the 74137 are jumpered (OP12) to the Interrupt Acknowledge pins of the ON-BOARD parallel and serial peripheral I/O chips. For the ON-BOARD devices, if Auto-Vector mode is selected, the appropriate Auto-Vector will be accessed and an interrupt service routine would be required to poll the devices to locate the interrupt source, if more than more one ON-BOARD device is connected to the OBIRQ encoder.

NOTE: The priority of the ON-BOARD Interrupt Request inputs (PIRQ,TIRQ and INTRN) at option OP12 must be the same as the ON-BOARD Interrupt Acknowledge outputs (PIACK, TIACK, and IACKN) at option OP13. i.e., If TIRQ is connected to level 1 (OP12 1-5), TIACK must be connected to level 1 (OP13 1-5).

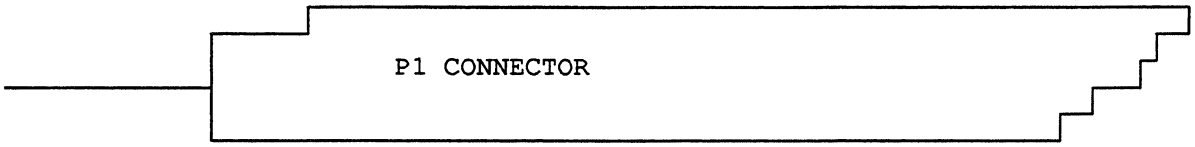
NOTE: ON-BOARD and OFF-BOARD INTERRUPTS can not share the same interrupt level.

Refer to page 23 for configuring VMEbus (Backplane) INTERRUPTS.
Refer to page 24 and 25 for configuring up ON-BOARD INTERRUPTS.
Refer to page 26 for a composite overview of the INTERRUPTS.

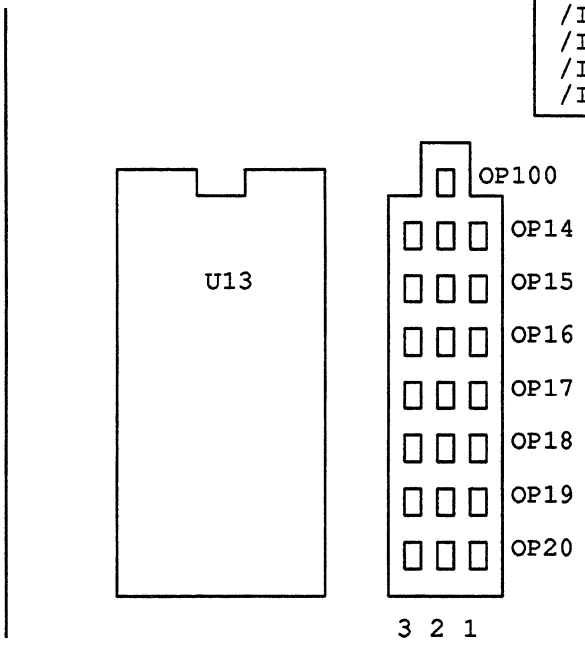
VMEbus (Backplane) Interrupt Jumper Options:



VMEbus Interrupt Inputs:	
IRQ7	OP3
IRQ6	OP4
IRQ5	OP5
IRQ4	OP6
IRQ3	OP7
IRQ2	OP8
IRQ1	OP9

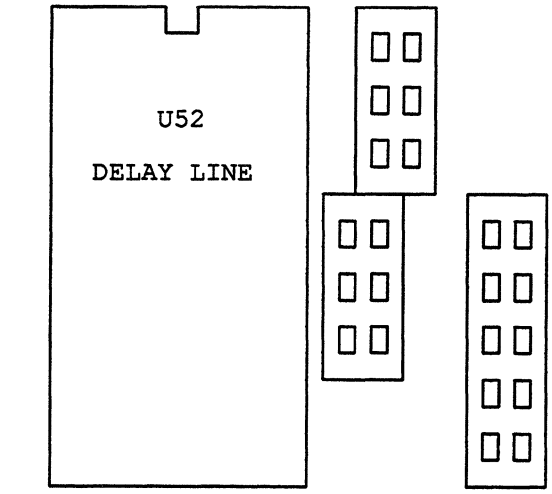


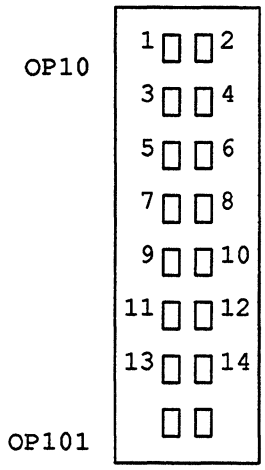
VMEbus	/IACK	AUTO-VECTOR	BUS-VECTOR
/IACK1	OP14	2 - 3	2 - 1
/IACK2	OP15	2 - 3	2 - 1
/IACK3	OP16	2 - 3	2 - 1
/IACK4	OP17	2 - 3	2 - 1
/IACK5	OP18	2 - 3	2 - 1
/IACK6	OP19	2 - 3	2 - 1
/IACK7	OP20	2 - 3	2 - 1



NOTE: Auto-Vector and Bus-Vector can not share the same interrupt level.

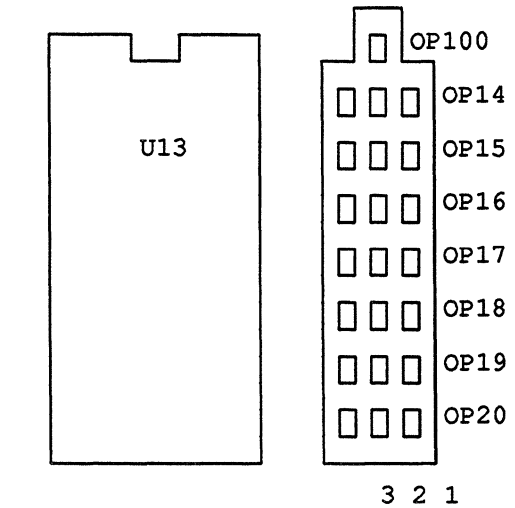
On-Board Interrupt Jumper Options:





OP10	On-Board Interrupt Level
1-2	INTR7
3-4	INTR6
5-6	INTR5
7-8	INTR4
9-10	INTR3
11-12	INTR2
13-14	INTR1

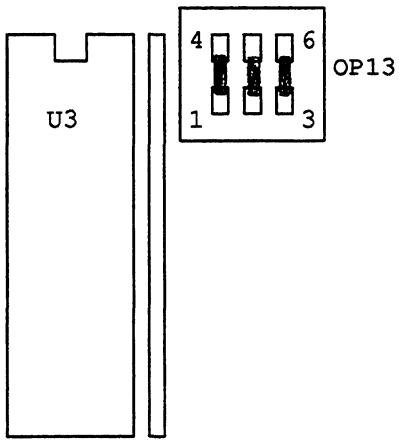
NOTE: ON-BOARD AND OFF-BOARD INTERRUPTS CAN NOT SHARE THE SAME LEVEL



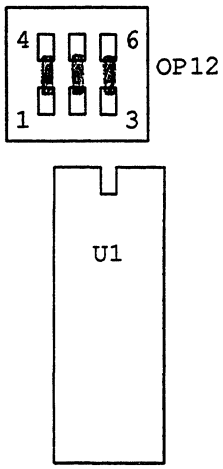
On-Board Interrupt Acknowledge		
Level	Bus-Vector	Auto-Vector
/IACK1	OP100 TO OP14-2	OP100 TO OP14-3
/IACK2	OP100 TO OP15-2	OP100 TO OP15-3
/IACK3	OP100 TO OP16-2	OP100 TO OP16-3
/IACK4	OP100 TO OP17-2	OP100 TO OP17-3
/IACK5	OP100 TO OP18-2	OP100 TO OP18-3
/IACK6	OP100 TO OP19-2	OP100 TO OP19-3
/IACK7	OP100 TO OP20-2	OP100 TO OP20-3

On-Board Interrupt Priority:

All three on-board interrupting devices use the same interrupt level. The user can configure which device has priority when more then one on-board device have an interrupt pending. OP13 selects the priority of the interrupts and OP12 returns the /IACK to the proper device.



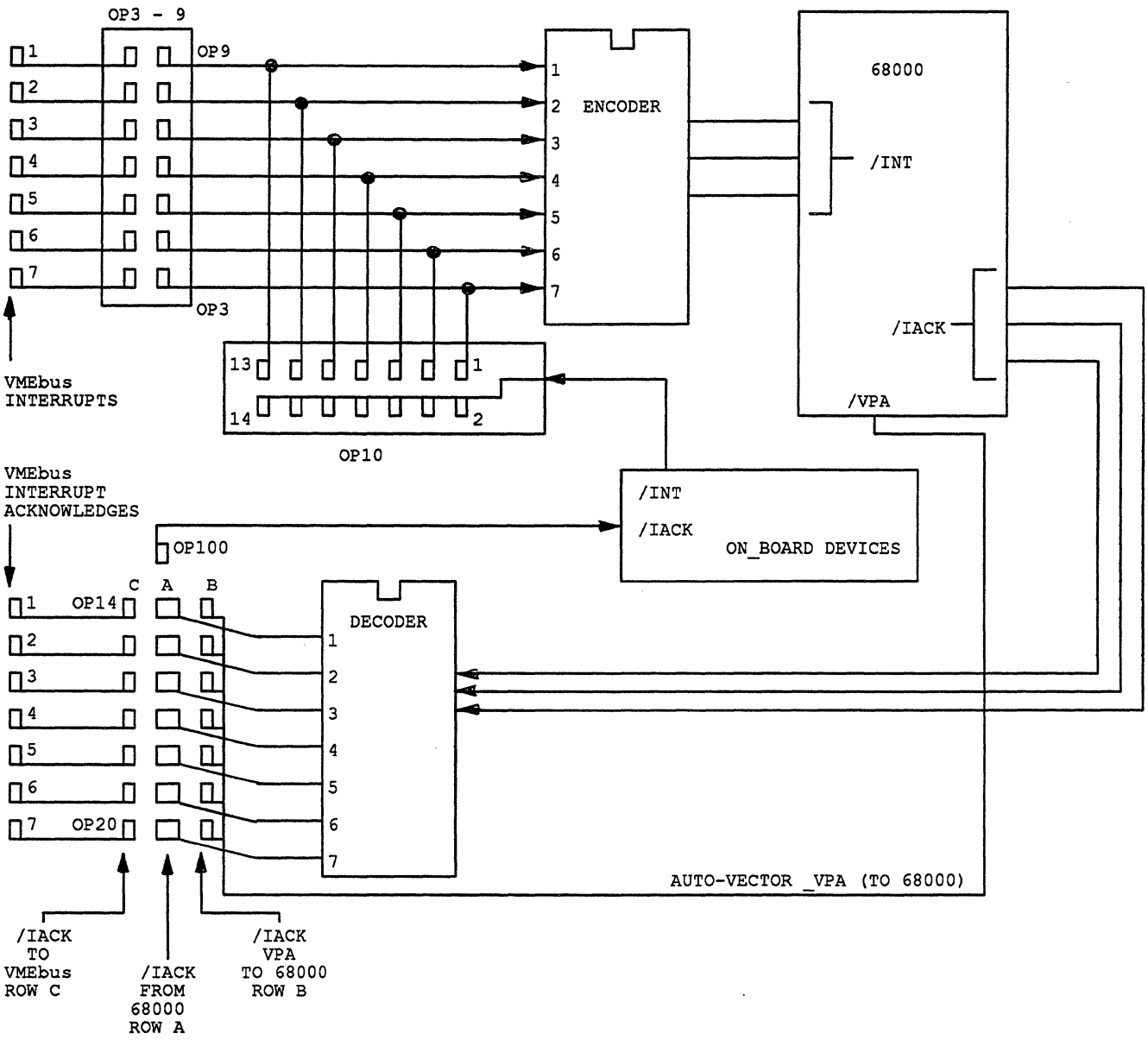
OP13 ON-BOARD INTERRUPT REQUEST PRIORITY SELECT		
4	PIRQ	IRQ FROM 68230 PARALLEL HANDSHAKE LINES
5	TIRQ	IRQ FROM 68230 TIMER
6	INTRN	IRQ FROM 68681 SERIAL CHIP
1	PRIORITY LEVEL 1 (LOWEST)	
2	PRIORITY LEVEL 2	
3	PRIORITY LEVEL 3 (HIGHEST)	



OP12 ON-BOARD INTERRUPT ACKNOWLEDGE PRIORITY SELECT		
4	PIACK	INTERRUPT ACK TO 68230 PARALLEL HANDSHAKE LINES
5	TIACK	INTERRUPT ACK TO 68230 TIMER
6	IACKN	INTERRUPT ACK TO 68681 SERIAL CHIP
1	PRIORITY LEVEL 1 (LOWEST)	
2	PRIORITY LEVEL 2	
3	PRIORITY LEVEL 3 (HIGHEST)	

NOTE: OP12 must mirror OP13 selection for proper operation.

INTERRUPT OPTIONS - CONTINUED
FIGURE 4.4



ON-BOARD INTERRUPTS:		COMMENTS:
OP10	Interrupt input level	OP10 and VMEbus interrupts can not share same level.
OP100	/IACK return from CPU	OP100 is jumpered to ROW A at same level as OP10.
OFF-BOARD INTERRUPTS (From VMEbus)		**COMMENTS:**
OP3-9 OP14-20	Interrupt inputs from VMEbus /IACK return from CPU	Can not share level with OP10. Jumper between ROW C and A for VMEbus Auto-Vector devices. Jumper between ROW C and B for VMEbus Bus-Vector devices.

4.5 Bus Arbitration (OP21-OP35, OP101-OP107)

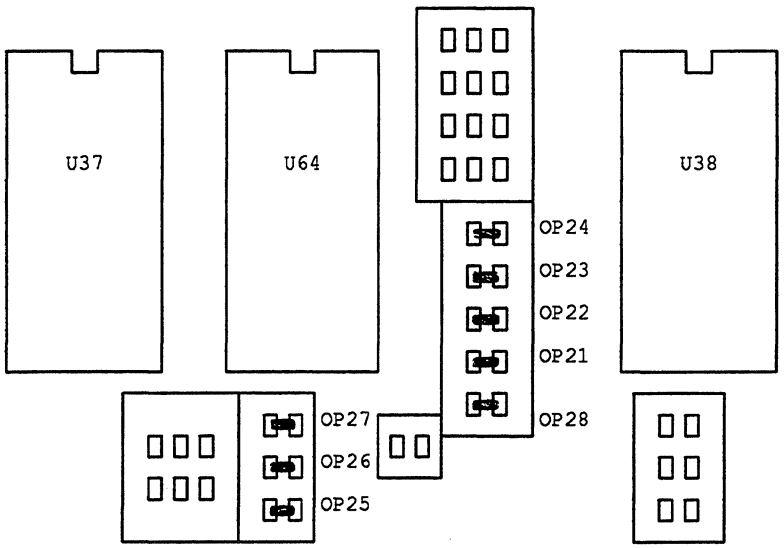
The bus arbitration functions on the OB68K/VME1 computer board can be divided into two categories, those functions that allow the OB68K/VME1 to be a VMEbus Slot 1 Controller, and those functions that allow the OB68K/VME1 to operate as a VMEbus master. Figure 4.5.1 and 4.5.2 show the location and standard jumper configuration for all the options associated with bus arbitration. Figure 4.5.1 shows a Slot 1 Bus Controller configuration, while Figure 4.5.2 illustrates a Non-Slot 1 Bus Master configuration. The following options are covered in section 4.5.1 and pertain to Bus Controller Slot 1; OP21-28, OP101, OP102, OP105, OP106 and OP107. Non-Controller Master options are covered in section 4.5.2 and include; OP35, OP29, OP30 and OP31-34. All options pertaining to Bus Arbitration should be examined during configuration to prevent cross selection between Controller and Master configurations.

4.5.1 VMEbus Controller Bus Arbitration Options

The OB68K/VME1 provides the full four-level bus arbitration functions to allow multi-master operation of the VMEbus. According to the bus specification, the bus arbiter must reside in Slot 1 and no other master may respond to bus request signals. The arbitration is accomplished using two Programmable Array Logic (PAL*) chips. Following the VMEbus protocol, the arbiter resolves the bus ownership during the execution of the current cycle, thereby minimizing the overhead time required for switching control of the bus.

The following jumper options are associated with the Slot 1 controller feature of the OB68K/VME1; OP21-28, OP101, OP102 OP105, OP106, and OP107.

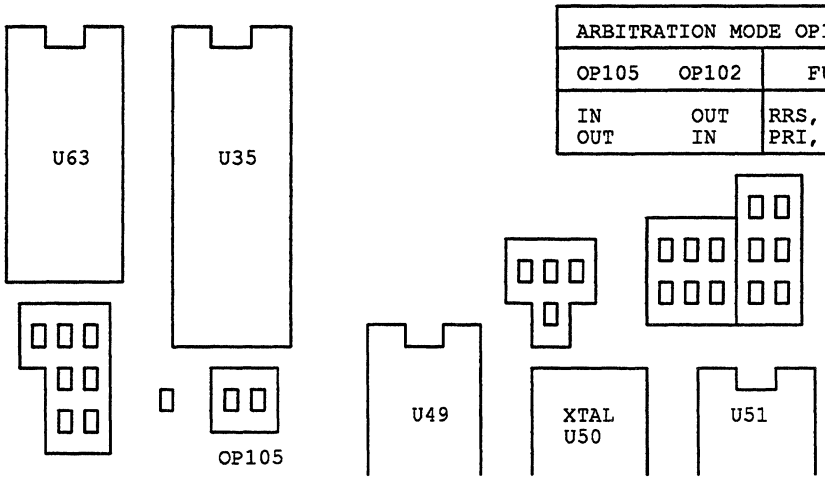
OP21-24 connects the arbiter to the VMEbus Bus Grant (BGx) lines. Options OP25- 28 connect the Bus Request (BRx) to the arbiter. If the OB68K/VME1 board is being used as a Slot 1 controller, options OP21-28 must be installed, these options must be removed in all other configurations.



CONTROLLER CONFIGURATION (SLOT 1)		
IN	OP25	BR0
IN	OP26	BR1
IN	OP27	BR2
IN	OP28	BR3
IN	OP24	BG0IN
IN	OP23	BG1IN
IN	OP22	BG2IN
IN	OP21	BG3IN

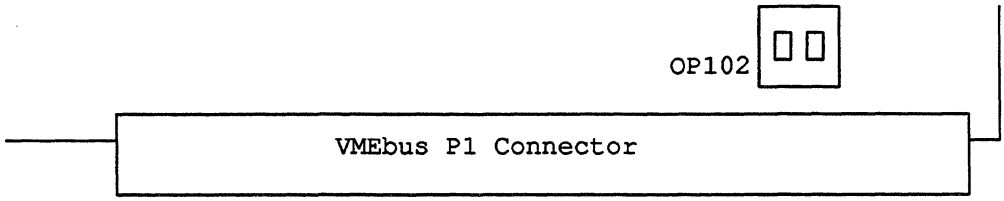
The VMEbus can arbitrate in either the Fixed Arbitration Mode (PRI ARBITER), which grants the bus based on the priority level of the request, or Round Robin (RRS ARBITER), which grants the bus on a first-come first-served basis. The choice is made using option OP105. When OP105 is removed, fixed arbitration is selected; installed, round robin arbitration is selected.

NOTE: If OP105 is installed, then OP102 must be removed, BCLR is not supported with fixed arbitration.



ARBITRATION MODE OP105 (OP102)		
OP105	OP102	FUNCTION
IN	OUT	RRS, Round Robin Mode
OUT	IN	PRI, Priority Mode

A PRI ARBITER, can drive the Bus Clear Line (BCLR). The Bus Clear Line is used by a PRI ARBITER to inform the MASTER currently in control of the bus that a higher priority request is now pending. The current MASTER is not required to relinquish control within any prescribed time limit. In multi-processor systems, only the Slot 1 Controller (MASTER) can drive BCLR. OP102 is installed if the OB68K/VME1 is used in Slot 1 and fixed arbitration mode is selected (OP105 removed); and removed for all other configurations.



NOTE: If OP102 is installed, then OP105 must be removed, BCLR is not supported with fixed arbitration.

* PAL is a trademark of Monolithic Memories, Inc.

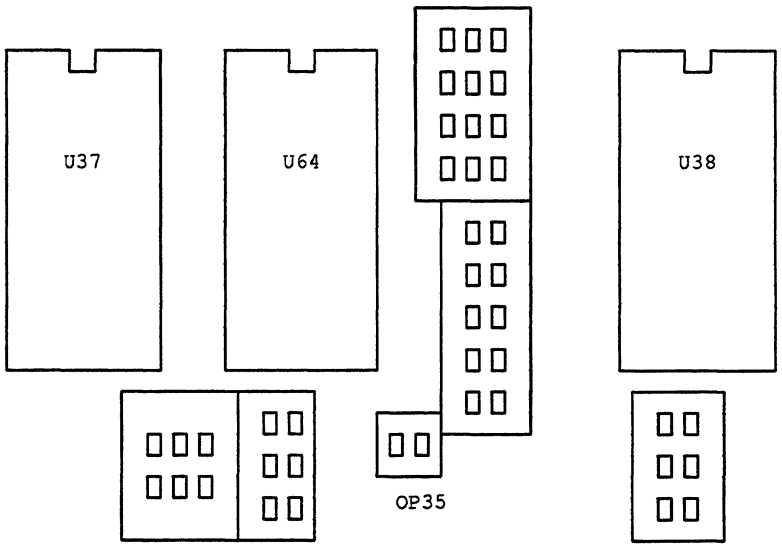
The three options not covered thus far are OP101, OP106 and OP107. These options are associated with the Slot 1 controller features, but do not allow the user additional functionality. Options OP101, OP106 and OP107 must be installed if the OB68K/VME1 is used in Slot 1 and removed otherwise.

OPTIONS INSTALLED IF IN SLOT 1	
OP101	SYSCLK to VMEbus
OP106	BBUSY to Arbitor
OP107	SYSRESET to Arbitor

4.5.2 VMEbus Master, Bus Arbitration Options

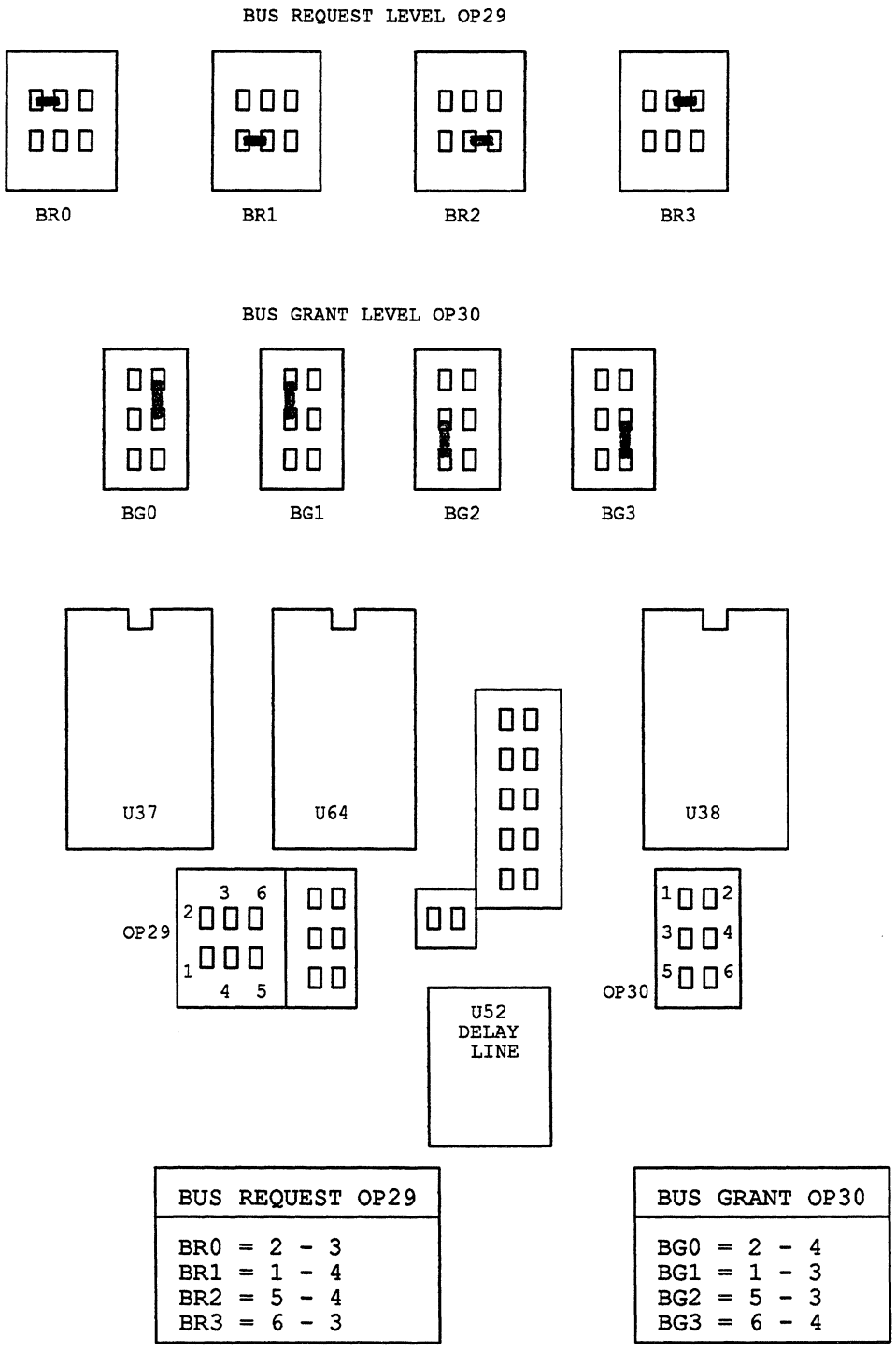
The following text describes the jumper options associated with the requesting and granting of the VMEbus for of the OB68K/VME1; OP35, OP29, and OP30.

The OB68K/VME1 can operate in the mode that releases the bus after each transfer, Release When Done (RWD), or Release On Request (ROR) of another master. The choice is made using jumper OP35 which is removed for RWD, Release When Done, and installed for ROR, Release On Request.



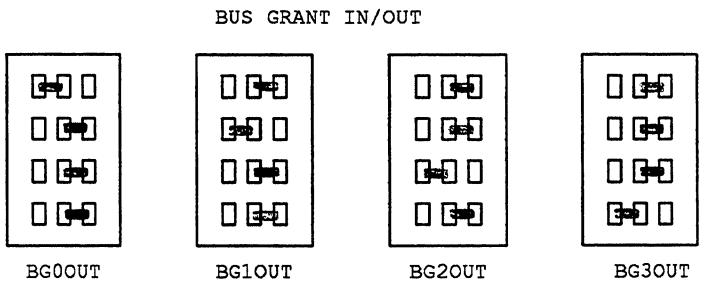
BUS OPERATION MODE OP35		
OP35	MODE	FUNCTION
IN	ROR	RELEASE ON REQUEST
OUT	RWD	RELEASE WHEN DONE

The bus priority level of the OB68K/VME1 board can be any one of the four priority levels. Priority level is selected using options OP29 and OP30. To select a particular bus request level install the appropriate jumper (OP29) for the desired priority level. The bus request level (OP29) and the bus grant level (OP30) must correspond to the same level. After selecting a bus request level, install the corresponding jumper at OP30 for bus grant priority level.

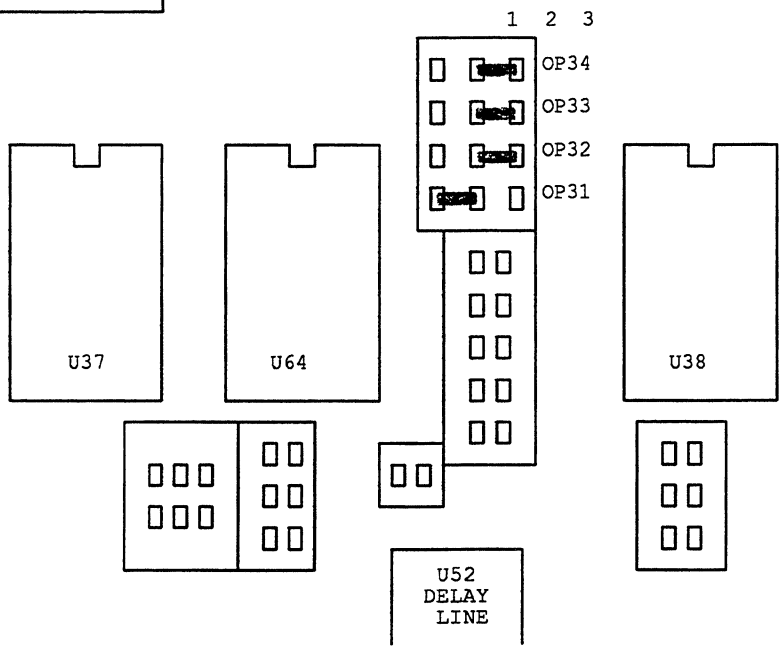


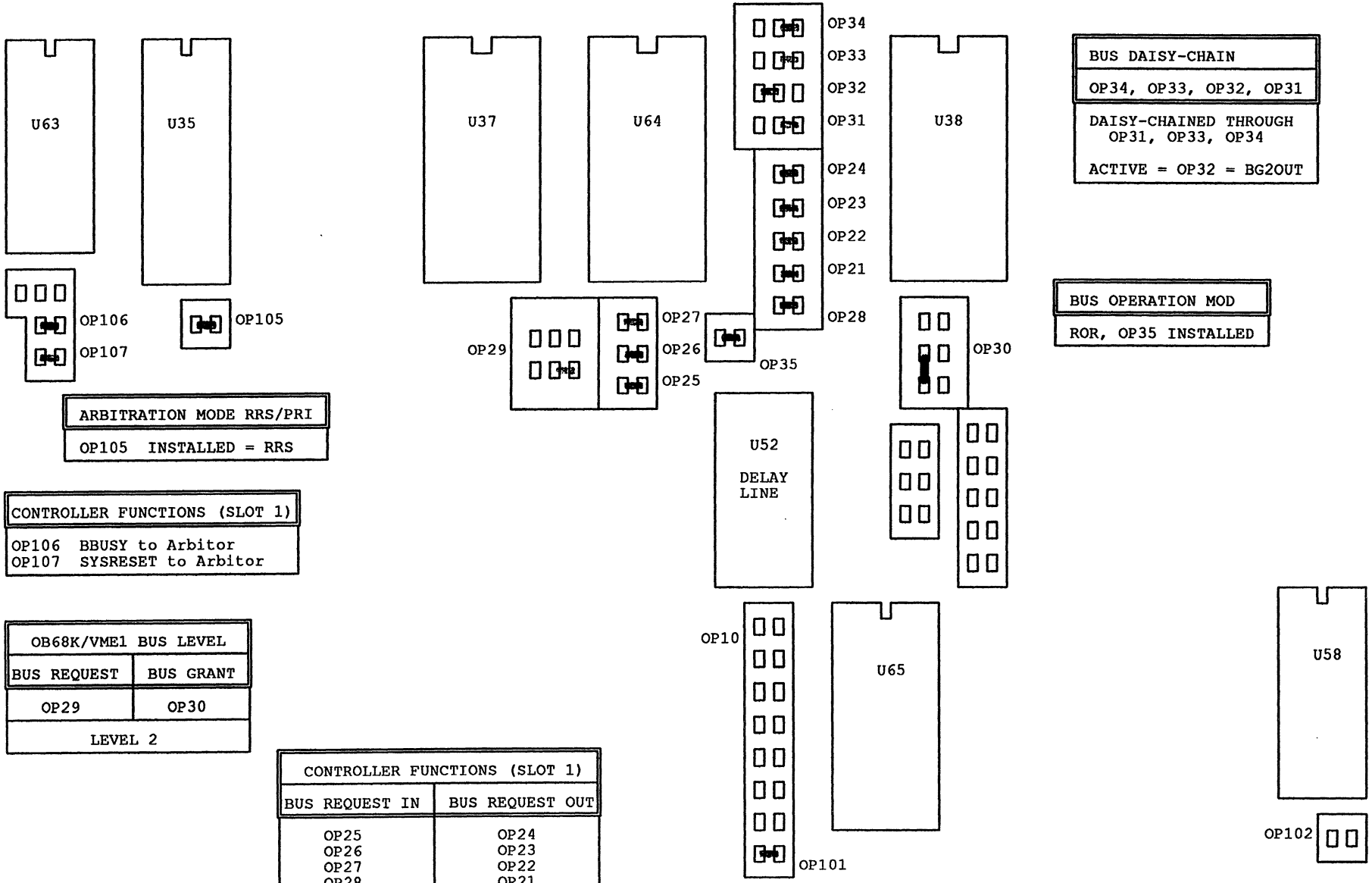
The VMEbus specifications allow several bus masters to share a single bus request/grant level, thus allowing serial arbitration within the parallel arbitration scheme. If a bus grant level is active on the bus and this board does not respond to that level or has not requested the bus, the BGnOUT signal must be passed to the downstream master(s). However, if this board has requested the bus and has been granted bus ownership for the next cycle, the BGnOUT signal corresponding to this board must not be driven onto the VMEbus.

The options associated with the BGnOUT signals are OP31 through OP34. If the priority level of this board is level 3, OP31 is jumpered 1-2 and options OP32, OP33, and OP34 are jumpered 2-3. Failure to install options OP32-34 will disable the Bus Grant to all other masters on the bus.



BUS GRANT DAISY-CHAIN
BG0OUT = OP34 BG1OUT = OP33 BG2OUT = OP32 BG3OUT = OP31





BUS DAISY-CHAIN
OP34, OP33, OP32, OP31
DAISY-CHAINED THROUGH OP31, OP33, OP34
ACTIVE = OP32 = BG2OUT

BUS OPERATION MOD
ROR, OP35 INSTALLED

ARBITRATION MODE RRS/PRI
OP105 INSTALLED = RRS

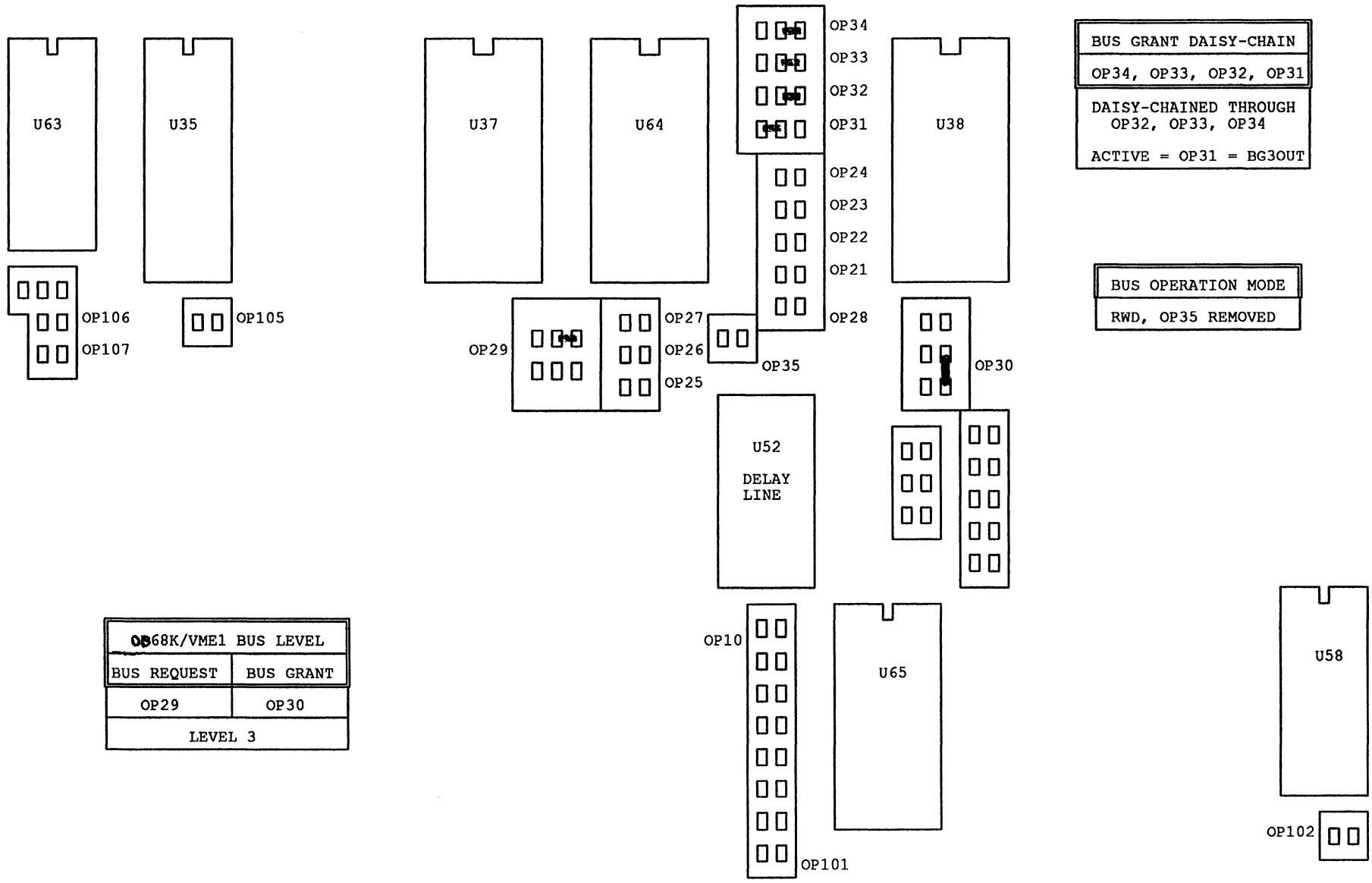
CONTROLLER FUNCTIONS (SLOT 1)
OP106 BBUSY to Arbitor
OP107 SYSRESET to Arbitor

OB68K/VME1 BUS LEVEL	
BUS REQUEST	BUS GRANT
OP29	OP30
LEVEL 2	

CONTROLLER FUNCTIONS (SLOT 1)	
BUS REQUEST IN	BUS REQUEST OUT
OP25 OP26 OP27 OP28	OP24 OP23 OP22 OP21
SYSCLK	OP101
/BCLR	OP102

EXAMPLE CONFIGURATION: SLOT 1 CONTROLLER
ROR, RELEASE ON REQUEST
RRS, ROUND ROBIN ARBITRATION
OB68K/VME1 BUS REQUEST/GRANT LEVEL 2

FIGURE 4.5.1

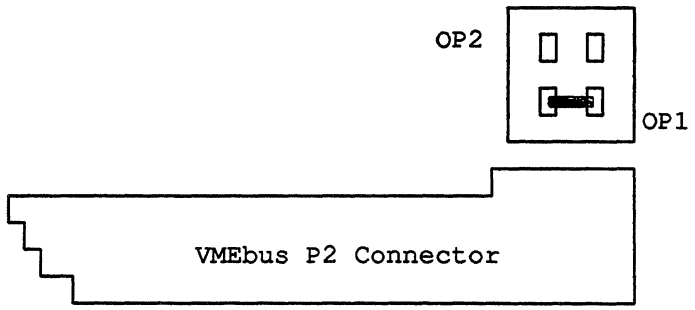


EXAMPLE CONFIGURATION: SLOT 2 VMEbus MASTER
RWD, RELEASE WHEN DONE
OB68K/VME1 BUS REQUEST/GRANT LEVEL 3

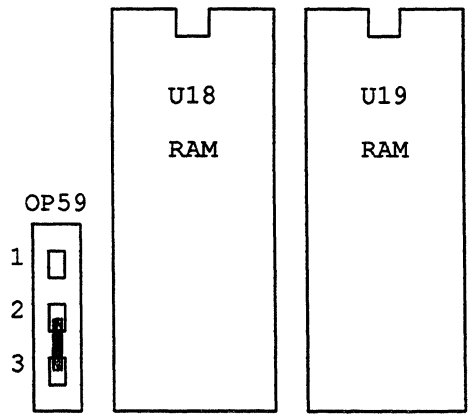
FIGURE 4.5.2

4.6 Initialize (OP1, OP59)

Jumpers are provided to select whether the onboard reset generator is to drive the VMEbus SYSRESET line or whether this board is to be reset by the SYSRESET signal. The onboard reset generator provides for both power-on and push button reset. If OP59 2-3 and OP1 are installed, SYSRESET will be driven by this board. In this configuration, the RESET instruction will also drive the SYSRESET line. If OP59 1-2 is installed and OP1 is removed, this board will be reset by the SYSRESET signal.



OP1	OP59	RESET OPTIONS
IN	2-3	Board Drives Vmebus SYSRESET
OUT	1-2	VMEbus SYSRESET Drives Board
ALL OTHER COMBINATIONS NOT SUPPORTED		



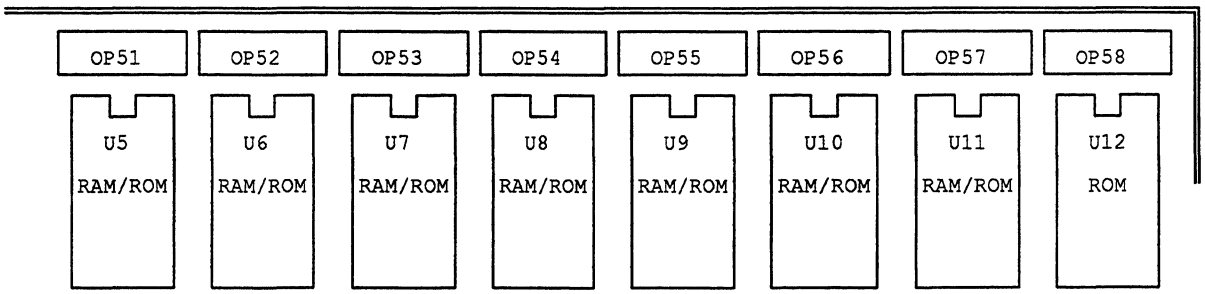
RESET OPTION CONFIGURATION
FIGURE 4.6

4.7 RAM/ROM Installation

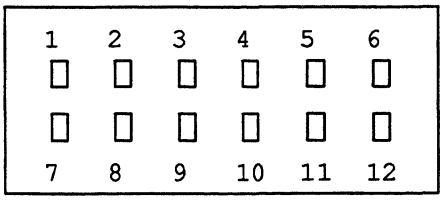
The OB68K/VME1 provides eight pairs of memory sockets that can be configured for 8K or 32K static RAM chips; or 8K, 16K, 32K, or 64K ROM, PROM, or EPROM chips. Several options must be configured when installing RAM/ROM chips on the OB68K/VME1 board; socket configuration, RAM/ROM type, base address, and block size. Note that only one type of RAM and one type of ROM may be used at any time. Also note that ROM must reside in sockets U25 and U26 to allow the board to reset properly, see Section 3.8 for additional information.

4.7.1 RAM/ROM Socket Configuration Options (OP51-OP58)

Jumper options OP51-OP58 configure the sockets to accept a particular type of RAM/ROM chip. Shown in Figures 4.7.1A through 4.7.1C are the location of the socket configuration options, RAM/ROM type configuration and RAM/ROM socket priority. Figures 4.8.2 and 4.8.3 show compatible RAM/ROM chip pinouts for reference.



PIN	FUNCTION
1	N/C
2	A15
3	A15
4	RAM/ROM PIN 1
5	A16
6	A14
7	R/W
8	RAM/ROM PIN 27
9	+5 VOLTS
10	+5 VOLTS
11	+5 VOLTS
12	RAM/ROM PIN 26

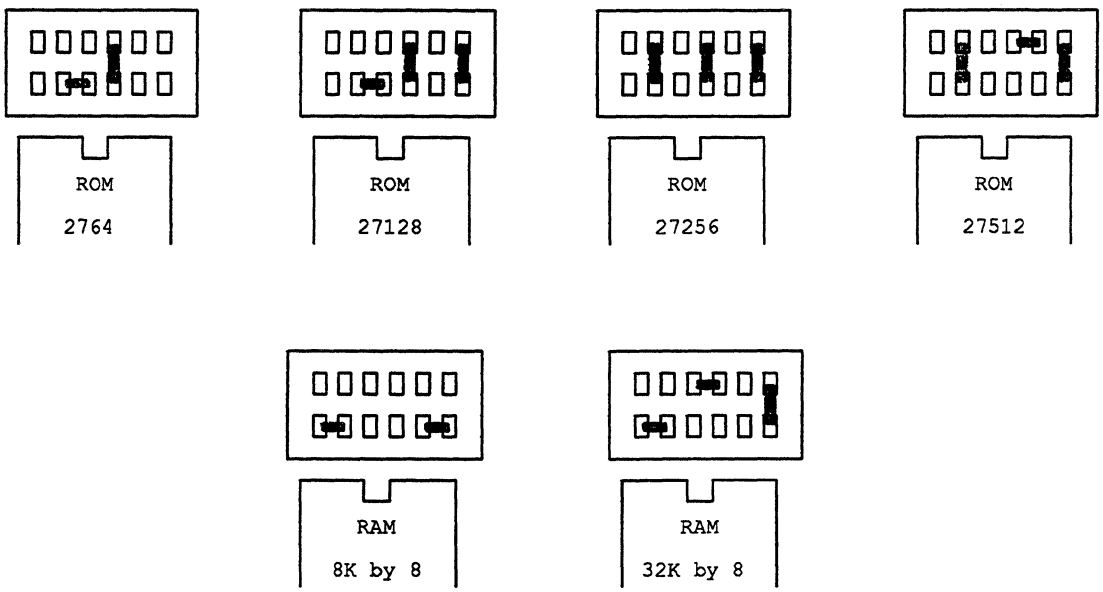


OP51 - OP58

OPTION	CONFIGURATION FUNCTION		
OP51	RAM PAIR 0		ROM PAIR 7
OP52	RAM PAIR 1		ROM PAIR 6
OP53	RAM PAIR 2		ROM PAIR 5
OP54	RAM PAIR 3	OR	ROM PAIR 4
OP55	RAM PAIR 4		ROM PAIR 3
OP56	RAM PAIR 5		ROM PAIR 2
OP57	RAM PARI 6		ROM PAIR 1
OP58	---------		ROM PAIR 0

FIGURE 4.7A RAM/ROM OPTION CONFIGURATION AND LOCATION

RAM/ROM OPTION CONFIGURATION (CONTINUED)



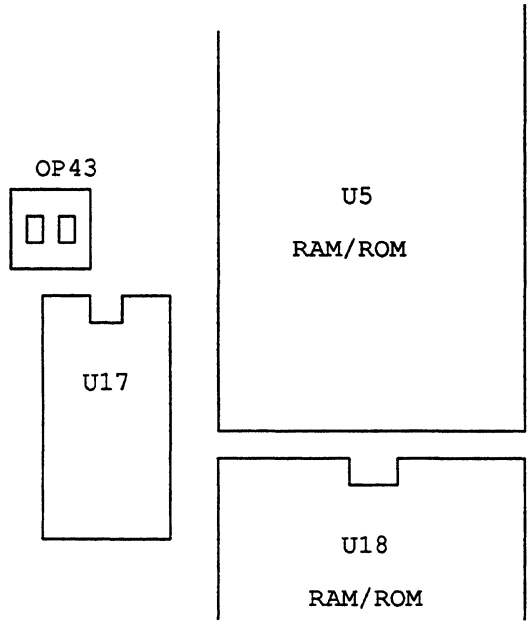
RAM/ROM TYPE OPTION CONFIGURATION
FIGURE 4.7B

ROM	EVEN BYTE	ODD BYTE	RAM
PR7	U18	U5	PR0
PR6	U19	U6	PR1
PR5	U20	U7	PR2
PR4	U21	U8	PR3
PR3	U22	U9	PR4
PR2	U23	U10	PR5
PR1	U24	U11	PR6
PR0	U25	U12	-----

RAM/ROM SOCKET CONFIGURATION
TABLE 4.7C

4.7.2.1 RAM Type Configuration (OP43)

The configuration of option OP43 selects the on-board circuitry for the type of RAM installed in the board, thereby, determining the amount of addressing space for each socket pair. Option OP43 installed, sets the RAM chip size for 32K chips, removed sets the RAM chip size for 8K chips.

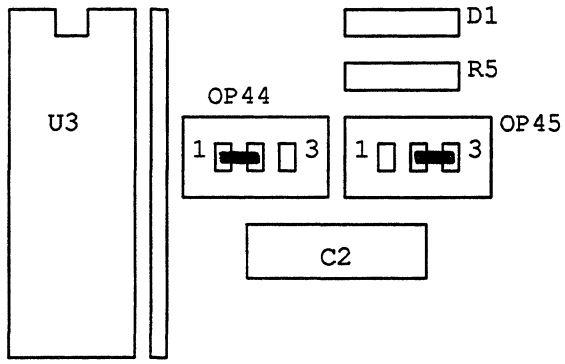


OP43	RAM CHIP SIZE
OUT	8K by 8
IN	32K by 8

RAM SIZE SELECTION OPTION
FIGURE 4.7.2.1

4.7.2.2 ROM Type Configuration (OP44,OP45)

The configuration of options OP44 and OP45 selects the on-board circuitry for the type of ROM chips installed. Use table below to configure for ROM type.



ROM TYPE	SIZE	OP44	OP45
2764	8K	2-3	2-3
27128	16K	1-2	2-3
27256	32K	2-3	1-2
27512	64K	1-2	1-2

ROM SIZE SELECTION OPTION
FIGURE 4.7.2.2

4.7.3 RAM/ROM Block Size (OP46-OP50, OP61,OP62)

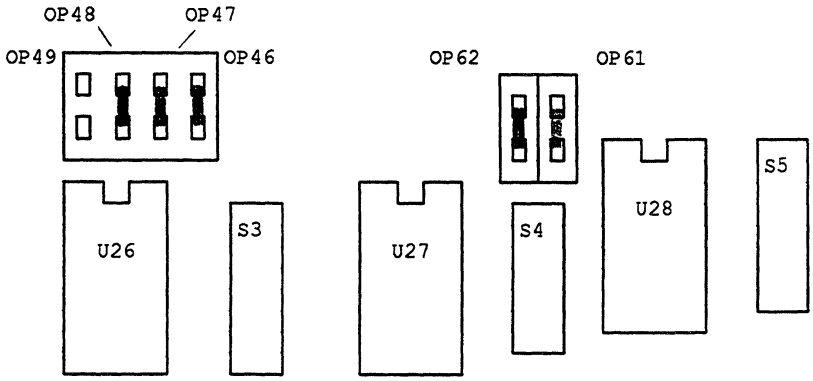
As the size of the memory chips increases, the size of the memory block allocated to on-board RAM and ROM may also need to increase (depending upon the number of chips installed).

The factory standard provides a 32K block of RAM space by connecting OP50-2 to OP50-3. This is increased to a 64K byte block by connecting OP50-1 to OP50-2. Removing jumpers OP49, OP61 and OP62 will further increase the RAM block to 128K, 256K, and 512K bytes, respectively. Choose a block size large enough to accommodate the total amount of RAM installed.

ROM space is selected for 64K bytes as the factory standard. Removing jumpers OP47, OP48 and OP46 will increase the ROM space to 256K, 512K and 1M bytes, respectively. Choose a block size large enough to accommodate the total amount of ROM installed.

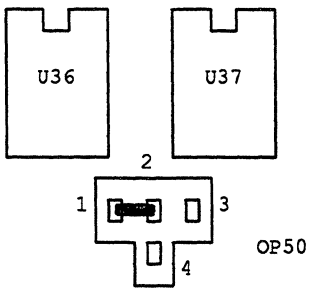
When jumper OP61 or OP62 is removed to increase RAM Block Size, the corresponding jumper in S3 must also be removed.

When jumper OP46, OP47 or OP48 is removed to increase ROM Block Size, the corresponding jumper in S4 must also be removed.



ROM CONFIGURATION			
BLOCK SIZE	OP46	OP47	OP48
128K	IN	IN	IN
256K	IN	OUT	IN
512K	OUT	IN	OUT
1Meg	OUT	OUT	OUT

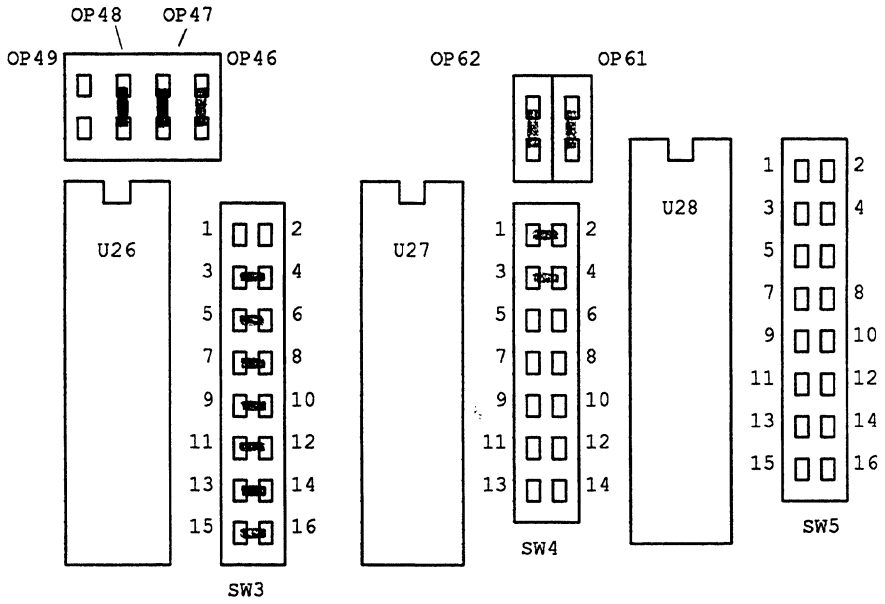
RAM CONFIGURATION		
BLOCK SIZE	OP61	OP62
128K	IN	IN
256K	OUT	IN
512K	OUT	OUT



OP50	BLOCK SIZE OPTION
1-2	64K or LARGER BLOCK SIZE
2-3	32K BLOCK SIZE
3-4	Setting no longer supported

4.8 Base Address Options (S3, S4, S5)

The base addresses of the RAM, ROM and I/O memory blocks are independently selectable using jumper groups S3, S4, S5, respectively. Each base address is established by comparing the upper address lines with the jumper configuration. The jumper configuration includes the block size options, which determine if an address line is "Active" or a "Don't Care". The S3, S4, and S5 jumpers, are viewed as an eight bit number (seven for ROM). These jumpers may represents a "zero" if installed, a "one" if removed, or a "don't care" if the block size jumper is removed. These jumpers are shown in Figure 4.8 in their factory standard configuration.



RAM ADDRESS = $00000			
S3 = RAM BASE ADDRESS			
PIN#	ADDR	ACT	D/C
1	A16		X
3	A17	IN	
5	A18	IN	
7	A19	IN	
9	A20	IN	
11	A21	IN	
13	A22	IN	
15	A23	IN	

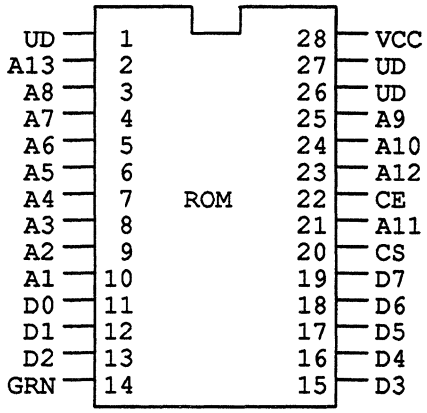
ROM ADDRESS = $F80000			
S4 = ROM BASE ADDRESS			
PIN#	ADDR	ACT	D/C
1	A17	IN	
3	A18	IN	
5	A19	OUT	
7	A20	OUT	
9	A21	OUT	
11	A22	OUT	
13	A23	OUT	

I/O ADDRESS = $FF0000			
S5 = I/O BASE ADDRESS			
PIN#	ADDR	ACT	D/C
1	A16	OUT	
3	A17	OUT	
5	A18	OUT	
7	A19	OUT	
9	A20	OUT	
11	A21	OUT	
13	A22	OUT	
15	A23	OUT	

ACT = Active Address Line:
IN = 0
OUT = 1
D/C = Don't Care Address Line:
Made don't care by BLOCK SIZE options.

See **APPENDIX** for detailed address configuration tables.

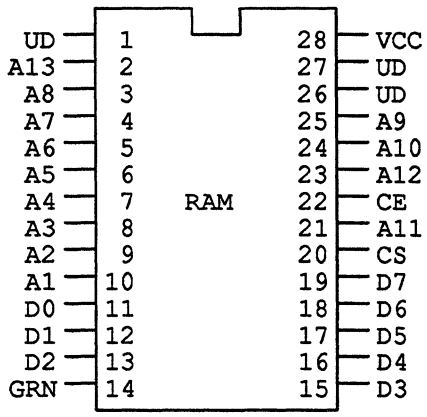
BASE ADDRESS OPTIONS
FIGURE 4.8.1



PIN NAME	FUNCTION:
A1-A13	ADDRESS LINES
D0-D7	OUTPUT LINES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
PGM	PROGRAM
Vcc	POWER
GND	GROUND
UD	USER DEFINABLE SOCKET PINS ON OB68K/VME1 (+5V; R/W; A12; A14; A15)

NOTE: ONLY EPROMS THAT HAVE COMPATIBLE PINOUTS (AS SHOWN) MAY BE USED ON THE OB68K/VME1.

ROM CHIP PINOUT
FIGURE 4.8.2



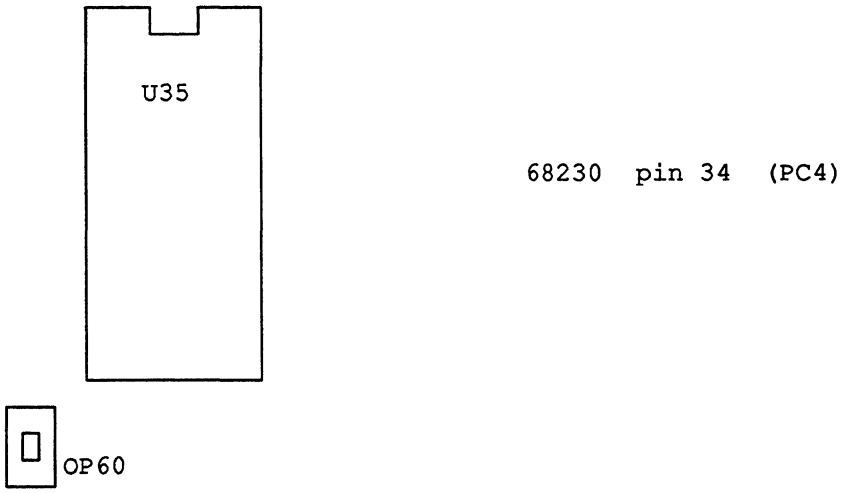
PIN NAME	FUNCTION:
A1-A13	ADDRESS LINES
D0-D7	INPUT/OUTPUT LINES
CE	CHIP ENABLE
	OUTPUT ENABLE
R/W	READ/WRITE ENABLE
Vcc	POWER
GND	GROUND
UD	USER DEFINABLE SOCKET PINS ON OB68K/VME1 (+5V; R/W; A12; A14; A15)

NOTE: ONLY STATIC RAMS THAT HAVE COMPATIBLE PINOUTS (AS SHOWN) MAY BE USED ON THE OB68K/VME1.

RAM CHIP PINOUT
FIGURE 4.8.3

4.9 Extra I/O Bit (Port C bit 4) Output (OP60)

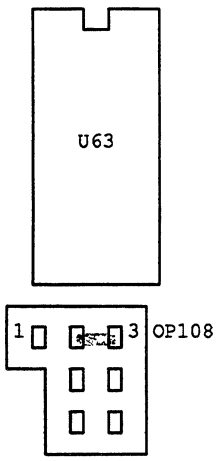
All of the available jumpers have been described above with the exception of OP60. This is the only pin of the 68230 that is undedicated. It has been terminated on a single wire wrap post to allow for user implementation of the signal, if so desired.



68230 PORT-C BIT4 OPTION
FIGURE 4.9

4.10 Miscellaneous Option (OP108)

Jumper OP108 has been included on the OB68K/VME1 to optimize the functionality of the board. This option is shown here for reference ONLY, and should NEVER be changed by the user.



MISCELLANEOUS OPTION
FIGURE 4.10

5.0 CONNECTOR PINOUTS

5.1 VMEbus P1 Connector

The P1 connector is pinned out according to the VMEbus specifications given in Table 5.1.

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

(1) See VMEbus Specification (Rev. C.1) for further information on these signals.

* Indicates Low Active.

IEEE P1014 P1 CONNECTOR PINOUT
TABLE 5.1

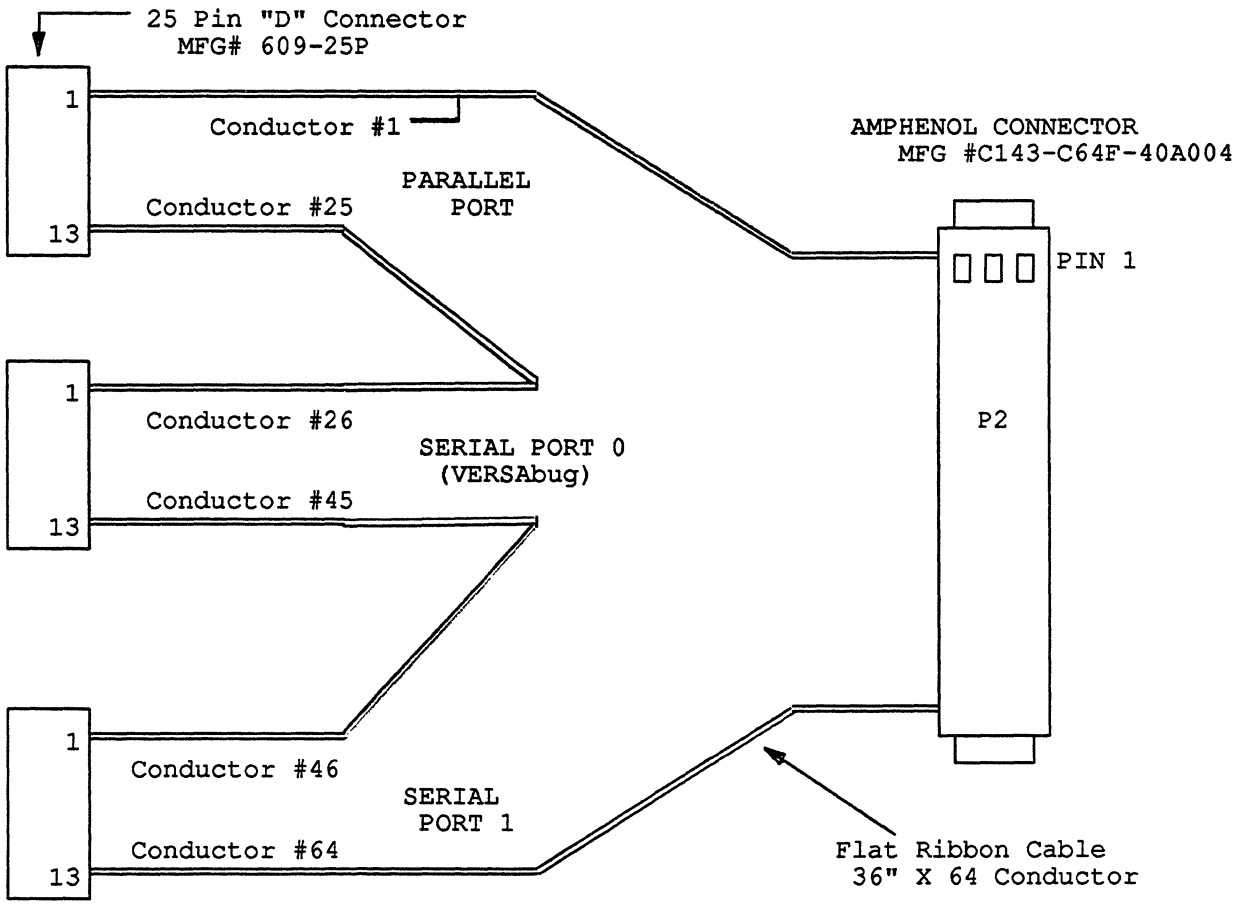
5.2 VMEbus P2 Connector

Row B of the P2 connector is defined for address and data lines needed for thirty-two bit systems. Because the OB68K/VME1 implements a 68000 processor, no connections are made to row B. Rows A and C are for user defined I/O. Both serial ports and the two parallel ports are available on P2 as shown in table 5.2.

A sixty-four pin, insulation displacement DIN 41612 connector may be used to access the I/O signals on the P2 connector. The 64 conductor ribbon cable may be terminated in three 25 contact "D" connectors as shown in Figure 5.2. The corresponding pinout for these connectors is also given in Table 5.2.

VMEbus P2	ROW C SIGNAL	= "D" CONN. PIN	VMEbus P2	ROW A SIGNAL	= "D" CONN. PIN	
1C	GND	1	1A	GND	14	
2C	PA0	2	2A	H2	15	
3C	PA2	3	3A	PA1	16	
4C	PA4	4	4A	PA3	17	
5C	PA6	5	5A	PA5	18	
6C	H1	6	6A	PA7	19	PARALLEL
7C	PB6	7	7A	PB7	20	PORT
8C	PB4	8	8A	PB5	21	
9C	PB2	9	9A	PB3	22	
10C	PB0	10	10A	PB1	23	
11C	GND	11	11A	GND	24	
12C	GND	12	12A	GND	25	
13C		13	13A	GND	1	
14C		14	14A	RXDB	2	
15C		15	15A	TXDB	3	
16C		16	16A	IP1	4	
17C		17	17A	0P1	5	SERIAL
18C		18	18A		6	PORT 0
19C		19	19A	GND	7	
20C		20	20A		8	
21C		21	21A		9	
22C		22	22A		10	
23C		23	23A	GND	1	
24C		14	24A	RXDA	2	
25C		15	25A	TXDA	3	
26C		16	26A	IP0	4	
27C		17	27A	OP0	5	SERIAL
28C		18	28A		6	PORT 1
29C		19	29A	GND	7	
30C		20	30A		8	
31C		21	31A		9	
32C		22	32A		10	

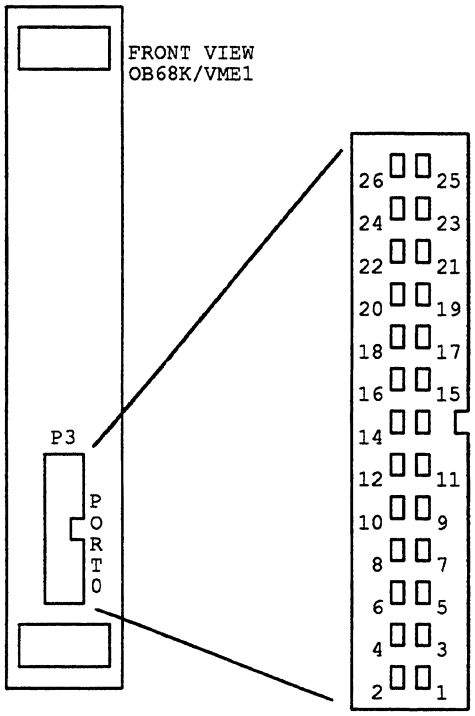
IEEE P1014 P2 CONNECTOR PINOUT
TABLE 5.2



P2 CONNECTOR CABLE
FIGURE 5.2

5.3 Front Panel Serial Port Connector

Serial port 0 is also brought out to a 26-pin connector on the front panel. The pinout of this connector, given in Table 5.3, is designed so that the user end of the cable will directly drive an RS-232C terminal using a 25-pin "D" type ribbon cable connector. Care should be taken to avoid connecting serial devices to both the front panel & P2 outputs simultaneously.



P3 Connector (Expanded View)

Signal	P3 Pin	P3 Pin	Signal
GND	1	2	N/C
RxDB	3	4	N/C
TxDB	5	6	N/C
CTS	7	8	N/C
RTS	9	10	N/C
N/C	11	12	N/C
GRN	13	14	N/C

EXPANDED P3 CONNECTION TABLE

Signal	25-"D"	P3 Pin	P3 Pin	25 "D"	Signal
GND	1	1	2	14	N/C
RxDB	2	3	4	15	N/C
TxDB	3	5	6	16	N/C
CTS	4	7	8	17	N/C
RTS	5	9	10	18	N/C
N/C	6	11	12	19	N/C
GRD	7	13	14	20	N/C
N/C	8	15	16	21	N/C
N/C	9	-	-	22	N/C
N/C	10	-	-	23	N/C
N/C	11	-	-	24	N/C
N/C	12	-	-	25	N/C
N/C	13	-	-	-	-

FRONT PANEL SERIAL PORT 0 CONNECTOR PINOUT
TABLE 5.3

5.4 Compatible Cable End Connectors

Connector numbers that are compatible with the serial and parallel I/O connectors of the OB68K/VME1 are given below. For your convenience, the numbers of the connectors for the user end of the cables are also listed below.

Serial I/O (Front Panel)

Cable connector for Computer end, 26 socket - Berg # 65484-009
Ansley # 609-2641

Cable connector for Terminal/Modem end; 25 pin "D" -
Berg # 66167-025
Ansley # 609-25P

P2 Connector Cable

Cable Connector at Computer end, 50 socket - Berg # 65484-021
Ansley # 609-5041

Cable connector for Terminal/Modem end; 3 - 25 pin "D" -
Berg # 66167-025
Ansley # 609-25P

NOTE that these are common ribbon cable connectors, and although the part numbers above are only for the Berg and T & /Ansley parts, equivalent connectors are available from several vendors.

For user convenience, Omnibyte can furnish an assembled parallel and serial and P2 connector cable. Order numbers for these cables are given in Section 9.0. The (front panel) serial I/O cable is a 26 conductor cable terminated in a 26 contact connector at the computer end and terminated in a 25 pin "D" connector on the user end. The P2 Connector (64 contact) connector and cable carry the signals from both serial ports and the two parallel ports. It is split into three sections, each terminated with a 25 pin "D" connector. See Figure 5.2 for a diagram of the P2 Connector Cable.

6.0 MEMORY DECODING

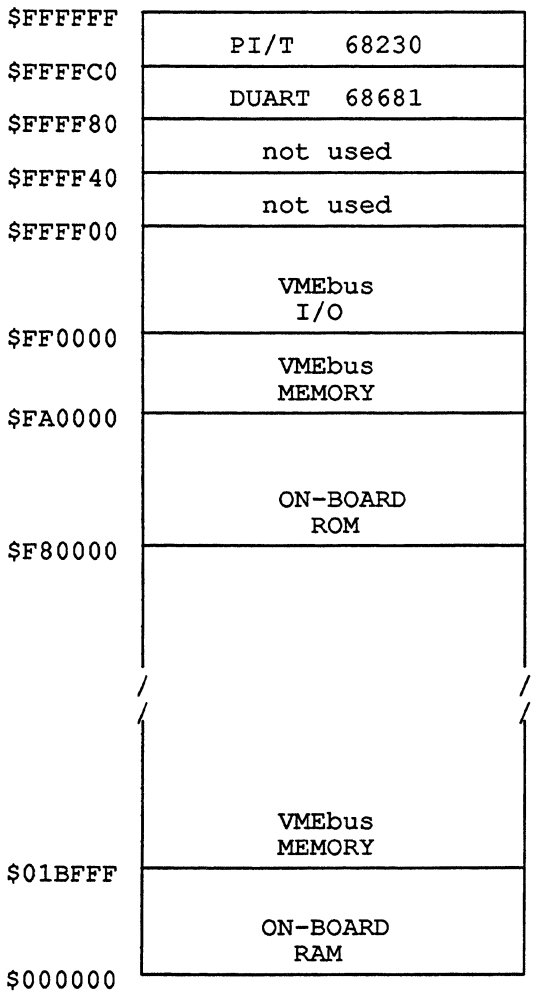
According to the VMEbus specification, the OB68K/VME1 supports a 16 megabyte address space using only connector P1. From this space, three blocks of memory are selected for use by I/O and onboard RAM and onboard ROM space. Any address that does not fall within these three blocks automatically defaults to global VMEbus memory.

6.1 Memory Map

The factory standard memory map is shown in Figure 6.1. Jumper setting for this memory map are as follows. See section 4.9 for additional information.

S3	Ram Base Address	00000000 = $00
S4	Rom Base Address	00011111 = $F8
S5	I/O Base Address	11111111 = $FF

JUMPER IN = 0
JUMPER OUT = 1



* Factory Standard

FIGURE 6.1 MEMORY MAP

6.2 I/O Address Assignments

Tables 6.2.1 and 6.2.2, show the address assignments for the serial and parallel circuits, respectively. The values given are the factory standard address assignments that may be relocated to any other 64K byte boundary using Jumper groups S3, S4 and S5. Note that on-board parallel and serial peripherals have 8- bit paths and that they are addressed at odd memory locations only.

68681 SERIAL PORT: PORT 0 = REGISTER B, PORT 1 = REGISTER A		
READ(R/WN=1)	WRITE (R/WN=0)	BASE ADDRESS
MODE REGISTER A (MR1A, MR2A)	MODE REGISTER A (MR1, MR2)	$FFFF81
STATUS REGISTER A (SRA)	CLOCK SELECT REG. A (CSRA)	$FFFF83
RESERVED	COMMAND REGISTER A (CRA)	$FFFF85
RX HOLDING REGISTER A (RHRA)	TX HOLDING REGISTER A (THRA)	$FFFF87
INPUT PORT CHANGE REG. (IPCR)	AUX. CONTROL REGISTER (ACR)	$FFFF89
INTERRUPT STATUS REG. (ISR)	INTERRUPT MASK REG. (IMR)	$FFFF8B
COUNTER/TIMER UPPER (CTU)	C/T UPPER REGISTER (CTUR)	$FFFF8D
COUNTER/TIMER LOWER (CTL)	C/T LOWER REGISTER (CTLR)	$FFFF8F
MODE REGISTER B (MR1B, MR2B)	MODE REGISTER B (MR1B, MR2B)	$FFFF91
STATUS REGISTER B (SRB)	CLOCK SELECT REG. B (CSRB)	$FFFF93
RESERVED	COMMAND REGISTER B (CRB)	$FFFF95
RX HOLDING REGISTER B (RHRB)	TX HOLDING REGISTER B (THRB)	$FFFF97
INTERRUPT VECTOR REG. (IVR)	INTERRUPT VECTOR REG. (IRB)	$FFFF99
INPUT PORT	OUTPUT PORT CONF. REG. (OPCR)	$FFFF9B
START COUNTER COMMAND	SET OUTPUT PORT BITS COMMAND	$FFFF9D
STOPCOUNTERCOMMAND	RESET OUTPUT PORT BITS COMMAND	$FFFF9F
	**	$FFFFA1
		$FFFFA3
NOTE:		$FFFFA5
		$FFFFA7
1) **READS AND/OR WRITES TO THESE ADDRESS LOCATIONS WILL CAUSE TRAP ERRORS, SINCE THESE ARE UNDEFINED AND UN-IMPLEMENTED LOCATIONS.		$FFFFA9
		$FFFFAB
		$FFFFAD
		$FFFFAF
		$FFFFB1
		$FFFFB3
2) *RESERVED*: READING OF THESE RESERVED REGISTERS WILL PLACE THE DUART IN A DIAGNOSTIC MODE; ONLY A HARDWARE RESET WILL EXIT THIS MODE.		$FFFFB5
		$FFFFB7
		$FFFFB9
		$FFFFBB
		$FFFFBD
		$FFFFBF

REGISTER ASSIGNMENT FOR 68681 DUART
TABLE 6.2.1

The following table is for users who use off-sets from a pointer register. For this example, the pointer register will be A0, and will have $FFFF81 written into it.

Address	Hex Off-Set	Decimal Off-Set	ADDRESS	HEX Off-Set	Decimal Off-Set
$FFFF81	$0	0	$FFFF91	$10	16
FFFF83	$2	2	FFFF93	$12	18
FFFF85	$4	4	FFFF95	$14	20
FFFF87	$6	6	FFFF97	$16	22
FFFF89	$8	8	FFFF99	$18	24
FFFF8B	$A	10	FFFF9B	$1A	26
FFFF8D	$C	11	FFFF9D	$1C	28
FFFF8F	$E	14	FFFF9F	$1E	30

PI/T PARALLEL PORT 68230		
REGISTER NAME	MNEMONIC	PHYSICAL ADDRESS
Port General Control Reg.	PGCR	$FFFFC1
Port Service Request Reg.	PSRR	$FFFFC3
Port A Data Direction Reg.	PADDR	$FFFFC5
Port B Data Direction Reg.	PBDDR	$FFFFC7
Port C Data Direction Reg.	PCDDR	$FFFFC9
Port Interrupt Vector Reg.	PIVR	$FFFFCB
Port A Control Reg.	PACR	$FFFFCD
Port B Control Reg.	PBCR	$FFFFCF
Port A Data Reg.	PADR	$FFFFD1
Port B Data Reg.	PBDR	$FFFFD3
Port A Alternate Reg.	PAAR	$FFFFD5
Port B Alternate Reg.	PBAR	$FFFFD7
Port C Data Reg.	PCDR	$FFFFD9
Port Status Reg.	PSR	$FFFFDB
N.A.		$FFFFDD
N.A.		$FFFFDF
Timer Control Reg.	TCR	$FFFFE1
Timer Interrupt Vector	TIVR	$FFFFE3
N.A.		$FFFFE5
Counter Preload Reg High	CPRH	$FFFFE7
Counter Preload Reg Middle	CPRM	$FFFFE9
Counter Preload Reg Low	CPRL	$FFFFEB
N.A.		$FFFFED
Count Reg High	CNTRH	$FFFFEF
Count Reg Middle	CNTRM	$FFFFF1
Count Reg Low	CNTRL	$FFFFF3
Timer Status Reg	TSR	$FFFFF5

REGISTER ASSIGNMENTS FOR 68230 PI/T
TABLE 6.2.2

The following table is for users who use off-sets from a pointer register. For this example, the pointer register could be A0, and would have $FFFF81 written into it.

ADDRESS	Hex Off-Set	Decmial Off-set	ADDRESS	Hex Off-Set	Decmial Off-Set
$FFFFC1	$0	0	$FFFFD9	$18	24
$FFFFC3	$2	2	$FFFFDB	$1A	26
$FFFFC5	$4	4	$FFFFDD	$1C	28
$FFFFC7	$6	6	$FFFFDF	$1E	30
$FFFFC9	$8	8	$FFFFE1	$20	32
$FFFFCB	$A	10	$FFFFE3	$22	34
$FFFFCD	$C	12	$FFFFE5	$24	36
$FFFFCF	$E	14	$FFFFE7	$26	38
$FFFFD1	$10	16	$FFFFE9	$28	40
$FFFFD3	$12	18	$FFFFEB	$2A	42
$FFFFD5	$14	20	$FFFFED	$2C	44
$FFFFD7	$16	22	$FFFFEF	$2E	46

6.3 Address Modifier Codes

On each memory access, VMEbus masters must assert an allowed value for the address modifier codes AM0...AM5. The OB68K/VME1 outputs FC0, FC1 and FC2 on AM0, AM1 and AM2, respectively. Address modifier 3 is strapped high because all allowed AM codes require AM3 to be be high. AM5 is high for all short address (16-bit) and standard address (24-bit) data transfers. Address modifier four distinguishes between standard accesses (AM4=High) and short accesses (AM4=L). Only I/O accesses are addressed using the short address mode. The following address modifier codes are supported:

Hexadecimal Code	Address Modifier	Functions
3E	HH HHHL	Std. Supervisory Prog.
3D	HH HHLH	Std. Supervisory Data
3A	HH HLHL	Std. User Prog.
39	HH HLLH	Std. User Data
2D	HL HHLH	Short Supervisory I/O
29	HL HLLH	Short User I/O

Note: Only the I/O space is accessed using the short (16-bit address) mode.

ADDRESS MODIFIER CODES
TABLE 6.3

7.0 VME1bug TERMINAL MONITOR/DEBUGGER PROGRAM

A terminal monitor/debugger program, VME1bug, is available from Omnibyte for use with your OB68K/VME1. This program is licensed from Motorola Inc. by Omnibyte and is provided as object code in two 16K (27128) PROMS.

VME1bug allows the usual terminal interaction features of display, modify, load and dump memory, run programs with breakpoints, and register display and modify. In addition VME1bug includes a HELP display, memory test, block fill, block move and one line assembler/disassembler capabilities.

8.0 WARRANTY INFORMATION

All items manufactured and sold by Omnibyte Corporation are warranteed against defects in materials or workmanship and are guaranteed to meet specifications in effect at the time of manufacture for a period of (2) years from the date of delivery, to the original purchaser only.

Omnibyte's responsibility under this warranty is limited to repair or replacement of any item (at our option) returned to the factory during the warranty period, freight prepaid. Omnibyte shall either repair or replace the item, provided that the failure of the item, in our opinion, was not due to abuse, modification or acts of God. **EXCEPT AS OTHERWISE INDICATED, THERE ARE NO OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.** Omnibyte's liability shall be limited to the purchase price of the item or items, and Omnibyte shall not be responsible or liable for any lost profits or consequential damages, or for any claim against the purchaser by any party.

"NOTE"

ALL BOARDS BEING RETURNED TO OMNIBYTE CORPORATION FOR REPAIR MUST BE ACCOMPANIED WITH AN RMA NUMBER (RETURN MATERIAL AUTHORIZATION). THIS NUMBER WILL BE ISSUED TO YOU BY OMNIBYTE WHEN REQUESTING AUTHORIZATION TO RETURN YOUR BOARD. ALSO, AN EXPLANATION OF THE PROBLEM AND NAME AND PHONE NUMBER OF THE PERSON USING THE BOARD WHEN THE PROBLEM OCCURRED SHOULD BE ENCLOSED WITH THE RETURNED BOARD. THIS PROCEDURE WILL HELP US TO SPEED UP THE REPAIR AND RETURN OF YOUR BOARD.

ANY BOARDS RECEIVED BY OMNIBYTE CORPORATION WITHOUT A RMA NUMBER WILL BE RETURNED TO SENDER, UNTIL A RMA NUMBER HAS BEEN OBTAINED.

9.0 ORDERING INFORMATION

Order numbers for the Omnibyte OB68K/VME1 computer, Monitor/Debugger program and other accessories are as follows:

```
OB68K/VME1 Single Board Computer (0K RAM,12.5MHz).....OB68K/VME1-0K-00-12

OB68K/VME1 Single Board Computer (16K RAM,12.5MHz).....OB68K/VME1-16K-00-12

VME1bug in two 16K X 8 PROMS.....OB68K/VERSA-VME1-128K

Front Panel Serial I/O Cable Assy.-10' long .....OB68K1SIC

VME1 P2 Connector Interface Cable .....OBFG01285
       (See Figure 5.2 for details)

Additional pair RAM chips (2-8KX8 CMOS, 120nS).....OBSA01839
```

OMNIBYTE's terms are: NET 30 DAYS with approved credit. The F.O.B. point is West Chicago, Illinois. Items will be shipped United Parcel Service surface unless otherwise instructed.

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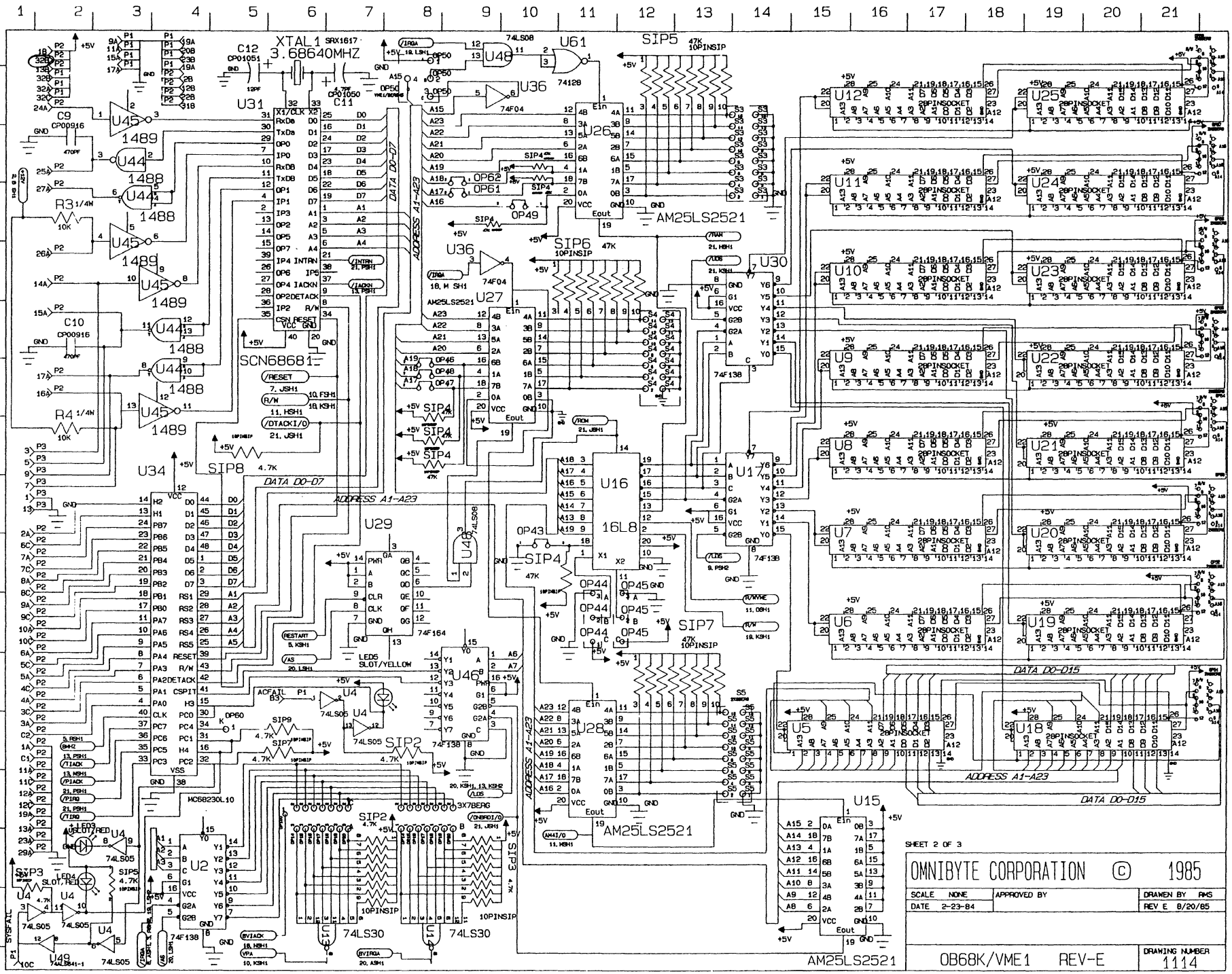
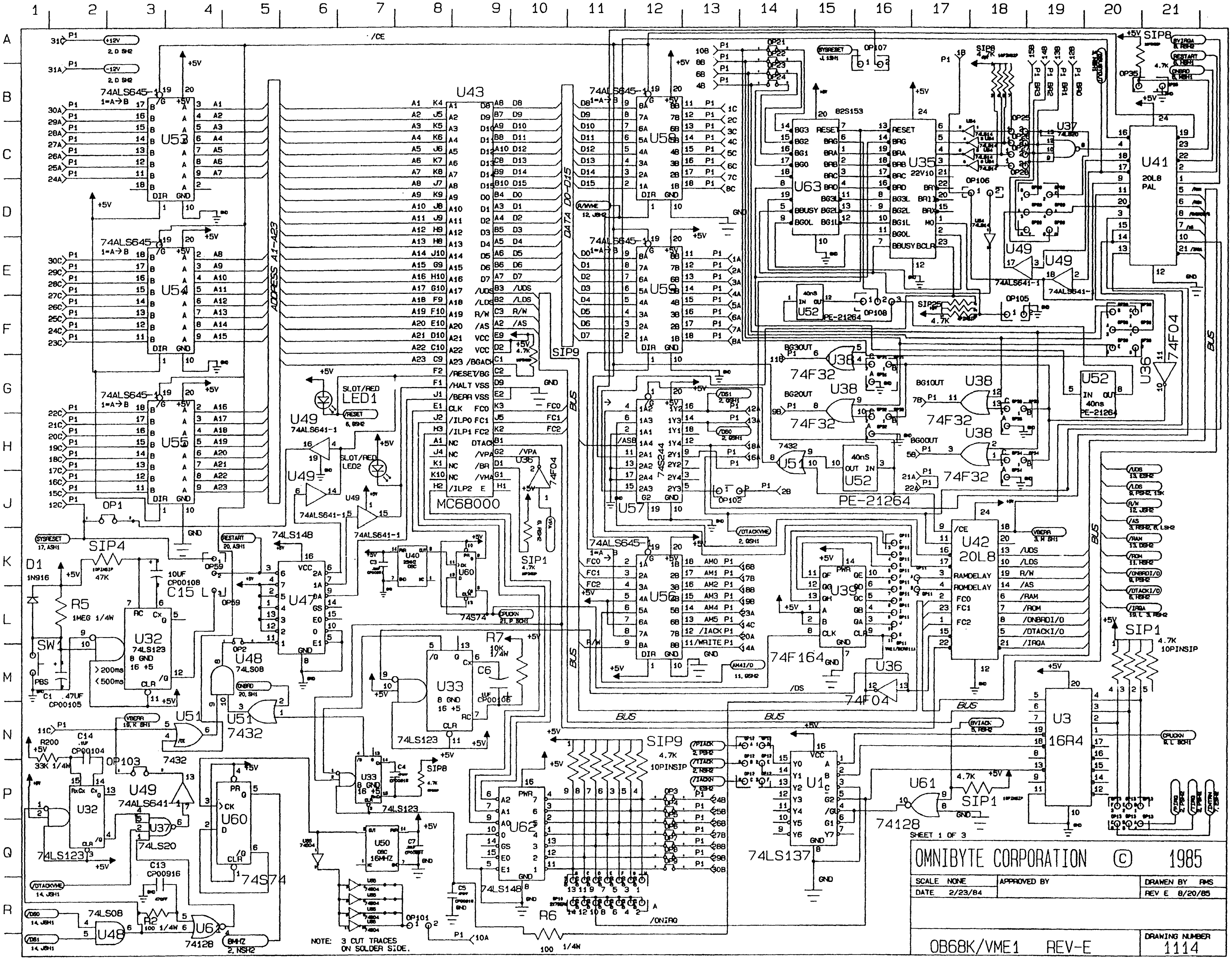
10.0 OB68K/VME1 SCHEMATIC DIAGRAMS

The electrical schematic diagrams are shown in Figures 10.1, 10.2 and 10.3. Factory standard jumper options are shown as dotted lines in these figures. The parts list for the OB68K/VME1 is listed in Table 10.1.

"NOTE"


XTAL1 SRX1617
3.68640MHZ
SCN68681
MC68230L10
74LS08
74128
74F04
74F138
74F164
74LS05
74LS30
AM25LS2521
16L8
74LS241-1
SIP1
SIP2
SIP3
SIP4
SIP5
SIP6
SIP7
SIP8
SIP9
10PINSIP
47K
4.7K
DATA D0-D7
ADDRESS A1-A23
DATA D0-D15
ADDRESS A1-A23
SHEET 2 OF 3
OMNIBYTE CORPORATION © 1985
SCALE NONE
APPROVED BY
DRAWN BY RMS
DATE 2-23-84
REV E 8/20/85
OB68K/VME1 REV-E
DRAWING NUMBER
1114


OMNIBYTE CORPORATION © 1985
SCALE NONE
APPROVED BY
DRAWN BY RMS
DATE 2/23/84
REV E 8/20/85
SHEET 1 OF 3
OB68K/VME1 REV-E
DRAWING NUMBER
1114
NOTE: 3 CUT TRACES ON SOLDER SIDE.
MC68000
ADDRESS A1-A23
DATA D0-D15

PART NUMBER	DESCRIPTION	# OF PIECES	LOCATION
OBCN00406	26 RT ANGLE PIN HEADERS	1	P3
OBCN01160	705-C133-714A-96P Connector	2	P1, P2
OBCP00104	.1 uF CAP	19	C8, 14, 17, 19, 21, 22 23, 30, 31, 32-38, 40-42
OBCP00105	.47 uF CAP	1	C1
OBCP00106	1.0 uF CAP	1	C6
OBCP00108	10 uF CAP (TANTALUM)	1	C15
OBCP00110	47 uF CAP	1	C2
OBCP00881	.22 uF CAP	8	C3, 7, 16, 20, 24, 25, 26, 28
OPCP00916	470 pF CAP	5	C4, 5, 9, 10, 13
OBCP01050	4.7 pF CAP	1	C11
OBCP01051	12 pF CAP	1	C12
OBDI00137	1N916	1	D1
OBHW01186	2-56 NUT	4	P1, P2
OBHW01187	2-56 X 1/2 IN MACHINE SCREW	4	P1, P2
OBIC00192	74LS08	1	U48
OBIC00209	74S74	1	U60
OBIC00340	MC68230L10 PI/T	1	U34
OBIC00364	PAL34.0 (PAL16L8CN)	1	U16
OBIC00585	PAL33.0 (PAL16R4ACN)	1	U3
OBIC00795	74LS137	1	U1
OBIC00822	74128	1	U61
OBIC00824	74LS148	2	U47, U62
OBIC00832	MC1488/75188P	1	U44
OBIC00833	MC1489/75189P	1	U45
OBIC00940	SCN68681ACIN40 DUART	1	U31
OBIC01040	12.5MHz MC68000 IN 'R' PK	1	U43
OBIC01132	74LS123	2	U32, U33
OBIC01154	74F20	1	U37
OBIC01155	74F138	4	U2, U17, U30, U46
OBIC01156	25LS2521PCB	4	U15, U26-U28
OBIC01157	74F164	2	U29, U39
OBIC01158	74F32	2	U38, U51
OBIC01159	74LS05	1	U4
OBIC01185	PE21264/DL34CB400 DELAY LINE	1	U52
OBIC01191	MC74F04	1	U36
OBIC01283	8K X 8 CMOS RAM HM6264-12P	2	U5, U18
OBIC01409	74LS30	2	U13, U14
OBIC01514	PAL35.0 (82S153)	1	U63
OBIC01515	PAL36.0 (PAL-AMD 22V10)	1	U35
OBIC01561	74ALS641-1	1	U49
OBIC01562	74AS244	1	U57
OBIC01565	PAL37.0 (PAL20L8ACN)	1	U41
OBIC01565	PAL38.0 (PAL20L8ACN)	1	U42
OBIC01718	74ALS645-1N	6	U53, U54, U55, U56, U58, U59
OBJP00809	B-JUMP	53	STD. FACTORY CONFIG

OB68K/VME1 PARTS LIST
TABLE 10.1

PART NUMBER	DESCRIPTION	# OF PIECES	LOCATION
OBLE00153	SLOT SELECT LEDS (RED)	3	L2, L3, L4
OBLE00835	DIALIGHT-YELLOW	2	L1, L5
OBPC01918	VME Circuit Board	1	
OBRE00011	100 OHM 1/4W 5%	2	R2, R6
OBRE00041	10K OHM 1/4W 1%	2	R3, R4
OBRE00042	10K OHM 1/4 5%	1	R7
OBRE00048	33K OHM 1/4W 5%	1	R200
OBRE00053	1M OHM 1/4W 5%	1	R5
OBSA00529	2 PIN BERG STICK	7	OP11, OP35, OP43, OP101, OP102, OP103, OP105
OBSA00649	7 PIN BERG STICK	1	OP14
OBSA00759	3 PIN BERG STICK	5	OP44, OP45, OP50, OP59 OP59, OP108
OBSA00760	4 PIN BERG STICK	1	OP31
OBSA00868	1 X 9 PIN STRIP	1	OP11
OBSA00921	1 PIN BERG STICK	3	OP50,OP60, OP100
OBSA00987	2 X 3 PIN STRIP	4	OP12, OP13, OP27, OP29
OBSA00988	2 X 2 PIN STRIP	2	OP1, OP106
OBSA01060	2 X 8 PIN STRIP	2	S3, S5
OBSA01061	2 X 6 PIN BERG STRIP	3	OP51, OP52, OP53
OBSA01062	2 X 4 PIN STRIP	4	OP21,OP28, OP31, OP46
OBSA01280	2 X 7 PIN STRIP	4	OP3, OP10, OP14, S4
OBSA01960	2 X 30 PIN STRIP	1	OP54 - OP58
OBSK00382	20 PIN LOW PROFILE SOCKET	3	U3, U16, U63
OBSK00385	28 PIN LOW PROFILE SOCKET	16	U5-U12, U18-U25
OBSK00386	40 PIN LOW PROFILE SOCKET	1	U31
OBSK00574	48 PIN SOCKET	1	U34
OBSK01056	68 PIN 'R' PACKAGE SOCKET	1	U43
OBSK01476	24 PIN SLIM LOW PROFILE SKT	3	U16, U41, U42
OBSK01519	4 PIN OSCILLATOR SOCKET	2	U40, U50
OBSP00064	4.7K OHM SIP (10-PIN)	5	SP1-3, SP8, SP9
OBSP00913	47K OHM 10 PIN SIP	4	SP4-7
OBSP01053	4.7K OHM 4 PIN SIP	1	SIP25
OBSW00163	PUSH BUTTON SWITCH	1	SW1
OBXT01020	3.6864 MHz CRYSTAL	1	X1
OBXT01764	25.0 MHz OSCILLATOR	1	U40
OBXT01151	16.0 MHz OSCILLATOR	1	U50

OB68K/VME1 PARTS LIST - CONTINUED
TABLE 10.1

FRONT PANEL

PART NUMBER	DESCRIPTION	# OF PIECES
OBCH01226	VME FRONT PANEL	1
OBHW01217	HEXAGON NUT; M 2.5	3
OBHW01218	SPRING WASHER (LOCKWASHER)	3
OBHW01219	FLATHEAD SCREW M2.5 X 10	1
OBHW01220	FILLISTER HEAD SCREW (X10)	2
OBHW01221	CAPTIVE SCREW RETAINER	2
OBHW01223	COLLAR SCREW	2
OBHW01224	P.C. BOARD HOLDER	3
OBHW01225	FRONT PANEL HANDLE	2

OB68K/VME1 PARTS LIST - CONTINUED
TABLE 10.1

11.0 APPENDICES

The Appendices in this manual contain information pertinent to the operation of the OB68K/VME1 Single Board Computer.

11.1 Appendix I (RAM/ROM CONFIGURATION TABLES)

Appendix I contains information and tables to help the user configure the RAM and ROM devices on the OB68K/VME1.

APPENDIX I (RAM/ROM CONFIGURATION TABLES)

The appendix is divided into two sections. Section one deals with configuring the ROM while section two deals with configuring RAM.

ROM CONFIGURATION:

To properly configure the Base Address for the On-Board ROM requires the following steps to be completed:

Step 1. Configure OP44 and OP45 for type of ROM chips (see section 4.7.2.1).

Step 2. Configure OP51-OP58, as needed, for type of ROM chip (see section 4.7.1).

Step 3. Configure S4 for base address per following charts.

Step 4. Verify proper /DTACK setting for type of ROM chips.

The following charts are used to configure ROM base address via S4.

0 = Jumper installed.
1 = Jumper removed.
B = Jumper must be removed for block size requirement.
NOTE: Corresponding OPtion jumpers must also be removed:
B in column 1 = OP47 removed.
B in column 3 = OP48 removed.
B in column 5 = OP46 removed.

ROM SIZE = 2764

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$000000	0	0	0	0	0	0	0
020000	0	0	0	0	0	0	1
040000	0	0	0	0	0	1	0
060000	0	0	0	0	0	1	1
080000	0	0	0	0	1	0	0
0A0000	0	0	0	0	1	0	1
0C0000	0	0	0	0	1	1	0
0E0000	0	0	0	0	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$100000	0	0	0	1	0	0	0
120000	0	0	0	1	0	0	1
140000	0	0	0	1	0	1	0
160000	0	0	0	1	0	1	1
180000	0	0	0	1	1	0	0
1A0000	0	0	0	1	1	0	1
1C0000	0	0	0	1	1	1	0
1E0000	0	0	0	1	1	1	1

ROM SIZE = 2764 (CONTINUED)

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$200000	0	0	1	0	0	0	0
220000	0	0	1	0	0	0	1
240000	0	0	1	0	0	1	0
260000	0	0	1	0	0	1	1
280000	0	0	1	0	1	0	0
2A0000	0	0	1	0	1	0	1
2C0000	0	0	1	0	1	1	0
2E0000	0	0	1	0	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$300000	0	0	1	1	0	0	0
320000	0	0	1	1	0	0	1
340000	0	0	1	1	0	1	0
360000	0	0	1	1	0	1	1
380000	0	0	1	1	1	0	0
3A0000	0	0	1	1	1	0	1
3C0000	0	0	1	1	1	1	0
3E0000	0	0	1	1	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$400000	0	1	0	0	0	0	0
420000	0	1	0	0	0	0	1
440000	0	1	0	0	0	1	0
460000	0	1	0	0	0	1	1
480000	0	1	0	0	1	0	0
4A0000	0	1	0	0	1	0	1
4C0000	0	1	0	0	1	1	0
4E0000	0	1	0	0	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$500000	0	1	0	1	0	0	0
520000	0	1	0	1	0	0	1
540000	0	1	0	1	0	1	0
560000	0	1	0	1	0	1	1
580000	0	1	0	1	1	0	0
5A0000	0	1	0	1	1	0	1
5C0000	0	1	0	1	1	1	0
5E0000	0	1	0	1	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$600000	0	1	1	0	0	0	0
620000	0	1	1	0	0	0	1
640000	0	1	1	0	0	1	0
660000	0	1	1	0	0	1	1
680000	0	1	1	0	1	0	0
6A0000	0	1	1	0	1	0	1
6C0000	0	1	1	0	1	1	0
6E0000	0	1	1	0	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$700000	0	1	1	1	0	0	0
720000	0	1	1	1	0	0	1
740000	0	1	1	1	0	1	0
760000	0	1	1	1	0	1	1
780000	0	1	1	1	1	0	0
7A0000	0	1	1	1	1	0	1
7C0000	0	1	1	1	1	1	0
7E0000	0	1	1	1	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$800000	1	0	0	0	0	0	0
820000	1	0	0	0	0	0	1
840000	1	0	0	0	0	1	0
860000	1	0	0	0	0	1	1
880000	1	0	0	0	1	0	0
8A0000	1	0	0	0	1	0	1
8C0000	1	0	0	0	1	1	0
8E0000	1	0	0	0	1	1	1

ROM = 2764	S4 CONFIGURATION						
ADDR:	13	11	9	7	5	3	1
$900000	1	0	0	1	0	0	0
920000	1	0	0	1	0	0	1
940000	1	0	0	1	0	1	0
960000	1	0	0	1	0	1	1
980000	1	0	0	1	1	0	0
9A0000	1	0	0	1	1	0	1
9C0000	1	0	0	1	1	1	0
9E0000	1	0	0	1	1	1	1

ROM SIZE = 2764 (CONTINUED)

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	0	0
A20000	1	0	1	0	0	0	1
A40000	1	0	1	0	0	1	0
A60000	1	0	1	0	0	1	1
A80000	1	0	1	0	1	0	0
AA0000	1	0	1	0	1	0	1
AC0000	1	0	1	0	1	1	0
AE0000	1	0	1	0	1	1	1

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	0	0
B20000	1	0	1	1	0	0	1
B40000	1	0	1	1	0	1	0
B60000	1	0	1	1	0	1	1
B80000	1	0	1	1	1	0	0
BA0000	1	0	1	1	1	0	1
BC0000	1	0	1	1	1	1	0
BE0000	1	0	1	1	1	1	1

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	0	0
C20000	1	1	0	0	0	0	1
C40000	1	1	0	0	0	1	0
C60000	1	1	0	0	0	1	1
C80000	1	1	0	0	1	0	0
CA0000	1	1	0	0	1	0	1
CC0000	1	1	0	0	1	1	0
CE0000	1	1	0	0	1	1	1

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	0	0
D20000	1	1	0	1	0	0	1
D40000	1	1	0	1	0	1	0
D60000	1	1	0	1	0	1	1
D80000	1	1	0	1	1	0	0
DA0000	1	1	0	1	1	0	1
DC0000	1	1	0	1	1	1	0
DE0000	1	1	0	1	1	1	1

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$E00000	1	1	1	0	0	0	0
E20000	1	1	1	0	0	0	1
E40000	1	1	1	0	0	1	0
E60000	1	1	1	0	0	1	1
E80000	1	1	1	0	1	0	0
EA0000	1	1	1	0	1	0	1
EC0000	1	1	1	0	1	1	0
EE0000	1	1	1	0	1	1	1

ROM = 2764 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	0	0
F20000	1	1	1	1	0	0	1
F40000	1	1	1	1	0	1	0
F60000	1	1	1	1	0	1	1
F80000	1	1	1	1	1	0	0
FA0000	1	1	1	1	1	0	1
FC0000	1	1	1	1	1	1	0
FE0000	1	1	1	1	1	1	1

ROM SIZE = 27128

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$000000	0	0	0	0	0	0	B
040000	0	0	0	0	0	1	B
080000	0	0	0	0	1	0	B
0C0000	0	0	0	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$100000	0	0	0	1	0	0	B
140000	0	0	0	1	0	1	B
180000	0	0	0	1	1	0	B
1C0000	0	0	0	1	1	1	B

ROM SIZE = 27128 (CONTINUED)

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$200000	0	0	1	0	0	0	B
240000	0	0	1	0	0	1	B
280000	0	0	1	0	1	0	B
2C0000	0	0	1	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$300000	0	0	1	1	0	0	B
340000	0	0	1	1	0	1	B
380000	0	0	1	1	1	0	B
3C0000	0	0	1	1	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$400000	0	1	0	0	0	0	B
440000	0	1	0	0	0	1	B
480000	0	1	0	0	1	0	B
4C0000	0	1	0	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$500000	0	1	0	1	0	0	B
540000	0	1	0	1	0	1	B
580000	0	1	0	1	1	0	B
5C0000	0	1	0	1	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$600000	0	1	1	0	0	0	B
640000	0	1	1	0	0	1	B
680000	0	1	1	0	1	0	B
6C0000	0	1	1	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$700000	0	1	1	1	0	0	B
740000	0	1	1	1	0	1	B
780000	0	1	1	1	1	0	B
7C0000	0	1	1	1	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$800000	1	0	0	0	0	0	B
840000	1	0	0	0	0	1	B
880000	1	0	0	0	1	0	B
8C0000	1	0	0	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$900000	1	0	0	1	0	0	B
940000	1	0	0	1	0	1	B
980000	1	0	0	1	1	0	B
9C0000	1	0	0	1	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	0	B
A40000	1	0	1	0	0	1	B
A80000	1	0	1	0	1	0	B
AC0000	1	0	1	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	0	B
B40000	1	0	1	1	0	1	B
B80000	1	0	1	1	1	0	B
BC0000	1	0	1	1	1	1	B

ROM SIZE = 27128 (CONTINUED)

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	0	B
C40000	1	1	0	0	0	1	B
C80000	1	1	0	0	1	0	B
CC0000	1	1	0	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	0	B
D40000	1	1	0	1	0	1	B
D80000	1	1	0	1	1	0	B
DC0000	1	1	0	1	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$E00000	1	1	1	0	0	0	B
E40000	1	1	1	0	0	1	B
E80000	1	1	1	0	1	0	B
EC0000	1	1	1	0	1	1	B

ROM = 27128 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	0	B
F40000	1	1	1	1	0	1	B
F80000	1	1	1	1	1	0	B
FC0000	1	1	1	1	1	1	B

ROM SIZE = 27256

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$000000	0	0	0	0	0	B	B
080000	0	0	0	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$100000	0	0	0	1	0	B	B
180000	0	0	0	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$200000	0	0	1	0	0	B	B
280000	0	0	1	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$300000	0	0	1	1	0	B	B
380000	0	0	1	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$400000	0	1	0	0	0	B	B
480000	0	1	0	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$500000	0	1	0	1	0	B	B
580000	0	1	0	1	1	B	B

ROM SIZE = 27256 (CONTINUED)

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$600000	0	1	1	0	0	B	B
680000	0	1	1	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$700000	0	1	1	1	0	B	B
780000	0	1	1	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$800000	1	0	0	0	0	B	B
880000	1	0	0	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$900000	1	0	0	1	0	B	B
980000	1	0	0	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	B	B
A80000	1	0	1	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	B	B
B80000	1	0	1	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	B	B
C80000	1	1	0	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	B	B
D80000	1	1	0	1	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$E00000	1	1	1	0	0	B	B
E80000	1	1	1	0	1	B	B

ROM = 27256 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	B	B
F80000	1	1	1	1	1	B	B

ROM SIZE = 27512

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$000000	0	0	0	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$100000	0	0	0	1	B	B	B

ROM SIZE = 27512 (CONTINUED)

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$200000	0	0	1	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$300000	0	0	1	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$400000	0	1	0	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$500000	0	1	0	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$600000	0	1	1	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$700000	0	1	1	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$800000	1	0	0	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$900000	1	0	0	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$A00000	1	0	1	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$B00000	1	0	1	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$C00000	1	1	0	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$D00000	1	1	0	1	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$E00000	1	1	1	0	B	B	B

ROM = 27512 S4 CONFIGURATION							
ADDR:	13	11	9	7	5	3	1
$F00000	1	1	1	1	B	B	B

RAM CONFIGURATION:

To properly configure the Base Address for the On-Board RAM requires the following steps to be completed:

Step 1. Configure OP43 for type of RAM chips (see section 4.7.2)

Step 2. Determine the total amount of RAM Memory (use table A-1 below).

Step 3. Configure OP50, 49, 61, and 62 for a block size large enough to encompass the total amount of RAM memory (use table A-2 below).

Step 4. Configure S3 using following charts per block size.

Step 5. Verify /DTACK option for RAM speed.

NUMBER OF PAIRS		1	2	3	4	5	6	7	XXX
SIZE	8K by 8	16K	32K	48K	64K	80K	96K	112K	XXX
	32K by 8	64K	128K	192K	256K	320K	384K	448K	XXX

NOTE: Only 7 pairs of RAM are allowed, U12 and U25 must have ROM.

TOTAL RAM MEMORY
TABLE A-1

	32K	64K	128K	256K	512K	BLOCK SIZE
OP50	2-3	1-2	1-2	1-2	1-2	
OP49	IN	IN	OUT	OUT	OUT	
OP61	IN	IN	IN	OUT	OUT	
OP62	IN	IN	IN	IN	OUT	
OPTION						

BLOCK SIZE CONFIGURATION
TABLE A-2

The following charts are used to configure RAM base address via S3.

0 = Jumper installed.
1 = Jumper removed.
B = Jumper must be removed for block size requirement.
NOTE: Corresponding OPtion jumpers must also be removed:
B in column 1 = OP49 removed.
B in column 3 = OP61 removed.
B in column 5 = OP62 removed.

RAM BLOCK SIZE = 32 OR 64K

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$000000	0	0	0	0	0	0	0	0
010000	0	0	0	0	0	0	0	1
020000	0	0	0	0	0	0	1	0
030000	0	0	0	0	0	0	1	1
040000	0	0	0	0	0	1	0	0
050000	0	0	0	0	0	1	0	1
060000	0	0	0	0	0	1	1	0
070000	0	0	0	0	0	1	1	1
080000	0	0	0	0	1	0	0	0
090000	0	0	0	0	1	0	0	1
0A0000	0	0	0	0	1	0	1	0
0B0000	0	0	0	0	1	0	1	1
0C0000	0	0	0	0	1	1	0	0
0D0000	0	0	0	0	1	1	0	1
0E0000	0	0	0	0	1	1	1	0
0F0000	0	0	0	0	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$100000	0	0	0	1	0	0	0	0
110000	0	0	0	1	0	0	0	1
120000	0	0	0	1	0	0	1	0
130000	0	0	0	1	0	0	1	1
140000	0	0	0	1	0	1	0	0
150000	0	0	0	1	0	1	0	1
160000	0	0	0	1	0	1	1	0
170000	0	0	0	1	0	1	1	1
180000	0	0	0	1	1	0	0	0
190000	0	0	0	1	1	0	0	1
1A0000	0	0	0	1	1	0	1	0
1B0000	0	0	0	1	1	0	1	1
1C0000	0	0	0	1	1	1	0	0
1D0000	0	0	0	1	1	1	0	1
1E0000	0	0	0	1	1	1	1	0
1F0000	0	0	0	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$200000	0	0	1	0	0	0	0	0
210000	0	0	1	0	0	0	0	1
220000	0	0	1	0	0	0	1	0
230000	0	0	1	0	0	0	1	1
240000	0	0	1	0	0	1	0	0
250000	0	0	1	0	0	1	0	1
260000	0	0	1	0	0	1	1	0
270000	0	0	1	0	0	1	1	1
280000	0	0	1	0	1	0	0	0
290000	0	0	1	0	1	0	0	1
2A0000	0	0	1	0	1	0	1	0
2B0000	0	0	1	0	1	0	1	1
2C0000	0	0	1	0	1	1	0	0
2D0000	0	0	1	0	1	1	0	1
2E0000	0	0	1	0	1	1	1	0
2F0000	0	0	1	0	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$300000	0	0	1	1	0	0	0	0
310000	0	0	1	1	0	0	0	1
320000	0	0	1	1	0	0	1	0
330000	0	0	1	1	0	0	1	1
340000	0	0	1	1	0	1	0	0
350000	0	0	1	1	0	1	0	1
360000	0	0	1	1	0	1	1	0
370000	0	0	1	1	0	1	1	1
380000	0	0	1	1	1	0	0	0
390000	0	0	1	1	1	0	0	1
3A0000	0	0	1	1	1	0	1	0
3B0000	0	0	1	1	1	0	1	1
3C0000	0	0	1	1	1	1	0	0
3D0000	0	0	1	1	1	1	0	1
3E0000	0	0	1	1	1	1	1	0
3F0000	0	0	1	1	1	1	1	1

RAM BLOCK SIZE = 32 OR 64K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$400000	0	1	0	0	0	0	0	0
410000	0	1	0	0	0	0	0	1
420000	0	1	0	0	0	0	1	0
430000	0	1	0	0	0	0	1	1
440000	0	1	0	0	0	1	0	0
450000	0	1	0	0	0	1	0	1
460000	0	1	0	0	0	1	1	0
470000	0	1	0	0	0	1	1	1
480000	0	1	0	0	1	0	0	0
490000	0	1	0	0	1	0	0	1
4A0000	0	1	0	0	1	0	1	0
4B0000	0	1	0	0	1	0	1	1
4C0000	0	1	0	0	1	1	0	0
4D0000	0	1	0	0	1	1	0	1
4E0000	0	1	0	0	1	1	1	0
4F0000	0	1	0	0	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$500000	0	1	0	1	0	0	0	0
510000	0	1	0	1	0	0	0	1
520000	0	1	0	1	0	0	1	0
530000	0	1	0	1	0	0	1	1
540000	0	1	0	1	0	1	0	0
550000	0	1	0	1	0	1	0	1
560000	0	1	0	1	0	1	1	0
570000	0	1	0	1	0	1	1	1
580000	0	1	0	1	1	0	0	0
590000	0	1	0	1	1	0	0	1
5A0000	0	1	0	1	1	0	1	0
5B0000	0	1	0	1	1	0	1	1
5C0000	0	1	0	1	1	1	0	0
5D0000	0	1	0	1	1	1	0	1
5E0000	0	1	0	1	1	1	1	0
5F0000	0	1	0	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$700000	0	1	1	1	0	0	0	0
710000	0	1	1	1	0	0	0	1
720000	0	1	1	1	0	0	1	0
730000	0	1	1	1	0	0	1	1
040000	0	1	1	1	0	1	0	0
750000	0	1	1	1	0	1	0	1
760000	0	1	1	1	0	1	1	0
770000	0	1	1	1	0	1	1	1
780000	0	1	1	1	1	0	0	0
790000	0	1	1	1	1	0	0	1
7A0000	0	1	1	1	1	0	1	0
7B0000	0	1	1	1	1	0	1	1
7C0000	0	1	1	1	1	1	0	0
7D0000	0	1	1	1	1	1	0	1
7E0000	0	1	1	1	1	1	1	0
7F0000	0	1	1	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$800000	1	0	0	1	0	0	0	0
810000	1	0	0	1	0	0	0	1
820000	1	0	0	1	0	0	1	0
830000	1	0	0	1	0	0	1	1
840000	1	0	0	1	0	1	0	0
850000	1	0	0	1	0	1	0	1
860000	1	0	0	1	0	1	1	0
870000	1	0	0	1	0	1	1	1
880000	1	0	0	1	1	0	0	0
890000	1	0	0	1	1	0	0	1
8A0000	1	0	0	1	1	0	1	0
8B0000	1	0	0	1	1	0	1	1
8C0000	1	0	0	1	1	1	0	0
8D0000	1	0	0	1	1	1	0	1
8E0000	1	0	0	1	1	1	1	0
8F0000	1	0	0	1	1	1	1	1

RAM BLOCK SIZE = 32 OR 64K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$900000	1	0	0	1	0	0	0	0
910000	1	0	0	1	0	0	0	1
920000	1	0	0	1	0	0	1	0
930000	1	0	0	1	0	0	1	1
940000	1	0	0	1	0	1	0	0
950000	1	0	0	1	0	1	0	1
960000	1	0	0	1	0	1	1	0
970000	1	0	0	1	0	1	1	1
980000	1	0	0	1	1	0	0	0
990000	1	0	0	1	1	0	0	1
9A0000	1	0	0	1	1	0	1	0
9B0000	1	0	0	1	1	0	1	1
9C0000	1	0	0	1	1	1	0	0
9D0000	1	0	0	1	1	1	0	1
9E0000	1	0	0	1	1	1	1	0
9F0000	1	0	0	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	0	0	0
A10000	1	0	1	0	0	0	0	1
A20000	1	0	1	0	0	0	1	0
A30000	1	0	1	0	0	0	1	1
A40000	1	0	1	0	0	1	0	0
A50000	1	0	1	0	0	1	0	1
A60000	1	0	1	0	0	1	1	0
A70000	1	0	1	0	0	1	1	1
A80000	1	0	1	0	1	0	0	0
A90000	1	0	1	0	1	0	0	1
AA0000	1	0	1	0	1	0	1	0
AB0000	1	0	1	0	1	0	1	1
AC0000	1	0	1	0	1	1	0	0
AD0000	1	0	1	0	1	1	0	1
AE0000	1	0	1	0	1	1	1	0
AF0000	1	0	1	0	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	0	0	0
B10000	1	0	1	1	0	0	0	1
B20000	1	0	1	1	0	0	1	0
B30000	1	0	1	1	0	0	1	1
B40000	1	0	1	1	0	1	0	0
B50000	1	0	1	1	0	1	0	1
B60000	1	0	1	1	0	1	1	0
B70000	1	0	1	1	0	1	1	1
B80000	1	0	1	1	1	0	0	0
B90000	1	0	1	1	1	0	0	1
BA0000	1	0	1	1	1	0	1	0
BB0000	1	0	1	1	1	0	1	1
BC0000	1	0	1	1	1	1	0	0
BD0000	1	0	1	1	1	1	0	1
BE0000	1	0	1	1	1	1	1	0
BF0000	1	0	1	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	0	0	0
C10000	1	1	0	0	0	0	0	1
C20000	1	1	0	0	0	0	1	0
C30000	1	1	0	0	0	0	1	1
C40000	1	1	0	0	0	1	0	0
C50000	1	1	0	0	0	1	0	1
C60000	1	1	0	0	0	1	1	0
C70000	1	1	0	0	0	1	1	1
C80000	1	1	0	0	1	0	0	0
C90000	1	1	0	0	1	0	0	1
CA0000	1	1	0	0	1	0	1	0
CB0000	1	1	0	0	1	0	1	1
CC0000	1	1	0	0	1	1	0	0
CD0000	1	1	0	0	1	1	0	1
CE0000	1	1	0	0	1	1	1	0
CF0000	1	1	0	0	1	1	1	1

RAM BLOCK SIZE = 32 OR 64K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	0	0	0
D10000	1	1	0	1	0	0	0	1
D20000	1	1	0	1	0	0	1	0
D30000	1	1	0	1	0	0	1	1
D40000	1	1	0	1	0	1	0	0
D50000	1	1	0	1	0	1	0	1
D60000	1	1	0	1	0	1	1	0
D70000	1	1	0	1	0	1	1	1
D80000	1	1	0	1	1	0	0	0
D90000	1	1	0	1	1	0	0	1
DA0000	1	1	0	1	1	0	1	0
DB0000	1	1	0	1	1	0	1	1
DC0000	1	1	0	1	1	1	0	0
DD0000	1	1	0	1	1	1	0	1
DE0000	1	1	0	1	1	1	1	0
DF0000	1	1	0	1	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$E00000	1	1	1	0	0	0	0	0
E10000	1	1	1	0	0	0	0	1
E20000	1	1	1	0	0	0	1	0
E30000	1	1	1	0	0	0	1	1
E40000	1	1	1	0	0	1	0	0
E50000	1	1	1	0	0	1	0	1
E60000	1	1	1	0	0	1	1	0
E70000	1	1	1	0	0	1	1	1
E80000	1	1	1	0	1	0	0	0
E90000	1	1	1	0	1	0	0	1
EA0000	1	1	1	0	1	0	1	0
EB0000	1	1	1	0	1	0	1	1
EC0000	1	1	1	0	1	1	0	0
ED0000	1	1	1	0	1	1	0	1
EE0000	1	1	1	0	1	1	1	0
EF0000	1	1	1	0	1	1	1	1

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 32 OR 64K

ADDRESS:	15	13	11	9	7	5	3	1
$F00000	0	0	0	0	0	0	0	0
F10000	0	0	0	0	0	0	0	1
F20000	0	0	0	0	0	0	1	0
F30000	0	0	0	0	0	0	1	1
F40000	0	0	0	0	0	1	0	0
F50000	0	0	0	0	0	1	0	1
F60000	0	0	0	0	0	1	1	0
F70000	0	0	0	0	0	1	1	1
F80000	0	0	0	0	1	0	0	0
F90000	0	0	0	0	1	0	0	1
FA0000	0	0	0	0	1	0	1	0
FB0000	0	0	0	0	1	0	1	1
FC0000	0	0	0	0	1	1	0	0
FD0000	0	0	0	0	1	1	0	1
FE0000	0	0	0	0	1	1	1	0
FF0000	0	0	0	0	1	1	1	1

RAM BLOCK SIZE = 128K

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$000000	0	0	0	0	0	0	0	B
020000	0	0	0	0	0	0	1	B
040000	0	0	0	0	0	1	0	B
060000	0	0	0	0	0	1	1	B
080000	0	0	0	0	1	0	0	B
0A0000	0	0	0	0	1	0	1	B
0C0000	0	0	0	0	1	1	0	B
0E0000	0	0	0	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$100000	0	0	0	1	0	0	0	B
120000	0	0	0	1	0	0	1	B
140000	0	0	0	1	0	1	0	B
160000	0	0	0	1	0	1	1	B
180000	0	0	0	1	1	0	0	B
1A0000	0	0	0	1	1	0	1	B
1C0000	0	0	0	1	1	1	0	B
1E0000	0	0	0	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$200000	0	0	1	0	0	0	0	B
220000	0	0	1	0	0	0	1	B
240000	0	0	1	0	0	1	0	B
260000	0	0	1	0	0	1	1	B
280000	0	0	1	0	1	0	0	B
2A0000	0	0	1	0	1	0	1	B
2C0000	0	0	1	0	1	1	0	B
2E0000	0	0	1	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$300000	0	0	1	1	0	0	0	B
320000	0	0	1	1	0	0	1	B
340000	0	0	1	1	0	1	0	B
360000	0	0	1	1	0	1	1	B
380000	0	0	1	1	1	0	0	B
3A0000	0	0	1	1	1	0	1	B
3C0000	0	0	1	1	1	1	0	B
3E0000	0	0	1	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$400000	0	1	0	0	0	0	0	B
420000	0	1	0	0	0	0	1	B
440000	0	1	0	0	0	1	0	B
460000	0	1	0	0	0	1	1	B
480000	0	1	0	0	1	0	0	B
4A0000	0	1	0	0	1	0	1	B
4C0000	0	1	0	0	1	1	0	B
4E0000	0	1	0	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$500000	0	1	0	1	0	0	0	B
520000	0	1	0	1	0	0	1	B
540000	0	1	0	1	0	1	0	B
560000	0	1	0	1	0	1	1	B
580000	0	1	0	1	1	0	0	B
5A0000	0	1	0	1	1	0	1	B
5C0000	0	1	0	1	1	1	0	B
5E0000	0	1	0	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$600000	0	1	1	0	0	0	0	B
620000	0	1	1	0	0	0	1	B
640000	0	1	1	0	0	1	0	B
660000	0	1	1	0	0	1	1	B
680000	0	1	1	0	1	0	0	B
6A0000	0	1	1	0	1	0	1	B
6C0000	0	1	1	0	1	1	0	B
6E0000	0	1	1	0	1	1	1	B

RAM BLOCK SIZE = 128K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$700000	0	1	1	1	0	0	0	B
720000	0	1	1	1	0	0	1	B
740000	0	1	1	1	0	1	0	B
760000	0	1	1	1	0	1	1	B
780000	0	1	1	1	1	0	0	B
7A0000	0	1	1	1	1	0	1	B
7C0000	0	1	1	1	1	1	0	B
7E0000	0	1	1	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$800000	1	0	0	0	0	0	0	B
820000	1	0	0	0	0	0	1	B
840000	1	0	0	0	0	1	0	B
860000	1	0	0	0	0	1	1	B
880000	1	0	0	0	1	0	0	B
8A0000	1	0	0	0	1	0	1	B
8C0000	1	0	0	0	1	1	0	B
8E0000	1	0	0	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$900000	1	0	0	1	0	0	0	B
920000	1	0	0	1	0	0	1	B
940000	1	0	0	1	0	1	0	B
960000	1	0	0	1	0	1	1	B
980000	1	0	0	1	1	0	0	B
9A0000	1	0	0	1	1	0	1	B
9C0000	1	0	0	1	1	1	0	B
9E0000	1	0	0	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$A00000	1	0	1	0	0	0	0	B
A20000	1	0	1	0	0	0	1	B
A40000	1	0	1	0	0	1	0	B
A60000	1	0	1	0	0	1	1	B
A80000	1	0	1	0	1	0	0	B
AA0000	1	0	1	0	1	0	1	B
AC0000	1	0	1	0	1	1	0	B
AE0000	1	0	1	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$B00000	1	0	1	1	0	0	0	B
B20000	1	0	1	1	0	0	1	B
B40000	1	0	1	1	0	1	0	B
B60000	1	0	1	1	0	1	1	B
B80000	1	0	1	1	1	0	0	B
BA0000	1	0	1	1	1	0	1	B
BC0000	1	0	1	1	1	1	0	B
BE0000	1	0	1	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$C00000	1	1	0	0	0	0	0	B
C20000	1	1	0	0	0	0	1	B
C40000	1	1	0	0	0	1	0	B
C60000	1	1	0	0	0	1	1	B
C80000	1	1	0	0	1	0	0	B
CA0000	1	1	0	0	1	0	1	B
CC0000	1	1	0	0	1	1	0	B
CE0000	1	1	0	0	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$D00000	1	1	0	1	0	0	0	B
D20000	1	1	0	1	0	0	1	B
D40000	1	1	0	1	0	1	0	B
D60000	1	1	0	1	0	1	1	B
D80000	1	1	0	1	1	0	0	B
DA0000	1	1	0	1	1	0	1	B
DC0000	1	1	0	1	1	1	0	B
DE0000	1	1	0	1	1	1	1	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1	
$E00000	1	1	1	0	0	0	0	B
E20000	1	1	1	0	0	0	1	B
E40000	1	1	1	0	0	1	0	B
E60000	1	1	1	0	0	1	1	B
E80000	1	1	1	0	1	0	0	B
EA0000	1	1	1	0	1	0	1	B
EC0000	1	1	1	0	1	1	0	B
EE0000	1	1	1	0	1	1	1	B

RAM BLOCK SIZE = 128K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 128K

ADDRESS:	15	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	0	0	B
F20000	1	1	1	1	0	0	1	B
F40000	1	1	1	1	0	1	0	B
F60000	1	1	1	1	0	1	1	B
F80000	1	1	1	1	1	0	0	B
FA0000	1	1	1	1	1	0	1	B
FC0000	1	1	1	1	1	1	0	B
FE0000	1	1	1	1	1	1	1	B

RAM BLOCK SIZE = 256K

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$000000	0	0	0	0	0	0	B	B
040000	0	0	0	0	0	1	B	B
080000	0	0	0	0	1	0	B	B
0C0000	0	0	0	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$100000	0	0	0	1	0	0	B	B
140000	0	0	0	1	0	1	B	B
180000	0	0	0	1	1	0	B	B
1C0000	0	0	0	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$200000	0	0	1	0	0	0	B	B
240000	0	0	1	0	0	1	B	B
280000	0	0	1	0	1	0	B	B
2C0000	0	0	1	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$300000	0	0	1	1	0	0	B	B
340000	0	0	1	1	0	1	B	B
380000	0	0	1	1	1	0	B	B
3C0000	0	0	1	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$400000	0	1	0	0	0	0	B	B
440000	0	1	0	0	0	1	B	B
480000	0	1	0	0	1	0	B	B
4C0000	0	1	0	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$500000	0	1	0	1	0	0	B	B
540000	0	1	0	1	0	1	B	B
580000	0	1	0	1	1	0	B	B
5C0000	0	1	0	1	1	1	B	B

RAM BLOCK SIZE = 256K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$600000	0	1	1	0	0	0	B	B
640000	0	1	1	0	0	1	B	B
680000	0	1	1	0	1	0	B	B
6C0000	0	1	1	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$700000	0	1	1	1	0	0	B	B
740000	0	1	1	1	0	1	B	B
780000	0	1	1	1	1	0	B	B
7C0000	0	1	1	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$800000	1	0	0	0	0	0	B	
840000	1	0	0	0	0	1	B	
880000	1	0	0	0	1	0	B	B
8C0000	1	0	0	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$900000	1	0	0	1	0	0	B	B
940000	1	0	0	1	0	1	B	B
980000	1	0	0	1	1	0	B	B
9C0000	1	0	0	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	0	B	B
A40000	1	0	1	0	0	1	B	B
A80000	1	0	1	0	1	0	B	B
AC0000	1	0	1	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	0	B	B
B40000	1	0	1	1	0	1	B	B
B80000	1	0	1	1	1	0	B	B
BC0000	1	0	1	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	0	B	B
C40000	1	1	0	0	0	1	B	B
C80000	1	1	0	0	1	0	B	B
CC0000	1	1	0	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	0	B	B
D40000	1	1	0	1	0	1	B	B
D80000	1	1	0	1	1	0	B	B
DC0000	1	1	0	1	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5		1
$E00000	1	1	1	0	0	0	B	B
E40000	1	1	1	0	0	1	B	B
E80000	1	1	1	0	1	0	B	B
EC0000	1	1	1	0	1	1	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 256K

ADDRESS:	15	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	0	B	B
F40000	1	1	1	1	0	1	B	B
F80000	1	1	1	1	1	0	B	B
FC0000	1	1	1	1	1	1	B	B

RAM BLOCK SIZE = 512K

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$000000	0	0	0	0	0	B	B	B
080000	0	0	0	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$100000	0	0	0	1	0	B	B	B
180000	0	0	0	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$200000	0	0	1	0	0	B	B	B
280000	0	0	1	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$300000	0	0	1	1	0	B	B	B
380000	0	0	1	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$400000	0	1	0	0	0	B	B	B
480000	0	1	0	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$500000	0	1	0	1	0	B	B	B
580000	0	1	0	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$600000	0	1	1	0	0	B	B	B
680000	0	1	1	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$700000	0	1	1	1	0	B	B	B
780000	0	1	1	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$800000	1	0	0	0	0	B	B	B
880000	1	0	0	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$900000	1	0	0	1	0	B	B	B
980000	1	0	0	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$A00000	1	0	1	0	0	B	B	B
A80000	1	0	1	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$B00000	1	0	1	1	0	B	B	B
B80000	1	0	1	1	1	B	B	B

RAM BLOCK SIZE = 512K (CONTINUED)

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$C00000	1	1	0	0	0	B	B	B
C80000	1	1	0	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$D00000	1	1	0	1	0	B	B	B
D80000	1	1	0	1	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$E00000	1	1	1	0	0	B	B	B
E80000	1	1	1	0	1	B	B	B

S3 CONFIGURATION FOR RAM

BLOCK SIZE = 512K

ADDRESS:	15	13	11	9	7	5	3	1
$F00000	1	1	1	1	0	B	B	B
F80000	1	1	1	1	1	B	B	B

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