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The RESEARCH LABORATORY *of* ELECTRONICS *at the* MASSACHUSETTS INSTITUTE OF TECHNOLOGY CAMBRIDGE, MASSACHUSETTS 02139

TX-0 Computer History

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OUTLINE

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ABSTRACT

The TX-0 Computer (meaning the Zeroth Transistorized Computer) was designed and constructed, in 1956, by the Lincoln Laboratory of the Massachusetts Institute of Technology, with two purposes in mind. One objective was to test and evaluate the use of transistors as the logical elements of a high-speed, 5 MHz, general-purpose, stored-program, parallel, digital computer. The second purpose was to provide means for testing a large capacity (65,536 word) magnetic-core memory.

The TX-0 was so sucessful, including the memory checkout, that construction was begun on the TX-2. During the spring of 1958, the large memory was transferred to the TX-2 and the TX-0 was outfitted with a 4096 word, transistor-driven core memory.

At that time the computer was moved to the Massachusetts Institute of Technology Campus in Cambridge, on a long term loan basis, to the Electrical Engineering Department. Here it was jointly supported by the Research Laboratory of Electronics and the Electronic Systems Laboratory, and made available as a do-it-yourself facility where both researchers and students could work on-line, having direct access to the machine.

The desirable features of this, at that time, unusual manner of operation were soon evident and this mode of usage was enhanced by the development of good utility programs. Further attraction was the very excellent input/output capability allowing for ease of communication with external equipment.

The transistorized computer proved to be so reliable that time, normally allocated to scheduled maintenance, was utilized to modify the machine. The core memory was doubled to 8192 words and the order code expanded. This included the addition of an index register. The modifications to the computer continued until 1963, at which time the efforts and funds of the group were directed towards the implementation of a time-sharing system on the PDP-1 Computer, which had been donated to the Electrical Engineering Department by the Digital Equipment Corporation. Several of the research groups, on the basis of demonstrated results on the TX-0, were able to negotiate funds to acquire their own computers, and the usage began to taper off.

The running-time clock now logs over 49,000 hours. Early in 1976 the TX-0 will be moved to the Computer Museum of the Digital Equipment Corporation in Marlborough, Mass.

PART I (at LINCOLN LABORATORY)

INTRODUCTION

The TX-0 Computer (meaning the Zeroth Transistorized Computer) is a 5 MHz, parallel, 18 binary digits, general-purpose, stored-program, digital machine with a cycle time of six (6) microseconds and capable of performing better than 80,000 additions per second. It was designed and constructed at the Lincoln Laboratory of the Massachusetts Institute of Technology by Group 63 of Division 6. The Group Leader was William Papian, with Wesly Clark responsible for the logical design and Kenneth Olsen heading the circuit design and construction aspects. The latter phase of the project was completed by Benjamin Gurley. The memory design and fabrication were the responsibility of Richard Best and Jack Mitchell.

The TX-0 was conceived with two purposes in mind. The first was to test and evaluate the use of transistor circuitry as the logical elements in a high-speed computer. The second objective was to provide means to test a 65,536 word, 18 binary digits plus parity, vacuum tube, switch-driven, magnetic-core memory.

The machine was the third in a succession of transistorized experimental digital systems, the first of which was a 100 transistor, double-rank shift register. The second was a small, high-speed, error-detecting multiplier.

After some thought about the possible minimal machine, a design was completed in which the word length would be 18 bits, just a half of the final projected form. This computer was referred to as the TX-0 and the projected machine as the TX-2. There was no TX-1. The TX-0 became operational in April 1956.

DESCRIPTION

In the original configuration, the TX-0 used 16 bits for addressing and two (2) bits were decoded for the four (4) instructions. The addressable instructions were, Store Accumulator (sto x), Add Memory to the Accumulator (add x), Transfer on Negative Accumulator (trn x). The fourth instruction, the Operate Command, had the feature of providing the facility to microprogram via time-pulses, thus allowing for the possibility of more than one function or register transfer, including input/output transfers, within the two (fetch and execute) cycles. Since all of the Memory Address bits were decoded in this instruction, it had many possibilities and because of this powerful feature, the TX-0 proved to be useful, even with the simple order code, as an extremely versatile measuring device. Previous to the time that the TX-0 was moved to Cambridge, it was used by Charles Molner, of the Communications Biophysics Laboratory under Professor Walter Rosenblith, to aid in the analysis of brain-wave data gathered from the auditory cortex of a cat's brain.

The original TX-0 included a Memory Buffer Register (MBR, 18 bits plus parity), and an Accumulator (AC, 18 bits), arranged as a ring adder. The one's complement arithmetic and logical operations are done between the MBR and AC. The Memory Address Register (MAR, 16 bits) and the Program Counter (PC 16 bits) along with the Instruction Register (IR, 2 bits) and the Live Register (LR, 18 bits) completes the list of active registers. The LR, at that time, was considered as just another storage register, using flip-flops rather than magnetic cores, and was especially useful, in conjunction with the microprogramming, for temporary storage.

Provided as a method of manual intervention, in both the test and normal modes, is sixteen (16) words of Toggle Switch Storage (TSS, 18 bits) and the single word registers, Toggle Buffer Register (TBR, 18 bits) and Toggle Switch Accumulator (TAC, 18 bits).

The machine has three (3) operating modes, Normal, Test and Read-In. The TX-0 is a synchronous machine with the time-pulses generated by ten (10) adjustable delays, forming a chain, with the last time-pulse connected back to retrigger the timing chain.

Initially the peripheral equipment consisted of a 250 lines/minute Ferranti Photo-Electric Paper Tape Reader that was modified to solid state circuitry, and a modified Flexowriter used to type-in, type-out and to punch-out paper tape.

In 1957, a 10 inch, electro-static deflection, cathode-ray tube, having 512 by 512 addressable locations, in a 7 by 7 inch raster, point by point display system was installed.

In 1958, a Light-Pen, a solid state version of an idea being developed for the Sage System, was added to the TX-0.

LOGIC

All of the high speed logic is performed with transistors, there are no diodes used as logic gates. The TX-0 uses RC coupled, negative logic, a "ONE" being -3 volts and a "ZERO" being ground level. The AND and OR functions are obtained by mixing and gating levels. The levels are generated by flip-flops which are set or cleared by a gated time pulse.

Timing pulses are negative with an amplitude of from 2.5 to 3.0 volts and a width of 100 nanoseconds. These are generated by vacuum tube circuits and stepped down by pulse transformers to supply the necessary drive currents. The pulse lines are kept as short as possible with the strobe pulses generated directly at the register where they are used.

The flip-flop outputs are fanned out, by means of open wiring, within the Central Processing Unit Rack or via coaxial cable or twisted-pairs, when conveyed any greater distance. All of the logical interconnections, other than the few of those made in coaxial cable, are terminated in taper-pin connections. The flexiblity of this method is very desirable in an experimental machine and along with the modular concept adopted for construction, allowed for the possiblity of the extensive changes which were later undertaken.

Except for the flip-flop module, the transistors are packaged one, two or three in a plastic, plug-in bottle, with the transistor leads brought out to the base. The importance of this type of construction will be evident later, when the ideas of transistor life history are discussed.

CIRCUITRY

The logical elements of the TX-0 use surface-barrier transistors and are formed from saturated inverter and saturated emitter-follower combinations. A two transistor cascode configuration, with fast rise and fall times, is used as a power amplifier. This is similiar to the TTL circuit used today in medium speed integrated circuits.

The TX-0 flip-flop module, an Eccles-Jordan flip-flop circuit, is capable of 5 MHz operation, has a built-in logical delay and uses 10 transistors including the cascode buffered outputs which give it good driving ability. The built-in delay in flip-flops allows the information clocked into a flip-flop to be a function of that flip-flop's outputs.

A dozen different types of plug-in-units are employed. Power supply voltages are +10, -3 and -10 volts. The inverter units have positive bias, calculated so that there is a safety margin in both the cut-off and the saturated conditions.

The careful, conservative circuit design, allowed for a wide variation in the transistor parameters and operating conditions and effort was made to minimize the effects of them.

MARGINAL CHECKING

The transistors in the computer are checked, while running a diagnostic type program in the Normal mode, by the use of the Marginal Check Panel. This selection panel provides a means to select any one of thirty (30) different lines, or sections, in the computer. In most cases, marginal checking of these lines allows for a +10 or -10 volt excursion on the +10 volt bias to the base of the inverters, including the inverters in the flip-flops, without causing the unit to malfunction.

In practice, from a preventative maintenance point of view, after the machine had been in operation for several hundred hours, and except when modifications were made to it, the greatest value of the marginal checking was to discover deterioration in the amplitude of the time pulses generated by the 100 vacuum tubes. Of course the system was invaluable as an aid in inducing the infrequent type of failure and assists in finding machine faults before they become serious enough to decrease reliability.

TRANSISTORS

The type L-5122 transistors used in the TX-0 were developed by the Philco Research Division under a subcontract, to determine a set of specifications that would guarantee the switching properties of the surface-barrier transistor (SBT) and to develop the necessary test facilities to measure their essential parameters. These transistors were later commercially available as the 2N240.

Each transistor was carefully tested before being accepted for the TX-0 and a record of the measured parameters was maintained.

In 1958, after 6000 hours of operation, some 800 transistors were removed and retested. The most serious change was found to be a slight decrease in current gain.

In 1959, after 10,000 hours of operation, these same transistors were again tested. The changes in the last 4000 hours were smaller than those of the first 6000 hours. A Lincoln Laboratory Technical Report was published, with detailed presentation of the test data, for each of the tests. The summary of the second report stated, that after 10,000 hours of operation, the surface-barrier transistor is shown to be a reliable computer transistor if used, within limitations of power, in circuits with adequate margins.

This was the last time that the extensive testing was done. At the time that this is written in 1974 , there is close to 49,000 hours of operation on these original transistors, with fewer than a dozen failures.

The transistor selection and evaluation was directed at Lincoln Laboratory by Donald J. Eckl and Robert J. Burke.

MEMORY (S Memory)

The TX-0 first used a high-speed, random access, magnetic-core memory with a storage capacity of 65,536 words, 19 bits long, including a parity bit. The words were read in parallel with a cycle time of five (5) microseconds. The 80 mils outside diameter, 50 mils inside diameter, ferrite cores, switched with an 820 milliampere current pulse and were manufactured at Lincoln Laboratory. The memory system contained 425 dual triodes and 625 transistors. The cores were fabricated into 64 by 64 subassemblies, each of which was a complete memory plane, and could be tested at this stage of construction. Sixteen (16) 64 by 64 subassemblies were then assembled into an array to form a 256 by 256 plane. Following the initial checkout period, the memory word lengh was doubled to 38 bits.

SOFTWARE (initial)

The availability of the high-speed, large capacity core memory opened the possibility for new techniques and philosophies in planning and programming computer applications. One technique was to use the bulk of memory as a secondary storage medium instead of using a drum or magnetic tape. A conversion program using this idea was written by Wesley Clark. This was a fast translation program, that allowed the use of symbolic language in address tags, address sections of instructions and constants.

Another valuable technique was the utility program written by Jack T. Gilmore, Jr. to coexist in core memory along with the user's program. This approach allowed the user to communicate with the computer via the on-line typewriter. Numbered among the features were the ability to examine a register, modify the contents of a register or a storage location in memory, search for all occurances of a specific word or address, the ability to list all or any part of a program, and the punchout routine that provided the user with the means to obtain an up to date binary tape of his program as it exists in core.

It is interesting to note the lengthy conversational approach that was used. For instance, when a printout was requested, the program responded with the following message, "DO YOU WANT A VERTICAL COLUMN LAYOUT". The required answer was always equally verbose. However there was a BE BRIEF feature that reduced each question to one or two words.

At that time, it was felt that only in certain critical situations, would one be able to justify the inefficient use of computer time, by working on-line. Of course that was thinking in terms of computers of that era, only large machines that rented for approximately three hundred dollars an hour. The TX-0 was a forerunner in helping to change much of that philosophy.

TX-0 was most successful, having fulfilled the objectives for which it was built. Transistors had been proven to be practical from a circuitry point of view and to be reliable. The memory checkout likewise was successful. In 1957 the decision was made to make the next step in the development program be the TX-2 Computer. The TX-1 was not constructed. The TX-2 incorporated several new ideas in general characteristics, logical operation, memories and circuits. Initially it had in the order of 22,000 transistors compared to the 3600 in the TX-0.

TRANSISTORIZED MEMORY (T Memory)

During the spring of 1958, the 65,536 word memory was transferred to the TX-2. A pluggable, 4096 word, 18 bit plus parity, entirely transistor driven memory was installed on the TX-0. This memory, expandable to 38 bits, was designed and constructed at Lincoln Laboratory, and was earmarked for use on the TX-2.

Memory planes, using ferrite cores, 50 mils outside diameter and 30 mils inside diameter, needing a full select current of 450 milliamperes, were developed at Lincoln Laboratory. Later there were development contracts with Radio Corporation of America, Needham, Massachusetts and with the General Ceramics Company of New Jersey, in order to release Lincoln Laboratory from the manufacturing phase, and to allow these memories to be commercially available.

The cycle time of the T Memory is 5.5 microseconds, with an access time of 2.4 microseconds. The system uses the four-wire, coincident current scheme of operation. Read and write currents are obtained from the Read/Write Drivers, returned in series with a variable, large resistor, to the -150 and +150 volt power supplies respectively, serving as a current source. The Read/Write Drivers use fast transistors. The Core Drivers are slower and are set-up earlier to gate the fast Read/Write pulse to the selected line.

The inhibit current is supplied from a -30 volt power supply via a gated Digit Plane Driver for each plane.

The Sense Amplifier is a nine (9) transistor module, including the preamplifier with a gain of 22. This is transformer coupled to a rectifying slicer. The slice level is individually adjustable, by a trimpot mounted on each module. The output is a cascode circuit which drives the Sense Amplifier level output to the Memory Buffer Register. Here it is strobed in by the strobe time pulse.

Marginal check voltage is provided to vary the slice level, so that the clipping level on each module , for each digit, may be optimized.

All of the T Memory system is mounted in the same rack as the Central Processing Unit.

The addition of the new memory represented an addition of 1460 transistors and 64 diodes, excluding the control. In all references to transistor testing and failure rate, these transistors are not included. Uncaused failures in this system have been somewhat greater, in the order of twenty (20), most of which were in the high current transistors in the selection line or Core Drivers. Since this memory was designated for the TX-2, the packaging is accomplished in TX-2 style modules.

POWER CONTROL

At the time of the changeover to the new, T Memory, the power control and power supply situation was reworked, in preparation for the forthcoming move of the TX-0 from Lincoln Laboratory to the Massachusetts Institute of Technology Campus in Cambridge. Originally some of the DC power was generated from motor generator sets and all of that system, along with it's power control, was transferred to the TX-2, which was approaching the stage for preliminary testing.

A second rack was furnished for the TX-0 to house the necessary power supplies for the Central Processing Unit logic, the newly added T Memory and various peripheral devices. Considerable space was required for the high voltage supplies associated with the display system.

In addition, a two-stage power control was provided for turn-on and turn-off. At turn-on, a 60 second warm-up was necessary for the filaments of the vacuum tubes of the time pulse generators. At the end of that time, first stage DC power was available and the time pulse chain had to be manually started. At the same time, CPU logic power was applied. After the second stage, power is applied to the Read/Write and Inhibit current power supplies for the memory.

DC power is distributed via a fuse panel, mounted on the Power Control Rack, to the various sections of the machine.

DC voltages are sensed by a Voltage Monitor Circuit which has provision for adjusting the trip level of the allowable excursion of each voltage. Cycle 1 voltages are monitored separately from cycle 2 and the later can drop-out or be held off independently. The fuses are of the grasshopper type, with an alarm actuating tail that crowbars the affected power supply, via a resistor, to a ground bus when any one of the fuses blows, thus tripping the Voltage Monitor. A short delay at the end of each cycle is provided to hold off the monitor until the voltages have been given time to stabilize.

IN-OUT RACK

A third rack was also provided to house the time pulse equipment and the planned for Extended Input/Output Facility, which will be discussed later, under that title.

CONSOLE

The TX-0 Console is L-shaped, each leg eight (8) feet long. This includes space for the Control Panel, Toggle Switch Storage Panel, Marginal Check Panel and Display Panel. Table space is ample for the Flexowriter, the Photo-Electric Paper Tape Reader, common program paper tape files and for the user's paper work.

PART II (at CAMBRIDGE)

INTRODUCTION

Late in 1957, the possibility of moving the TX-0 to the MIT Campus was discussed and early in 1958, Prof. J. F. Reinjes, Chairman of the Ad Hoc Committee on Computation, with the support of the committee, took direct responsibility for the future operation of the TX-0. Earl W. Pughe, Jr. was appointed to have the immediate responsibility for the installation and operation, assisted by John A. McKenzie, who at that time was transferred, full time, to Lincoln Laboratory to gain experience with the computer and participate in the transfer.

The TX-0 was to be housed on the second floor of Building 26, (the newly completed Compton Laboratory), in 9000 sq. ft. of area with expansion possibilities. This was prime space, on the same floor as the Research Laboratory of Electronics Administrative Offices.

The agreement was to transfer the TX-0, on a long term loan basis, to the Electrical Engineering Department. The facility was initially jointly supported by the Research Laboratory of Electronics, the Electronic Systems Laboratory and the Electrical Engineering Department.

Lincoln Laboratory furnished funds for the purchase and installation of a fifteen (15) ton air conditioning system in the new location.

MOVE TO CAMBRIDGE

The decision at Lincoln Laboratory, to cooperate and furnish support, set the tone for the transfer, which went very smoothly due to the excellent cooperation of everyone there, whether directly or indirectly involved. Remember that this was a laboratory built machine, not constructed with the idea that it would be portable, or even moved. Interconnections were not pluggable. Racks were bolted to bases, which in turn were bolted to the floor.

On July 1, 1958, the TX-0 was shut down, and work begun cutting free all of the interconnections, which numbered in the hundreds, of individually tagged wires.

By the end of the month the machine had been installed at Cambridge, under the guidance of Robert Hudson of Lincoln Laboratory. Complete checkout was delayed, first by the lack of cooling and second by the need to shut down while the air conditioner was being installed. Operation started to become marginal whenever the temperature exceeded 80 degrees F., and there was a caution not to run the machine under those conditions.

However by the end of August, everything had been checked out, and the users started to use the machine. The group from the Communications Biophysics Laboratory, having previously used the TX-0 at Lincoln, had working programs and, of course, were anxious to get back to reducing their data. The goal, to be ready by the start of the fall term, had been met.

EXTENDED INPUT/OUTPUT FACILITY- Addition of

Soon after operation began at Cambridge, the TX-0 was provided with an extensive, Extended Input/Output System, designed by Benjamin Gurly, built at Lincoln Laboratory, and installed in the newly provided In-Out Rack. The idea was to make available a very flexible input-output arrangement. Actually, there was so much flexibility inherent in the system, that a series of adapter panels were built, including switches and patchcords, to defeat some of the logical options, and to make it easier for the user, requiring only the simplest kind of setup, to attach his equipment to the machine. At the same time, none of the defeat logic was hard wired, and the user having need of the full capability of the system, was still accomodated.

Data is exchanged, in both directions, between the users' external equipment and the Live Register (LR) of the TX-0. Data outputs are available from all eighteen (18) bits of the LR. Up to eight (8) External Commands or trigger pulses are available to control the external equipment and/or to select which device, attached to one of the six possible input connections, is to be read in. The configuration of the way that it is read in is programmable if desired.

An Epsco Datrac, eleven (11) bit A/D Converter, with a sample and hold input, is mounted in the In-Out Rack. It's input is sampled and the digitized result read into the LR, under program control. The digital output can be patched, in any format, to the LR. A D/A Converter, looking at nine (9) bits of the LR, is permanently hooked up.

Since there is nc interrupt system, external intervention is accomplished via various means. One, a Transfer on Level (tlv) instruction is available which senses the signal level on it's input. Two, there are inputs provided where an external pulse may be used to set either the Light Pen 1 or Light Pen 2 flip-flops. These are sensed by the light pen (pen) instruction. Three, the external instructions (ex0 thru ex7) cause the computer to wait for a completion pulse. Normally the output pulse is patched back in, to form it's own completion, but it may be patched to an external device or delay, which in turn will be used to provide the completion pulse.

Time pulses are available for use, for example, to control external synchronizers.

A complement of eighty (80) Digital Equipment Corporation (DEC) Building Blocks, whose logic levels are directly compatible with TX-0 levels, is available to allow the user to extend the computer logic, to suit his own needs.

The ease with which a user may append external equipment, such as his own special hardware, to the TX-0, with a minimum of hardware necessary on his part, has proven to be

a very powerful and popular attraction to the research groups. This aspect will be mentioned again, when the variety of applications is discussed.

FIRST YEAR AT CAMBRIDGE

The installation of the 4096 word core memory obsoleted the old utility routines. John C. Gilmore, Jr. and Charles Woodward wrote a new utility program, titled Utility Tape-3 (UT-3), with subroutines to do register examination and modification, to do a memory word search, to print out a listing and to punch out paper tape. It occupied 1184 registers, residing in the top quarter of core memory. New programs were typed in, on-line, using UT-3, since there was no assembly program.

Late in 1958, a conversion program, Golux, was finished by Lawrence Gitten. The users then prepared the symbolic language, alphanumeric coded paper tape on the off-line Flexowriters, and using Golux, produced a binary tape.

Early in 1959, the new and much improved assembly program, Macro, was completed by Prof. J. B. Dennis. This program was a major step forward, and will be discussed later under software development.

Dating back to the start of operation at Cambridge, many of the staff members of the Electronic Systems Laboratory were interested in becoming familiar with the machine. The most ambitious project of that nature was a demonstration program, written by John E. Ward and Douglas Ross, simulating a mouse, searching through a maze, hunting for a cheese. Other programs were documented and submitted as subroutines.

Later the Speech Group of the Research Laboratory of Electronics, under Prof. Kenneth Stevens, became active on the machine, studying ways to characterize speech. Among the new users were groups working in picture processing, transmission bandwidth simulation, pattern and character recognition. Several graduate students used the computer in connection with their theses. (See applications section later, for a more detailed account.)

MODE OF OPERATION

The TX-0 Facility was set up as a do-it-yourself operation, with the user doing his own programming, tape preparation and computer operation. The machine was available, to qualified users, on a round the clock, seven days a week basis. The computer proved to be so reliable, as has been stated before, that this type of operation was feasible, and the users seldom experienced catastrophic type machine failures during off-hours operation. If trouble occured and if time was tightly scheduled, the staff would respond at any reasonable hour. At worst, the malfunction was corrected early the next day.

The idea of working on-line caught on immediatly. It was easily demonstrated that a researcher could get a working program off the ground in much less time, and secondly, the output could be monitored so that a useless amount of data was not generated when it was initially apparent that the program was not fully debugged, or that some unforseen event had not been taken into account.

In addition to the Flexowriter, a large number of interactive facilities, such as, Toggle Switch Storage, Toggle Buffer Register, Toggle Accumulator and the Light Pen provides good means to change parameters in, or to direct, a running program.

The manner of operation is very informal, no exact number of hours is billed to a user. Records are kept only as a way of knowing what percentage of time is utilized by the various groups or affiliations. That data is then used as bargaining power to obtain funds for capital expenditures, when the computer facility is expanded.

MACHINE EXPANSION PHASE

During the summer of 1959, when Earl W. Pughe, Jr. resigned, Prof. J. B. Dennis, of the Research Laboratory of Electronics, accepted the appointment, by the Ad Hoc Committee on Computation, to be in charge of the TX-0 Facility. The usefulness and versatility of the machine was evident, and the Committee was receptive to his proposals for the expansion of the computer. The only restriction being that the changes had to be accomplished with a minimum of downtime or inconvenience to the users. In order to help expedite the modifications, the group was increased to three, by the addition of John T. Connolly, who transferred to the TX-0 when the Whirlwind Computer was phased out.

One day a week had been reserved for scheduled maintenance. Since only a minimum of time was necessary for that purpose, that day was usually devoted to modifications. Due to the modular, physical structure of the TX-0, i.e., each gate was pluggable and each flip-flop used as a register bit or in control, along with its associated gates, was plugged into a removable panel interconnected with taper pin connections, it was feasible to rework the control and registers, bit by bit, and have the computer usable at the end of each day. In only a few cases was it necessary to take more time, on a scheduled shutdown, to cut-in new logic.

T-MEMORY EXPANSION

The first major enlargement, in 1959, was to double the size of the T-Memory from 4096 to 8192 words. Another Memory Address bit was used so that all of core memory is directly addressable. The T-Memory had been designed and packaged as a 64 by 64 array, 38 bits long, for the TX-2. It had been fabricated for the TX-0 with only 19 planes installed. The additional planes were purchased from RCA, Needham, and were wired into the stack by the Memory Development Group at Lincoln Laboratory.

Another set of input gates was added to the Memory Buffer Register (MBR) to accomodate the Sense Amplifier outputs of the additional planes.

The new arrangement is to read out both the top and bottom halves of core memory using the common set of Core Drivers. The wanted (addressed) half is gated into the Memory Buffer Register as before. The unwanted half is gated into the newly constructed Memory Buffer Auxiliary register (MBA), used only to provide the necessary information to the Inhibit Drivers during the rewrite cycle.

The MBA was constructed using TX-2 type modules.

ORDER CODE ENLARGEMENT

The installation of the smaller capacity T Memory left three (3) unused Memory Address Register (MAR) bits available. These were added to the Instruction Register (IR), increasing its length from two (2) to five (5) bits, to allow for the future enlargement of the order code. The new addressable commands, expandable up to a possible twenty-four (24) instructions, were grouped into the store class, add/load class, and transfer class. The operate class commands remained, decoded as a single instruction, to perform the majority of the arithmetic and logical operations.

The first instructions, added in 1959, were reasonably easy to implement, in that they required no additional register transfer gates and only slight changes in control. The orders added were, Store Live Register (slr), Load Live Register (llr), and the Unconditional Transfer (tra), giving a new total of six (6) addressable commands.

The large scale changes, required to realize the Future TX-0 System Organization, were implemented piecemeal over the period from 1960 to 1962. However the logical design, of what was close to being the final system, was completed by Prof. J. B. Dennis in 1960, and the new logic was simulated on the TX-0 with a program written by Robert Wagner.

The procedure chosen to implement the proposed changes was to update any register bit, or control, plug-in-unit mounting panel completely, even though only a fraction of the changes would be used at the time of the rework. That meant providing, at that time, all of the components and wiring necessary to achieve the future machine organization.

The design considerations were more than deciding what would be a desireable order code. There were many physical constraints imposed by hardware and space limitations. In some cases, new type plug-in-units were designed in order to gain a tighter density of packaging. The TX-0 Group constructed all of the additional CPU logic modules, since that style was not comercially available.

The most important addition was an Index Register (XR) consisting of a sign and thirteen (13) binary digits. In order to perform effective address calculation and index addition, a new Program Counter (PC) with a full adding circuit, was constructed, using TX-2 type modules. The old program counter was then reworked to become the Index Register (XR). Some of the indexed instructions required three machine cycles, so this necessitated changes in the machine cycle control. Input transfer gates were added to the Memory Buffer Register (MBR) for the XR→MBR data path.

Shift right circuitry and new input gates were added to the Live Register (LR) to accomodate the future Magnetic Tape System. Also added, were new gates to transfer the LR, zero sides, to the MBR, to allow for a jam transfer.

A Program Flag Register (PFR), six bits long and expandable to ten bits, was installed. This is used as a sense register, setable and readable under program control, via the Memory Buffer Register and the Accumulator. Inputs to the PFR are brought out to the In-Out Rack for use with external equipment.

The Operate Class Commands, operate micro-orders, required some reordering of bit combinations and the time pulses on which the events occurred. This change only affected nine basic orders, although used in many more combinations, and was necessary in order to work the Index Register transfer to and from the Memory Buffer Register into the system. A restore tape, providing the new definitions, was available to the users for use in reconverting their tapes. All other changes were additions to the order code and did not affect existing programs.

DIGITAL MAGNETIC TAPE SYSTEM

A Potter M 906, MK II Tape Transport System, along with the associated Drive Electronics and Record-Playback Amplifier System, was added to the TX-0 in 1961. The control logic, capable of handling up to three transports, was designed by C. Gordon Bell, who was with the TX-0 Group at that time. The system was constructed using Digital Equipment Corporation (DEC), 4000 Series System Modules.

The information is stored on the tape in a format which is compatible with the IBM seven track system, two hundred characters per inch, which was then the standard. The non-return to zero system of recording is used, and information may be written in the binary or binary-code-decimal (BCD) mode. Information is transferred to and from the TX-0, via the Live Register. Since there is only a six bit read/write buffer in the control logic, the 18-bit word assembly is done in the Live Register. The transfer takes place during the execution of a copy (cpy) instruction, which is used to synchronize the transfer. Program timing is automatic since a copy (cpy) is held up until the previous (cpy) has been executed. Four binary digits of the Program Flag Register are set by the tape control logic, and sensed under program control, for tape error conditions.

Final checout and debugging of the tape system was started by Robert Spinrad and completed by Natalio Kerllenevich, who participated while working as research assistants.

SOFTWARE DEVELOPMENT

Starting with the early work by Gilmore, covered in Part I, there has been an interesting history of software development on the TX-0. The utility program (UT-3), by Woodward of Lincoln Laboratory, was discussed in the section, First Year at Cambridge.

The new assembly program, Macro, written by Prof. J. B. Dennis in 1959 as an extra curricular activity before he became officially associated with the TX-0, was considered to be an outstanding piece of work, it being at least as flexible as assembly programs written for computers having much more storage. At that time the TX-0 had only 4096 words of core memory and four decoded instructions. In addition to the use of symbols to represent addresses and the use of the mnemonic form for all instructions, Macro provided two special features. The user could define, as a macro-instruction, any sequence of instructions which appeared several places in his program, thus saving typing effort. Provision was made for automatically storing constants, thus saving storage space. Macro handled integers in either octal or decimal form. Symbols could be up to three characters long and either fixed or symbolic addresses were handled. Symbols could be defined and symbol values could be reassigned. A total of nine (9) pseudo-instructions were included. An informative printout, at the time of conversion, listed all error stops and indicated the type of error that was encountered. Following the punching of the binary tape, a Macro Symbol Punch could be requested, which produced a binary symbol tape, of the symbol table from the conversion.

Macro underwent several revisions, including Macro IIA and Macro III. New features included the ability to nest macro-instructions and to nest constants within constants. The new pseudo-instruction "variables" , automatically allocated storage for each distinct variable. The pseudo-instruction, of the form, "repeat n,x", caused the quantity x to be repeated n times in the program. The pseudo-instruction "text" gave the user the ability to quote an arbitrary string of characters as text. The pseudo-instructions, "relocatable", "entry" and "exit", were used in connection with programs to be assembled in relocatable format. The work on Macro III was done by Robert Saunders.

A utility program, Flexowriter Interrogation Tape (Flit), for use as an aid in on-line debugging, was written by Prof. Thomas G. Stockham and Jack B. Dennis in 1959. This was done as a voluntary contribution since neither was on the TX-0 staff. Flit was programmed for use after the memory expansion to 8192 words of core memory, and occupied the upper 2500 registers. The largest single advantage gained was that the user could now type in and reference memory using, whenever he desired, any of the three character tags in his Macro symbol table as well as any additional ones that he might wish to define. In addition to the usual register examination and modification, the extra feature of color code was used to indicate what was typed in by the user (red) and what was typed out by the computer (black). This meant that any modification, in a long list, was easily spotted. The feature of doing breakpoint testing was introduced. This allowed the user to insert up to four breakpoints in his program. At the time a breakpoint is encountered, the state of the Accumulator and of the Live Register is typed out. Then the user continues by doing a "proceed". This idea proved to be a great convenience in debugging programs and a tremendous improvement over the previous scheme of stepping through a routine at the console, a single cycle, or at most a single instruction, at a time. Flit incorporated the idea of using some single character operators or commands. Also provided was the ability to control the print mode and the radix mode. Flit interpreted a vocabulary of twenty-four (24) pseudo-instructions to set the mode and twenty-nine (29) single character control commands determined the action.

In 1962, when most of the proposed improvements were completed, new software was written making use of the enlarged order code and the magnetic tape system.

A new and improved assembly program, Midas, was written by Robert Saunders. He had been active on the TX-0 as an undergraduate and joined the TX-0 staff after graduation. Among the new features, Midas recognized symbols up to six characters in length. Much more flexibility in the use of macro-instructions was provided, such as, the use of recursive macro definitions, the use of pseudo-instructions within macros, the ability to create symbols to solve the problem of address tags within macro definitions, and the use of the "garbage collect" feature to recover space when a macro is redefined. Midas stores macro definitions by remembering the exact representation in text form. When a macro is called, arguments are "plugged" into the macro body in text form. The entire macro expansion is then supplied to the assembler proper as if it had occurred in the source program. The pseudo-instructions "1if", "0if", and the qualifiers, "vp" for value positive and "vz" for value zero are provided, useful particulary in macro-instructions, to test an expression and to condition part of an assembly on the result of the test. The location counter may be set, or offset, during an assembly, to the value of an expression. The pseudo-instructions "equals and "opsyn" are used to give a symbol a logical or operation value. The Midas on-line feature enables the user to make simple corrections, via the on-line Flexowriter, to an assembly without preparing additional tapes off-line. With all the features, Midas interpreted twenty-eight (28) pseudo-instructions and over one hundred (100) instructions, i.e., including the commonly used combinations of the operate class commands. Much of the testing and debugging of Midas was done by Robert Wagner.

Doctor (Midas Debugger) is a symbolic debugging program occupying the upper one-quarter of core memory, written by Alan Kotok while an undergraduate, and used as a replacement for Flit, when Midas was introduced. The symbolic syntax is the same as that of Midas, and Doctor uses the symbol tape punched by Midas. Doctor uses single character operators exclusively, for control commands and the ever present arguments prevailed as to, what constituted a reasonable character set and meaningful operators.

With the completion of the new software and the magnetic tape system, Alan Kotok and David Gross wrote a Utility System that has a copy of Midas and Doctor, residing between two loadpoints, at the front end of the reel of magnetic tape. Either of these programs may be called by reading in a short (4 instruction) paper "call" tape. This system has the feature of requiring only a single pass of the paper tape during an assembly. The second pass makes use of the information stored on the magnetic tape during pass 1. At the time of assembly, the binary copy of the program may be read into core memory from the magnetic tape or punched out onto paper tape. Several options are available to the user by the various settings of the Test Accumulator(TAC).

This system was updated by John Currano in 1966, with the facility to store "dump" any area of core onto magnetic tape and read it back at a later time, under control of Doctor. The information is stored on the tape in a format that can be read by the IBM tape units, thus providing a convenient method to exchange data.

An English Text Editor (Acorn) was written for the TX-0 in 1967 by Eric Jensen. This is a TX-0 version of the Expensive Typewriter (ET) used on the PDP-1.

It should be noted that practically all of the system software mentioned was done on a voluntary basis by users not on the TX-0 staff at the time their programs were written.

APPLICATIONS

There have been a wide variety of applications on the TX-0. As mentioned earlier, the first research group to use the TX-0 was the Communications Biophysics Laboratory (CBL), under Prof. Walter Rosenblith, of the Research Laboratory of Electronics (RLE). The group used the computer to aid in the processing of electrophysiological data gathered from the auditory cortex of a cat's brain. The computer processed output was usually in the form of a histogram plotted on the display scope and recorded by a Polaroid camera. Active in this work were Prof. Thomas Weiss, Prof. William Peake, George Gerstein and Charles Molnar.

The Speech Group of RLE, under Prof. Kenneth Stevens, used the TX-0 for several years exploring efficient ways of characterizing, and the computer recognition of, speech sounds. The initial work, done by Prof. John Heinz, was to get the frequency spectra of speech sounds into the TX-0 in digital form and to plot this information as a curve on the display. Programs were written by C. Gordon Bell to investigate the poles of the frequency function and to provide manual and automatic means of having the computer fit a curve to the given curve, leading to automatic identification of speech sounds.

The Cognitive Information Processing Group (CIPG) of RLE, under Prof. Samuel Mason, began using the TX-0 in 1958. A number of theses on transmission bandwidth simulation and picture coding were completed. The binary data tape had six bit reflectance values of the sample points along scan lines of the picture. The transmission was simulated using one or two bits of information and image enhancement techniques were developed to upgrade the quality of the processed picture. The Polaroid camera attachment to the display made it possible to record and easily evaluate the results of the various methods tried. The earliest work was done by James Cunningham.

The Sensory Aids for the Blind Section of CIPG was active on the TX-0 over the years 1964 to 1968. The objective was to develop a reading machine for the blind that could be built for a modest sum. The first phase of the effort was a Doctoral thesis by Jon Clements, under the direction of Prof. Donald Troxel, studying various algorithms for recognizing the sample characters scanned when interposed between the display and a photomultiplier tube viewing the raster. The initial output was spoken letters or spelled speech generated from stored data. This was the work of Dr. Kenneth Ingham. Later Thomas Barnwell, under the supervision of Prof. Francis Lee, investigated computer synthesized speech as an output for the machine. On the basis of the progress made on the TX-0 a scanner was constructed, and operated under control of the PDP-1, that handled and could read a whole page of text. The activity was transferred from the TX-0 when the group obtained their own computer.

The Laboratory for Nuclear Science (LNS) had a study under the direction of Prof. Martin Deutsch, in 1959, to use a computer to analyze bubble chamber data pictures. The development was begun by Adam Boyarski on the TX-0. The data input was recorded on a roll of 35mm film that was passed, initially about 15 or 20 frames per second, between the display and a photomultiplier tube, called the light gun, which viewed the full raster of the display. By displaying all points and using the light gun to check the transmission of light through the film, data could be read into the computer and processed using pattern recognition techniques. One of the methods used was a Master's thesis by Paul Mermelstein in 1960, who programmed the TX-0 to detect and locate several well-defined patterns in pictures of the particle track. Previous to that time, operators had manually reduced the data, a slow and tedious job in which the event of interest sometimes occured only once in a thousand frames. Following the successful start on this work, the grouped purchased their own PDP-1 computer and continued to develop more highly sophisticated methods of film reading.

Lawrence Roberts in 1958 as a seminar project, modeled an adaption of Rosenblatt's perceptron, which he had never been able to test experimentally. The simulation, to have the computer "learn" to recognize the difference between two or more characters, showed only 60 per cent recognition. However with modifications developed by Roberts, the percentage increased to better than 90 per cent. The TX-0 was ideally suited for this type problem because the input capability of the light pen was unique at that time.

The frequency analysis of a human postural reflex was undertaken as a Doctoral thesis by Avery Johnson of the RLE Neurophysiology Laboratory in 1960. The torque applied by the flexor muscles tending to hold the wrist angle fixed and the resultant angle, were measured and recorded on magnetic tape. The TX-0 was employed to produce a cross-correlation function between the two signals and an auto-correlation of each separately.

William Daly, in 1960 as part of an MS thesis, programmed the TX-0 to play Cubic, a three dimensional Tic-Tac-Toe. At the conclusion of the game the player was rated and the computer strategy for the next game was based on the users current rating. When the program look-ahead discovered that the computer had won, the play was taken away from the player and the computer listed suggested moves for him. Anything other than the suggested moves would allow the computer to win sooner.

A Master's thesis by Peter Katona in 1961 involed the experimental determination of the relationship between heart rate and blood pressure, and was titled "Analysis of Blood Pressure Regulation Using Correlation Techniques". The data, recorded on magnetic tape, was easily digitized and inputed by the TX-0.

In 1962 Henry Ernst worked on a Doctoral thesis using the computer to control a mechanical hand that was equipped with half a dozen sensors and made use of a large portion of the input-output capability, including the D/A and A/D converters in the closed loop of the computer and the hand. Operated by commands typed in via the on-line typewriter, the hand would grope along the platform hunting for a block or a box. It could differentiate between them, could stack the blocks upon each other or it could deposit the blocks in a box. The program incorporated an awareness concept so that if the hand experienced a situation that it had not encountered before, or that had not been specified in the commands, it could initiate some reasonable alternative action.

During the period, 1960-61, several theses in connection with handwriting analysis were done on the TX-0. One approach was an attempt to recognize the handwriting by means of cross-correlation with a set of standard stokes.

One thesis involed measuring aspects of previously prepared handwriting samples of subjects known to have muscular coordination disorders. This data was read in using the light gun or the light pen. The objective was to study the possibility of evaluating the signatures on life insurance applications.

Peter Sampson worked with various means of giving the computer the description of a piece of music. The computer "played back" the music by changing the state of a flip-flop at the frequency of the desired pitch of each note. An amplifier was attached to the flip-flop as output. The music program was first written to handle one voice, then later to handle three voices and three flip-flops whose outputs were mixed as the input to the audio amplifier.

The TX-0 has been seen on television several times. The first appearance was a local show on WGBH-TV showing computer demonstration programs. Later the same sort of thing was done for the Canadian Broadcasting Company with the commentary done in French. The big show was a sponsored program on the national CBS Network with the TX-0 writing the script for a TV Western. The program, called Saga, set the scene and detailed the actions of the robber and the sheriff, kept track of the gun, the shots fired, hits and misses, and governed the rationality of the actors action by the number of drinks that each had consumed from the bottle of liquor on the table. Each computer run was a completely new and unpredictable skit. Saga was programmed by Douglas Ross and Harrison Morse of the Electronic Systems Laboratory.

The Radio Astronomy Group of RLE used the TX-0 in the spring of 1970 to aid in the processing of a large amount of pulsar data stored on magnetic tape. The procedure is a way of getting an early view of the data by displaying it in a series of intensity coded histograms, recorded on film, for evalution to determine what might be of interest for further processing.

Most of the applications mentioned have made use of some of the unique properties of the TX-0. During the same period many other projects and theses were handled in areas such as information theory, computer simulation, network synthesis, control systems, and in 1959, the simulation of a servo system with the driving and error function computed digitally.

During the same period the TX-0 was used in connection with introductory computer courses and many students used the machine for formal class work.

The TX-0 history would not be complete without some reference to the computer "hackers". These were students who were highly motivated in learning all that they could with respect to the computer, and in the process, spent long nights and weekend sessions on the machine, exploring their pet projects, usually not connected with anything for academic credit. Much of the good software and innovative ideas were contributed by the "hackers".

TIMESHARING (PDP-1)

The advantages gained by providing a researcher with the facility to work on-line had been clearly demonstrated. While this procedure greatly reduced the delay usually encountered from the conception of a programming idea to the completion of the operating program, the inefficient use f the computer's resources in that mode was also apparent. In 1961 Prof. J. B. Dennis wrote a proposal describing a timesharing operating system for the TX-0.

However in September of 1961, the Digital Equipment Corporation (DEC) presented a PDP-1, serial number 3, to the Electrical Engineering Department and the machine was operated as a part of the TX-0 facility. The need for a commercial computer, oriented to scientific applications, was shown by the ever expanding range of activities pioneered on the TX-0. The people at DEC, having built the TX-0 at Lincoln Laboratory, started with a strong background of experience in this field.

The PDP-1 was better suited as a base to use to implement a mixed hardware/software timesharing system. A Master's thesis by John Yates in 1962, under the supervision of Prof. Dennis, became the starting point for the timesharing systems that have continued to evolve on the machine since that time.

The TX-0 has a parallel 18 bit, two-way data link with the PDP-1 and information may be exchanged while timesharing.

CONCLUSION

Since 1962, just about all of the group's efforts and funds for capital expenditures have been devoted to enlarging the capability of the PDP-1.

The TX-0 continues to serve, has over 49,000 hours of running time, requires a minimum of maintenance, and is operated as a part of the Electrical Engineering /Research Laboratory of Electronics PDP-1/TX-0 Computer Facility.

Early in 1975 the TX-0 is going to be moved to a Computer Museum being set up by the Digital Equipment Corporation in Marlborough, Massachusetts.

ACKNOWLEDGEMENT

In this condensed form it has not been possible to more than briefly sketch the topics included. The fact that many groups and the majority of the users have not been mentioned in no way reflects upon their contribution to the activity, but was necessitated by lack of space. Names have been used chiefly to lend authenticity, so that interested parties might delve further into the developments covered.

Whatever success the TX-0 has achieved during its years at MIT is due in no small part to the ready support and encouragement given to the TX-0 group by the administrative people directly involved with providing the means to improve and maintain the installation. Equally important was their williness to sponser the very informal open-shop type of operation, making the computer easily accessible, on just about the best conceivable terms, to researchers and students.

Ralph A. Sayers, the Assistant Director of the Research Laboratory of Electronics, was always the person to call on when advice and action were needed concerning administrative policy decisions and problems, and he in turn was supported by the Director, Prof. Henry Zimmerman.

In the Electronic Systems Laboratory the Deputy Director John E. Ward and the Director Prof. J. F. Reinjes were especially active during the early years in setting the direction and pattern that the new type facility was to sucessfully follow.

During most of the time covered, the direct contact with the Electrical Engineering Department was the Executive Officer John A. Tucker, who, along with a succession of Department Heads, Prof. Gordon S. Brown, Prof. Jerome E. Wiesner, Prof. Peter Elias, and Prof. Louis D. Smullin, were always sensitive to the group's interests.

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