Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: DIGITAL DATA TRANSMITTER

To: N. H. Taylor

From: E. B. Glover

Date: 3 March 1955

Approved: R L Best
R. L. Best

Abstract: Levels from three flip-flops (combined through a resistor mixer) modulate a sine wave; the latter, when amplified and filtered, gives an output which will carry digital information over phone lines. The three test points show important phases of circuit operation. The two marginal check lines permit investigation of circuit deterioration.

I. Purpose

In the digital-data transmitter (DDT) the outputs from three Model C flip-flops are modified for transmission over phone lines and final separation into the three original channels.

II. Principle of Operation

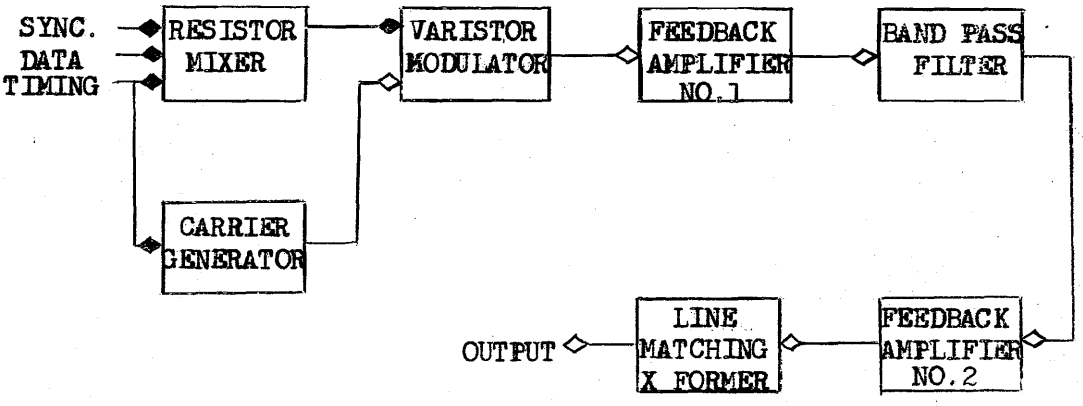


Fig. 1

Block Diagram

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Figures 1 and 2 are the block diagram and the circuit schematic, respectively, of a DDT. The explanation of circuit operation follows both these diagrams simultaneously in order to show the correlation between them.

The three inputs to the DDT are the output of the timing flip-flop, a fixed frequency of 650 cps (obtained by complementing the flip-flop at 1300 cps); the output of the synchronization flip-flop, a gate having the width of one timing box (one-half cycle of timing) and a repetition rate depending on the system in which the DDT is operating; and the output of the data flip-flop, a gate having a width of any integral number of timing boxes and a random repetition rate. These three inputs enter the resistor mixer, composed essentially of resistors R13 - R17. The first three of these resistors set the relative amplitudes of the mixed signal to the following values (Fig. 3): synchronization, 1.0; data, 0.5; timing, 0.12. The last two resistors merely govern the over-all amplitude of the signal presented to the modulator.

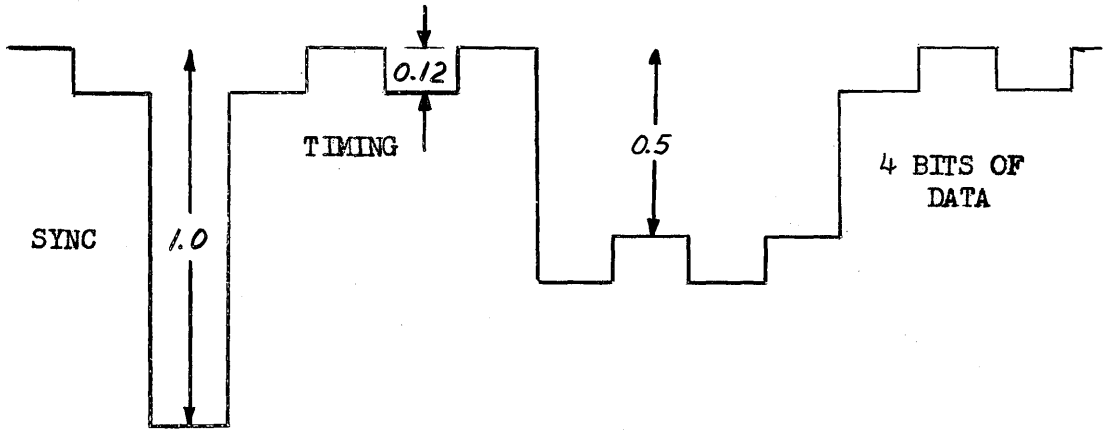


Fig. 3

Test Point 1 (Output of Resistor Mixer)

The output of the timing flip-flop is also the input to the carrier generator. This unit is composed of a cathode-follower, V1B (used as an impedance-matching device), and a high Q filter (condensers C3 - C7, inductors L1 - L3) tuned to the third harmonic of the timing frequency (650 cps). The filter output is consequently a 1950-cps sine wave and is used as a carrier for the information signals.

Both the carrier and the signal from the resistor mixer are fed to the varistor modulator, which yields a simple amplitude-modulated wave. The carrier enters the modulator through a 10:1 transformer, T1.

The amount of carrier that passes to the modulator output transformer T2 (i.e. the percentage of modulation) depends on the direct current flowing through the modulator. The amount of this current is, of course, dependent on the flip-flop states at the three inputs. No signal, and

consequently least current, corresponds to all three inputs being at the +10 level. The value of current for this condition can be regulated by the carrier-gain pot R5: for the no-signal condition, R5 is set to give an amplitude at T2 which is 25% of that produced when there is a signal (-30) at the synchronization input (Fig. 4).

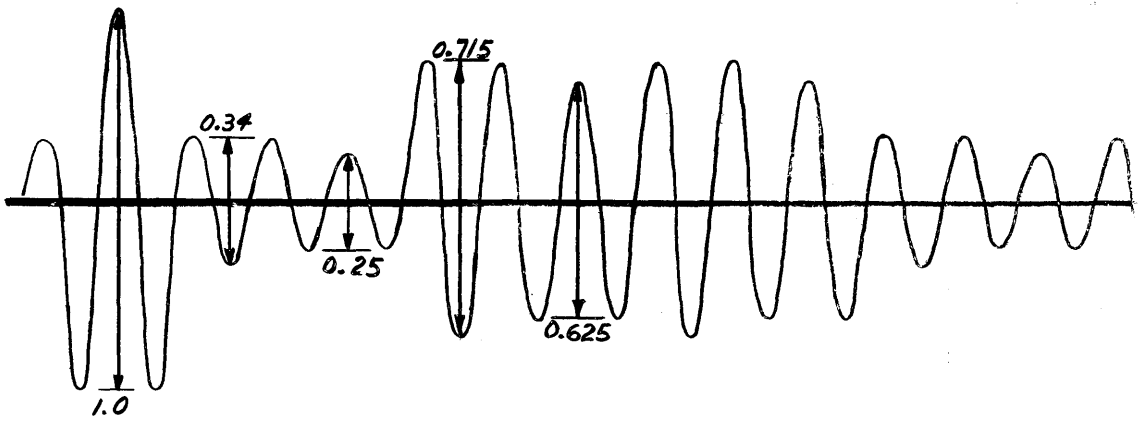


Fig. 4

Test Point 3

The modulated wave is then fed into the first feedback amplifier V2; the amplified wave goes into a band-pass filter which removes all frequencies not in the pass-band of the phone lines, thus preventing distortion. This filter, composed of condensers C11 - C4, inductor L4, and resistors R26 and R27, has a pass-band of roughly 550-2130 cps. R27 (labeled output gain) is a potentiometer and allows adjustment of the signal amplitude fed to the second feedback amplifier V3.

The output of the second feedback amplifier is fed through a line-matching transformer, T3, to the phone line. The final output signal has the following relative amplitudes: synchronization, 1.0; carrier, 0.25; data plus carrier, 0.625; timing and carrier, 0.34; data plus timing and carrier, 0.715. (Fig. 4)

III. Test Points

Three test points in the DDT show the important phases of its operation (Fig. 2). Test point 1 shows the output of the resistor mixer; Fig. 3 is a typical signal. Test point 2 shows the carrier, which is the output of the high Q filter. (Since this output is a simple sine wave, a typical signal of this test point is not given here.) Test point 3 shows the output of the second feedback amplifier, the output of the circuit before it is stepped-down by transformer T3. Figure 4 is a typical signal at this point.

IV. Marginal Checking

The complete circuit has two marginal check lines. The +150-volt marginal check line controls the plate supply voltage of V1B,

the cathode follower. Figure 5 shows how the carrier amplitude is decreased as this marginal check voltage is lowered. Under bogie conditions, the marginal check voltage can be lowered to +50 volts before any change can be detected in the output of the DDT. By adjustment of the gain pot and the carrier-level pot, marginal check +150 voltage can be lowered to 0 with no appreciable effect on the DDT output.

The other marginal check voltage is +250. Decreasing this voltage lowers the amplitude of the DDT output. Failure in Figs. 6, 7, 8, and 9 is defined as the value of marginal check voltage that causes an output signal of 2.2 volts to drop to 1.78 volts. The phone line specifications require that no more than 2.2 volts be applied to any line; with maximum attenuation on a line, 1.78 volts is the minimum signal voltage that can be applied to meet receiving equipment input specifications. Under bogie conditions, the marginal check voltage can be lowered to +100 volts before failure occurs.

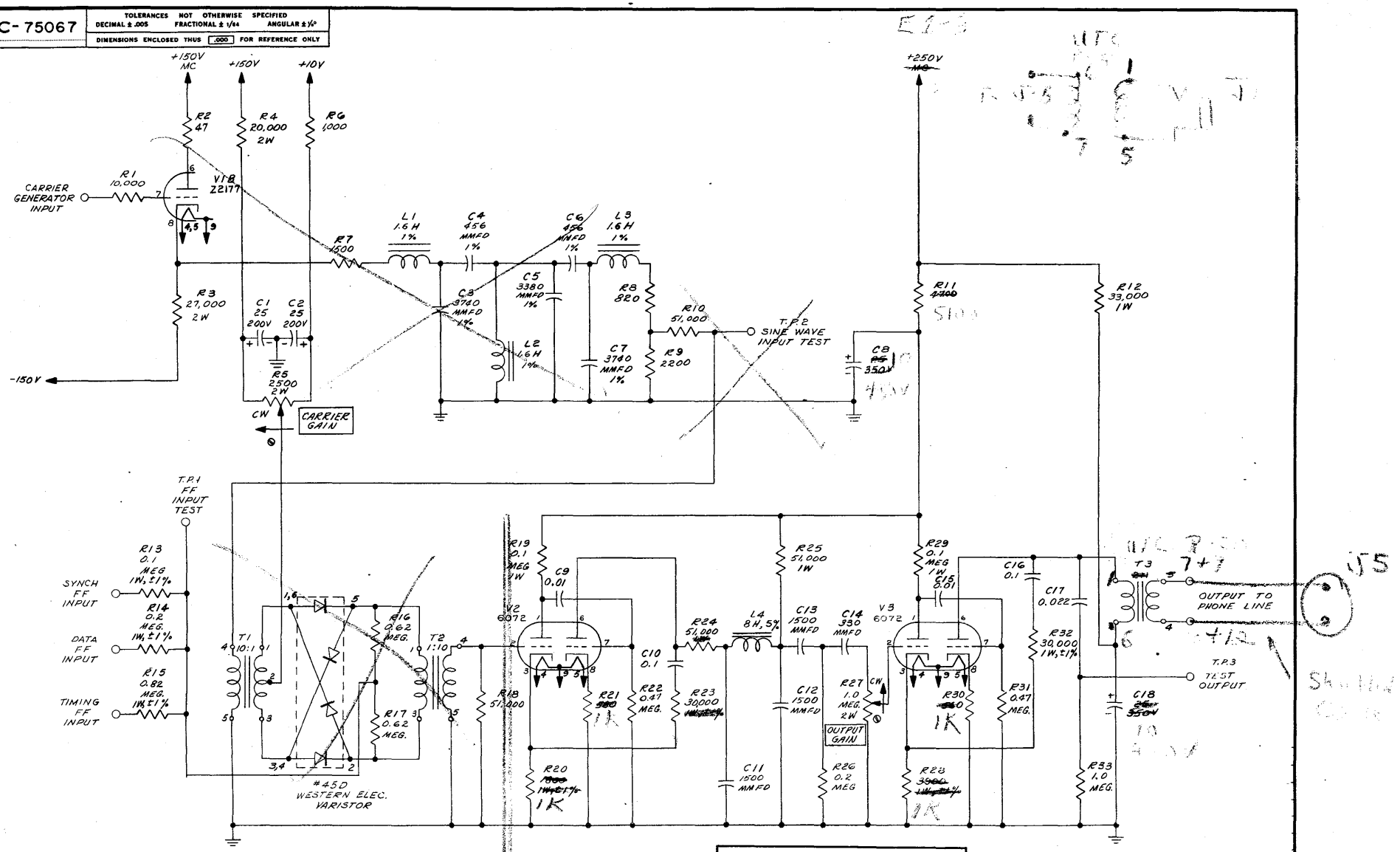
Signed: E. B. Glover
E. B. Glover

EBG/er

Attached:
Fig. 2 C-75067
Fig. 5 A-61850
Fig. 6 & 7 B-61848
Fig. 8 & 9 B-61849

DISTRIBUTION LIST

Group 62 Section Leaders
Vacuum Tube Circuits Section (Staff Members)
Paul Harris
Paul Rosen
O. V. Fortier
I. Aronson
Paul Messenheimer
J. Ogg (IBM)
F. Ordeman (IBM)
T. Digan (IBM)



4M-7-54-Boston Blue Print

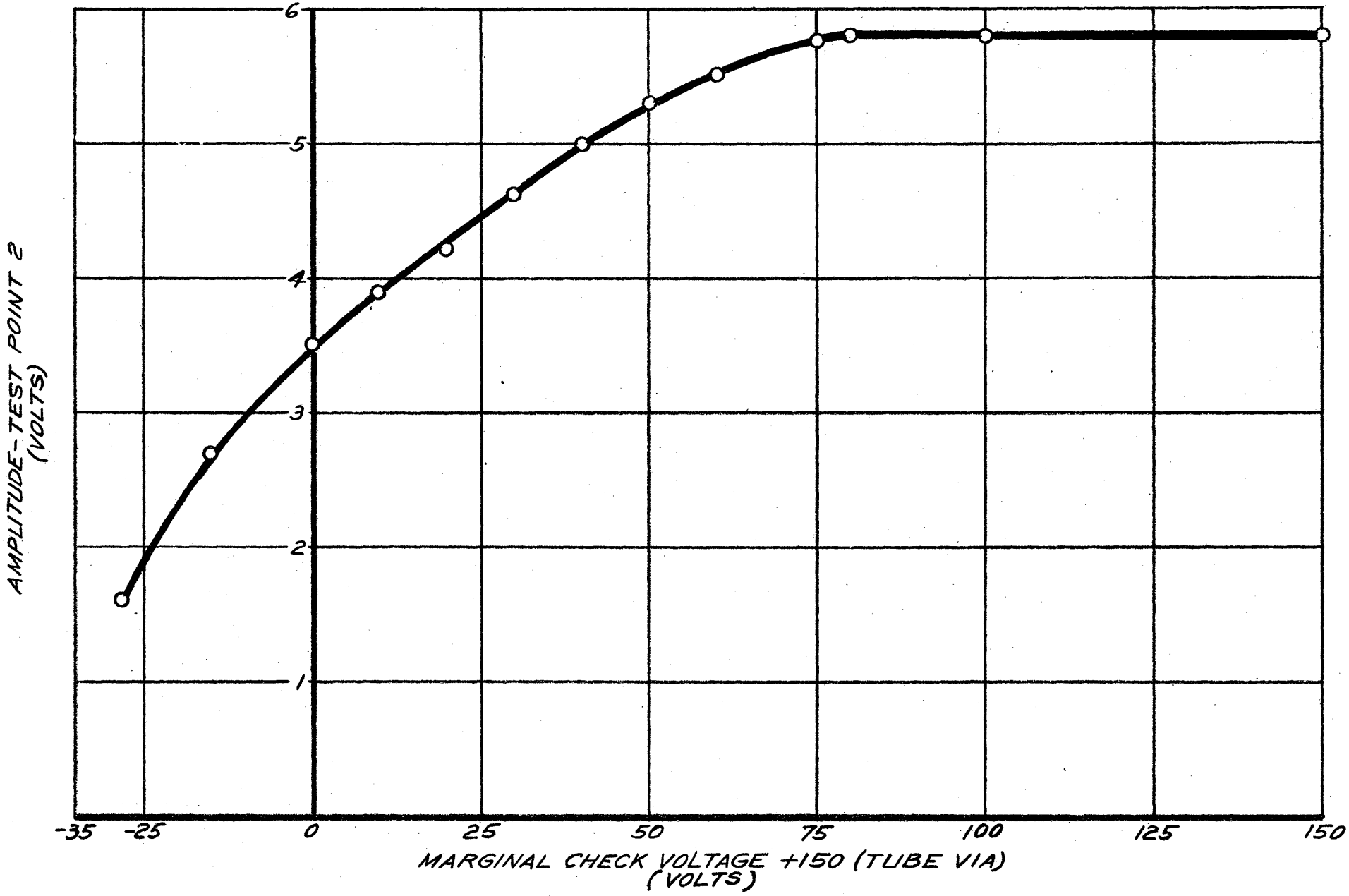


FIG. 5

VARIATION OF CARRIER AMPLITUDE AGAINST A MARGINAL CHECK VOLTAGE

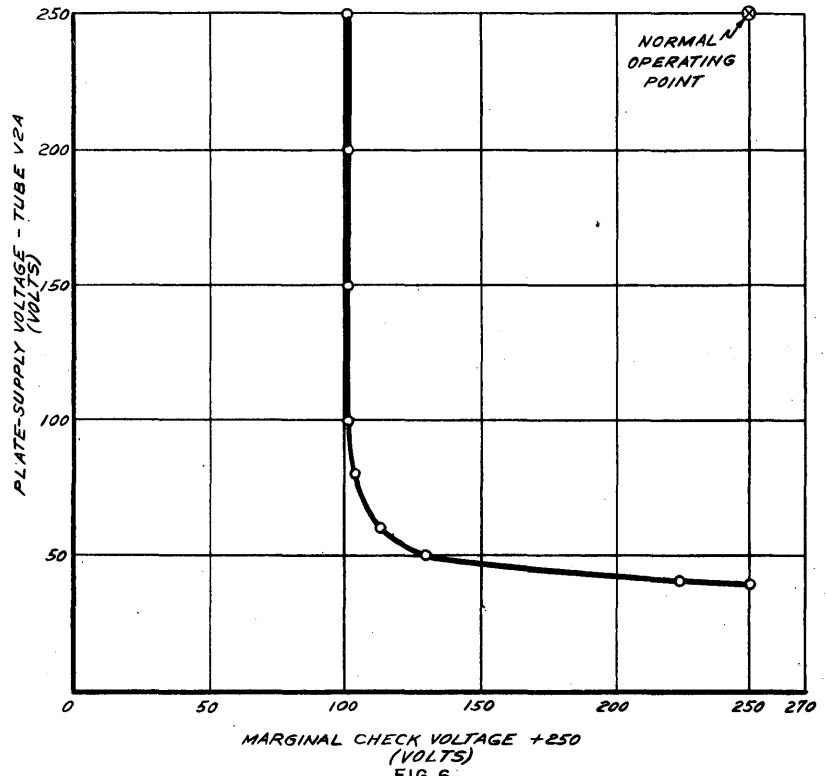


FIG. 6

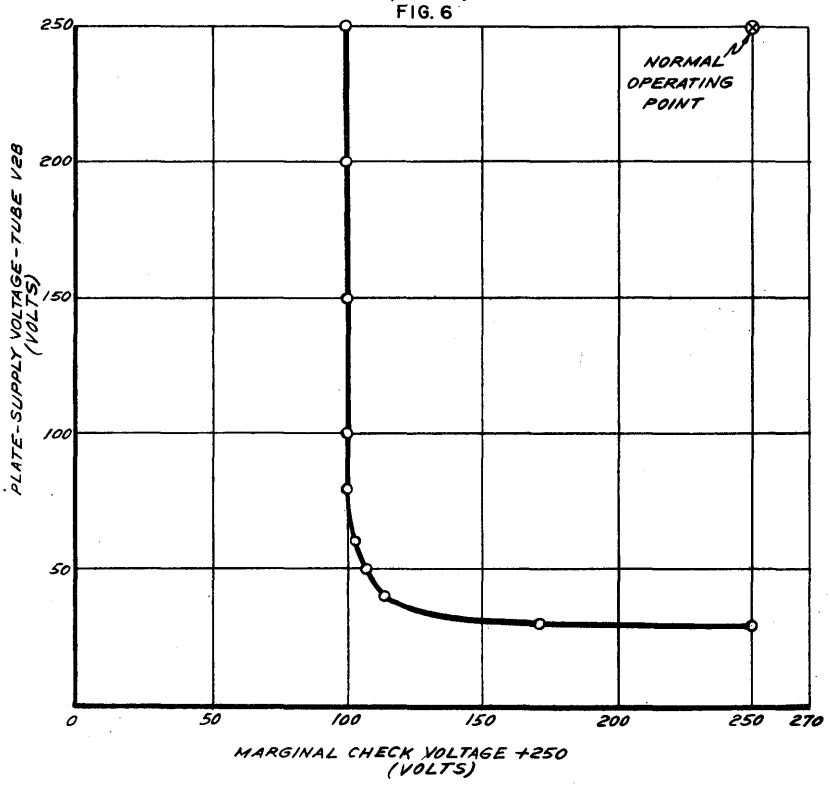


FIG. 7

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE (GRAPH IV)

8-61848

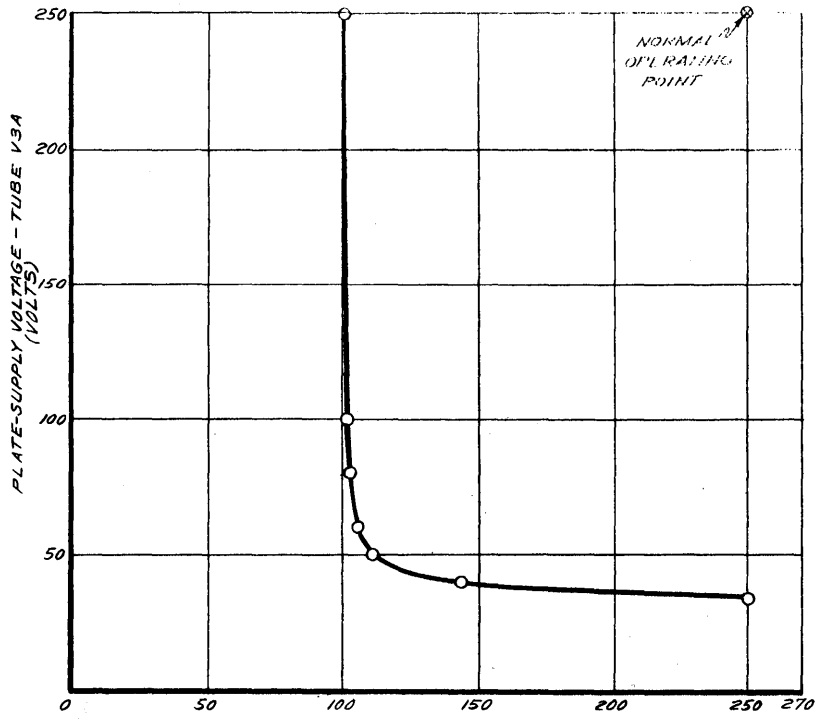


FIG. 8

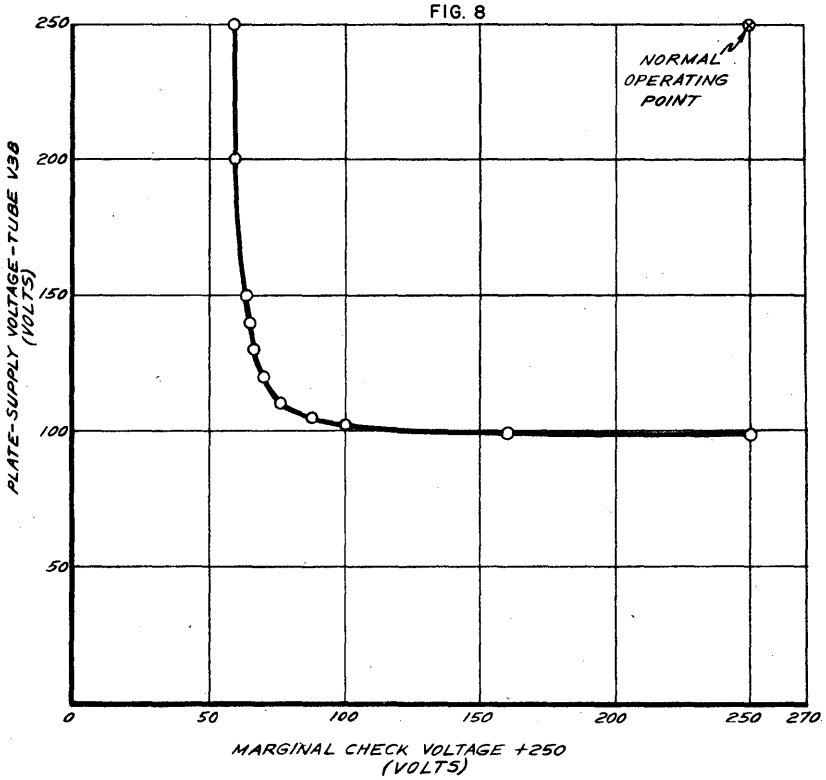


FIG. 9

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE (GRAPH V)

B-61849