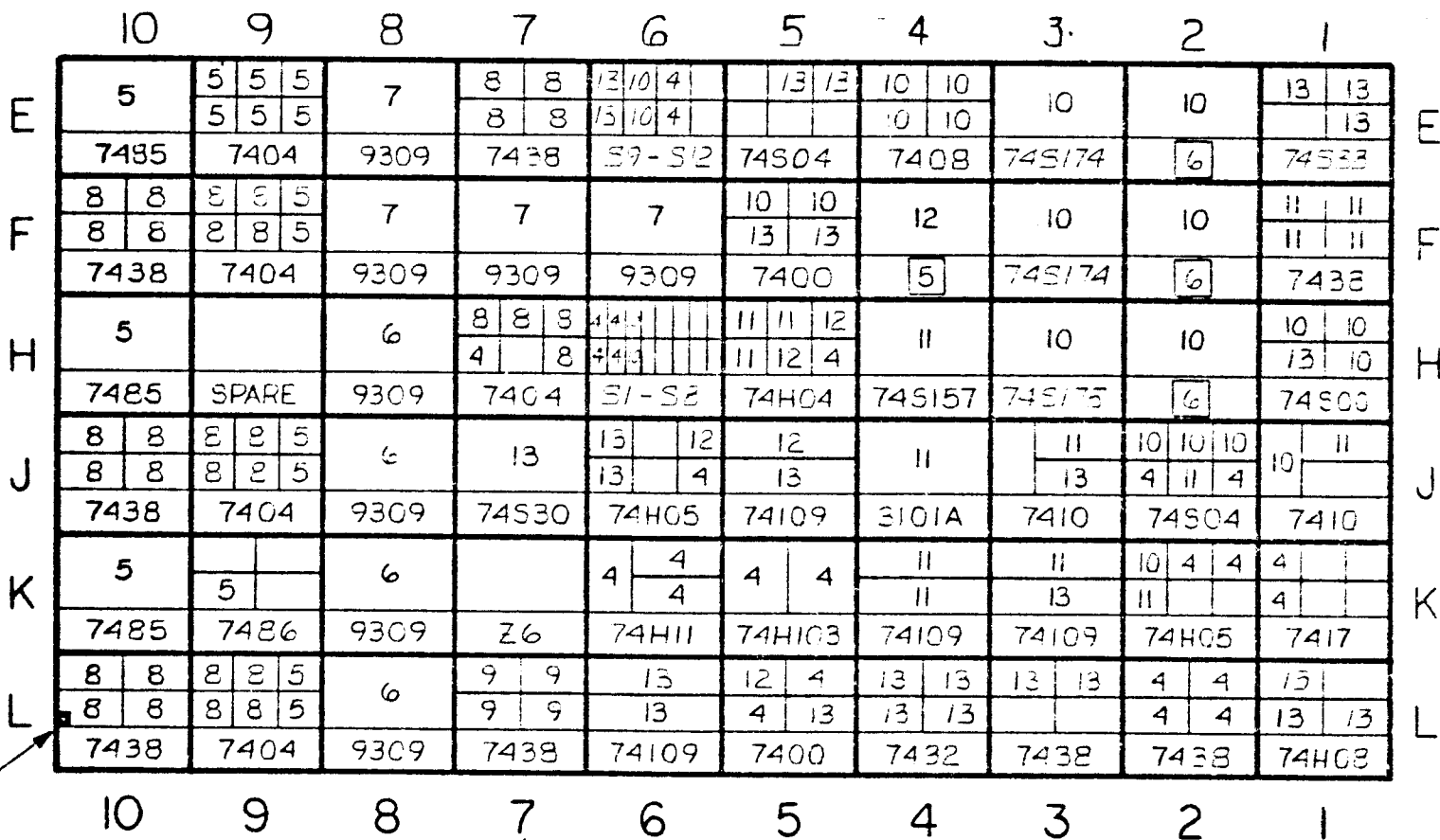
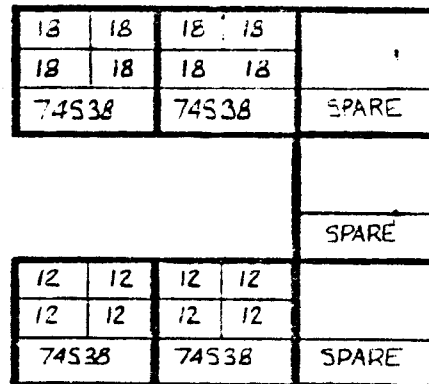
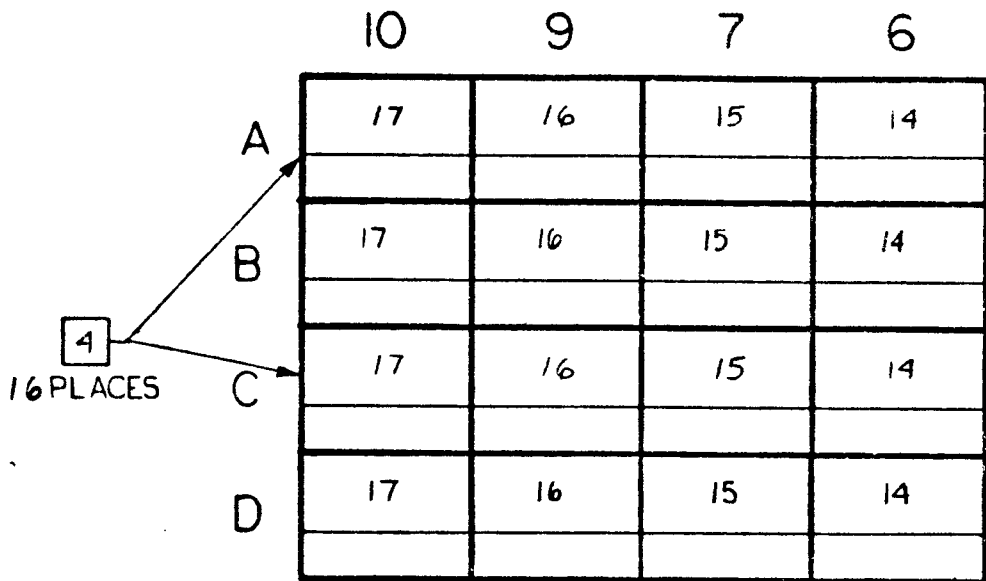


REV	EO	ZONE	DESCRIPTION	DWN	CHG	APP	D
AX	9454		PROTO RELEASE				
A	9518		PILOT RELEASE				

COMPONENTS USED	LAST REF DES USED	REF DES NOT USED
CAPACITORS	C50	C12,15,16
RESISTORS	R15	
RESISTOR MOD	Z9	
DIODES	CR16	
TRANSISTOR	Q1	
TEST POINTS	TP2	
E POINTS	E43	
SWITCHES	S12	S4-8,512



6 PCB BOARD LOCATION 2E IS PR20005058-001, LOCATION 2F IS PR20005058-002 & LOCATION 2H IS PR20005058-003.

5 PCB BOARD LOCATION 4F IS LAYED OUT FOR SP54610187 (MICRODATA) PROM AND WILL BE PROGRAMMED AND INSTALLED AT NEXT ASSEMBLY LEVEL.

4 PCB BOARD LOCATIONS 6A-6D, 7A-7D, 9A-9D, 10A-10D ARE LAYED OUT FOR SP5450136 (MICRODATA) PROMS & MUST BE PROGRAMMED TO INDIVIDUAL BOARD APPLICATION.

3. ALL CAPACITORS ARE .01UF, 100V.

2. ALL RESISTORS ARE 1/4W, ±5%, VALUED IN OHMS.

1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.

UNINCORPORATED ENGINEERING ORDERS

SC20001281	DESIGNED BY	DATE
	ENGINEER	
	APPROVED	
	DATE	
	BY	

TITLE  
PCB SCHEMATIC -  
BK ROM MAINTENANCE  
INTERFACE

**Microdata**  
IRVINE, CALIFORNIA

C SC20001281

SCALE N/A/E

IDENT CODE 52936

DWG SIZE

SHEET 1 OF 3

PAGE NO.	A	P1	B	PAGE NO.
	GND	1	+5V	
	GND	2	+5V	
12	TTIN/	3		
11	MUA1/	4	RUNX	4
11	MUA2/	5	CLKF/	4
10	CPH1/	6	STPF/	4
4	RUNF/	7	M04A/	7
		8	MUAQ/	11
6	NOTA/	9	M06A/	7
		10		
7	M01A/	11	A04L/	6
7	M02A/	12		
6	A00L/	13	M03A/	7
6	A01L/	14	M00A/	7
6	N06A/	15	RS00	12
14	LOOX	16		
5	L11X	17	RS04	12
14	LO4X	18	M05A/	7
12	RS01	19	L10X	5
14	LO1X	20		
		21	RS05	12
14	LO5X	22		
12	RS02	23		
14	LO2X	24	MERR/	13
14	LO6X	25	RS06	12
		26		
12	RS03	27		
14	LO3X	28		
6	A02L/	29	RS07	12
14	LO7X	30		
		31		
		32		
4	CPEN/	33	LO8X	14
6	A03L/	34		
		35	LO9X	5
		36	RS08	18
18	RS09	37		
		38	A05L/	6
4	RINH/	39		
13	CG1B/	40		
10	CSTP/	41	A06L/	6
18	RS10/	42		
18	RS11	43	SP2	9
		44	MRST/	4
11	DMAS/	45	ES06	4
4	INTF/	46	SP7	9
18	RS13	47	M07A/	7
18	RS14	48	A07L/	6
4	RTN	49	ES05	4
6	N03A/	50	INLR	4
18	RS12	51	N00A/	6
		52	MPFR/	13
6	N04A/	53	N01A/	6
6	N05A/	54	MPSS/	13
13	MPFD/	55	N02A/	6
		56	ES04	4
4	ES07	57	AENP/	4
		58		
18	RS15	59		
		60	CPH2/	10
		61		
		62		
4	SCAN/	63	RPSS/	4
	GND	64	+5V	
	GND	65	+5V	

J4		PAGE NO.
1	CRO0F/	8
2	CRO3F/	8
3	CRO1F/	8
4	CRO2F/	8
5	RPSS/	4
6	SCAN/	4
7	RUNA/	4
8	GND	
9		
10	ASSW	4
11	GND	
12	GND	
13	MERR/	13
14	LEDQ/	6
15	LED1/	6
16	MPSS/	13
17		
18		
19	ES04	4
20		
21	CLKF/	4
22	MRSTA/	4
23	GND	
24	ES07	4
25	+5V	
26	+5V	
27	LED3/	6
28	LED2/	6
29	CLDST/	9
30	CLDST	9
31	MPFR/	13
32	MPFD/	13
33	GND	
34	GND	
35	ES06	4
36	GND	
37	ES05	4
38	INTF/	4
39	GND	
40	CPSE/	4
41	LED7/	6
42	LED6/	6
43	CRO4F/	8
44	CRO7F/	8
45	LED5/	6
46	LED4/	6
47	CRO5F/	8
48	CRO6F/	8
49	GND	
50	GND	

J2		PAGE NO.
1	CR10F/	8
2	CRO8F/	8
3	LEDA/	7
4	STPF/	4
5	CR15F/	8
6	GND	
7	LED9/	7
8	CR14F/	8
9	LEDD/	7
10		
11	RS1X	7
12	LEDE/	7
13	+5V	
14	CR11F/	8
15	CRO9F/	8
16	LEDB/	7
17	RUNF/	4
18	CR12F/	8
19	GND	
20	LEDB/	7
21	CR13F/	8
22	LEDC/	7
23	GND	
24	RS0X	7
25	LEDF/	7
26	+5V	

J5		PAGE NO.
1	CLDST	9
2	CLDST/	9
3	GND	9
4		

"E" POINT DEFINITIONS			
	CUT ETCH		
	FROM	E1	E3
DISABLES COLD START FROM FRONT PANEL TO BACKPLANE	TO	E2	E4
ENABLES COLD START FROM FRONT PANEL TO BACKPLANE	TO	-	-

SWITCH DEFINITIONS						
	S1	S2	S3	S9	S10	S11
1600 PROC.	X	X	X	B	B	B
1683 PROC.				A	A	A

PEP

'200'  
'150'

3X  
4X

	CUT ETCH			ADD JUMPER
	FROM	E6	E8	E10
128 K ONLY	TO	E7	E9	E11
512 K	TO	-	-	-

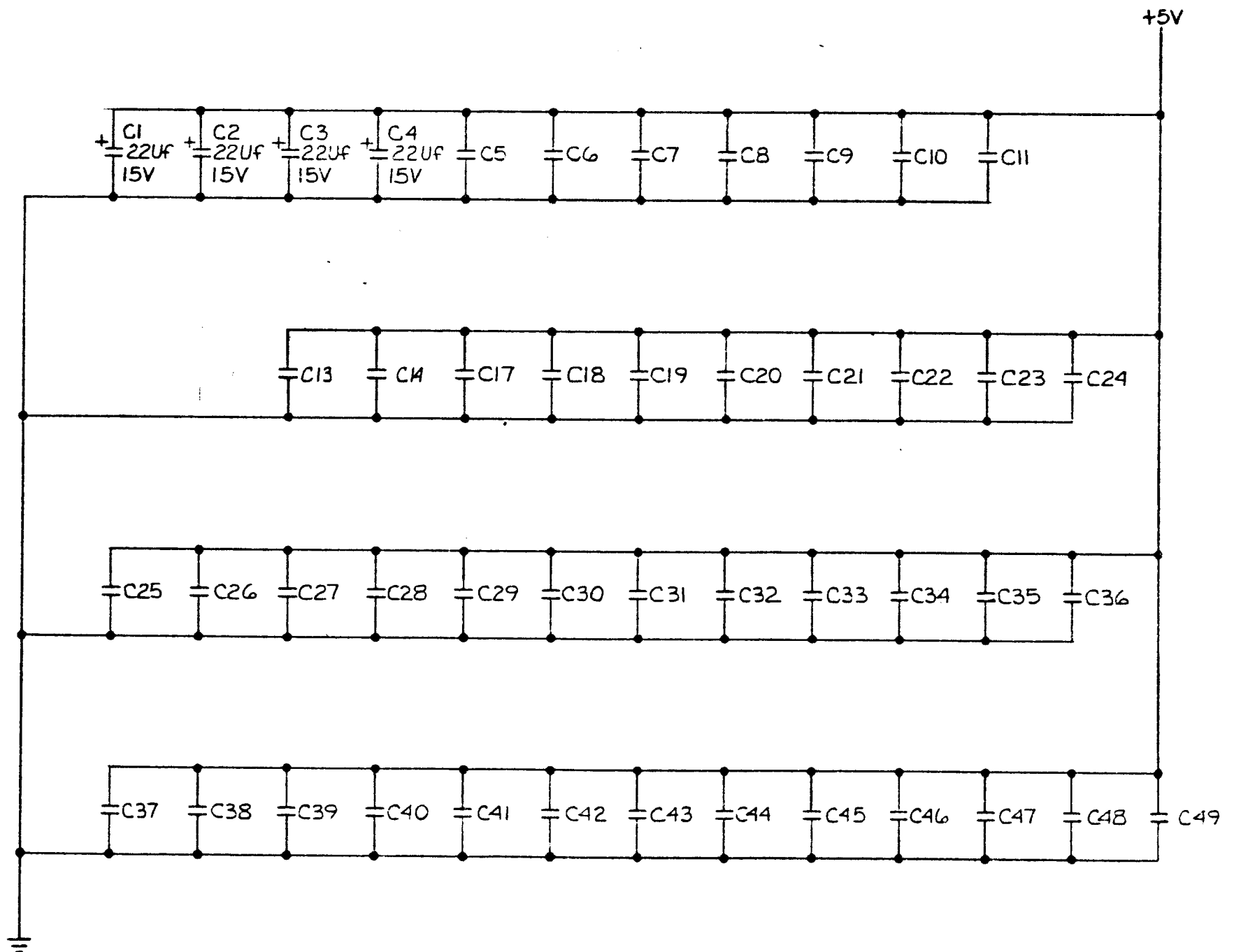
X = SWITCH CLOSED

-001  
-002

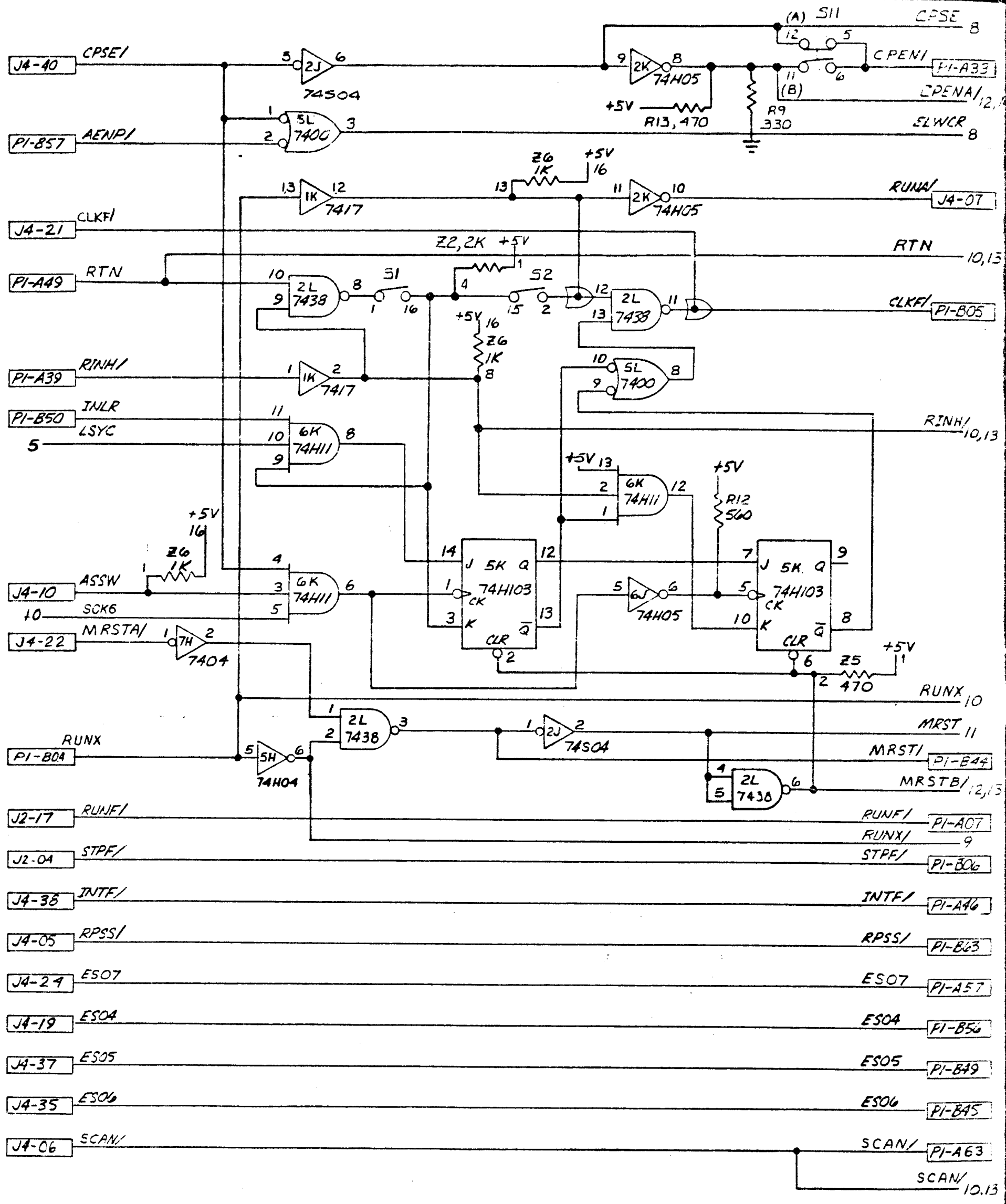
C

B

A

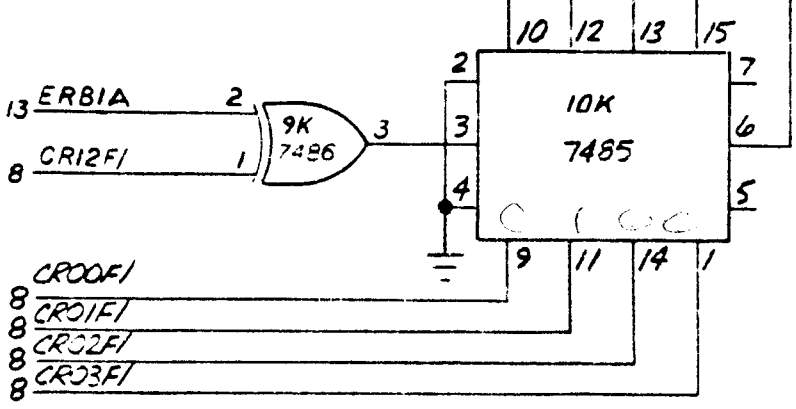
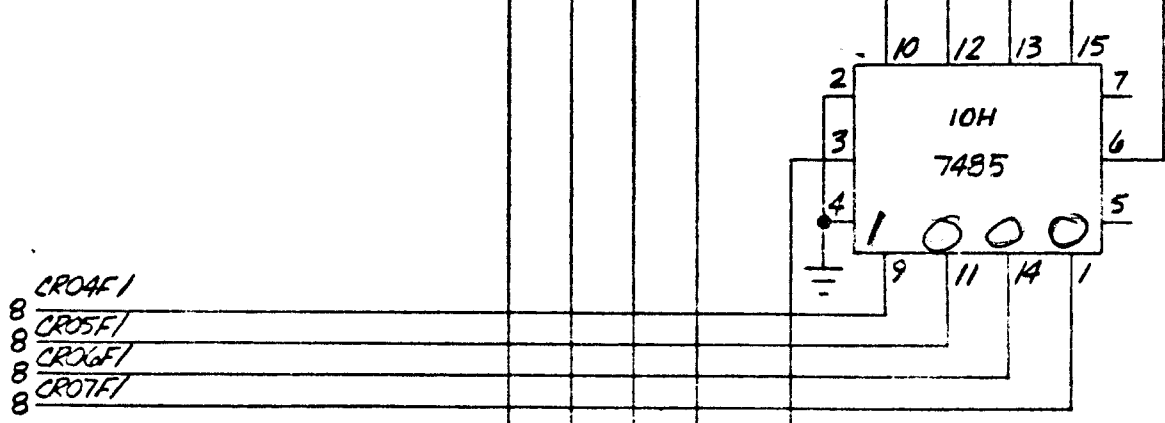
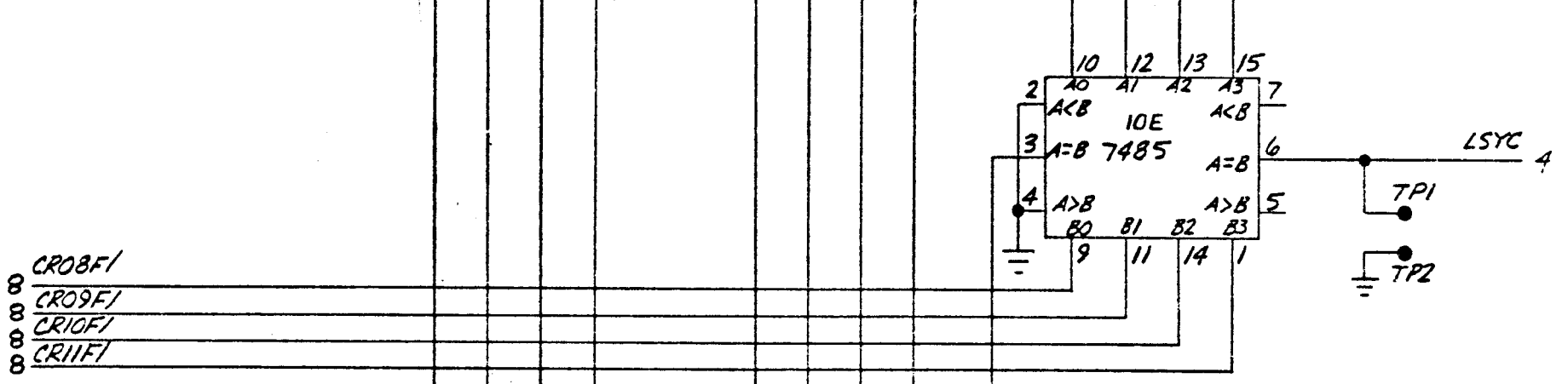
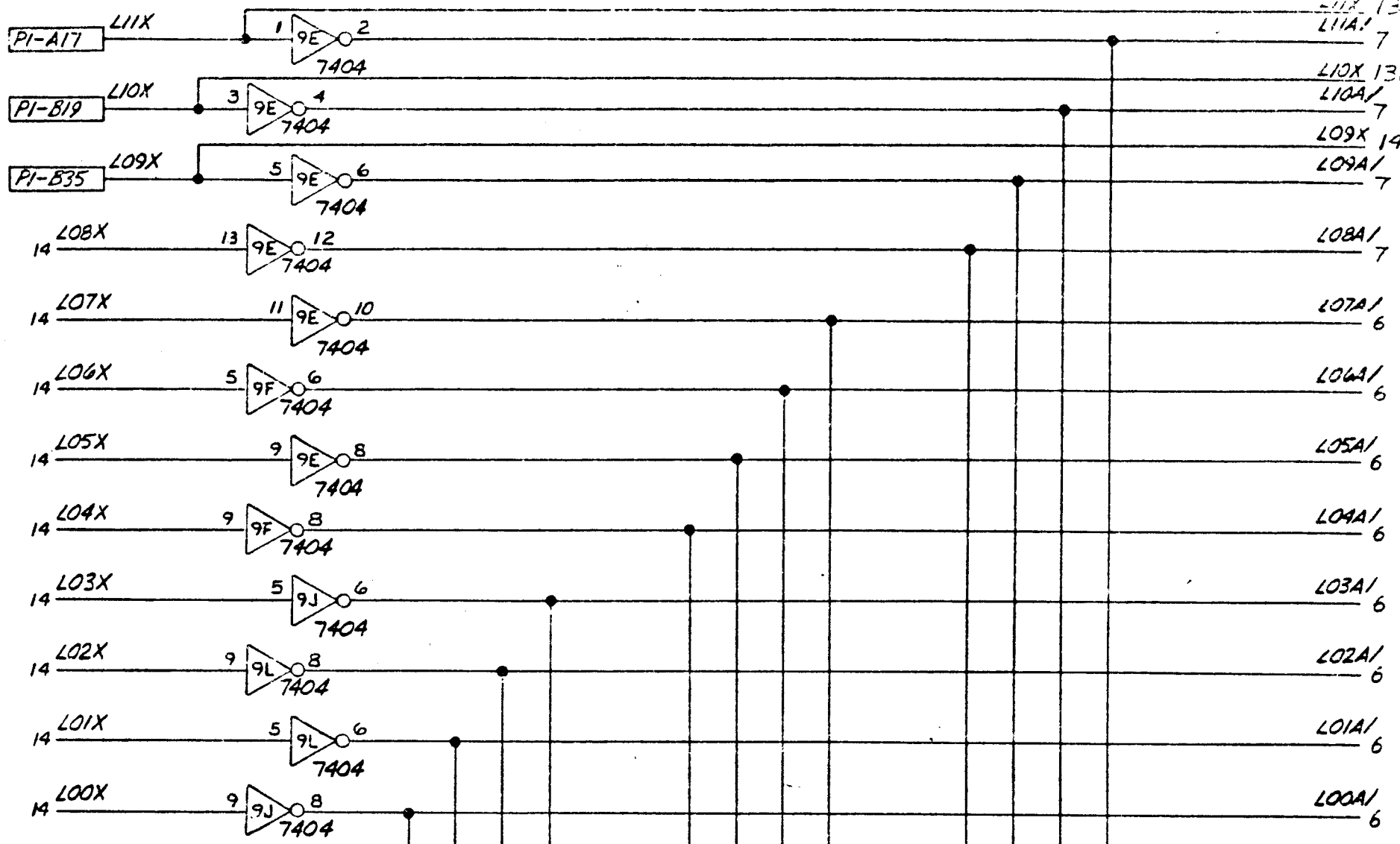


C	SC2000:281
DWG SIZE	SHEET 5 OF 8



CONTROL MEMORY & MAINTENANCE

C	SC20001281
DWG SIZE	SHEET 4 OF 15



CONTROL MEMORY & MAINTENANCE

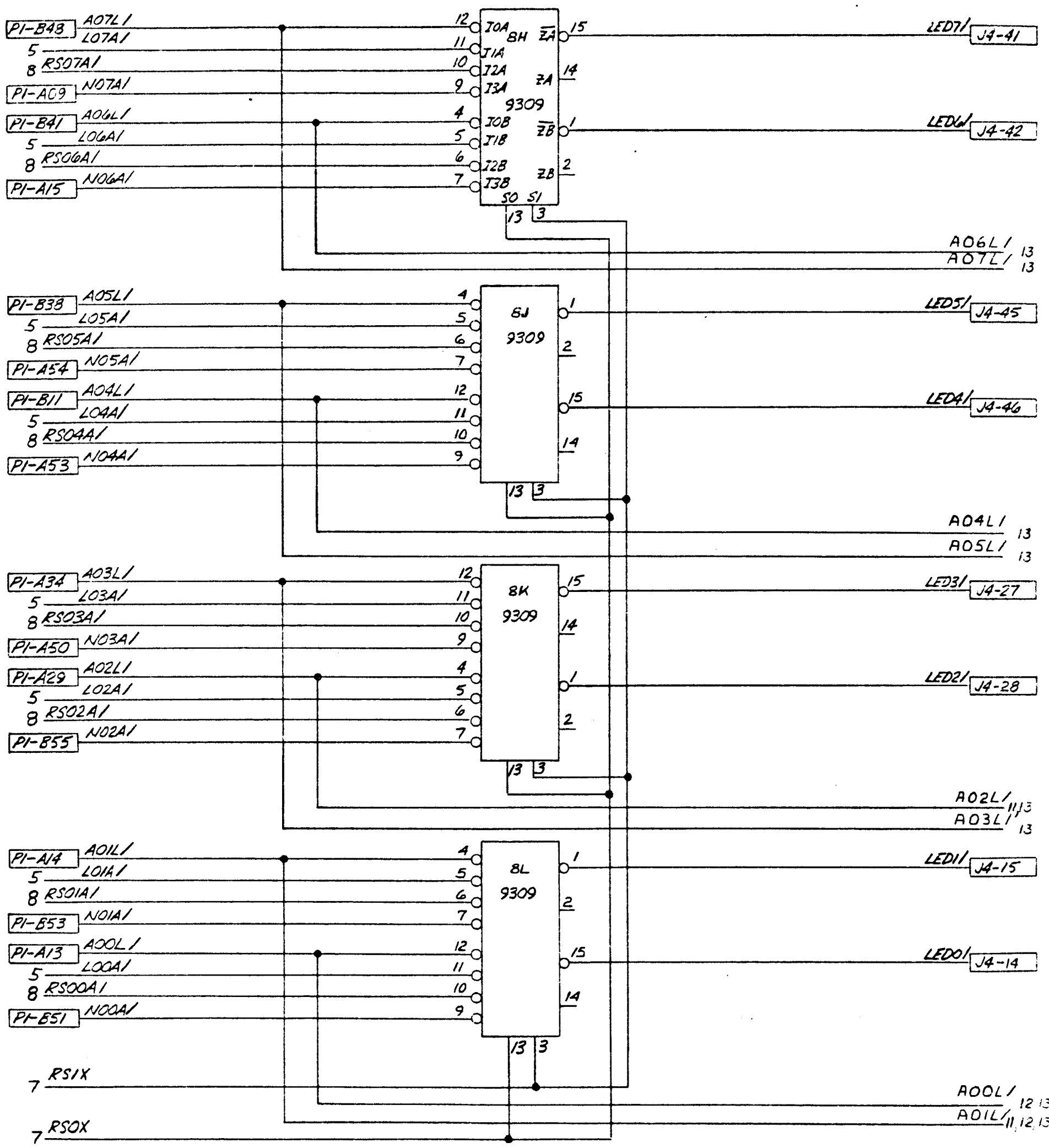
<b>C</b>	SC20001281
DWG SIZE	SHEET 5 OF 5

D

C

B

A



CONTROL MEMORY & MAINTENANCE

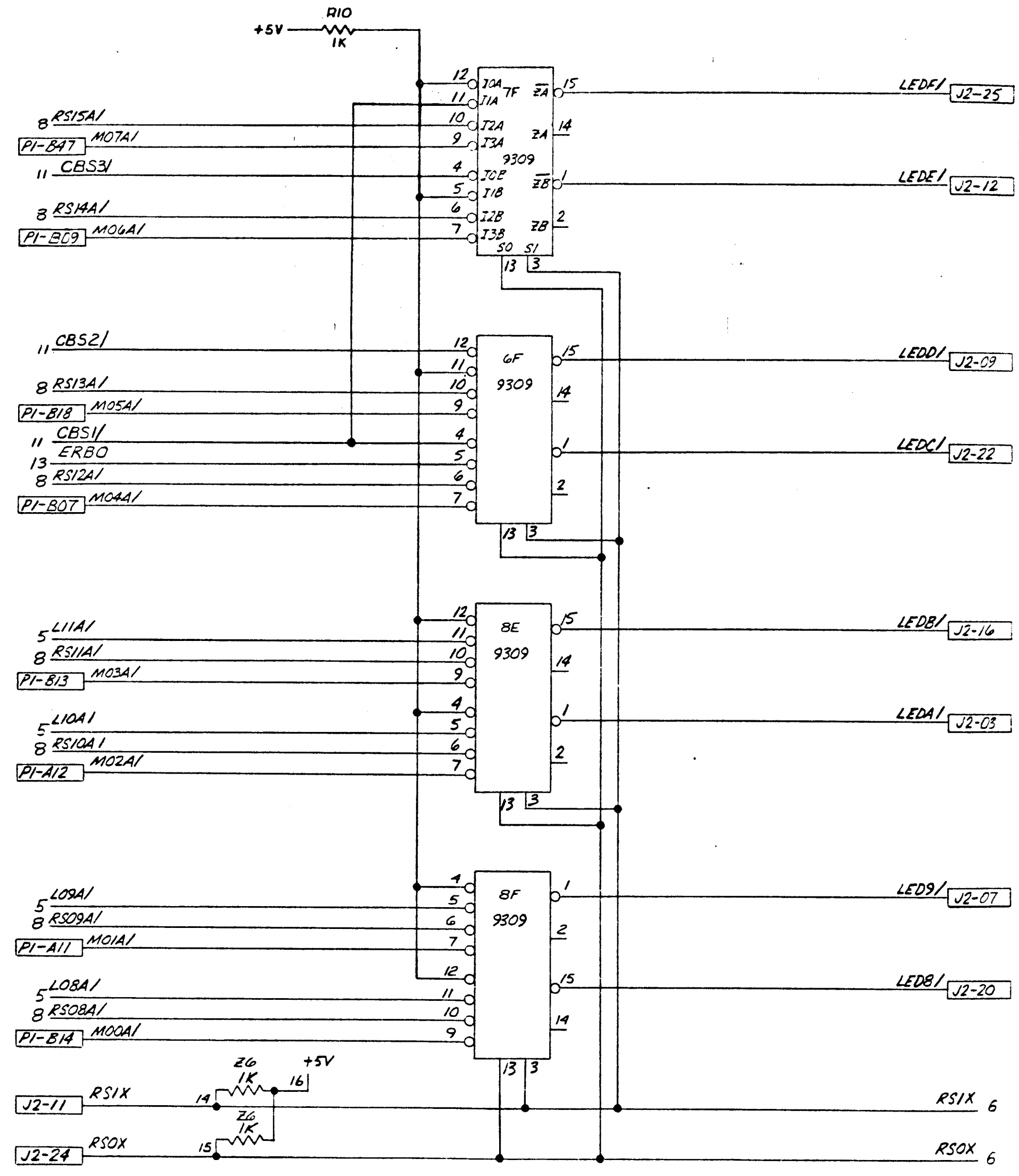
<b>C</b>	SC20001261
DWG SIZE	SHEET 6 OF 15

D

C

B

A



CONTROL MEMORY & MAINTENANCE

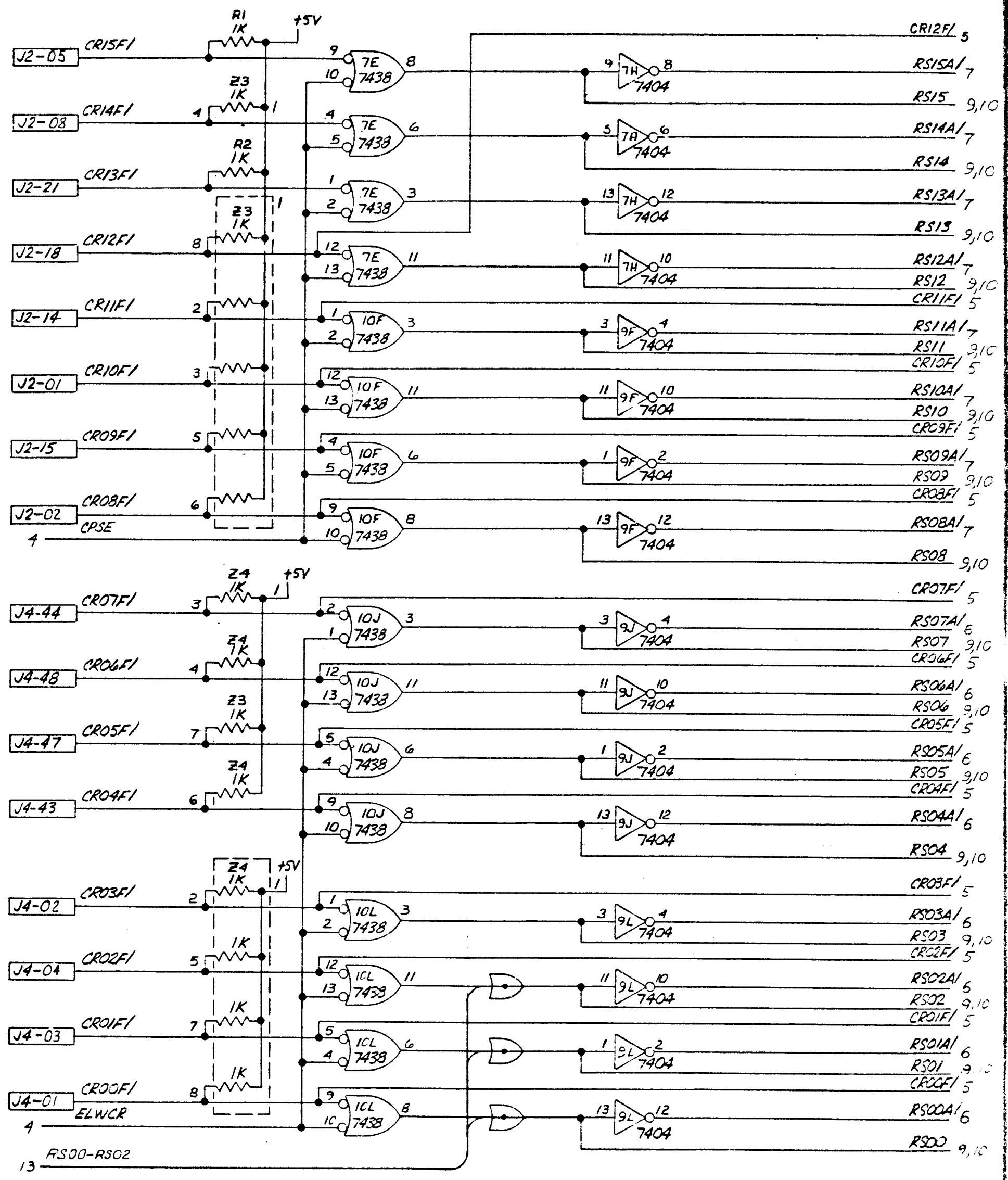
C	SC20001281
DWG SIZE	SHEET 7 OF 15

D

C

B

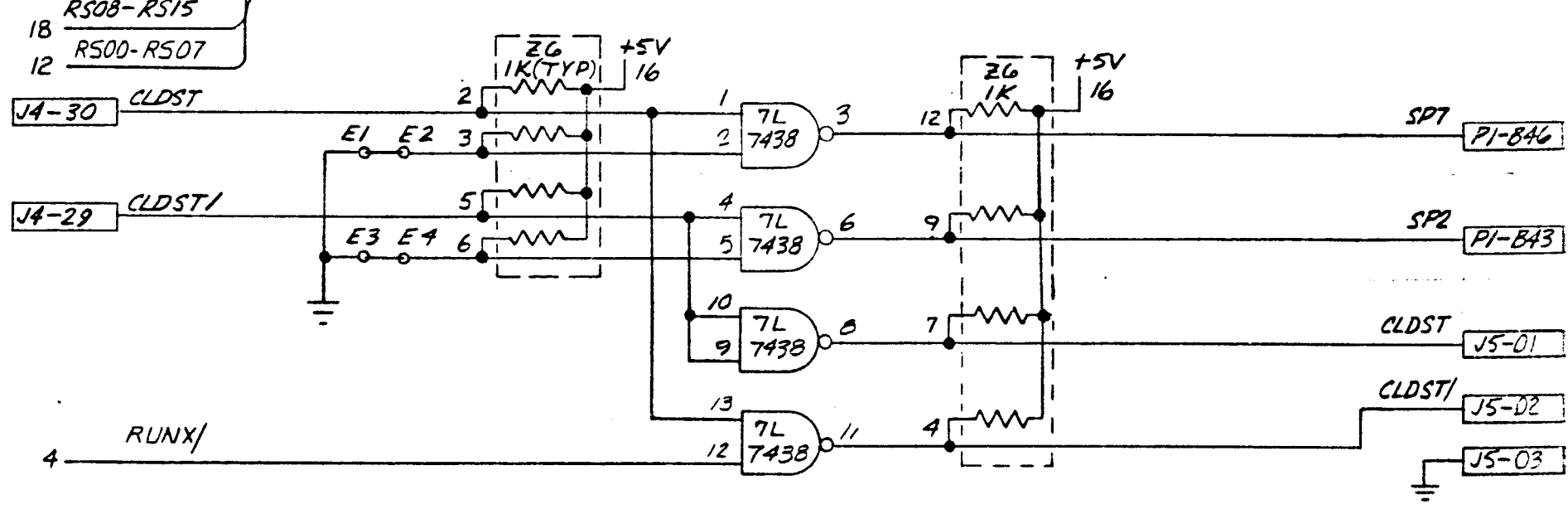
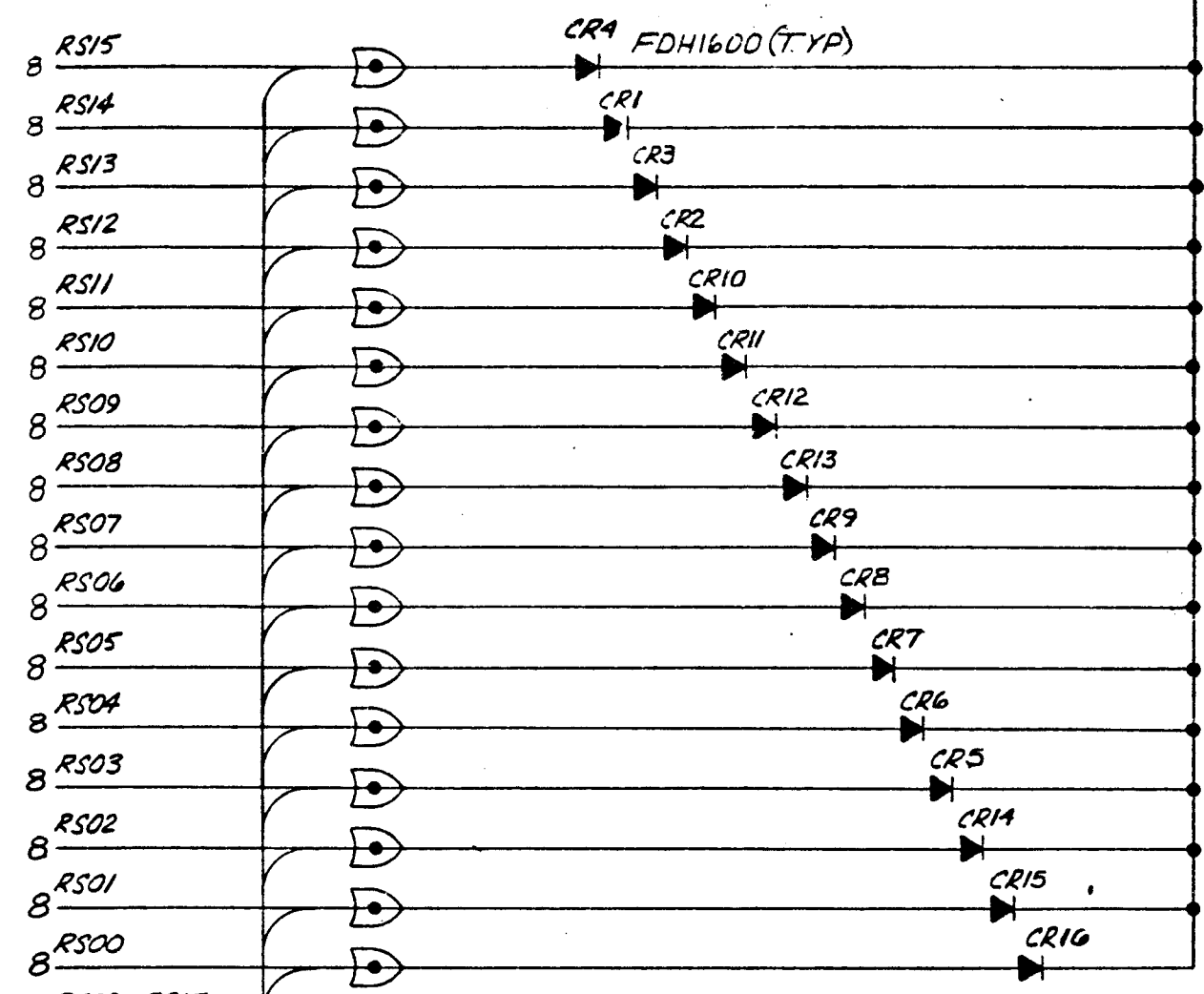
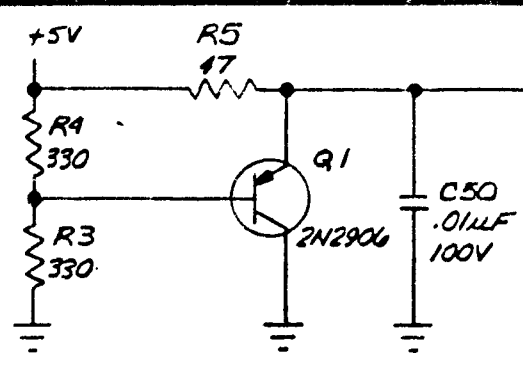
A



CONTROL MEMORY & MAINTENANCE

<b>C</b>	SC20061281
DWG SIZE	SHEET 8 OF 8





CONTROL MEMORY & MAINTENANCE

C	5C20001281
DWG SIZE	SHEET 9 OF 13

D

C

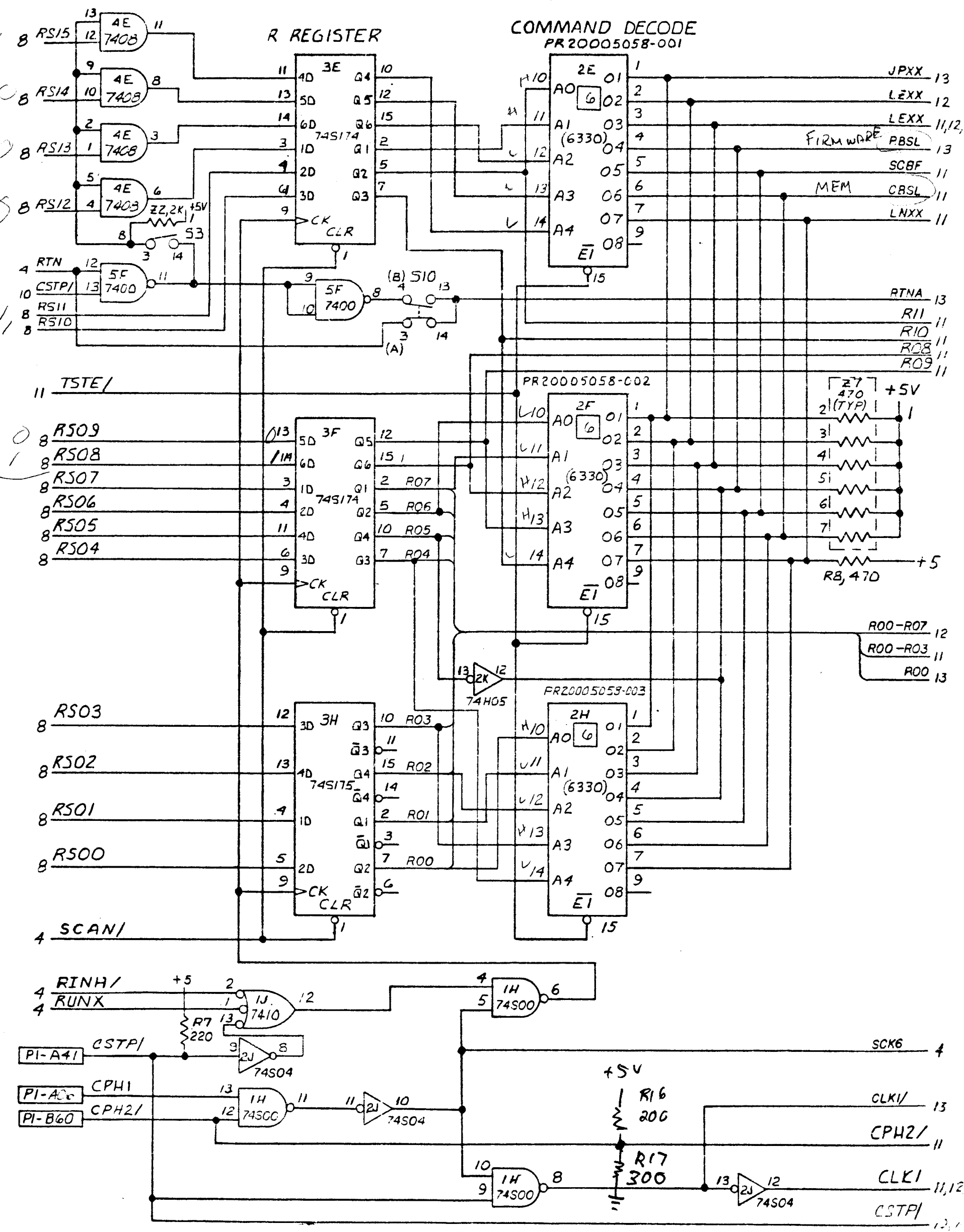
B

A

### R REGISTER

### COMMAND DECODE

PR20005058-001

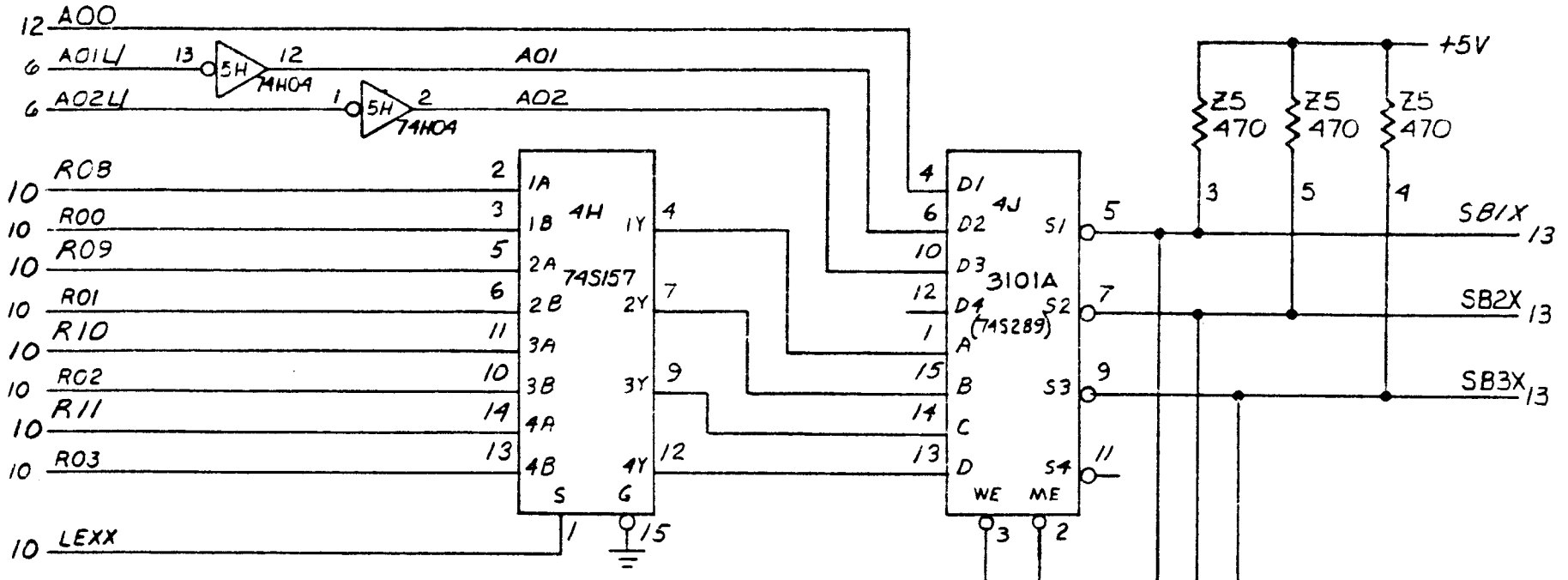


E0# 9872  
9868

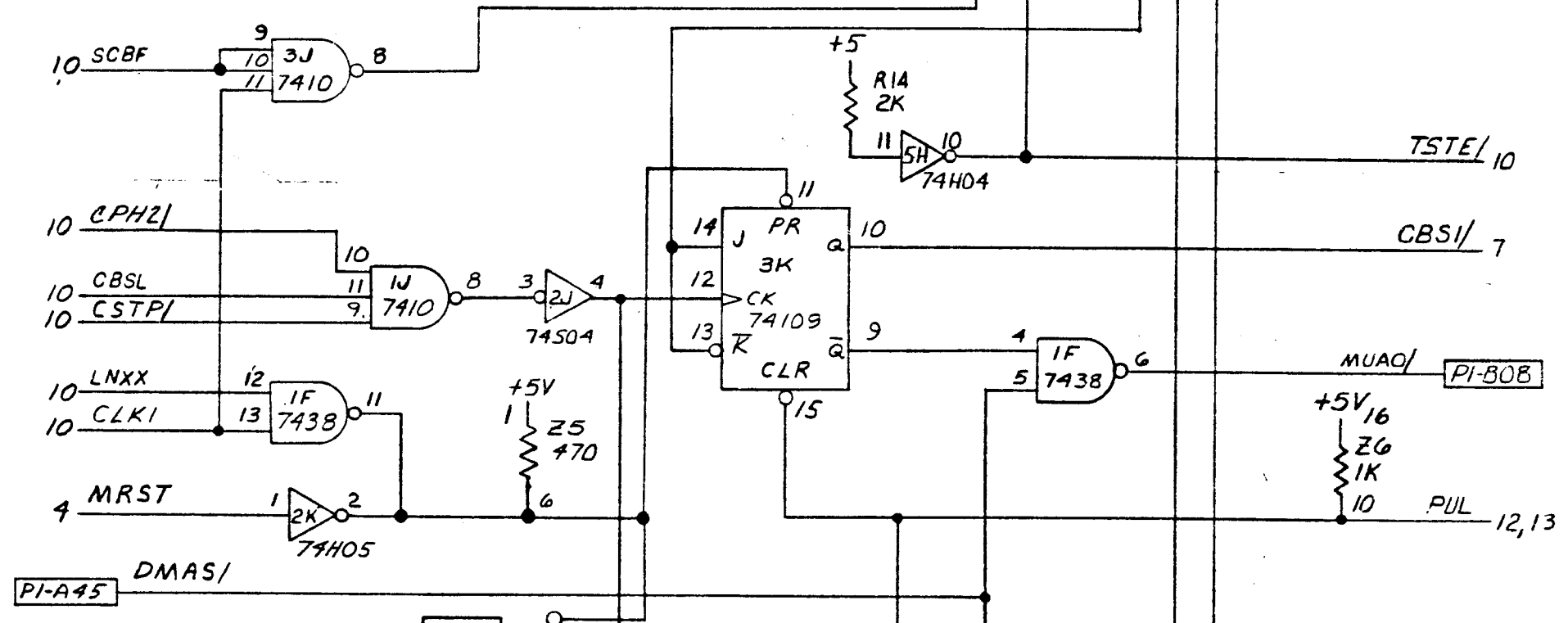
C	SC20001281
	DWG SIZE SHEET 10 OF #

CPU CORE BANK HOLDING REGISTER

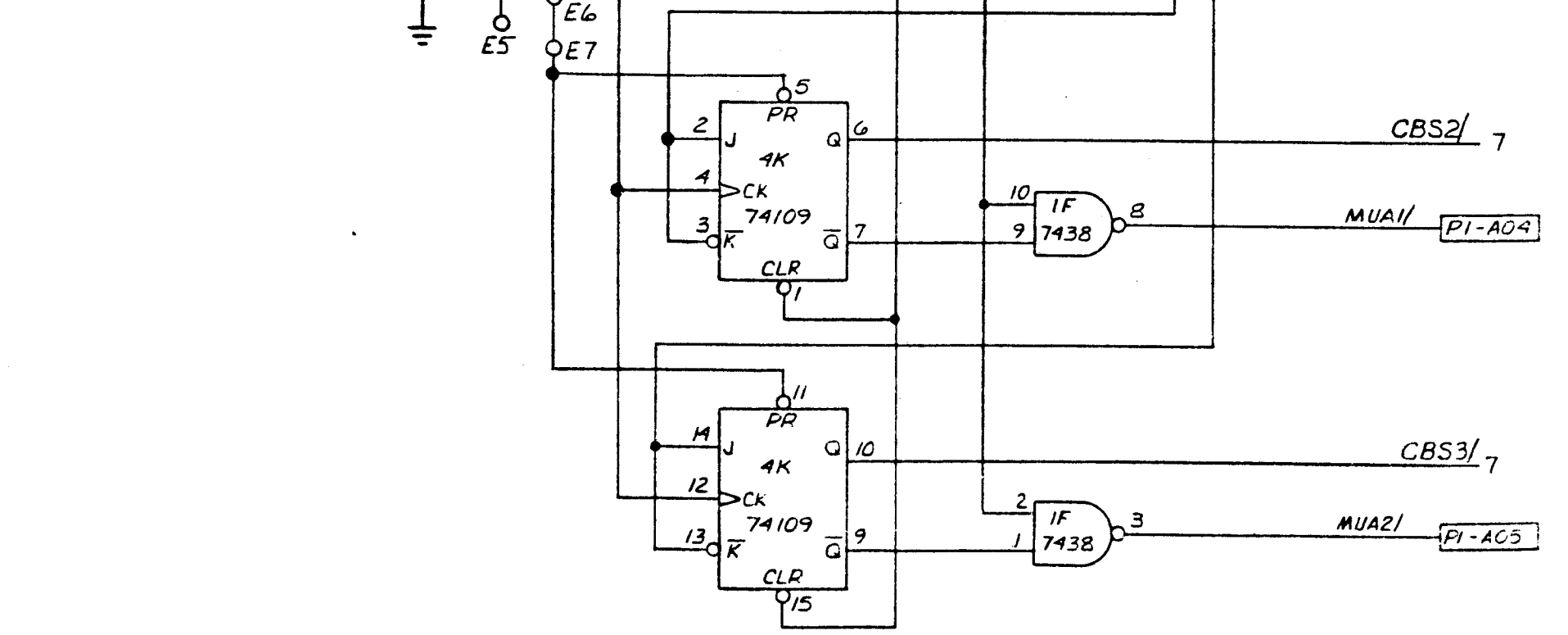
D



C



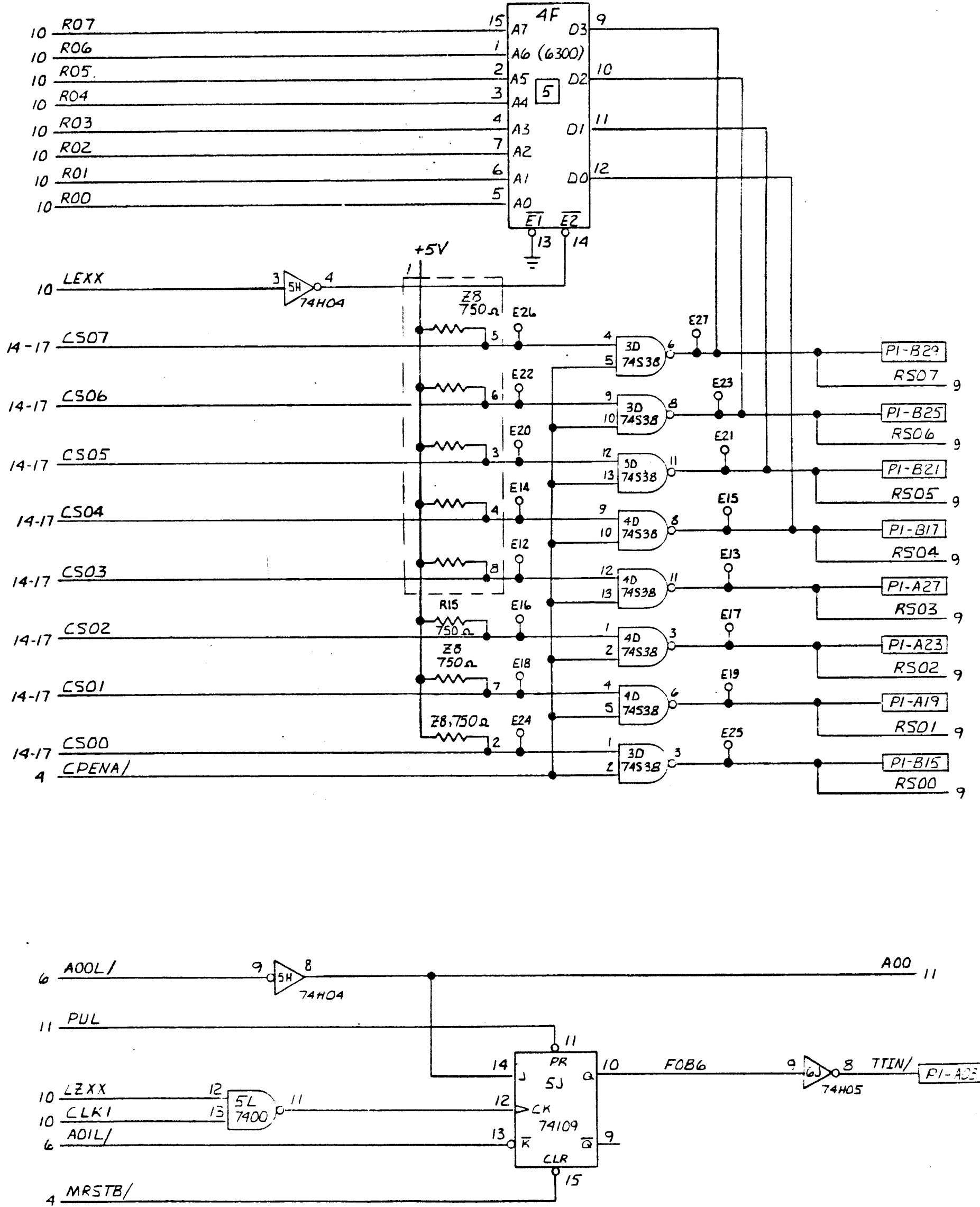
B



A

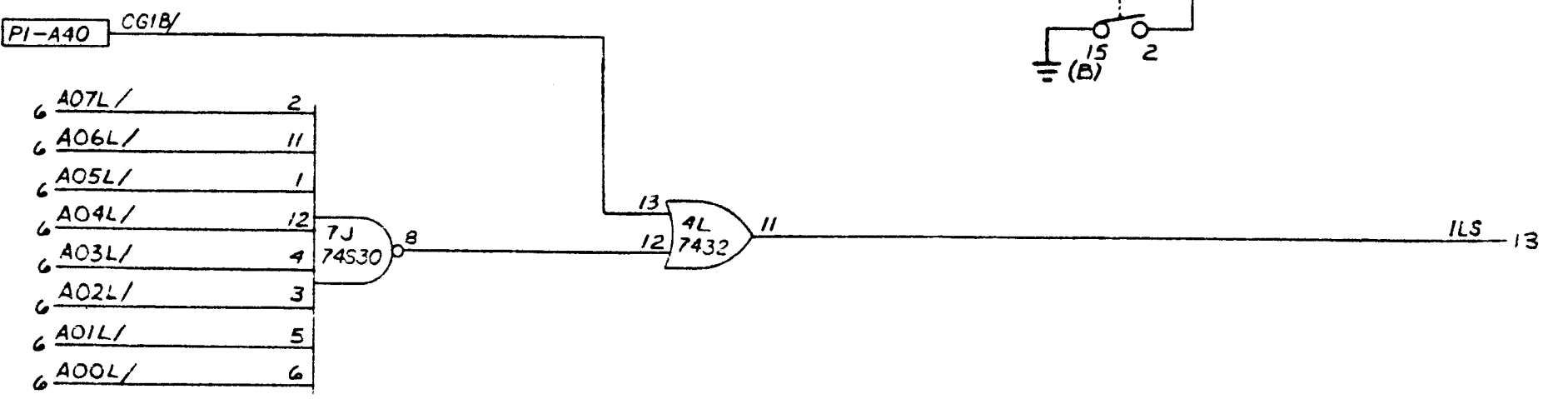
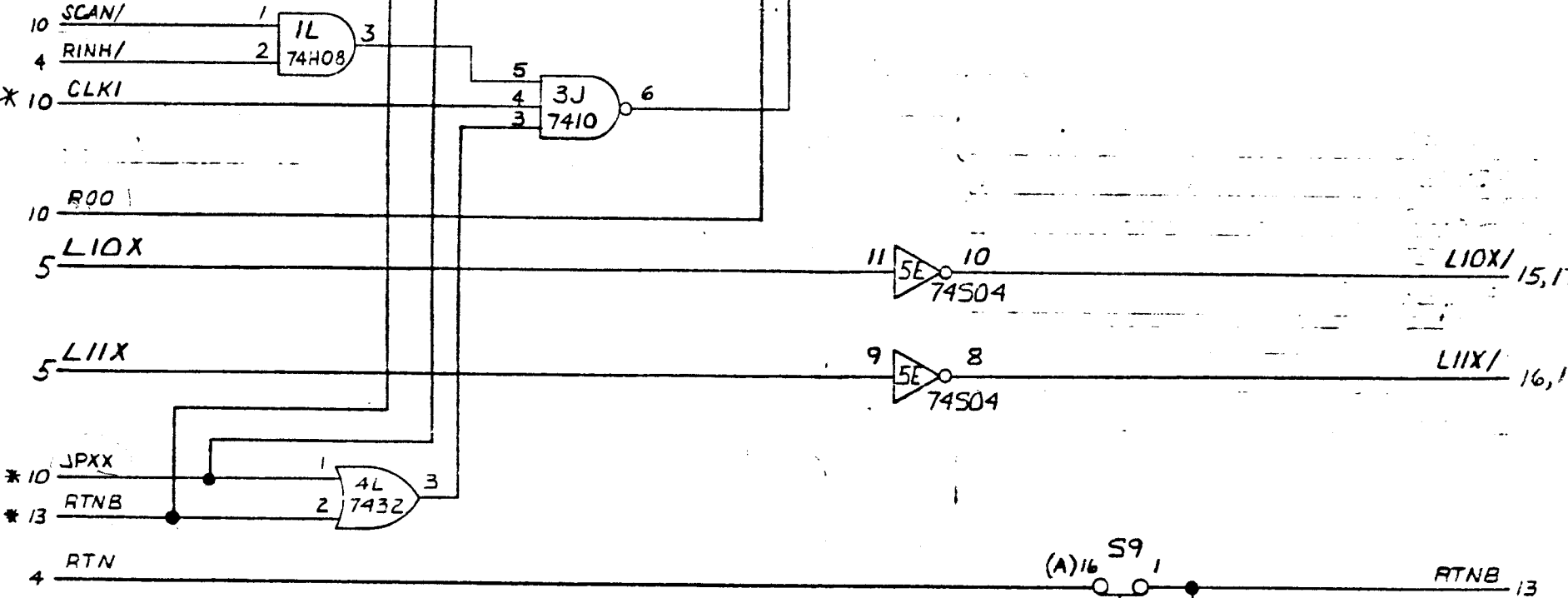
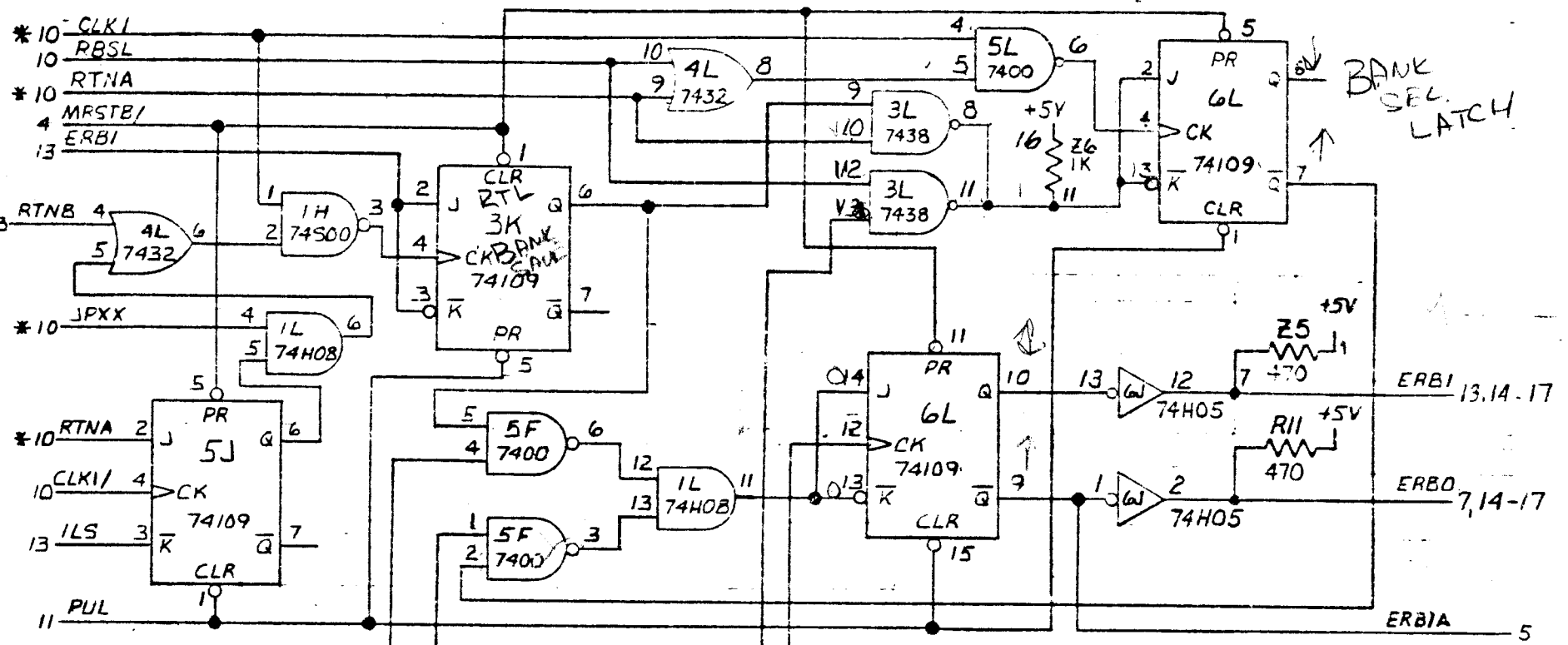
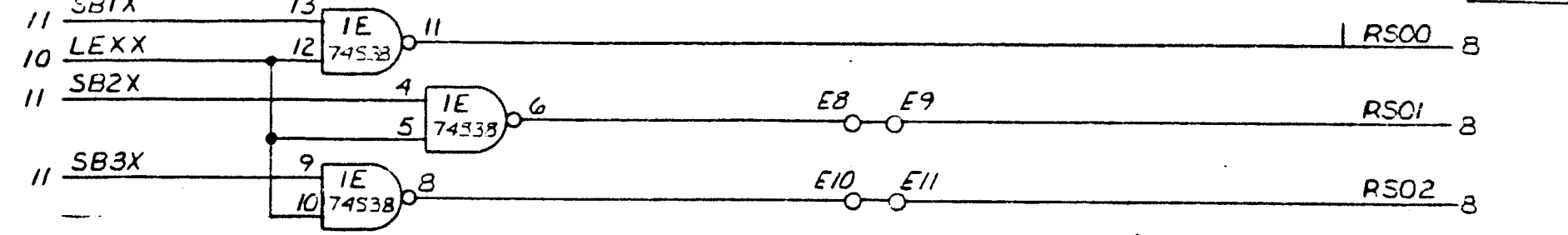
<b>C</b>	SC20001281
DWG SIZE	SHEET // OF 15

# CONFIGURATION ROM



<b>C</b>	SC 20001281
DWG SIZE	SHEET 14 OF 15

PI-B24	MERR/	MERR/	J4-13
PI-A55	MPFD/	MPFD/	J4-32
DI-B52	MPFR/	MPFR/	J4-31
PI-B54	MPSS/	MPSS/	J4-16



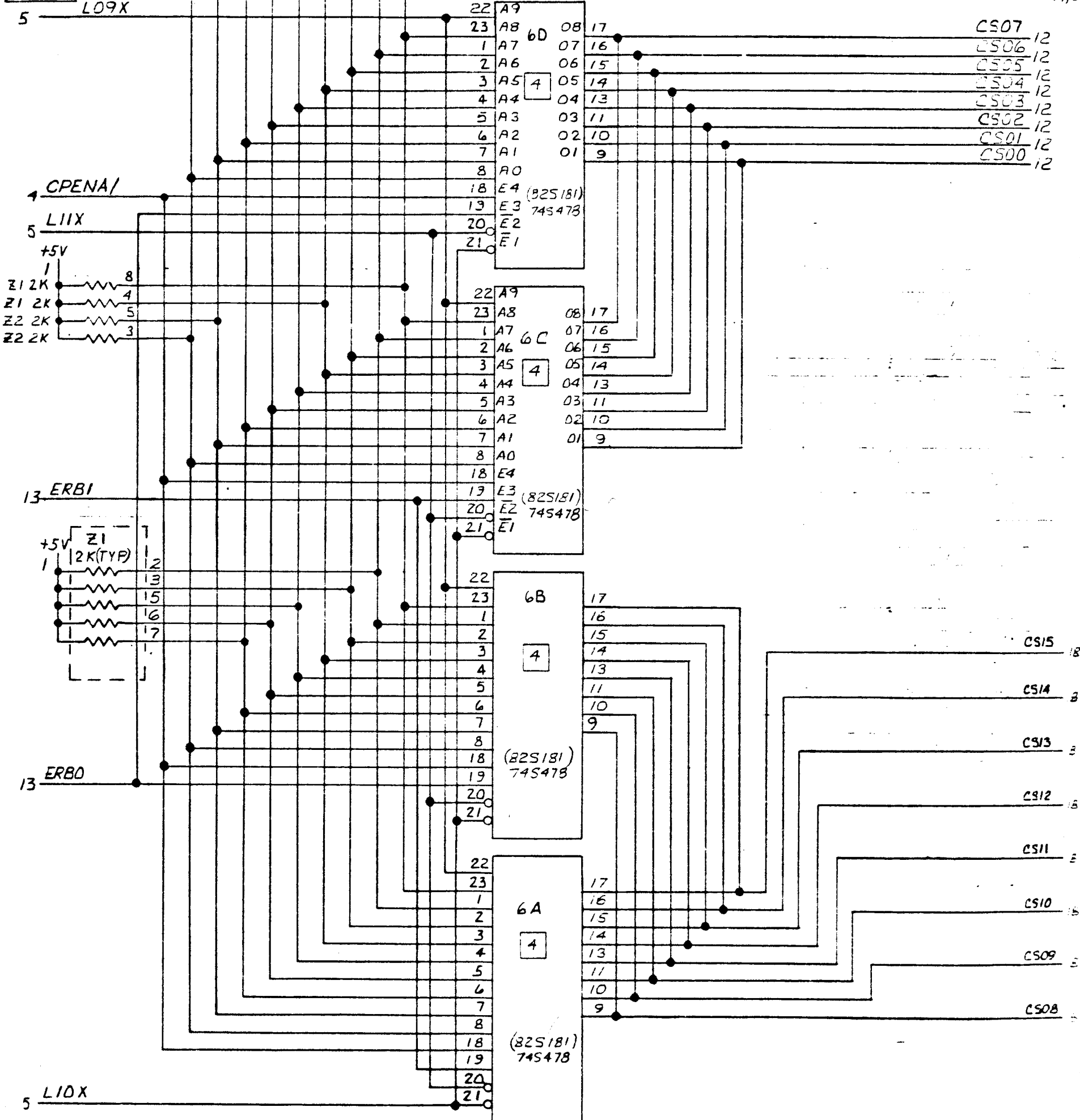
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C	SC20001281
DWG SIZE	SHEET 13 OF 15

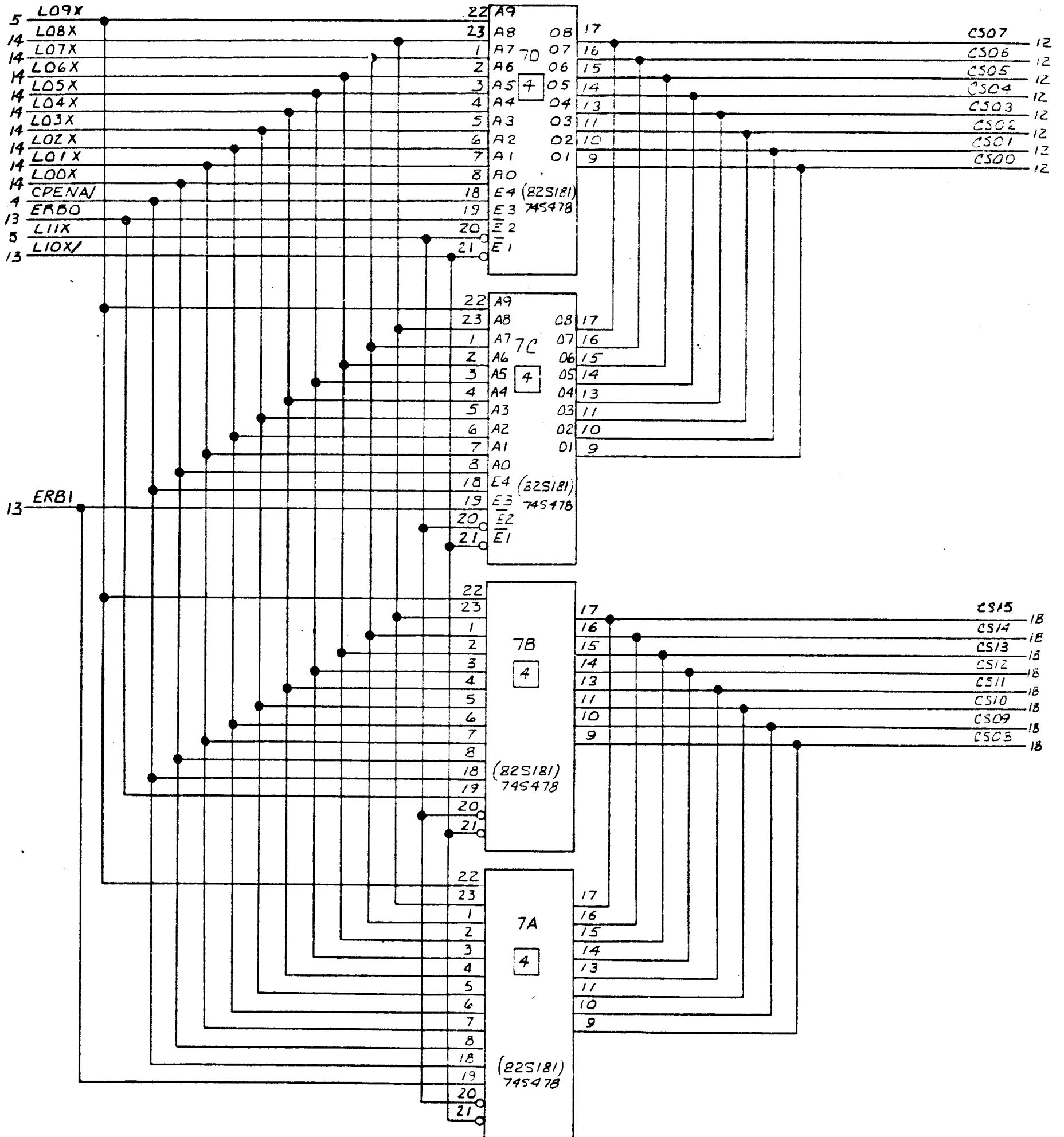
RDM BANK 0, 1 - PAGES 0-3

PI-B33	LO8X
PI-A30	LO7X
PI-A25	LO6X
PI-A22	LO5X
PI-A18	LO4X
PI-A28	LO3X
PI-A24	LO2X
PI-A20	LO1X
PI-A16	LO0X

LO8X	15-17
LO7X	15-17
LO6X	15-17
LO5X	15-17
LO4X	15-17
LO3X	15-17
LO2X	15-17
LO1X	15-17
LO0X	15-17



ROM BANK 0,1-PAGES 4-7



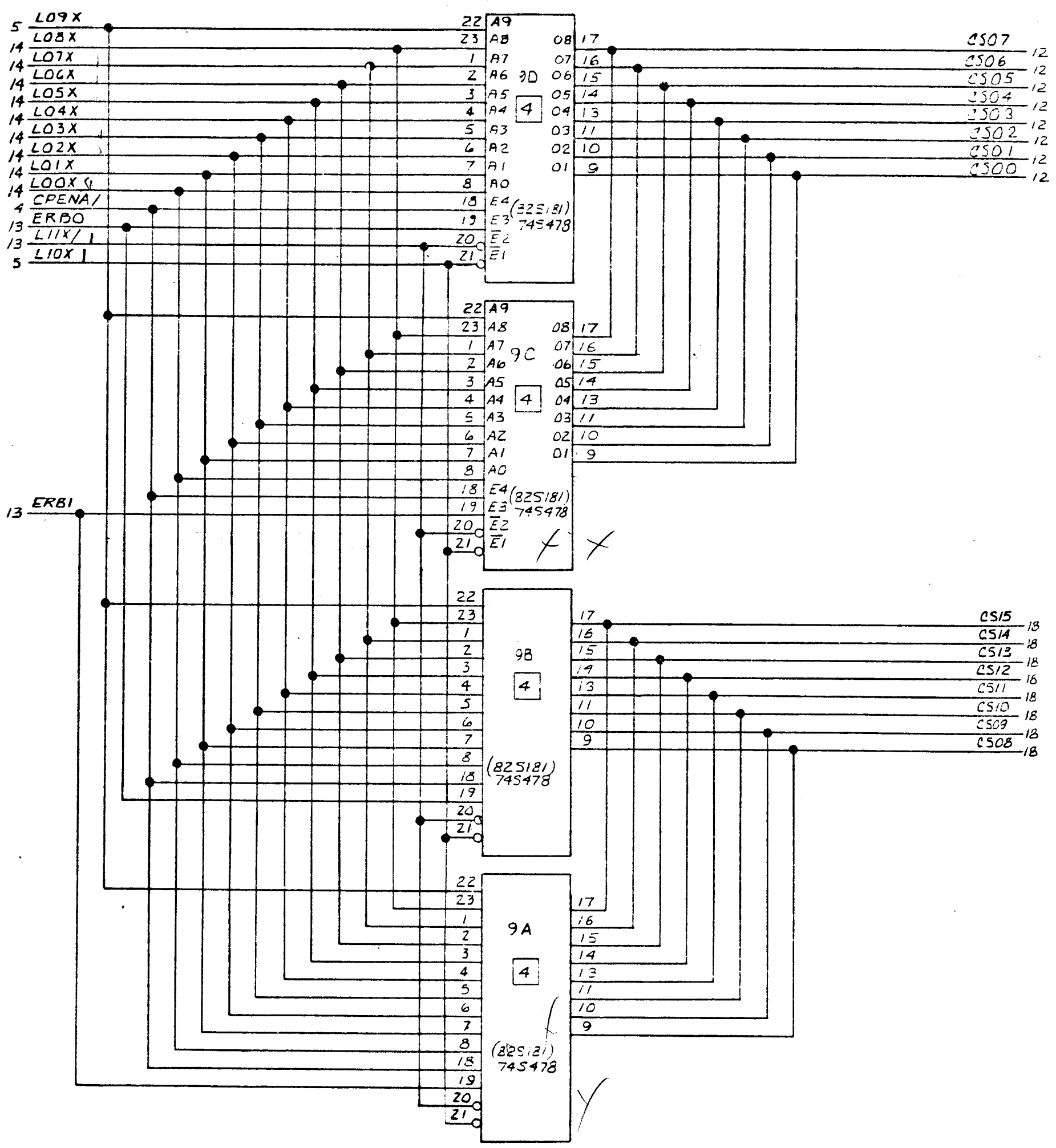
E 8 7 F SEA  
 1110 0000 0111 F

(1101101)

101 0

A

ROM BANK QI-PAGES B-B



D

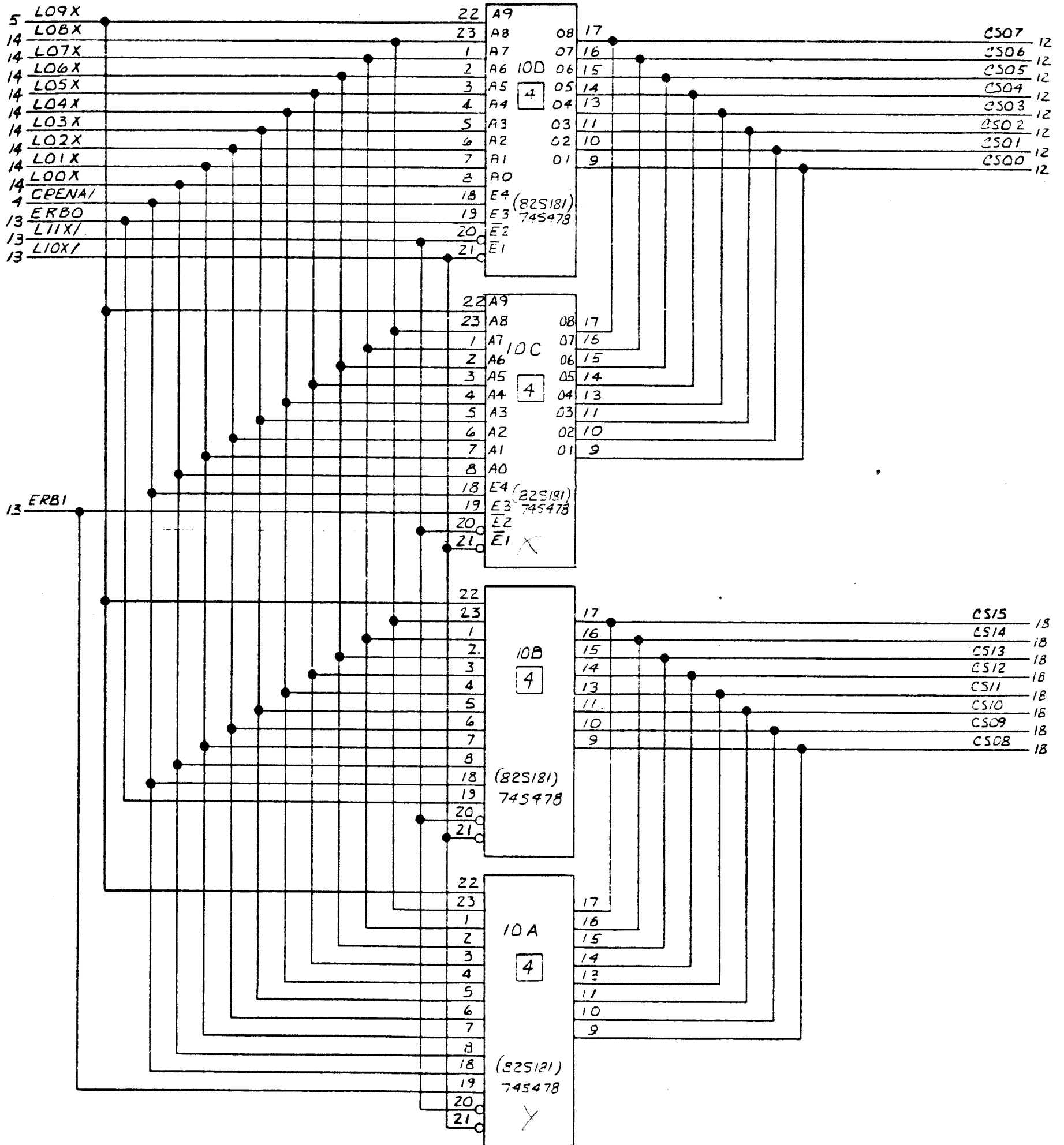
C

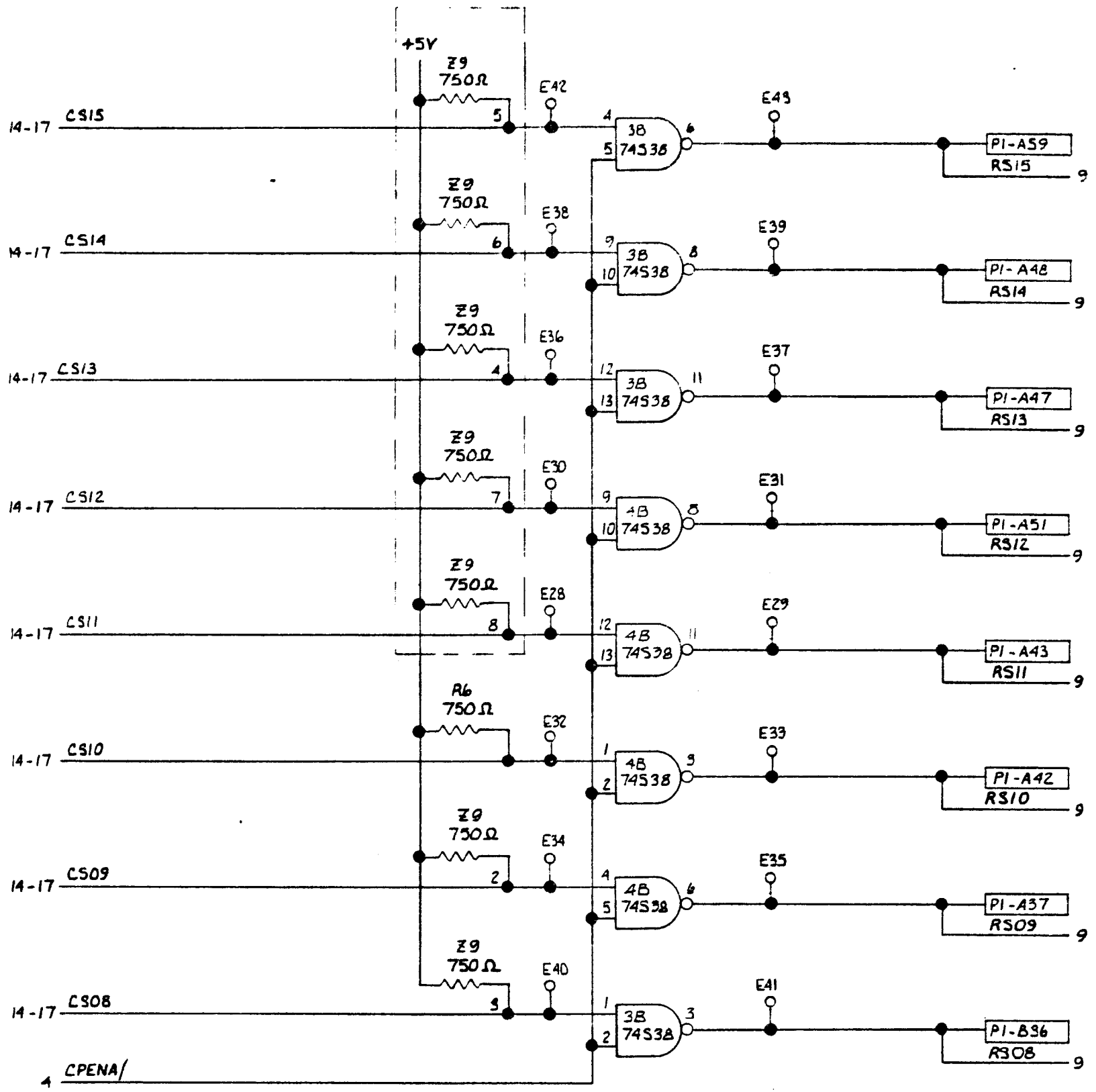
B

A



ROM BANK 0, PAGES C-F





C SC20001281  
 DWG SIZE SHEET 14 OF 13