MDB 1710

GENERAL PURPOSE INTERFACE MODULE

INSTRUCTION MANUAL
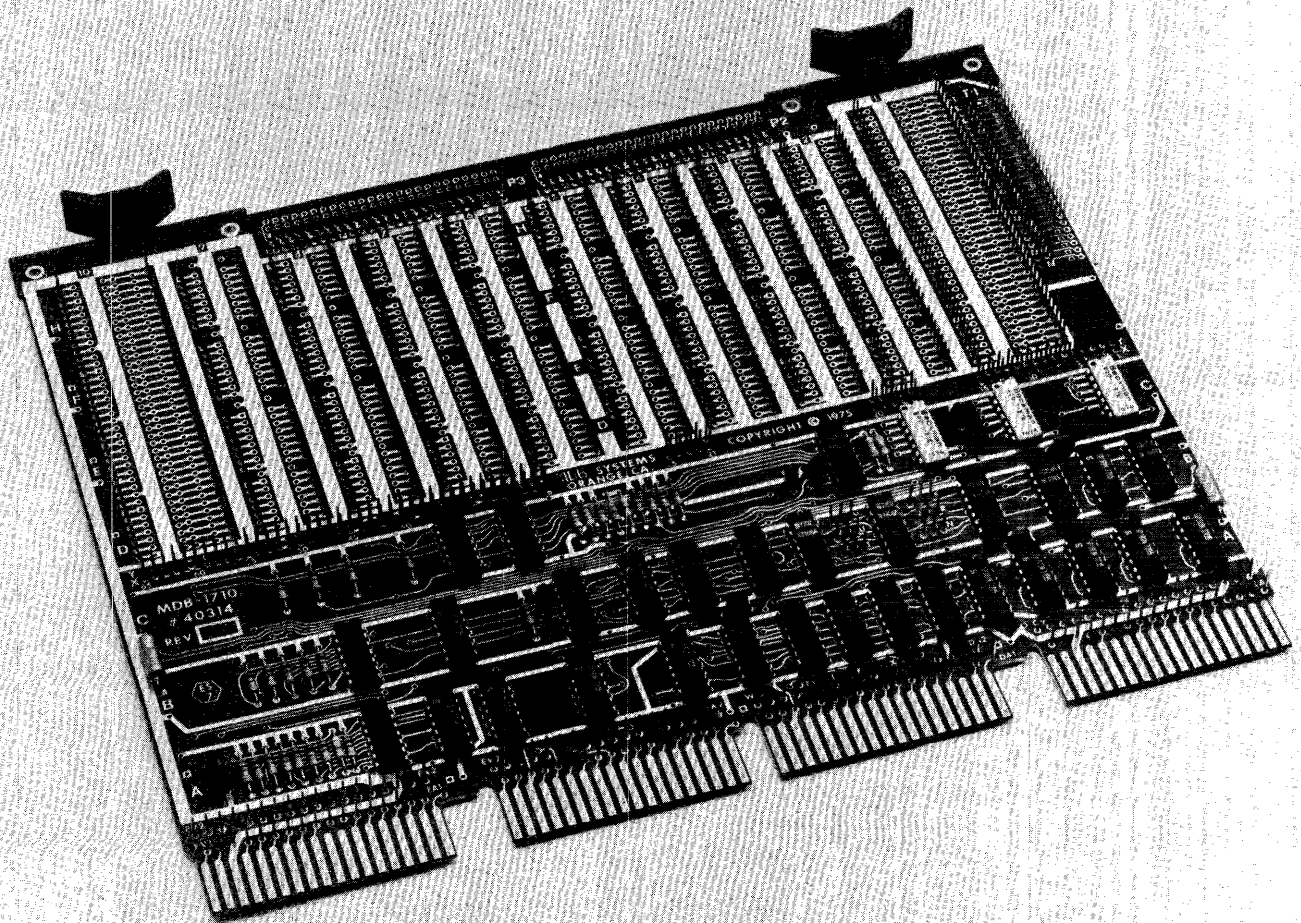
TABLE OF CONTENTS

MDB-1710
GENERAL-PURPOSE INTERFACE MODULE

INTRODUCTION

The MDB-1710 General-Purpose Interface Module acts as an interface to transfer information between a Digital Equipment Corp. PDP-11 Unibus™ and the user's peripheral device.

The MDB-1710 consists of a single quad module containing the following:

- fixed logic to interface with the PDP-11 and with user's interface logic built on the module. Fixed logic includes receivers and drivers, device address selection and decoder logic, and dual interrupt vector logic (see figure 1).

- circuit board facilities and wire-wrap posts to accommodate up to 40 integrated-circuit devices. These facilities are used to build logic interfacing the fixed logic on the module with the user's peripheral device.

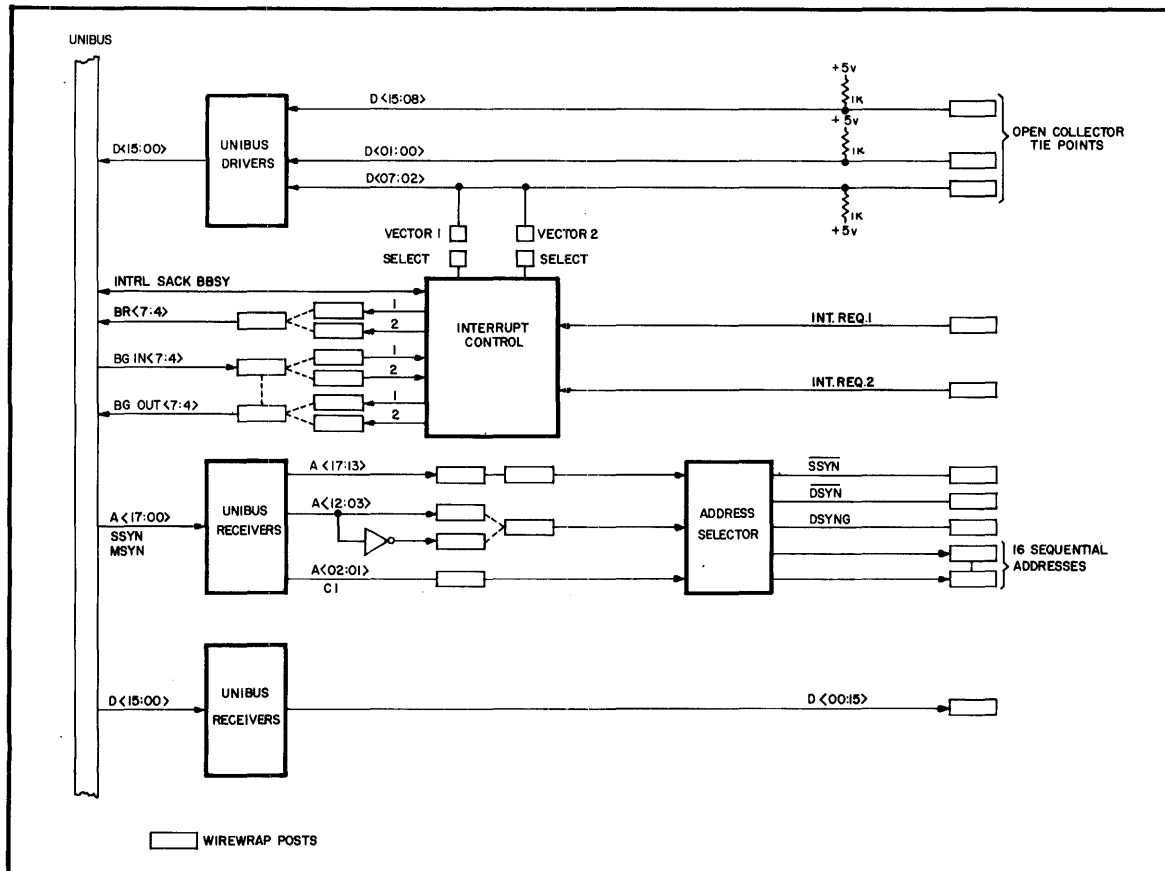The MDB-1710 fits into either the DEC BB-11, DD-11A, or DD-11B Peripheral Mounting Panel.

Figure 1 MDB-1710, Block Diagram

1

PHYSICAL DESCRIPTION

FIXED LOGIC

Logic provided on the module consists of integrated-circuit devices in dual-in-line (DIP) packages; and wire-wrap posts used to select interrupt levels and vector addresses, to program the device address, and to make Unibus driver inputs and receiver outputs, and interface address and control lines, available for connection to user interface logic.

Fixed logic is connected to the Unibus through etched fingers that engage the printed-circuit board connector. The module may include three (optional) ribbon cable connectors for interconnection between the MDB-1710 and the user's peripheral device or other MDB modules.

USER INTERFACE LOGIC

The module accommodates up to 40 integrated circuit devices in wire-wrap terminations. Sixteen positions (in locations 2H through 8H, and 2D through 8D) are dedicated for 14-pin DIP devices and have prewired power and ground connections (pins 14 and 7, respectively).

The remaining positions will also accommodate 14-pin devices, or 16-pin devices if jumpers connecting pins 7 and 8 are removed.

Columns 1 and 10 will accept devices with 22, 24, or 40 pins, as well as 14- or 16-pin devices. Use of three 24-pin devices, or two 40-pin devices, will reduce the number of possible 16-pin positions by four.

Columns 1 and 10 will also accept discrete components when space is not used for I-C devices. Wire-wrap posts are provided to accommodate discrete components in plated-through holes at 0.3-, 0.4-, and 0.6-inch centers.

All Unibus driver inputs and receiver outputs appear at wire-wrap posts for use in multiple-controller interfaces. Unibus driver inputs have pull-up resistors that permit using open-collector gates (7403 or equivalent) to OR-tie additional inputs to the drivers. Receiver outputs will handle up to 30 unit loads.

UNIBUS INTERFACE

Table 1 lists signals at the Unibus/MDB-1710 interface, and other signals that pass between the master device and the module.

Table 1   Master Device/MDB-1710 Interface Signals

Signal	Description
D00L-D15L	Unibus bidirectional data lines. Low (ground) is true, +3V is false.
INITL	Low-level true or negative-going transition received from master device. Use to produce internal master reset.

Table 1   Master Device/MDB-1710 Interface Signals (cont'd)

Signal	Description
A00L-A17L	Address lines from master device. Low level is true. Bits A01L, A02L, and A03L, and control line C1L encode one of sixteen addresses. Bits A04L through A17L are used to enable the decoder. Bit A001 is available for use by user interface logic, and may be strapped to carry byte-transfer signal generated by user interface logic.
C1L	Control line, low-level true, from master device. Controls address decoder and is available to control I/O status at user interface logic.
C0L	Control line, low-level true, from master device. Available to control I/O status at user interface logic, and may be used to transfer data from Unibus receivers into user interface logic.
MSYNL	Timing pulse from master device. Negative transition initiates internal timing sequence enabled by address decoding.
SSYNL	Negative-going pulse (approx 200 nsec) sent by MDB-1710 to master device. Follows (by approx 100 nsec) the negative-going transition of MYSNL when device address has been decoded.
BR4L-BR7L	One of four possible bus request levels sent by MDB-1710 to master device in response to request from user interface logic. Level is selected by means of wire-wrap jumper. Negative level is true.
BG4INH-BG7INH	One of four possible bus grant input levels sent by master device to MDB-1710 in response to bus request. Level is selected by means of wire-wrap jumper. High level is true.
BG4OUTH-BG7OUTH	One of four possible bus grant output levels selected by wire-wrap jumper and sent to another controller to extend a serial interrupt priority link. High level is true.
SACKL	Control level (low-level true) sent to master device by either interrupt circuit to acknowledge receipt of bus grant input. Reset when vector address has been transferred onto Unibus.
INTRL	Control level (low-level true) sent to master device by either interrupt circuit as vector address is transferred onto Unibus.
BBSYL	Busy signal (low-level true) sent to master device by either interrupt circuit. Level falls on receipt of bus grant input and rises as vector address is transferred onto Unibus.

USER LOGIC INTERFACE

Table 2 lists signals at the interface between fixed logic on the module and user interface logic. Connections are made at wire-wrap terminals on the module.

Table 2   Fixed Logic/User Logic Interface Signals

Signal	Description
Signals to User Logic	
DATA00-DATA15	Unibus data receiver outputs. High level true.
Device Address	Sixteen decoded discrete address lines. Eight may be used for input, and eight for output. Input address bits A00L, A01L, and A02L also available.
$\overline{\text{MSYNL}}$	Control signal from master device (inverted) used to initiate address timing.
DSYNG	Positive-going pulse (approx 300 nsec in duration) following MSYNL by approx 50 nsec, if device address is recognized. Useful for gating input data onto Unibus.
$\overline{\text{SSYN}}$	Negative-going pulse (approx 200 nsec) following MSYNL by approx 100 nsec, if device address is recognized.
$\overline{\text{DSYN}}$	Negative-going pulse (approx 200 nsec in duration) following rise of SSYN. Useful for loading registers in a DATO operation.
C1L	Control line from Unibus used to control I/O mode. Low-level true.
C0L	Control line from Unibus used to control I/O mode. Low-level true.
$\overline{\text{MR}}$	Negative-going pulse (inverted INITL pulse from Unibus) used as master reset.
INTADR1, INTADR2	Control level high when related vector address is transferred onto Unibus data lines.
DSEL1, DSEL2	Device-select control level rising when related interrupt circuit receives bus grant input, and falling when vector address is transferred onto Unibus lines.
Other Interrupt Signals	Status of "select" and "busy" flip-flops in both interrupt circuits.

4

Table 2   Fixed Logic/User Logic Interface Signals (cont'd)

Signal	Description
Signals from User Logic	
IDATA00-IDATA15	Unibus data driver inputs. Low-level true.
DEVINT1, DEVINT2	Bus request from user interface logic. High level true. User logic must drop DEVINT when DSEL becomes true.
BYTE XFER	Positive-going control pulse may be strapped to A00L input line and used for byte control.
DATA TO BUS	Positive-going control pulse generated by user interface when MDB-1710 is acting as the master device. May be strapped to C1L line to control data transfer.
DATA FROM BUS	Positive-going control pulse generated by user interface when MDB-1710 is acting as the master device. May be strapped to C0L line to control data transfer.
MSYNC	Positive-going control pulse generated by user interface when MDB-1710 is acting as the master device. May be strapped to MSYNL line to control initiation of address timing.

THEORY OF OPERATION

The logic diagram (Dwg. 40314) shows details of fixed logic furnished on the MDB-1710 module, and identifies wire-wrap posts at which data, address, and control signals are terminated.

In general, logic on the module includes:

- data bus receivers and drivers,

- address selection logic,

- interrupt logic, and

- user interface logic designed and built on the module for the particular device application.

The following paragraphs describe the theory of operation of this logic.

5

DATA BUS

The 16-bit data word DnL at the Unibus data interface is received and made available (as DATAn) at wire-wrap posts for connection to user interface logic (see figure 2).

The 16-bit data word $\overline{\text{IDATAn}}$ from the user interface, connected at wire-wrap posts, is applied through drivers to the Unibus lines. In an interrupt sequence, either of two vector addresses (strapped at wire-wrap posts) is enabled onto lines $\overline{\text{IDATA02}}$ through $\overline{\text{IDATA07}}$ by a respective INTADR1 or INTADR2 pulse.

ADDRESS SELECTION LOGIC

The address for the MDB-1710 is selected by jumper connections at wire-wrap posts. Any address from 760000 through 777777 may be selected. The logic provides eight DATI addresses, and eight DATO addresses.

Sixteen sequential addresses are decoded, with the decoders enabled by address lines A04L through A17L which control an open-collector wired-AND circuit (see figure 3).

Bus address lines A13L through A17L are hard-wired and all must be true at the input terminals to enable the wired-AND bus. Bus address lines A04L through A12L each provide two complementary outputs, either of which may be strapped to the wired-AND bus. If the user-selected address bit is to be true, the bus receiver output is strapped to the wired-AND bus. If that bit is to be false, the inverter output is strapped to the bus.

Bus address line A03L is hardwired to select either of the two decoder chips (in location 5C when A03L = "1", and location 6C when A03L = "0"). Address bits A01L and A02L, and control line C1L, are the least-significant bits of the address and are hard-wired to the decoders. Bit A00L is not used at the decoders.
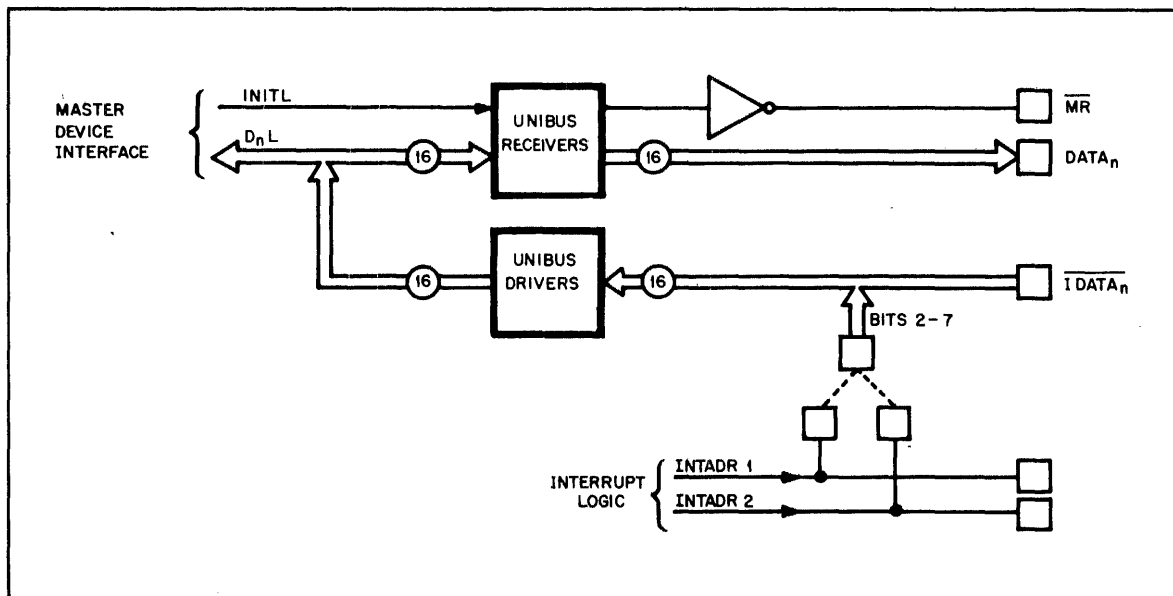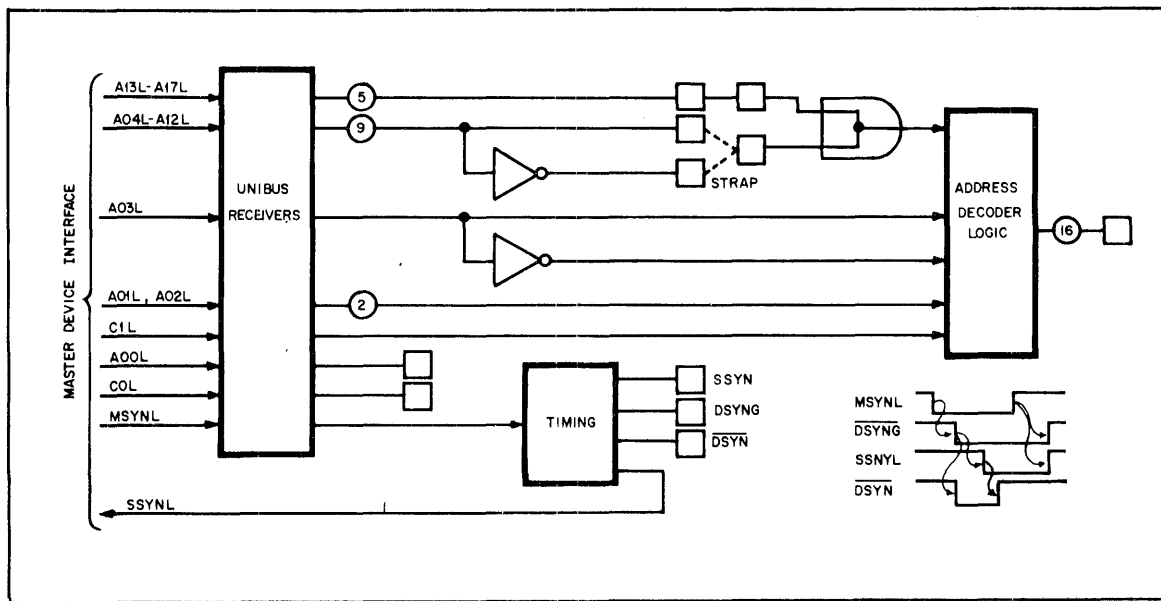

Figure 2 Data Bus, Block Diagram

A03	A02	A01	C1	Y35 X30	X36 Y30	Y36 X31	X37 Y31	Y37 Y32	Y39 Y33	X40 X34	X41 Y34
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

□ Decoder 6C   ▦ Decoder 5C

Figure 3   Address Selection Logic, Block Diagram and Truth Table

Address selection logic also provides sync and loading signals. When the user address is decoded and the master device asserts MSYNL, the logic produces a series of timing signals DSYNG, SSYN, and DSYN. Term DSYN is a negative-going pulse approximately 200 nano-seconds in duration, and is useful for loading data registers when the master device is performing a DATO operation. The signal SSYN is sent to the user interface and terminates DSYN. Simultaneous with SSYN, SSYNL is sent to the Unibus interface to indicate that the address has been acknowledged.

INTERRUPT LOGIC

The MDB-1710 includes two separate sets of interrupt control logic, permitting the user to interrupt the PDP-11 processor through two unique vector addresses. Wire-wrap facilities on the module are used to select any two vector addresses from 4 through 374. A logic "1" in the address is made by connecting a wire-wrap jumper. Logic "0's" need not be jumpered. Either address is put onto the output data lines by a respective signal INTADR1 or INTADR2.

7

As shown in figure 4, bus request levels (BRnL) 4 through 7 are selected by wire-wrap jumpers.

An interrupt request is initiated when user interface logic puts a "1" (+3V) on a DEVINTn line, dropping the level on a selected bus request line at the master device interface.

When the master device sends the bus grant signal (BGnINH), interrupt logic sends DSELn to the user interface which may then remove the DEVINTn signal. The interrupt acknowledge signal SACKL is sent to the master device when the bus grant signal is received.

The vector address is then sent to the master device when the bus becomes available; that is, BBSYL becomes false, raising INTADR1 or INTADR2.

Other control signals BBSYL and INTRL sent to the master device reflect the state of either INTADRn line.
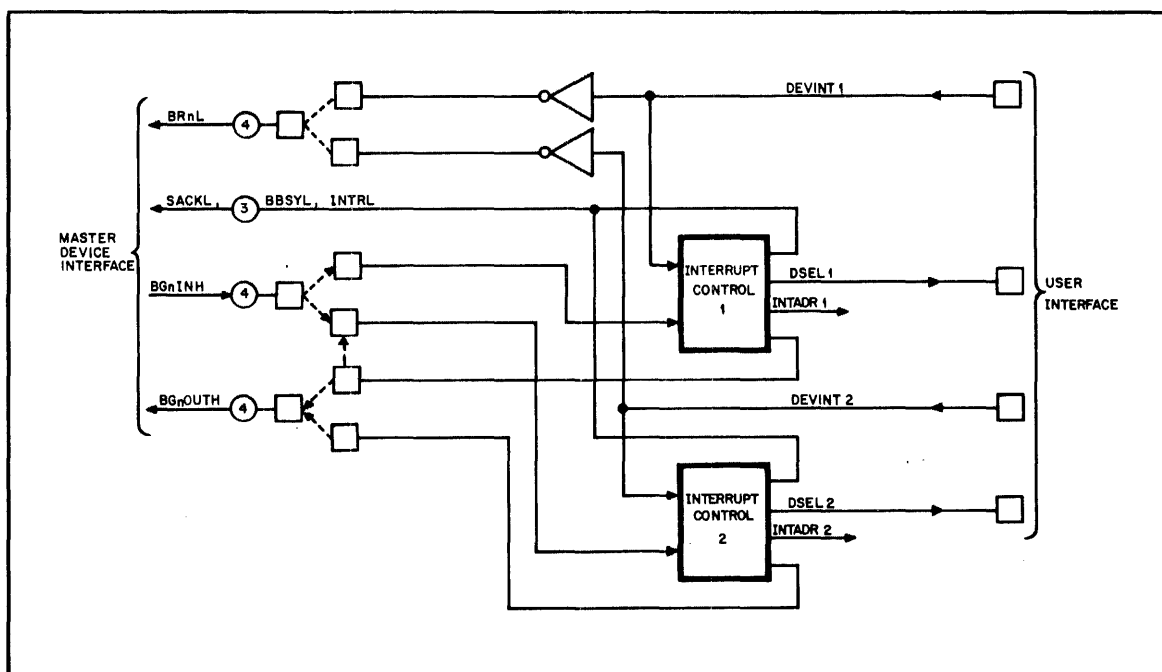

Figure 4   Interrupt Logic, Block Diagram

USER INTERFACE LOGIC

User interface logic is designed for a specific application, and is built in the 40 integrated-circuit device locations provided on the module.

All Unibus driver inputs and receiver outputs are available at wire-wrap posts and may be used for multiple controller interfaces. Inputs to Unibus drivers have pull-up resistors to accommodate open-collector gates (7403 or equivalent) which may be used to OR additional inputs to the drivers. Unibus receivers will handle up to 30 unit loads.

JUMPER CONNECTIONS

Certain jumper connections must be prepared on the module (other than the fixed logic/user logic connections) in order to configure the module for its application. Wire-wrap jumpers are to be prepared for both device address selection, and interrupt management and addresses.

ADDRESS LOGIC

Unibus address bits A04L through A12L must be connected to encode the device address. As shown on the logic diagram, for each bit an output may be taken from either the receiver output, or the output of an open-collector driver.

If a bit is to be true in the user-selected address, strap the receiver output to the wired-AND circuit. If the bit is to be false, strap the driver output to the wired-AND circuit.

Bits A13L through A17L are hardwired and must be true (low) at the Unibus lines to enable the address decoder.

INTERRUPT LOGIC

Interrupt logic must be connected for each of the two vector interrupt circuits. Perform connections as follows:

Vector Addresses. The 6-bit vector address for each circuit is formed by jumpers at three rows of three wire-wrap posts on both sides of the I-C device in location B5.

To encode the vector address for either interrupt circuit, connect a jumper between the output of a INTADR1 or INTADR2 inverter and the related IDATAn line (see logic diagram 40314). If both interrupts are to be used, wire addresses for both to IDATAn lines.

A jumper creates a logic "1". A logic "0" is implied by lack of a jumper.

Interrupt Management. Select the interrupt level for each interrupt circuit by connecting a jumper from terminal J or X to one of the four bus request (BRnL) terminals.

Unless both interrupts are to be at the same level, strap the selected bus grant input terminals to each interrupt circuit at terminal K or W.

If the interrupts are to be at the same level, strap the first-in-order interrupt circuit to a bus grant input, and then strap the bus grant input of the second circuit to the bus grant output of the first. For example:

    a. jumper terminal K to BG4INH, then

    b. jumper terminal W to terminal M.

If the interrupt is to be extended through another controller, connect the bus grant output from the appropriate interrupt circuit (terminal M or L) to the related bus grant output level (BGnOUTH).

USER LOGIC EXPANSION MODULE

The MDB-11WW wire-wrap expansion module is available to expand user interface logic beyond the space allowed on the interface module. The MDB-11WW is designed for custom interface applications with Digital Equipment Corporation PDP-11 and PDP-8 computers, and occupies a single quad slot. Two-level wire-wrap posts, installed on the component side of the board, permit ½-inch board spacing within the computer mainframe.

The module accommodates combinations of as many as 70 dual-in-line ICs or sockets having 14, 16, 18, 22, 24, or 40 pins. IC positions are identified with a column and row identification. Two of the 10 columns (4 and 8) will handle ICs with from 14 to 40 pins, with up to three 40-pin ICs, or five 24-pin ICs, per column. Discrete components may be installed in these columns with components on 0.3-, 0.4- or 0.6-inch centers wherever no IC is installed.

Sixteen of the 70 IC positions are dedicated for 14-pin sockets (positions A1 through A10, and H3 through H8), and have prewired power and ground connections (pins 14 and 7, respectively). All the remaining positions will accommodate 16-pin devices, but the connection between pins 7 and 8 must be removed for any position to hold a 16-pin device.

Each position has power and ground decoupling pads to accommodate high-frequency disc capacitors. Decoupling pads next to column 10 will hold six low-frequency tantalum capacitors on 0.4-inch centers.

Up to four ribbon cable connectors (optional) may be furnished on the module. Two connectors (opposite the card connector fingers) may be used for I/O cables to external devices, or for interconnection of other MDB modules. The remaining connectors may be used for cabling to peripheral devices. Connectors may be ordered with 20, 26, 34, 40, or 50 pins.
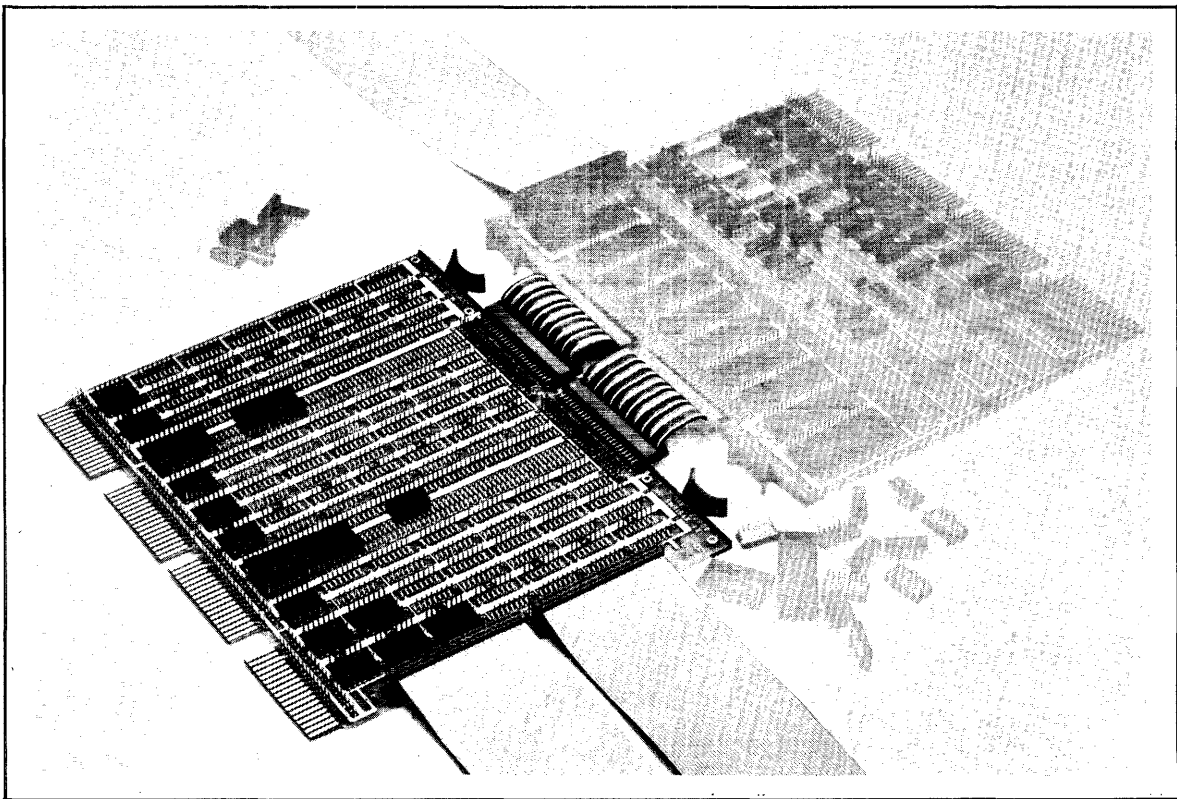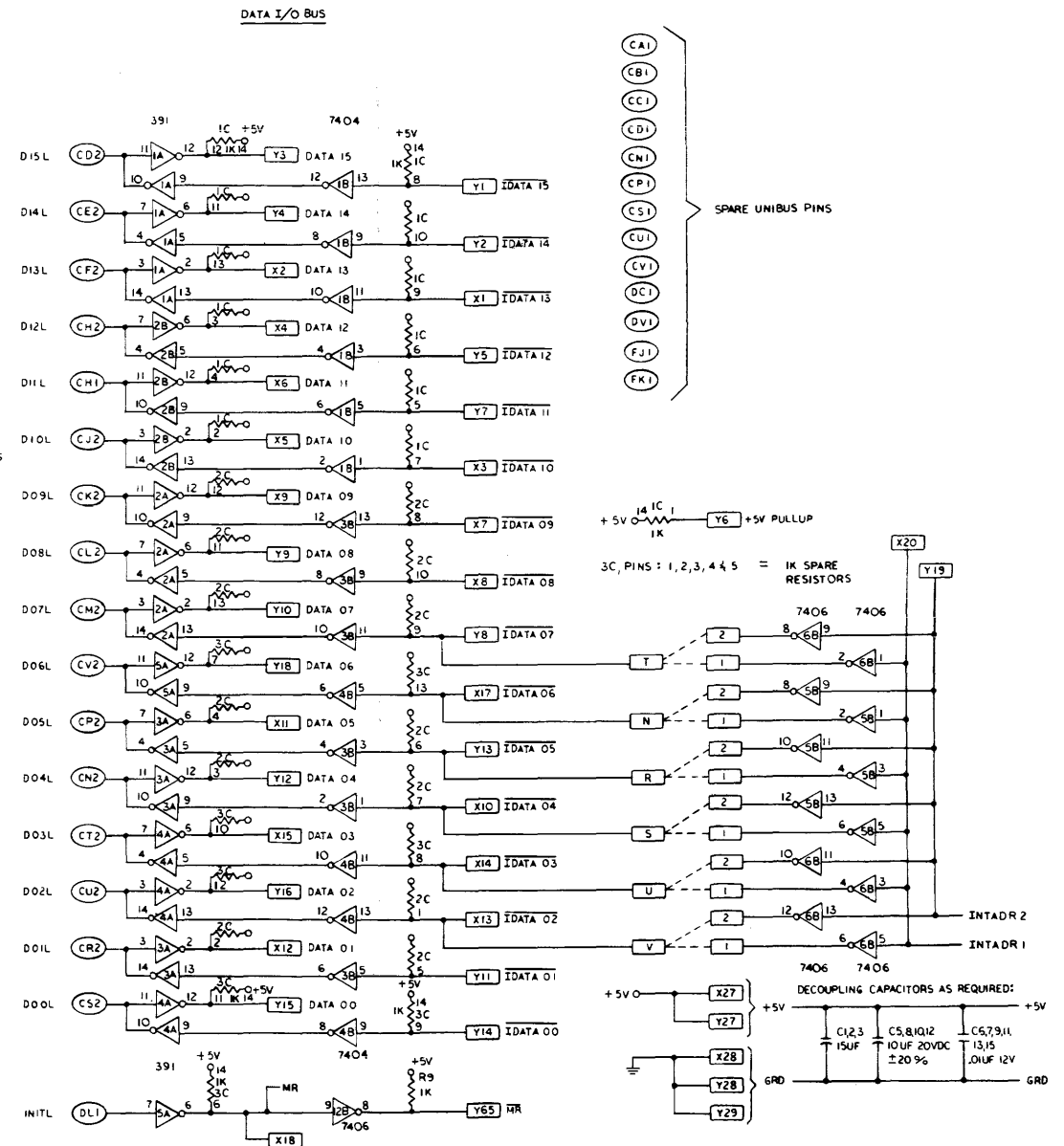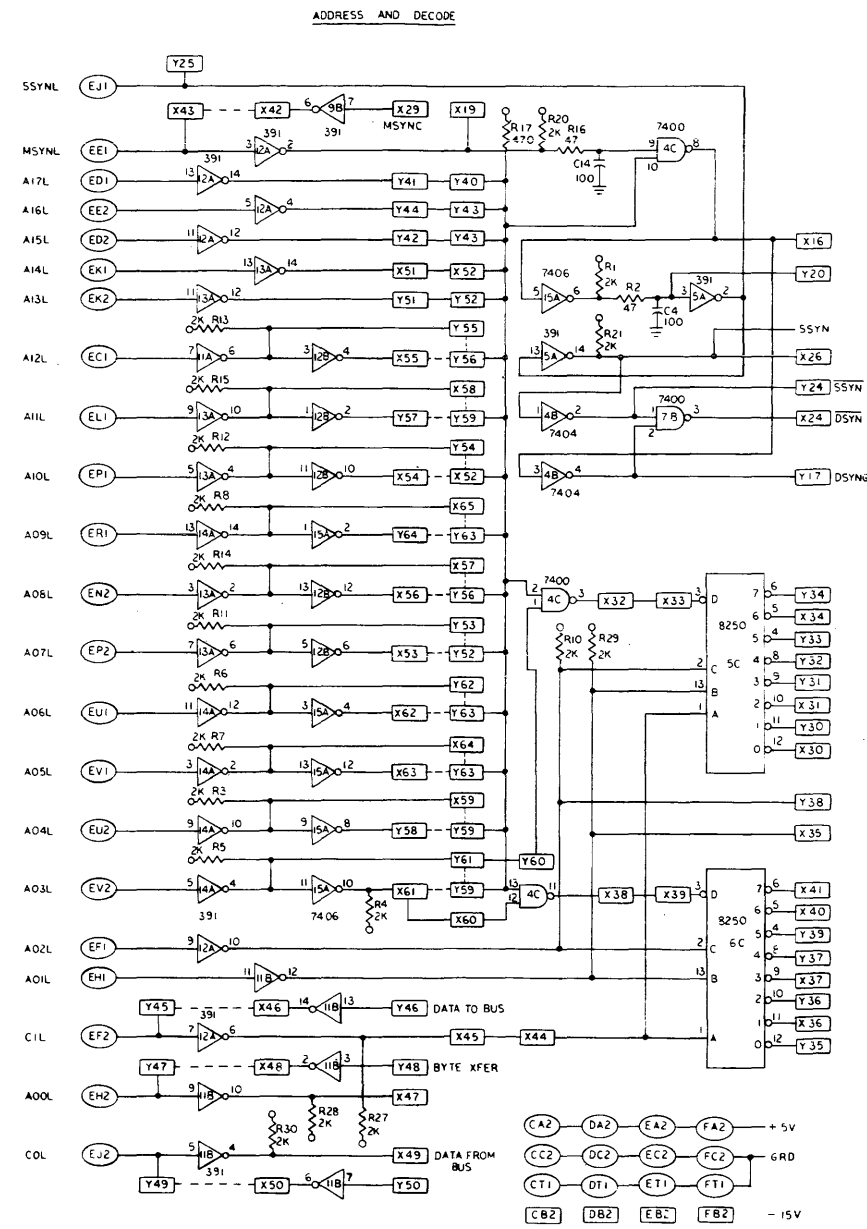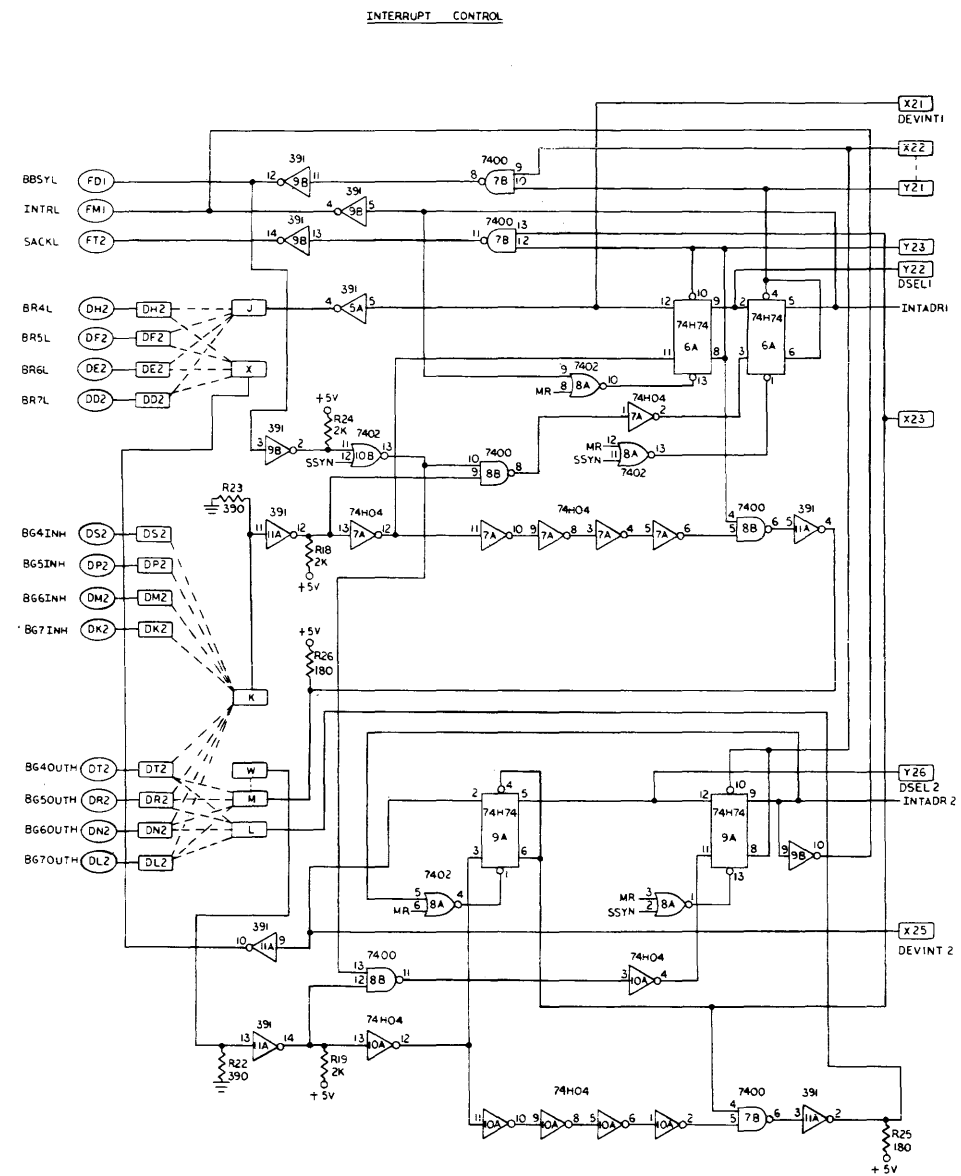
LOGIC DIAGRAM, MDB-1710

11
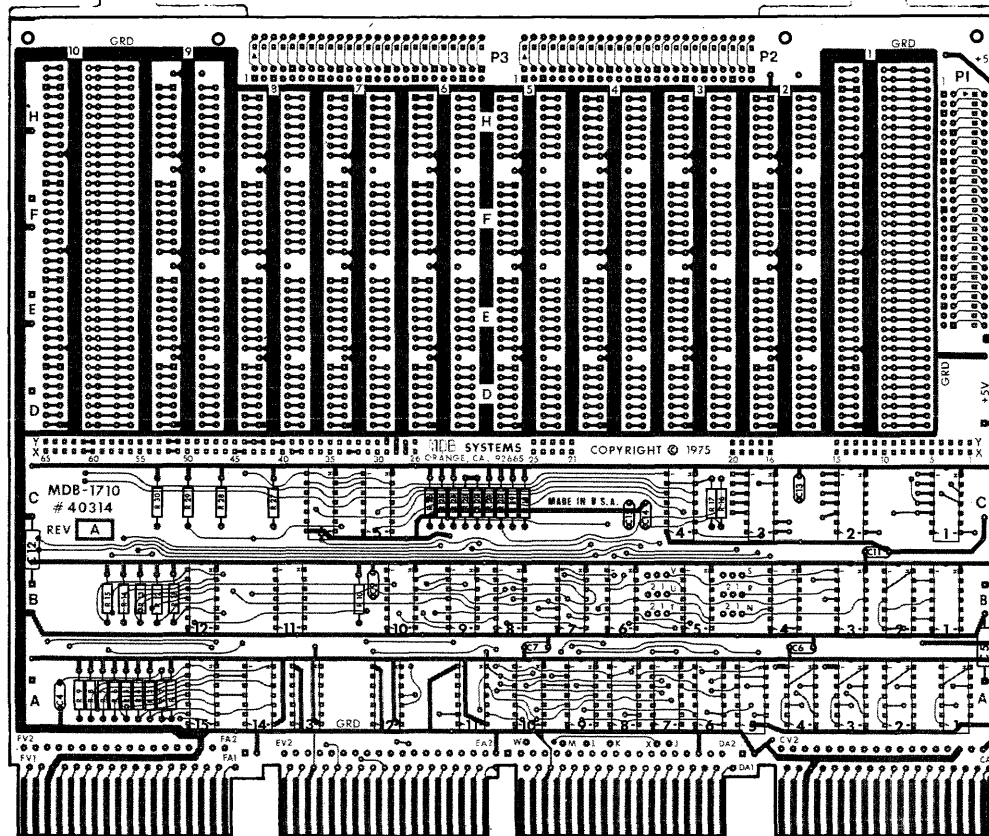
COMP. SIDE

NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER QUALIFIED MANUFACTURING STANDARDS

2. SQUARE PADS INDICATE POSITIVE SIDE OF CAPACITORS AND/OR CATHODE SIDE OF DIODES

3. FOR LIST OF MATERIAL SEE SEPARATE SHEETS

4. DECOUPLING CAPACITORS AS REQUIRED

ASSEMBLY DWG.

MDB SYSTEMS, INC.		
TITLE: MDB - 1710		
DATE: DEC. 74	SCALE: 1:1	
SHEET NO 1 of 1	D NO. 40314	REV A

MDB

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