VIP-640A/VIP-1024A
VIDEO DIGITIZER BOARDS

for the VMEbus

TECHNICAL MANUAL

268-MH-01

Rev. 0

February 10, 1987

matrox
electronic systems

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This Manual Is Valid For The Following Products		
Name	**Hardware I.D.**	**Firmware I.D.**
VIP-640A	**REV. 1**	—
VIP-1024A	**REV. 1**	—

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Chapter 1

INTRODUCTION

The VIP-640A and VIP-1024A are real-time video frame-grabbers for the VMEbus and are configured as VME slave modules. The VIP can grab picture frames from a video input on a single or continuous basis and send them to a CRT while performing instructions on frame storage, video keying, color enhancement, and pixel clarification from a host. This manual provides all of the information required to install and operate the two versions of the VIP.

An overview of the boards' specifications and features is provided in Chapter 2 and a more detailed description of the VIP's capabilities may be found in the functional description in Chapter 3. Chapter 4 is dedicated to programming, and provides information that the programmer must have in order to write access routines. Chapter 5 outlines the VIP's strap options and Chapter 6 gives the pin assignments for all of the board's connectors. Chapter 7 provides information on maintenance and warranty. Appendix A gives a brief installation procedure. Appendix B contains the CRTC data sheets. A "nominal gain and offset" algorithm is listed in Appendix C. Appendix D contains an initialization program written in Whitesmith C. A layout of the main board can be found in Appendix E. A list of reference sources is given in Appendix F.

This manual contains all the information required to install and operate both versions of your VIP. However, if you do have problems, feel free to telephone our Applications Engineering Department. They will be happy to answer any questions you may have.

Chapter 2

SPECIFICATIONS

- **Display Specifications :**

MODEL	DESCRIPTION
VIP-640A	NORMAL MODE 1024 × 1024 × 8-bit Frame Buffer 640 × 512 (European)/480 (U.S.) display and grab resolution 2 display image areas stored ZOOM MODE 1024 × 1024 × 8-bit Frame Buffer 320 × 256 (European)/240 (U.S.) display resolution 12 display image areas stored
VIP-1024A	NORMAL MODE 1024 × 1024 × 8-bit Frame Buffer 512 × 512 (European)/480 (U.S.) display and grab resolution 4 display image areas stored ZOOM MODE 1024 × 1024 × 8-bit Frame Buffer 256 × 256 (European)/240 (U.S.) display and grab resolution 16 display image areas stored

Table 2.1: FRAME BUFFER AND DISPLAY SPECIFICATIONS

- Bus :
  - Double-height VMEbus
  - All signals in accordance with VMEbus specification
  - A32 or A24, D16 slave
  - supervisor or non-privileged access
- Special Functions :
  - Operates in continuous grab or snapshot mode
  - Software provides switching between four video sources (three external and one internal feedback)
  - Software vertical and horizontal pans with 16 line and 8 pixel resolution respectively
  - Software enabled video keying on any pattern written into the least significant bit of the frame buffer
  - Write mask to allow the user to mask off any or all of the bit planes in the frame buffer
  - Software controlled offset and gain of input signal for optimization of dynamic range of A/D converter
  - Input and output video lookup tables
  - Software selectable lookup table maps
  - Video bus through P2 connector for expansion and to gen-lock multiple boards together for true RGB input
- Video Sync :
  - Software switch between video sync rates for American EIA RS-170 (VIP-1024A only) or RS-330 (60Hz, 525 lines) and European CCIR (50Hz, 625 lines) TV standards
  - Software selectable internal sync generator (block or serrated for the VIP-1024A; block sync only for the VIP-640A) or PLL on external sync source
  - Input for external synchronization (NB: it is not possible to synchronize the VIP to an external block sync source.)
  - Provide vertical and horizontal or composite sync and pixel clock on J5 connector

SPECIFICATIONS

- Video Timing :
  - Active Video : 51.2μs
  - Horizontal Sync Frequency : 15.75kHz
  - Horizontal Sync Width : 4.8μs
  - Vertical Sync Frequency : 60Hz (American) 50Hz (European)
  - Vertical Sync Width : 190.5μs
  - All these parameters (except vertical sync width) can be changed if block sync is selected.
- Memory Access :
  - Word (2 pixels) or byte (1 pixel) access to video RAM
  - Direct access to the video RAM through a 1 Megabyte window on VMEbus
  - Address of video RAM window can be strap-selected
  - Fully transparent memory in both display and grab modes
  - Simultaneous display of memory while digitizing
- Register Access :
  - Direct access to the registers through a 64 Kbyte window in standard or extended address space
  - Word or byte access to all devices except the LUTs which are accessible through byte access
- Connectors :
  - Three BNC connectors for RGB input
  - One female DB9 connector for RGB output with separate sync and composite sync available on all channels
  - One male DB9 connector with sync and pixel clock for camera
  - 36 signals defined on P2 for expansion or gen-lock
- Power Requirements :
  - VIP-640A - 16.14W $\pm$10%
    - +5VDC 2.85A $\pm$10%
    - +12VDC 85mA $\pm$10%
    - -12VDC 40mA $\pm$10%
  - VIP-1024A - 16.14W $\pm$10%
    - +5VDC 2.85A $\pm$10%
    - +12VDC 85mA $\pm$10%
    - -12VDC 40mA $\pm$10%

- Dimensions :
  - Standard VMEbus double-height board
    - 160mm (6.299in) deep
    - 233.35mm (9.187in) high
    - 20.32mm (0.8 in) thick
    - 373.4sq cm (57.9sq in) in area
- Environment :
  - 5°C to 46°C operating temperature
  - 8% to 80% relative humidity; non-condensing
- Storage :
  - -40°C to 60°C
  - 5% to 100% relative humidity; non-condensing

Chapter 3

FUNCTIONAL DESCRIPTION

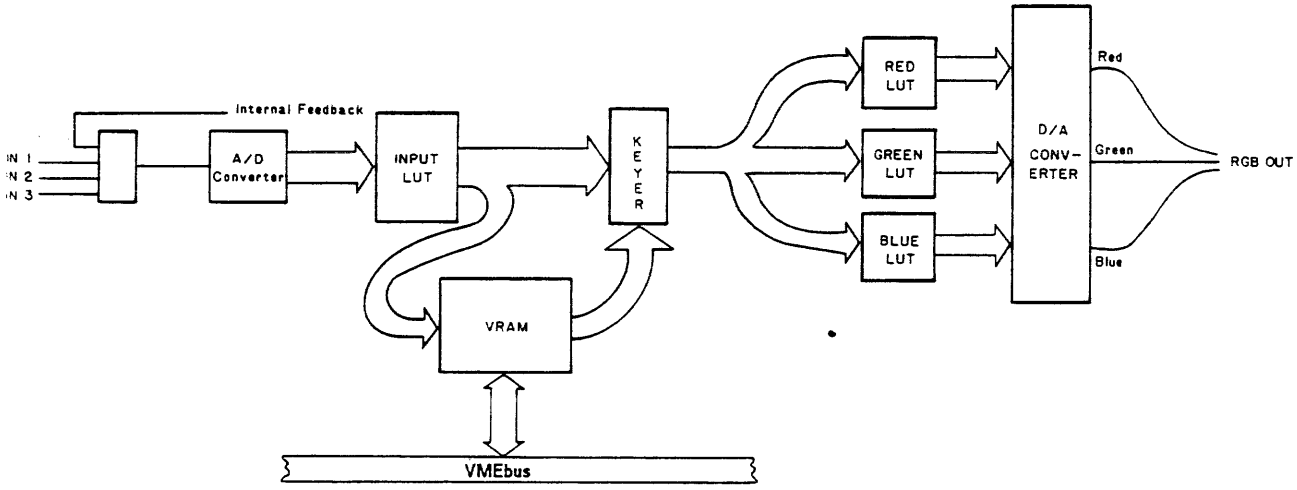
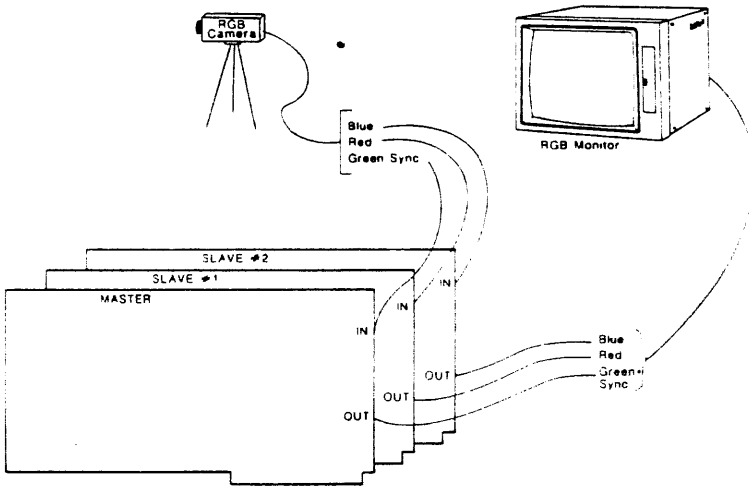


Figure 3.1: BLOCK DIAGRAM OF VIP

The VIP is a plug-in video frame grabber–digitizer board for the VMEbus. It has a resolution of 512 × 512/480 or 640 × 512/480 pixels (depending on model) in normal (non-zoom) mode with eight bits per pixel and a power consumption of approximately 17W. The VIP is capable of operating in a continuous or single frame grab mode and has built-in video keying capabilities as well. Frames which have been stored in the on-board frame buffer can be loaded into the system memory or onto disk. Conversely, video data, as well as lookup table data, can be written to the VIP by the system CPU. The VIP has one input and three output lookup tables, each of which has eight maps to choose from. There are three input ports and an RGB output as well as an internal feedback channel. The operation of the VIP is illustrated in Figure 3.1.

3.1 Master/Slave Operation

Up to four VIP boards can be combined, one master and three slaves, to simultaneously process information. To implement a Master/Slave setup, one VIP is strapped as master and one, two, or three others are configured as slaves (see section on strapping). This type of setup can be used to separately process the signals of an RGB input and produce a real color (as opposed to a pseudo-color) RGB output. An example of an RGB setup is shown in Figure 3.2. Synchronization signals are transmitted via the sync bus which must interconnect pins 1 through 5 of Rows A and C on connector P2. A fourth board may be used for another spectral input or for other purposes.



(Boards not drawn to scale.)

Figure 3.2: THREE BOARDS COMBINED FOR RGB OPERATION

3.2 Board Control

The user controls the board by accessing a number of registers and direct access lookup tables (LUTs). This section gives a brief overview of these resources. More detailed descriptions are provided in the following sections.

- Input Lookup Table: 2K bytes, 8-bit wide, write-only, divided into eight 256 byte LUTs selected through Control Register 0
- Red Lookup Table: 2K bytes, 8-bit wide, write-only, divided into eight 256 byte red LUTs selected through Control Register 0
- Green Lookup Table: 2K bytes, 8-bit wide, write-only, divided into eight 256 byte green LUTs selected through Control Register 0
- Blue Lookup Table: 2K bytes, 8-bit wide, write-only, divided into eight 256 byte blue LUTs selected through Control Register 0
- CRTC Data Register: an 8-bit read/write data port to CRTC internal registers.
- CRTC Address Register: A 5-bit register used to set the address of the internal CRTC register to be accessed through the CRTC data register.
- CRTC Status Register: a 1-bit register used to read the status of the CRTC.
- Video Offset Register: an 8-bit write-only register used to set the offset of the input video before it reaches the A/D converter.
- Video Gain Register: an 8-bit write-only register used to set the gain of the input video during conversion.
- Control Register 0: an 8-bit write-only register used for miscellaneous control functions.
- Control Register 1: an 8-bit write-only register used to select the input source and type as well as some output processing options.
- Mask Register: an 8-bit write-only register used to define a mask to select which bit-planes can be overwritten in the frame buffer.
- Status Register: A 4-bit read-only register indicating the vertical blanking interval, master or slave configuration of the board, and video grabber status.
- Snapshot Register: A 0-bit read/write register used to trigger the digitizing of a single frame.

3.3 Input and Conversion

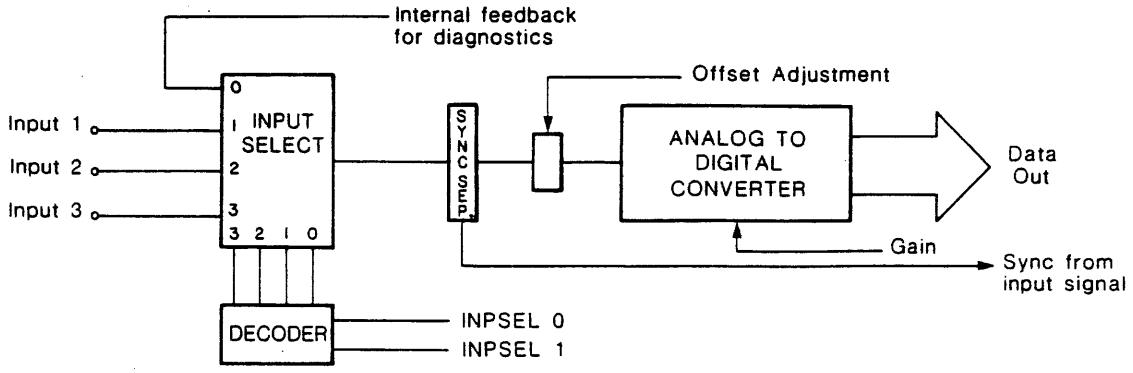


Figure 3.3: INPUT SECTION

The user inputs video to the VIP via any one of 4 software selectable inputs. The VIP may be synchronized to the video source or the video source may be synchronized to the VIP. When the VIP is to be synchronized to the video source, the user supplies composite sync as part of the video signal at the selected input or as a separate signal at input 2 (a strap determines which mode is used). Note that the VIP can only be used with an external sync source that supplies serrated vertical sync pulses. When the video source is to be synchronized to the VIP, the VIP-1024A is strapped to generate either block or serrated sync while the VIP-640A only generates block sync. This internally generated sync is then output to the video source via J5.

In addition to vertical sync, J5 provides a pixel clock and horizontal or composite sync for cameras that may need these extra signals. The polarity of these signals is strap selectable. The sync signal, generated internally or externally, is routed via a sync separator to a phase locked loop that generates all of the video timing signals required by the VIP.

After the video signal drives the sync separator, it is subject to an adjustable DC offset voltage (see Figure 3.4), which, along with adjustable gain, allows the user to center any portion of the video signal in the analog-to-digital converter's operating range. These two controls are similar to the brightness and contrast controls on a television, and allow the user to digitize only that part of the video that is of interest to him.

After the signal has been adjusted, it is processed by an A/D converter. It is then digitized in real time, producing 8-bit codes that are used as indices or addresses to the input lookup table which provides resulting pixel data. This pixel data is then stored in the frame buffer or is output to the CRT.

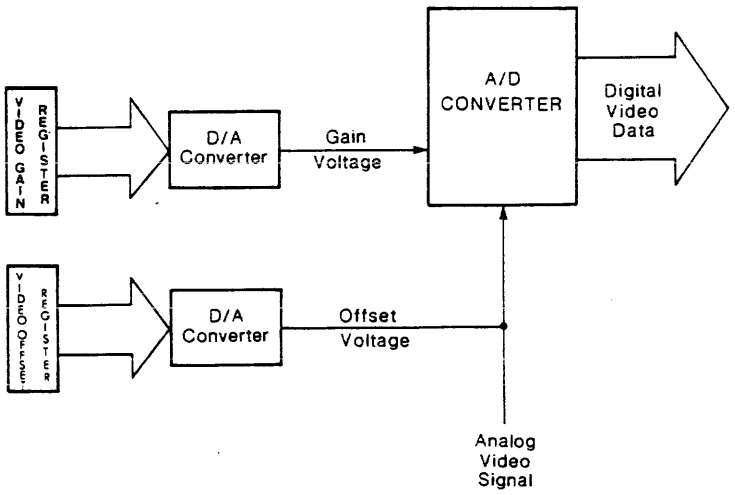


Figure 3.4: INPUT SIGNAL ADJUSTMENT

3.4 Input Lookup Table

An input lookup table is provided to enable the user to manipulate the video data as it is taken from the A/D converter. The input LUT can be loaded from the VMEbus and is subdivided into eight individual 256 byte maps. This allows the user to load eight discrete sets of data into the LUT in order to modify or manipulate the current frame. The input LUT maps the

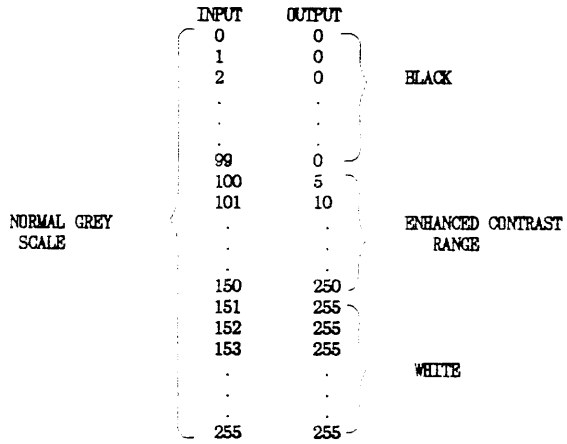


Figure 3.5: INPUT LUT CONFIGURED FOR CONTRAST ENHANCEMENT

incoming data to values set up by the user, and can be used as an image processing device when it is loaded with the appropriate data. Figure 3.5 illustrates a LUT map set up for contrast enhancement. In this example the lighter greys will exit the LUT as white and the darker greys as black. The middle greys (values 100 to 150) have their grey range expanded so that their values will represent the full range of greys from black to white. This technique is used to isolate details in what would otherwise be an almost continuous field of grey.

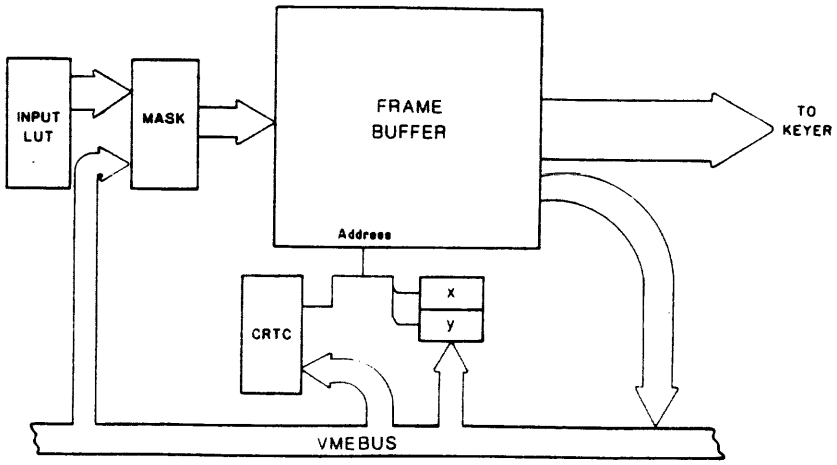


Figure 3.6: FRAME BUFFER

3.5 Frame Buffer

The VIP is shipped with 1MB of memory mapped VRAM (video RAM) for the frame buffer, a memory used to store frame grab data. Both the system bus and the CRT Controller have simultaneous transparent access to the frame buffer. This simultaneous transparent access is achieved by giving the CRT Controller access to the frame buffer when the controlling clock signal is high and giving access to other processes when the clock is low. Starting at a user supplied address in the frame buffer, the CRTC sends pixel data to the output LUT's in a continuous scan. The starting address is the address of the pixel that the user wants located in the upper left corner of the display. As the CRTC always sends the same number of pixels for each output scan line, it is possible, by loading a different starting address into the CRTC, to affect horizontal and vertical scrolling in the output video signal with eight pixel and sixteen line precision. (See also the SY6845E data sheets in Appendix B.) This gives the ability to pan both vertically and horizontally, which is particularly useful because of the VIP-1024A's 1024 $\times$ 1024 storage area and 512 $\times$ 512 display area, and the VIP-640A's 1024 $\times$ 1024 storage area and 640 $\times$ 512 display area.

3.6 The Bit Mask

Data that is written from the bus to the VIP pass through a bit mask. This mask is set up through software and enables the user to selectively write data from the host to any or all of the eight bit-planes of the frame buffer. For example, if bit 0 of the mask register is set to 1 no data will be written into bit-plane 0 of the frame buffer. This applies to data from the bus as well as video input data.

This mask can be used to load different images into each individual bit plane in the frame buffer, allowing the user to form graphics and text overlays on protected planes by using the output LUTs to distinguish the overlay from the rest of the frame buffer. The mask can prevent writing from the digitizing port. The mask is also useful when setting up the frame buffer with the appropriate values in the least significant bit in each pixel which has a special function for video keying (See Sections 3.10 and 4.5).

3.7 Frame Grabbing

When in frame grabbing mode, an A/D converter grabs a frame pixel-by-pixel from the selected input port, digitizes it, and sends it on to the LUT. Each pixel is mapped to a new value corresponding to the entries in the LUT. Finally, the frame buffer stores the pixel information.

There are two image aquisition modes: continuous grab mode, and snapshot mode. Continuous grab mode continually digitizes and updates the frame buffer with video data from the inputs. Frames are continuously digitized and stored in this buffer. Snapshot mode allows one frame to be grabbed beginning at the first VSYNC following the snapshot request. In both modes the display is at no time inhibited. This allows simultaneous display of the frame buffer while grabbing is in progress. Also, a continuous grab may be stopped, in effect freezing the last frame aquired.

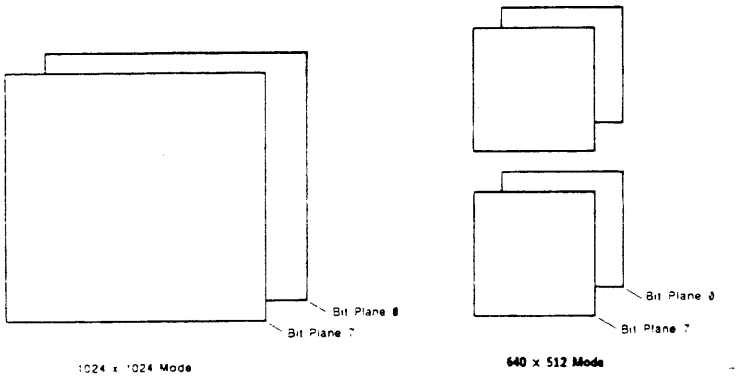


Figure 3.7: VIP-1024 VIDEO MODES

3.8 Video Modes

3.8.1 Normal Mode

The VIP-1024A incorporates a 1024 × 1024 pixel frame buffer with a display area consisting of a 512 × 512/480 window in this buffer. This window may be panned and scrolled throughout the entire frame buffer. In QUADBUF mode the frame buffer is divided into 4 quadrants, with each the size of the display window. This division allows the user to rapidly switch between the images stored in each quadrant. The pan and scroll functions used in the QUADBUF mode wraparound within the viewed quadrant.

The VIP-640A also incorporates a 1024 × 1024 pixel frame buffer, but with a display area consisting of a 640 × 512/480 window in this buffer. This display window can be panned and scrolled throughout the frame buffer allowing two complete images to be stored. QUADBUF mode can be employed on the VIP-640A if the user enables this feature and reduces the horizontal display width to 512 pixels by modifying register R1 of the CRTC. This reduction in width retains the square pixel aspect while it also alows rapid switching between images. Note that QUADBUF is not normally used with the VIP-640A because of the required reduction in display width.

Both versions of the VIP can be panned horizontally and vertically by changing the starting address in the CRTC. The video mode is selected using various bits in the control registers. In 1024 by 1024 mode the frame buffer wraps as a whole, in 512 by 512 mode, or 640 by 512 mode, each of the frame buffers is completely independent of the others.

MODEL	DESCRIPTION
VIP-640A	NORMAL MODE 1024 × 1024 × 8-bit Frame Buffer 640 × 512 (European)/480 (U.S.) display and grab resolution 2 display image areas stored ZOOM MODE 1024 × 1024 × 8-bit Frame Buffer 320 × 256 (European)/240 (U.S.) display resolution 12 display image areas stored
VIP-1024A	NORMAL MODE 1024 × 1024 × 8-bit Frame Buffer 512 × 512 (European)/480 (U.S.) display and grab resolution 4 display image areas stored ZOOM MODE 1024 × 1024 × 8-bit Frame Buffer 256 × 256 (European)/240 (U.S.) display and grab resolution 16 display image areas stored

Table 3.1: FRAME BUFFER AND DISPLAY INFORMATION

3.8.2 Zoom Mode

The VIP zoom function allows the aquisition and display of images in 2x Zoom Mode. This Zoom Mode is enabled by rewriting the CRTC parameters and setting bit 6 of Control Register 0. It can be used to enlarge a portion of a previously grabbed image or to grab images with reduced resolution.

When an image is grabbed in the normal display mode, the user can then utilize the Zoom Mode to display an enlarged view of the grabbed image. He can then scroll and pan to view other parts of the enlarged image.

The Zoom Mode halves the number of pixels grabbed (and displayed) both horizontally and vertically. Images grabbed in Zoom Mode occupy one quarter of the memory space required by normally grabbed images. In Zoom Mode the VIP-1024A can store 16 images while the VIP-640A can store 12 (of which 4 are stored in the unused portion of the Frame Buffer).

Continuous grabbing in different Frame Buffer areas allows up to 16 video frames to be stored dynamically during aquisition. This may be used for negative time event recording or simple animation sequences.

3.9 Video Output

There are two sources of data for output from the VIP: the frame buffer and the video input. The user can select the output to come from either the frame buffer or the input LUT. Alternatively, the output can be dynamically switched between these two sources using Video Keying.

3.10 Video Keying

When video keying is selected, the video input does not go into the frame buffer but passes through to the video output. As each pixel of the input image enters the VIP, the keyer, on a pixel by pixel basis, tests the least significant bit of the corresponding pixel in the frame buffer. When this bit is set to 0, the pixel from the input LUT is sent to the output LUTs, otherwise the frame buffer pixel is sent. This results in the contents of the frame buffer being displayed where the user has set the least significant bit to 1 and the input LUT being displayed elsewhere, giving the ability to overlay video, text or graphics onto the input video signal. Video Keying is described in greater detail in Section 4.5.

3.11 Output Lookup Tables

Input	Red	Green	Blue	Output
100	0	0	255	blue
101	255	0	0	red
102	0	255	0	green
103	100	100	100	grey

Table 3.2: GREY LEVEL - COLOR TRANSFORMATION

The 8-bit output of the keyer is sent to the three output LUTs. Each LUT receives all eight bits, and then, using one of its eight maps, generates a new value. Separate values, for the red, green, and blue output signals, allow the user to have access to 256 shades of grey or 16.7 million colors (maps are loaded with appropriate intensities). The colors that are produced by a single board are pseudo-colors. This means that the colors do not represent what the camera sees but rather represent the level of intensity. The user can assign very different colors to greys which are very close – allowing the user to distinguish details with much greater ease than when the output is in greys only. An example is illustrated in Table 3.2.

The output of each LUT is sent to a digital to analog converter. These D/A converters produce, in real time, the three analog signals for the RGB output. The output of these converters can be strapped for block or serrated sync (VIP-1224A only). This sync can be individually disabled on each video output channel by selecting the appropriate strap.

Chapter 4

PROGRAMMING

This chapter provides information necessary to write access routines. It is loosely divided into two sections. The first section contains descriptions of how to utilize the various functions of the board. The second section contains information on the various registers available to the user.

4.1 The Memory Map

With 32-bit addressing, the maximum addressable memory space is 4 Gbytes. With 24-bit addressing, the maximum addressable memory space is 16M bytes. Extended 32-bit (A32) or standard 24-bit (A24) addressing modes are strap-selectable. In A32 mode, the VIP decoder must find the Video RAM and the register map in the same 16 Mbyte page (strap selected). One page of 1 Mbyte (strap selected) is decoded as direct access Video RAM. One section of 64 Kbytes is decoded as register and LUT locations. It is not necessary, however, to strap all system VIP boards into the same page (see Figure 4.1). Remember that all intervening memory space is usable and anything inadvertently written to a VIP board in the course of loading or running a program will be lost to the program and will randomly affect the board.

4.2 Pixel Access

The frame buffer can be loaded with a frame grab from the video input or the video bus, and it can be both written to and read from the system bus.

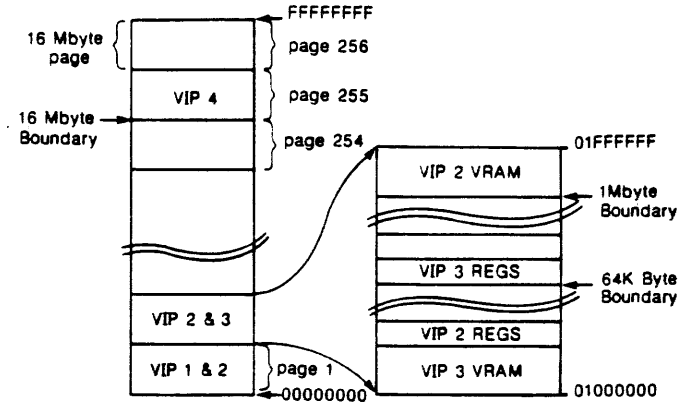


Figure 4.1: SAMPLE MEMORY MAP FOR 4 BOARDS

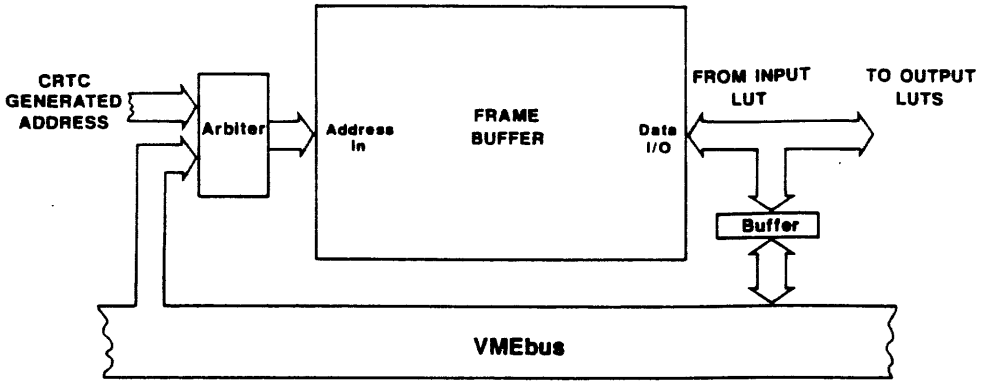


Figure 4.2: PIXEL DATA ACCESS

The in-bus host accesses the frame buffer by using X and Y addressing in the following format:

Buffer Selection	BY	BX
Address Bit	A19	A18

Y Location	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Address Bit	A19	A17	A16	A15	A14	A13	A12	A11	A10	A9

X Location	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
Address Bit	A18	A8	A7	A6	A5	A4	A3	A2	A1	A0

If word access is used, then 2 pixels are written at the same time. The high byte is placed in the even numbered pixel locations (A0 = 0) and the low byte is placed in the odd numbered pixel locations (A0 = 1). The frame buffer may be regarded in two ways. If only one buffer of 1024 × 1024 is defined, then a tenth bit is added to each coordinate by changing the two buffer selection bits BY and BX to coordinates Y9 and X9 respectively. All access to the frame buffer is by direct addressing.

Frame grabbing is accomplished by using either a snapshot grab or a continuous grab. A snapshot grab stores a single video frame and is accomplished by reading from or writing to the Snapshot Register. A continuous grab is initiated by writing a 1 to the CONFGR bit in Control Register 1. The VIP then, starting at the begining of the next frame, grabs one frame after another into the frame buffer until the user writes a 0 to CONFGR, at which point the VIP terminates the current frame and stops grabbing. For both types of frame grab, the FGRACT bit in the Status Register indicates when frame grabbing is active.

The VIP has a mask register to mask access to selected bit-planes in the display buffer. It masks access from both the system bus and the frame grabbing process and allows the user to selectively write to any combination of the 8 bit-planes.

For further information on these commands refer to Section 4.7 Registers and Lookup Tables.

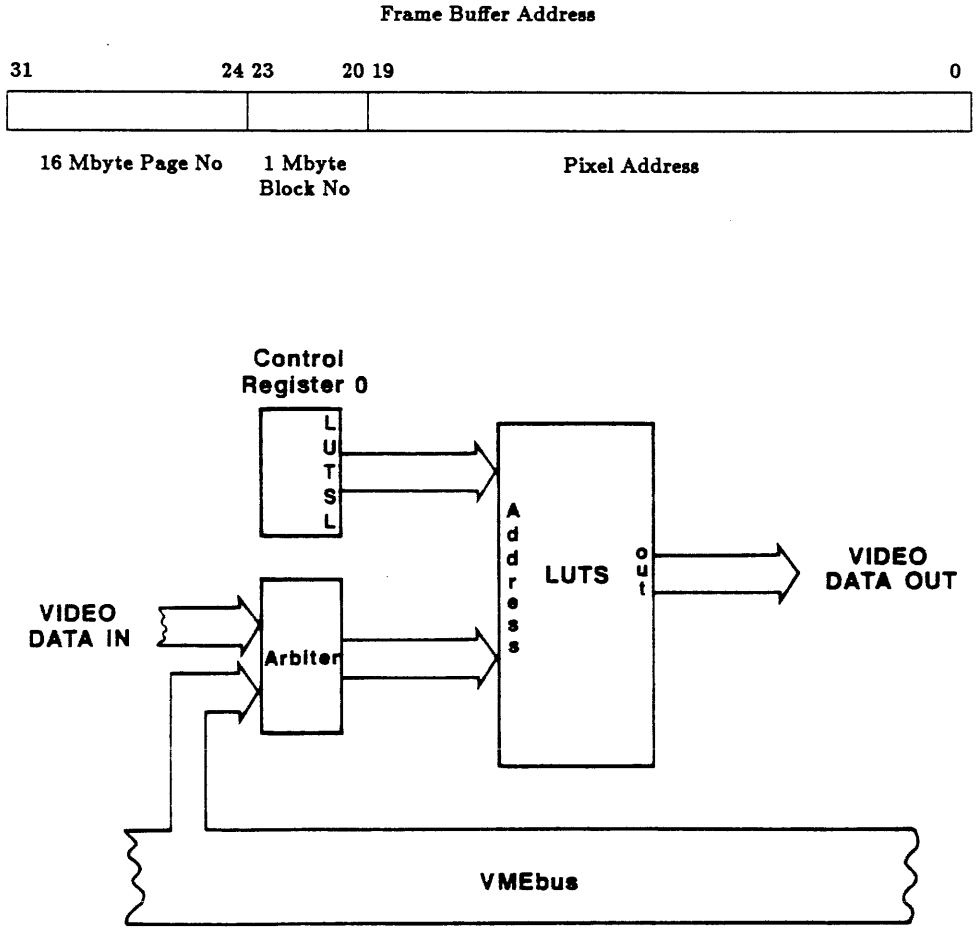


Figure 4.3: LUT DATA ACCESS

4.3 LUT Access

The VIP has four lookup tables: one input and three output. The input LUT allows the user to manipulate data as it is taken from the A/D converter. Each of the three output LUTs can be used to control one of the primary colors (red, green, and blue) in the RGB output signal.

Each LUT is a 2 Kbyte static RAM subdivided into eight individual 256 byte tables. This allows the user to load eight sets of data into each LUT. The user selects the map to be used with the control bits LUTSL0, LUTSL1 and LUTSL2 in Control Register 0.

The currently selected 256 byte tables from all LUTS are mapped onto the VMEbus, from which they can be written to but not read. Modification of the lookup tables is by direct access from the in-bus host CPU to the tables' addresses as outlined in Section 4.7 and Table 4.2. Thus, of the eleven bits used to address any given lookup table, the high order 3 bits are ignored and only the low order 8 bits representing values 00 - FF are used by the decoder. The particular 256 byte block within the LUT's offset is selected by the 3 MSB bits supplied by LUTSL0, LUTSL1, and LUTSL2 of Control Register 0. For more information on this selection process see Section 4.7.1 Control Register 0.

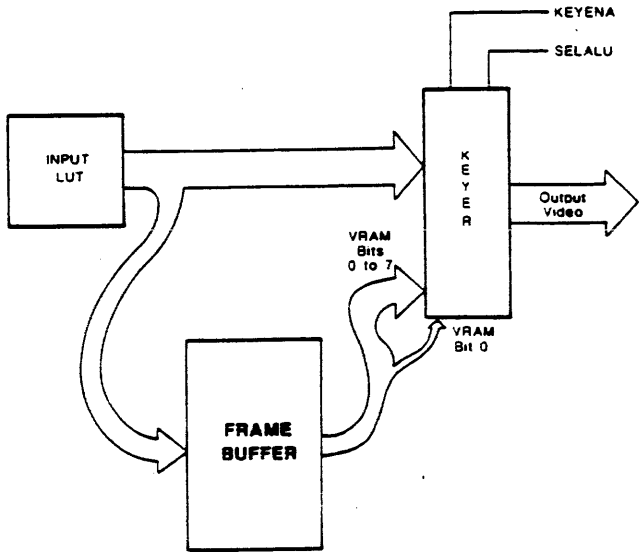


Figure 4.4: VIDEO KEYING

4.4 CRTC Access

The VIP uses a SY6845E CRT controller. Control parameters are loaded into the CRTC using two registers: the CRTC Data Register and the CRTC Address Register. The CRTC Status Register is used to read the chip's status. Additional information on the SY6845E can be found in Appendix B while additional information on the registers used to access the CRTC is given in Section 4.8. Furthermore, if block sync is enabled on the VIP-1024A (always enabled on the VIP-640A), the CRTC may be reprogrammed for any format consistent with a 10 MHz pixel rate used in the 256 $\times$ 256 display mode.

4.5 Video Keying

The VIP is capable of keying the frame buffer contents over the input video signal and outputing the resulting combined video. Keying is controlled by the three bits: KEYENA, SELALU, and the least significant bit in each pixel (Key Bit), as shown in Table 4.1. As you can see, when SELALU and KEYENA are 1, the Key Bit determines whether the output video comes from the input LUT or from the frame buffer. The bit mask can be used to set up the keying bit-plane without affecting the other planes. Note, however, that since one of the frame buffer's 8 bit-planes is used for the key, the number of colors that you can key onto the input video is 128 and not the 256 that can normally be produced by output from the frame buffer. For more information see Section 4.7.2

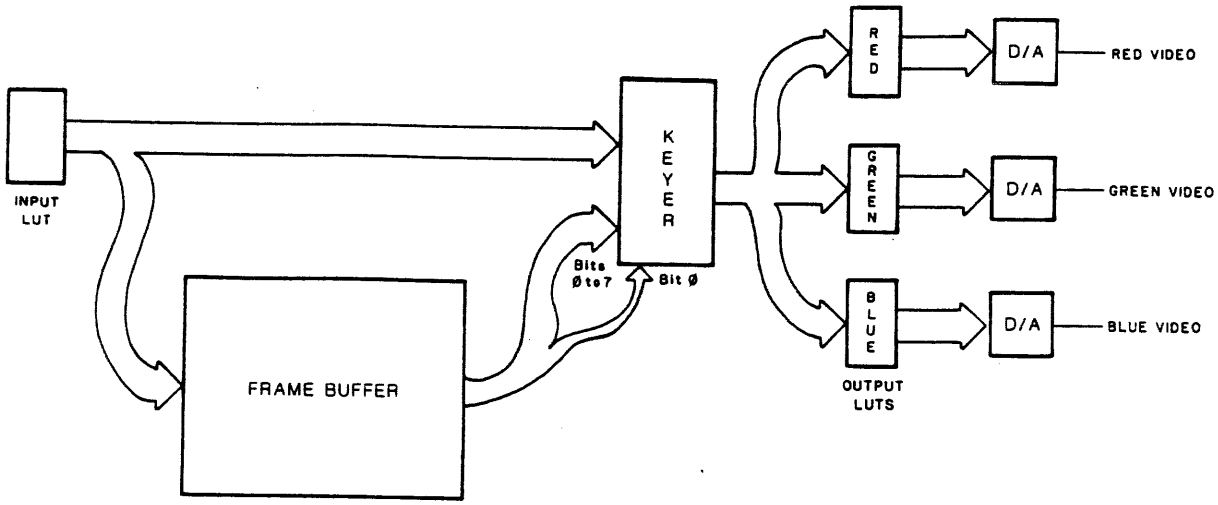


Figure 4.5: KEYING AND OUTPUT SECTION

SELALU	KEYENA	KEY BIT	OUTPUT SOURCE
0	0	0	input LUT
0	0	1	input LUT
0	1	0	input LUT
0	1	1	input LUT
1	0	0	frame buffer
1	0	1	frame buffer
1	1	0	input LUT
1	1	1	frame buffer

Table 4.1: KEYING CONTROL

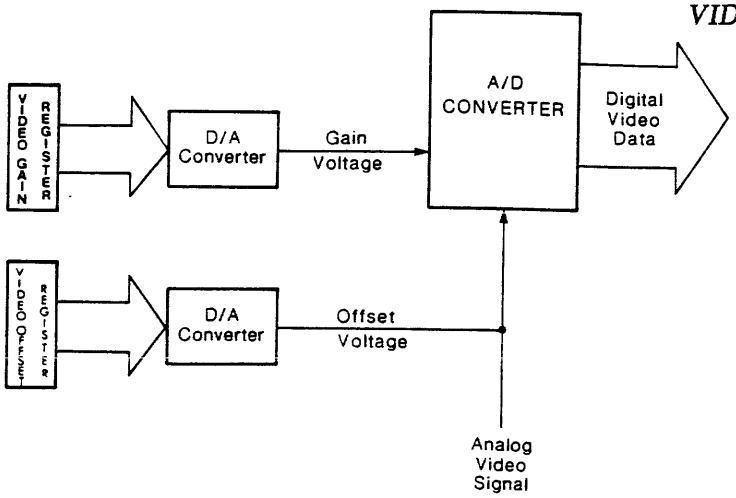


Figure 4.6: INPUT SIGNAL ADJUSTMENT

4.6 Video Adjustments

The VIP provides two registers for the adjustment of the gain and offset of the input analog-to-digital converter (Figure 4.6). The offset adjustment is a DC voltage that is applied to the input analog signal in order to clamp the black level to 0V. These two adjustments have the same effect as the brightness (gain) and contrast (offset) controls on a household television receiver.

The use of these two adjustments is illustrated in Figure 4.7. The analog-to-digital converter's gain and offset parameters are adjusted either to optimize digitization of a specific portion of the video signal or to ensure maximum conversion range for specific video inputs.

In order to optimize conversion range, the following procedure is used. A black level signal is repeatedly digitized while the offset value is decremented until this level corresponds to a to a digital value of 00H. This yields the value for the offset parameter.

Using the previous offset value, a white level signal is digitized repeatedly while decrementing the gain until the white level corresponds to a digital value of FFH. The resulting parameters are valid as long as the characteristics of the video input signal do not change.

The most effective algorithm for this procedure is a binary search of the 256 possible values of the offset and gain. This results in a maximum of seven passes to determine each parameter. A summary of an algorithm to set the nominal gain and offset may be found in Appendix C.

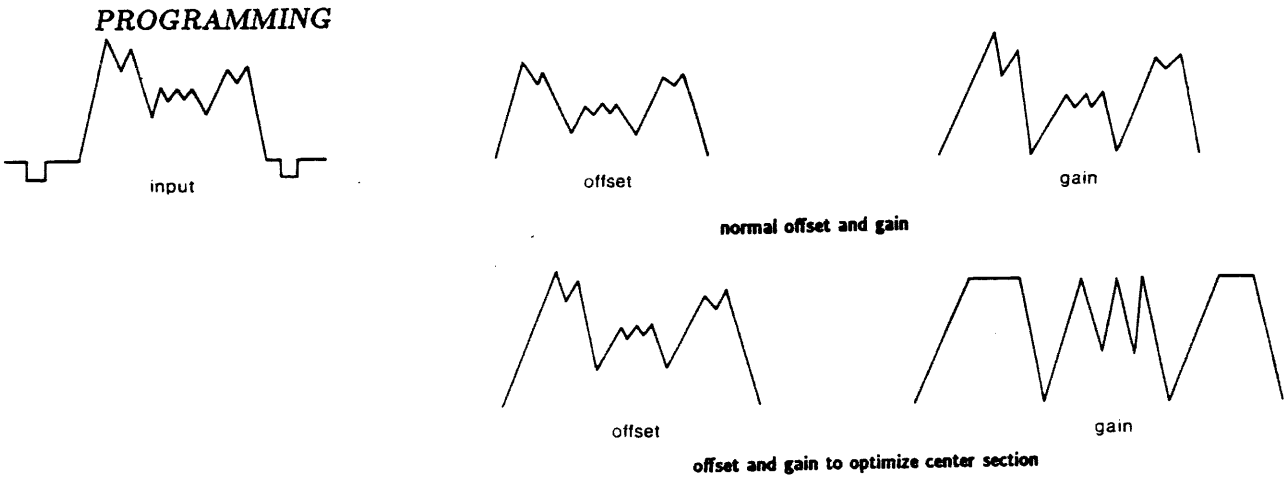


Figure 4.7: EXAMPLE OF OFFSET AND GAIN ADJUSTMENTS

RESOURCE	ACC	MODE	RANGE ALLOCATED	USED
Input lookup table	W	B	0000 - 07FF	256 [1]
Red lookup table	W	B	0800 - 0FFF	256
Green lookup table	W	B	1000 - 17FF	256
Blue lookup table	W	B	1800 - 1FFF	256
N / A			2000 - 27FF	
Control Register 0	W	B/W	2800 - 28FF	low byte
Control Register 1	W	B/W	2900 - 29FF	low byte
Mask Register	W	B/W	2A00 - 2AFF	low byte
Status Register	R	B/W	2B00 - 2BFF	low byte
Snapshot Register	R/W	B/W	2C00 - 2CFF	
N / A			2D00 - 2FFF	
CRTC Address/Status Register	R/W	B/W	3000 - 33FF	low byte
CRTC Data Register	R/W	B/W	3400 - 37FF	low byte
Video Gain Register	W	B/W	3800 - 3BFF	low byte
Video Offset Register	W	B/W	3C00 - 3FFF	low byte
N / A			4000 - FFFF	

ACC: Method by which the resource may be accessed i.e. Read or Write or both.
MODE: Manner by which the resource may be accessed i.e. Byte or Word.

Table 4.2: REGISTER AND LUT OFFSETS

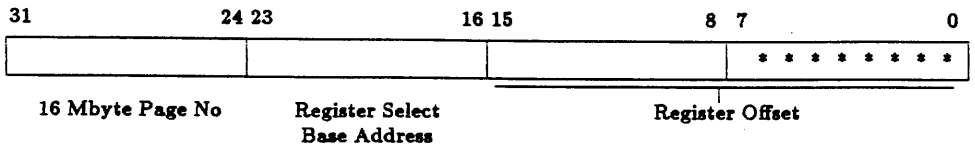
4.7 Registers and Lookup Tables

There are 9 memory mapped registers and 4 lookup tables in the VIP. They occupy a 64 KByte user-strapped memory space on the VMEbus. The addresses specified in Table 4.2 are offsets from the Register Base Address assigned to the registers and LUT's on the VMEbus when the board is strapped. The operation and the functions of the VIP are controlled by the system CPU through read and write accesses to the VIP's internal registers and lookup tables. Registers are used for miscellaneous control functions such as input and output processing options, bit-plane access, board status, processing status, etc. They are also used for specific functions such as setting the video gain and offset, accessing the CRTC, snapshot enable, etc. For more information concerning the LUTs refer to Section 3.4

[1] 256 of 2048 bytes accessable at a time, selected by LUTSEL 0,1,2

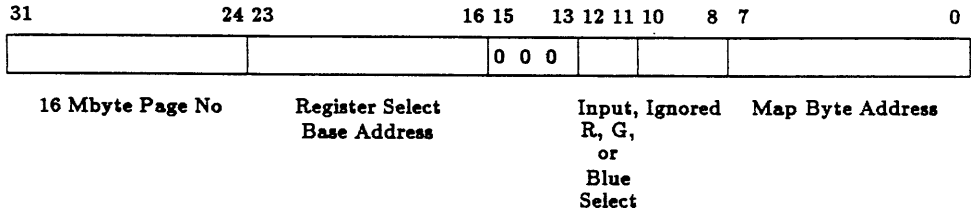
and Section 3.11. The following diagrams show register and LUT addressing for the VIP.

Register Address

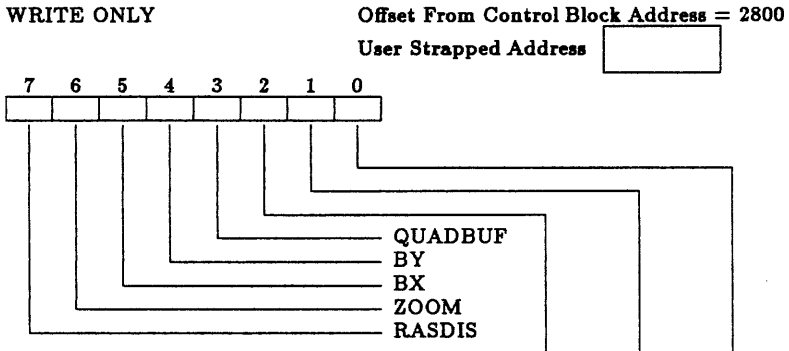


* Don't Care

Lookup Table Address



4.7.1 Control Register 0



LUT Map	LUTSL2	LUTSL1	LUTSL0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Note: all bits in this register are set to the default value (0) upon power-up (cold reset).

Bits 0,1,2: LUTSL0, LUTSL1, and LUTSL2. Write a 0 or a 1 to each of these bits to select the corresponding set of lookup table maps used for grab or display. Write only.

Bit 3: QUADBUF. Use this bit to set the display format. Write a 1 to this bit to select 4 independent 512 × 512 frame buffers. Write a 0 to this bit to select one 1024 × 1024 frame buffer. The QUADBUF mode is not normally used with the VIP-640A because of the reduction in horizontal display width.

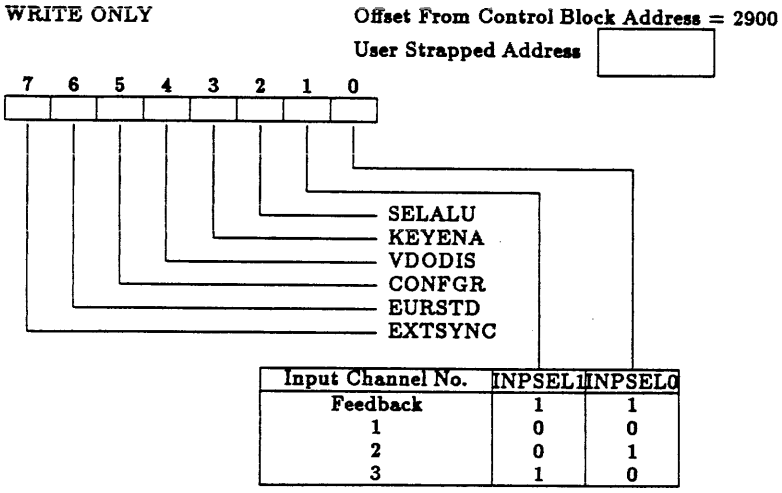
Bit 4: BY. Use this bit along with BX to select the quadrant of the display memory to be displayed when in 4 × 512 × 512 mode. Not normally used with the VIP-640A as explained above. (Used with VIP-1024A when QUADBUF=1; set to 0 on VIP-640A.)

Bit 5: BX. Use this bit along with BY to select the quadrant of the display memory to be displayed when in 4 × 512 × 512 mode. Not normally used with the VIP-640A as explained above. (Used with VIP-1024A when QUADBUF=1; set to 0 on VIP-640A.)

Bit 6: ZOOM. Use this bit to enable or disable the Zoom function. Set this bit to 1 to enable Zoom, or set it to 0 to disable Zoom.

Bit 7: RASDIS. Write a 1 to this bit to prohibit video memory refresh. Write a 0 to this bit to enable a video memory refresh. This bit should always be set to 0 except when switching between internal and external synchronization.

4.7.2 Control Register 1



Input Channel No.	INPSEL1	INPSEL0
Feedback	1	1
1	0	0
2	0	1
3	1	0

Bits 0 and 1: INPSEL0 and INPSEL1. These two bits are used to select the input source according to the table above.

Bit 2 and 3: SELALU and KEYENA. These two bits are used to determine the source of the video output. The following table shows the keying and LUT options selected by the bit values of SELAU,KEYENA, and the Key Bit. The Key Bit is the least significant bit of each pixel in the frame buffer.

SELALU	KEYENA	KEY BIT	OUTPUT SOURCE
0	0	0	input LUT
0	0	1	input LUT
0	1	0	input LUT
0	1	1	input LUT
1	0	0	frame buffer
1	0	1	frame buffer
1	1	0	input LUT
1	1	1	frame buffer

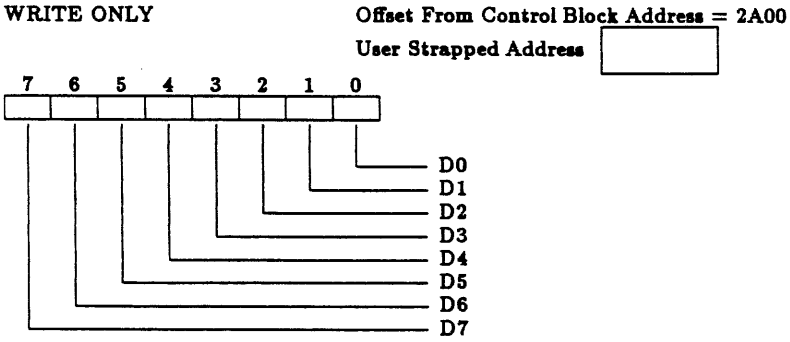
Bit 4: VDODIS. Write a 1 to this bit to disable the video output. Write a 0 to enable the video output.

Bit 5: CONFGR. Write a 1 to this bit to enable continuous frame grabbing. Write a 0 to disable continuous frame grabbing. In the frame grab mode video frames are continuously grabbed, digitized and then stored in the video memory. The frame grab active bit in the status register is set to 0 after the continuous grab operation is disabled and a complete frame has been grabbed.

Bit 6: EURSTD. Write a 1 to this bit to select the European TV standard of 50Hz and 625 lines. Write a 0 to select the American TV standard of 60Hz and 525 lines.

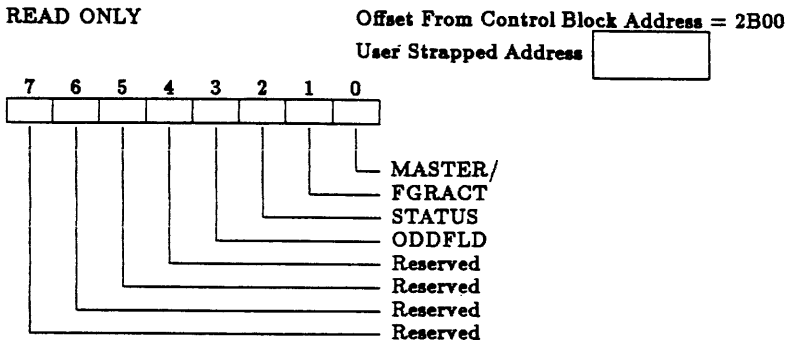
Bit 7: EXTSYNC Write a 1 to this bit to select external sync and to use the PLL to lock onto the horizontal sync in the video signal at the selected video input. Write a 0 to this bit to select a master (internal) sync and to make the on board crystal oscillator available.

4.7.3 Mask Register



Use this register to define a mask to selectively control write access to the different bit-planes in the frame buffer. This allows the user to set up the data in the frame buffer for video overlaying. Writing FF_{16} to this mask will mask write operations to all bit-planes in the frame buffer.

4.7.4 Status Register



Bit 0: MASTER/. When the VIP is configured as a slave, this bit is 1. When the board is configured as a master then this bit is 0.

Bit 1: FGRACT. This bit is set to 1 when frame grabbing is active. It is set to 1 immediately after the snapshot strobe to indicate that the frame grabbing process has started and is reset to 0 once the complete frame has been grabbed. This bit is also set during continuous frame grabbing.

Note: This bit is cleared on system reset.

Bit 2: STATUS. This bit reflects the state of the strap 43-46. It is 0 when 43-46 is IN and 1 when 43-46 is OUT.

Bit 3: ODDFLD. Bit 3 is 1 when the display frame is in an odd field. Bit 3 is 0 when the display frame is in an even field.

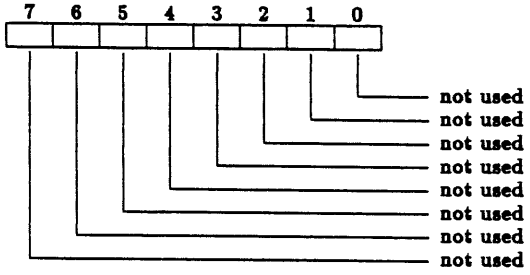
Bits 4-7: reserved.

4.7.5 Snapshot Register

READ/WRITE

Offset From Control Block Address = 2C00

User Strapped Address



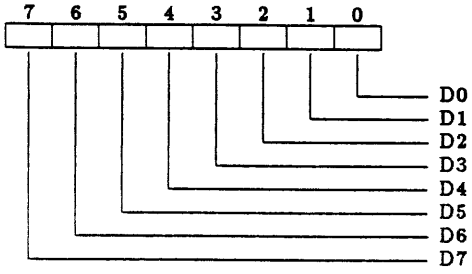
Make an access to this 0-bit read/write register to enable the video digitizer to take a snapshot of the next frame. This register has no effect on continuous grabbing mode.

4.7.6 Video Gain Register

WRITE ONLY

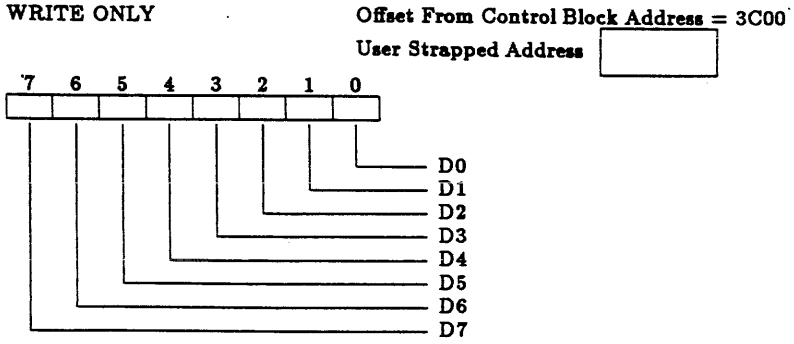
Offset From Control Block Address = 3800

User Strapped Address



This 8-bit register is used to control the video gain through the A/D converter. The gain can be set for 256 levels by loading these bits with values 00_{16} through FF_{16}. This register is used in conjuction with the Video Offset Adjust Register to adjust the input signal. See Section 4.6 for detailed instructions on this register's use.

4.7.7 Video Offset Register



This 8-bit register is used to clamp the input analog video signal to a 5V reference level for the A/D converter. There are 256 different offset levels from 00_{16} to FF_{16}. 00_{16} represents 5.98V offset, and FF_{16} an offset of 4.26V. See Section 4.6 for instructions on this register's use.

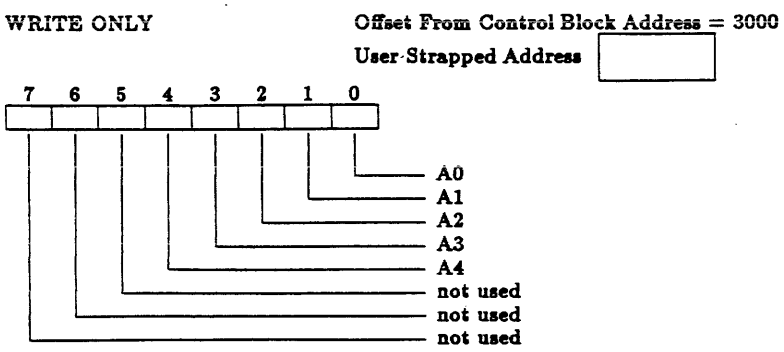
4.8 SY6845E CRT Controller

The SY6845E CRT Controller has 22 accessible internal registers which are used to define and control the raster scan CRT display. One of these registers, the Address Register, is used as a pointer for the Data Register which is used to load the other 20 (since the Status Register is directly accessable) registers.

In order to load any of the other registers, first load the Address Register with the necessary pointer. Then load the Data Register with the data to be placed in the selected register. Likewise, the user can read the internal registers (if applicable) by writing their address to the Address Register and then reading the Data Register. For further explanation see the SY6845E data sheets in Appendix B.

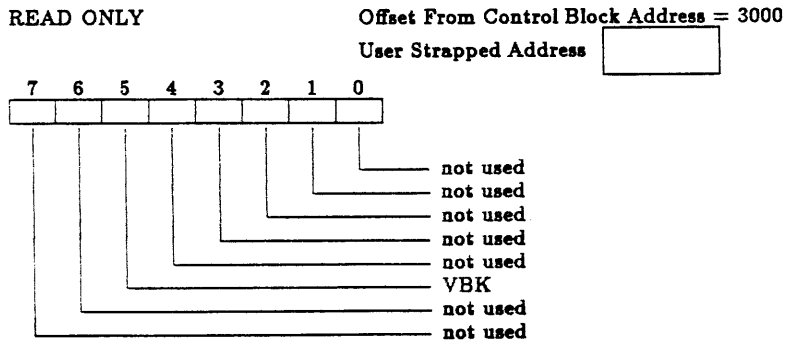
Note: The SY6845E is capable of generating sync frequencies other than 50Hz and 60Hz. It is strongly recommended that the CRTC be loaded as specified in this manual. See Table 4.3. For information on other frequencies, contact our Applications Engineering Department.

4.8.1 CRTC Address Register



This 5-bit register is used as a pointer to the CRT controller's internal registers when initializing the CRT controller for use. Only the five least significant bits are used.

4.8.2 CRTC Status Register



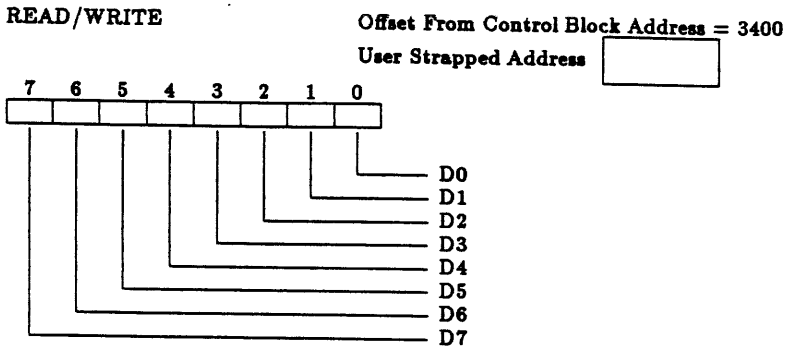
This 1-bit register holds the same place in memory as the CRTC Address Register. It is used to determine when the scan is in its vertical blanking period.

Bits 0-4: not used.

Bit 5: VBK. Bit 5 is 1 when the scan is in its vertical blanking period.

Bits 6,7: not used

4.8.3 CRTC Data Register



This 8-bit register is used in conjunction with the CRTC Address Register to indirectly load data to or read data from the CRT controller's internal registers.

4.8.4 Pan Control

Pan control is achieved through register 13 of the CRTC. In order to access this register, it is necessary to write D_{16} into the CRTC Address Register. Panning is by 8 pixels (one character) at a time and is absolute with a continuous wrap around effect. Therefore, if the upper left hand corner of the screen is at coordinates (0,0) in the frame buffer, writing a one into the CRTC Data Register will move the screen right by 8 pixels and writing a two will move the screen right by 16 pixels. However, if the upper left hand corner of the screen is at coordinates (6,5), then writing a one to the data register will move the screen left 40 pixels.

4.8.5 Scroll Control

Scroll control is achieved through register 12 of the CRTC. In order to access this register, it is necessary to write C_{16} into the CRTC Address Register. Scrolling is by 16 pixels (one character) at a time and is absolute with a continuous wrap around effect. Therefore, if the upper left hand corner of the screen is at coordinates (0,0) in the frame buffer, writing a 1_{16} into the CRTC Data Register will move the screen down by sixteen pixels and writing a 2_{16} will move the screen down by 32 pixels. However, if the upper left hand corner of the screen is at coordinates (0,4), then writing a one to the data register will move the screen up 48 pixels.

4.9 SY6845E CRT Controller

4.9.6 SY6845E Internal Registers

The following two tables list the SY6845E internal registers and the values that you must load these registers with for the North American (U.S.) video standard and the European video standard. Included are values for both the Normal Mode (Non-Zoom Mode) and the Zoom Mode.

Reg Addr	Reg No.	Register Type	Unit	I/O Type	US Std	Eur Std	ZOOM Mode US Std	ZOOM Mode Eur Std
0	R0	Horizontal Total	Char	Write	51	52	28	30
1	R1	Horizontal Displayed	Char	Write	40	40	20	20
2	R2	Horizontal Sync Position	Char	Write	42	43	20	21
3	R3	Vertical and Horizontal Sync Width	Char/ Scan Line	Write	4E	8E	47	87
4	R4	Vertical Total	Char Row	Write	1F	26	0F	12
5	R5	Vertical Total Adjust	Scan Line	Write	06	00	06	00
6	R6	Vertical Displayed	Char Row	Write	1E	20	0F	0F
7	R7	Vertical Sync Position	Char	Write	1E	23	0F	11
8	R8	Mode Control	—	Write	07	07	05	05
9	R9	Scan Line	Scan Line	Write	0F	0F	0F	0F
A	R10	Cursor Start	Scan Line	Write	XX	XX	XX	XX
B	R11	Cursor End	Scan Line	Write	XX	XX	XX	XX
C	R12	Displayed Start Address (H)	—	Write	00	00	00	00
D	R13	Displayed Start Address (L)	—	Write	00	00	00	00
E	R14	Cursor Position (H)	—	Read/ Write	XX	XX	XX	XX
F	R15	Cursor Position (L)	—	Read/ Write	XX	XX	XX	XX
10	R16	Light Pen Register (H)	—	Read	XX	XX	XX	XX
11	R17	Light Pen Register (L)	—	Read	XX	XX	XX	XX
12	R18	Update Location (H)	—	Write	XX	XX	XX	XX
13	R19	Update Location (L)	—	Write	XX	XX	XX	XX
1F	R31	Dummy Location	—	—	XX	XX	XX	XX

Table 4.3: VIP-1024A REGISTER SUMMARY

Reg Addr	Reg No.	Register Type	Unit	I/O Type	US Std	Eur Std	ZOOM Mode US Std	ZOOM Mode Eur Std
0	R0	Horizontal Total	Char	Write	51	52	30	30
1	R1	Horizontal Displayed	Char	Write	40	40	28	27
2	R2	Horizontal Sync Position	Char	Write	42	43	2A	28
3	R3	Vertical and Horizontal Sync Width	Char/ Scan Line	Write	4E	8E	47	88
4	R4	Vertical Total	Char Row	Write	1F	26	0F	12
5	R5	Vertical Total Adjust	Scan Line	Write	06	00	06	0A
6	R6	Vertical Displayed	Char Row	Write	1E	20	0F	10
7	R7	Vertical Sync Position	Char	Write	1E	23	0F	11
8	R8	Mode Control	—	Write	07	07	05	05
9	R9	Scan Line	Scan Line	Write	0F	0F	0F	0F
A	R10	Cursor Start	Scan Line	Write	XX	XX	XX	XX
B	R11	Cursor End	Scan Line	Write	XX	XX	XX	XX
C	R12	Displayed Start Address (H)	—	Write	00	00	00	00
D	R13	Displayed Start Address (L)	—	Write	00	00	00	00
E	R14	Cursor Position (H)	—	Read/ Write	XX	XX	XX	XX
F	R15	Cursor Position (L)	—	Read/ Write	XX	XX	XX	XX
10	R16	Light Pen Register (H)	—	Read	XX	XX	XX	XX
11	R17	Light Pen Register (L)	—	Read	XX	XX	XX	XX
12	R18	Update Location (H)	—	Write	XX	XX	XX	XX
13	R19	Update Location (L)	—	Write	XX	XX	XX	XX
1F	R31	Dummy Location	—	—	XX	XX	XX	XX

Table 4.4: VIP-640A REGISTER SUMMARY

Chapter 5

STRAPS

5.1 Strap Notation

User configured straps select or control several functions on the VIP. This chapter describes those functions and indicates what the different strap options are. All straps on the board are made by tying together numbered wire wrap pins. When a particular strap is referred to, it is done so by giving the numbers of the two pins that are to be tied together to form the strap. In some cases the pin numbers are followed by an IN or OUT suffix to indicate whether the pins are to be strapped or left free.

5.2 Status Bit

This strap determines the logic level read at bit 2 in the Status Register and it is meant to be user defined. The user may want to use it to tell the system CPU something about the VIP's current strap configuration. For example, we can use this strap to inform the host CPU that something else is using the Video-Bus.

STATUS = 0 43-46 IN
STATUS = 1 43-46 OUT

5.3 Board Address Selection

The number of Video Digitizer Boards that can be installed into the system is dependant upon the number of boards which can be connected on the same Sync-Bus. It is necessary, however, for each board to have a different base address. In 32-bit addressing, the user can include the VIP boards in the same 16 Mbyte page arranging them so that no memory space overlaps, or they can select a different 16 Mbyte page for one or more VIPs. For an example of this see Figure 4.1. In 24-bit addressing mode there is only one 16 Mbyte page so all VIPs must be in the same page.

5.3.1 Addressing Mode

The following straps select the addressing mode.

Supervisor mode only	62-63 OUT
Supervisor or non-privileged	62-63 IN

5.3.2 Memory Space

The following straps select either a 16 Mbyte (24-bit address) or 4 Gbyte (32-bit address) memory space.

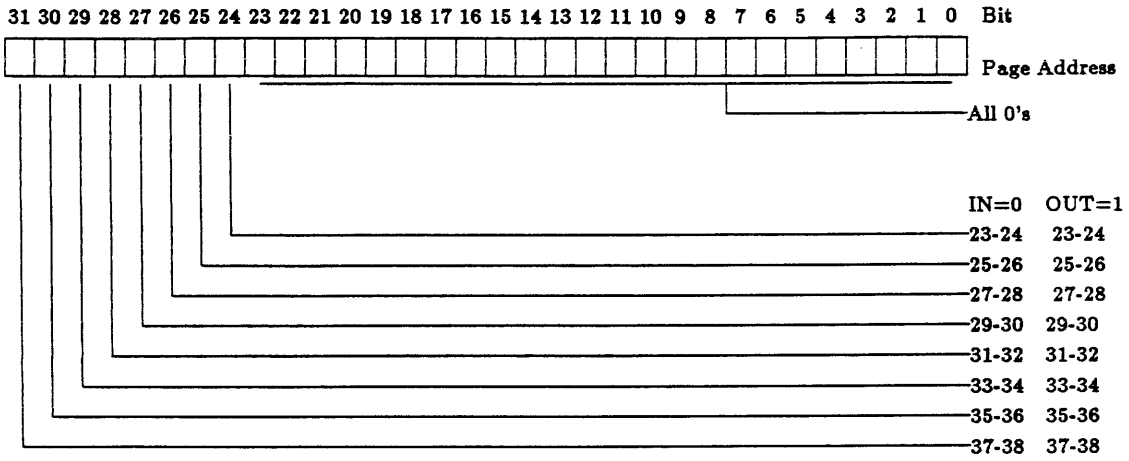
Address Size	Address Space	Strap
24-bit address	16 Mbyte	65-66 IN
32-bit address	4 Gbyte	65-66 OUT

5.3.3 Page and Register Address Selection

There are three sets of straps. One set determines the 16 Mbyte page for the VIP's location. Another set determines the 1 Mbyte block for the Video RAM and a third set determines the 64K block for the Registers and LUT's. In A32 mode, the VIP decoder must find the Video RAM and the register map in the same strap selected 16 Mbyte page. Thus note that in the following diagrams, the page of both the register access block and the VRAM is dependant upon the page that the the high order eight bits of the 32-bit address have been strapped to on the VIP. With 24-bit addressing, this does not apply.

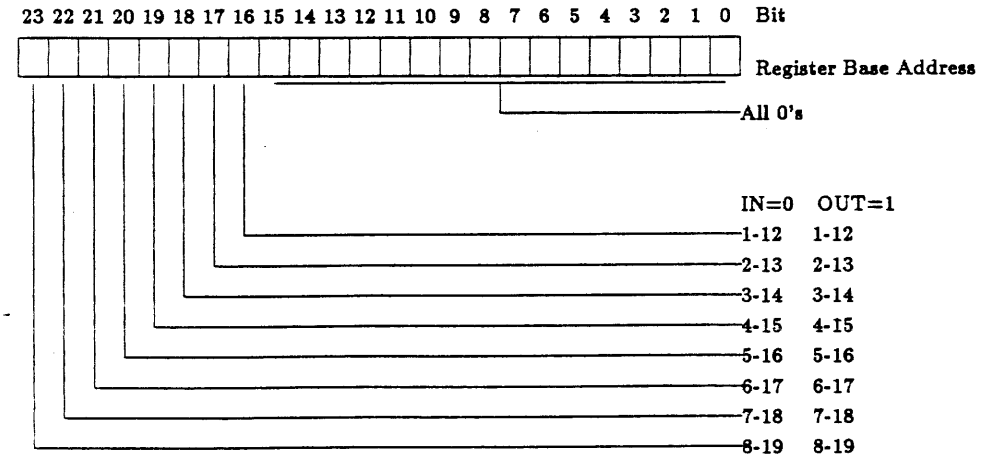
16 Mbyte Page Selection

If your system uses a 32-bit address use the straps in the following diagram to select the 16 Mbyte page that the VIP is to be located in.



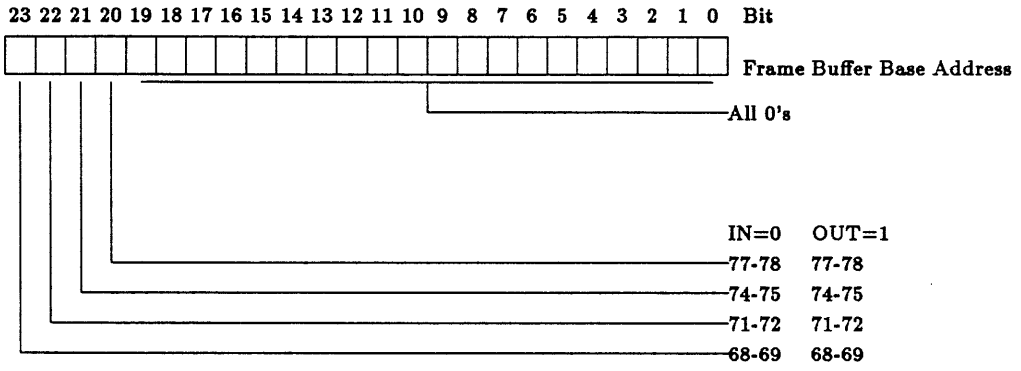
Register Access Block

The following diagram shows how to strap the position of the VIP's register access block on any 64 Kbyte boundary in the 16 Mbyte page selected by the page select straps.



1 Mbyte Frame Buffer Boundary Selection

The following diagram shows how to strap the VIP's frame buffer on any 1 Mbyte boundary in the 16 Mbyte page selected by the page select straps.



5.4 Master and Slave Setup

The following straps determine whether the VIP is a master (controls the video bus) or a slave. Refer to Section 6.2.1 for information on the Sync-Bus.

Master	39-40 IN	47-48 OUT
Slave	39-40 OUT	47-48 IN

5.5 Sync Selection

The following straps select various sync options. See Section 3.3 for input sync description. Note that block sync (RS 330) must not be selected when the board is in external sync mode.

	OPTION	IN	OPTION	OUT
Input channel sync type	RS170	42-45	RS330	42-45
Composite sync on output red gun	YES	83-84	NO	83-84
Composite sync on output green gun	YES	81-82	NO	81-82
Composite sync on output blue gun	YES	79-80	NO	79-80

5.5.1 Input Sync Source

When the VIP is taking its sync from an external source, that sync can be combined with the video on the currently selected video input or it can be a separate composite sync signal on channel 2 (green input), with one of the other inputs selected to input video. The following straps most be used to select one mode or the other.

Sync combined with video	85-86 IN	86-87 OUT
Separate sync on channel 2 (green)	85-86 OUT	86-87 IN

5.5.2 Composite Sync Type

The following straps allow you to select the type of sync at the output of the VIP-1024A. The VIP-640A must always be strapped for RS330 sync.

RS170	51-53 IN	53-55 OUT (VIP-1024A only)
RS330	51-53 OUT	53-55 IN

5.5.3 Output Channel Sync Polarity

Active High	50-52 IN	52-54 OUT
Active Low	50-52 OUT	52-54 IN

5.5.4 Feedback Channel Input Impedance

The following strap determines whether an internal 75 ohm termination impedence will be connected to the feedback channel input. It is used only if no load is connected to the green video output.

Internal Termination Impedence In Place	97-98 IN
Internal Termination Impedence Absent	97-98 OUT

5.6 Camera Connector

5.6.1 Pixel Clock

The following straps set the polarity of the Pixel Clock.

Active high	70-73 IN	73-76 OUT
Active low	70-73 OUT	73-76 IN

5.6.2 Vertical Sync

The following straps set the polarity of the vertical sync at the output.

Active high	64-67 IN	61-64 OUT
Active low	64-67 OUT	61-64 IN

5.6.3 Sync

The following straps select the type and polarity of the sync that is provided at pin 2 of J5.

	58-60	56-58	57-58	58-59
Active high composite sync	IN	OUT	OUT	OUT
Active low composite sync	OUT	IN	OUT	OUT
Active high horizontal sync	OUT	OUT	IN	OUT
Active low horizontal sync	OUT	OUT	OUT	IN

5.7 Factory-Set Straps

5.7.1 Expansion Strap

The following straps are provided for eventual expansion but in the meantime they must be positioned as follows:

9-10	10-11	20-21	21-22	41-44	44-49
IN	OUT	IN	OUT	OUT	IN

5.7.2 Configuration Straps

The straps connected to pins 88 through 96 are factory configured as follows and should not be changed.

VIP-640A	VIP-1024A
88-89 IN	88-89 OUT
90-91 IN	90-92 IN
92-93 IN	91-93 IN
95-96 IN	95-96 IN
94-95 OUT	94-95 OUT

5.8 Strap Summary

Pin	Name	Connecting Pin
1	Register Base Addr Sel A16	12
2	" A17	13
3	" A18	14
4	" A19	15
5	" A20	16
6	" A21	17
7	" A22	18
8	" A23	19
9	Expansion Strap	10
10	"	9
11	"	
12	Register Base Addr Sel A16	1
13	" A17	2
14	" A18	3
15	" A19	4
16	" A20	5
17	" A21	6
18	" A22	7
19	" A23	8
20	Expansion Strap	21
21	"	20
22	"	
23	VIP Base Address Sel A24	24
24	" A24	23
25	" A25	26
26	" A25	25
27	" A26	28
28	" A26	27
29	" A27	30
30	" A27	29
31	" A28	32
32	" A28	31
33	" A29	34
34	" A29	33
35	" A30	36
36	" A30	35
37	" A31	38
38	" A31	37
39	Master Select	40
40	"	39
41	Expansion Strap	
42	RS170/RS330 Input Sync Type	45
43	STATUS	46
44	Expansion Strap	49

Table 5.1: STRAP SUMMARY Part One

Pin	Name	Connecting Pin
45	RS170/RS330 Input Sync Type	42
46	STATUS	43
47	Slave Select	48
48	"	47
49	Expansion Strap	44
50	Output Channel Sync Polarity/High	52
51	Composite Sync Type/RS170	53
52	Output Channel Sync Polarity High/Low	50 or 54
53	Composite Sync Type RS170/RS330	51 or 55
54	Output Channel Sync Polarity/Low	52
55	Composite Sync Type/RS330	53
56	Active Low Composite Sync	58
57	Active High Horizontal Sync	58
58	High/Low Composite/Horizontal Sync	60,56,57,or59
59	Active Low Horizontal Sync	58
60	Active High Composite Sync	58
61	Active Low Vertical Sync	64
62	Supervisor/Non-privileged	63
63	Supervisor/Non-privileged	62
64	Active Low/High Vertical Sync	61 or 67
65	Address Select 24/32	66
66	"	65
67	Active High Vertical Sync	64
68	VRAM Base Address A23	69
69	" A23	68
70	Active High Pixel Clock	73
71	VRAM Base Address A22	72
72	" A22	71
73	Pixel Clock High/Low	70 or 76
74	VRAM Base Address A21	75
75	"	74
76	Active Low Pixel Clock	73
77	VRAM Base Address A20	78
78	"	77
79	Output Composite Sync/Blue	80
80	"	79
81	Output Composite Sync/Green	82
82	"	81
83	Output Composite Sync/Red	84
84	"	83
85	Input Sync Source Select	86
86	Input Sync Source	85 or 87
87	Input Sync Source Green	86
88	factory pin	89
89	factory pin	88
90	factory pin	91 or 92
91	factory pin	90 or 93
92	factory pin	90 or 93
93	factory pin	91 or 92
94	factory pin	95
95	factory pin	94 or 96
96	factory pin	95
97	75 ohm internal termination	98
98	75 ohm internal termination	97

Table 5.2: STRAP SUMMARY Part Two

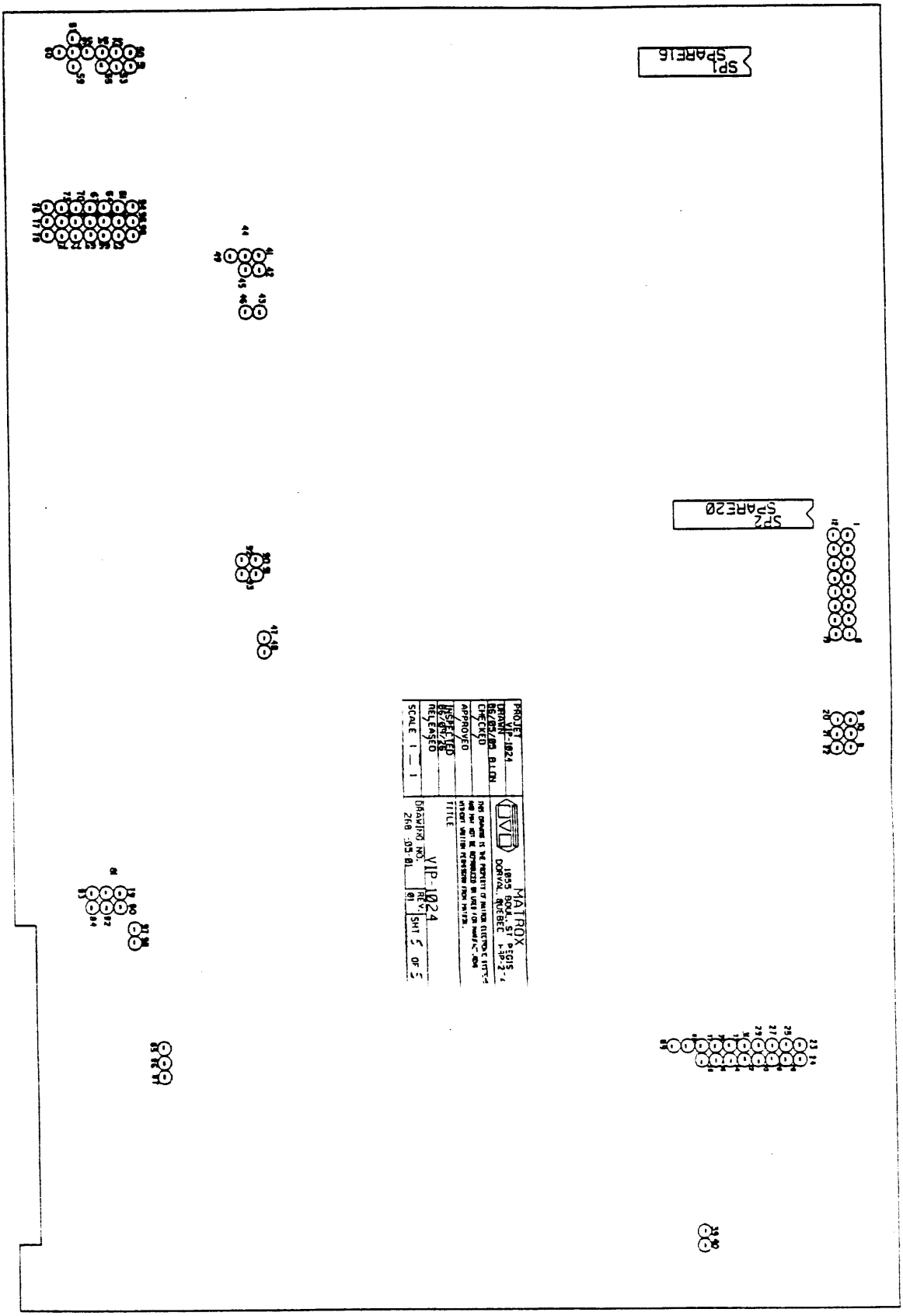


Figure 5.1: STRAP LOCATIONS

Chapter 6

CONNECTORS

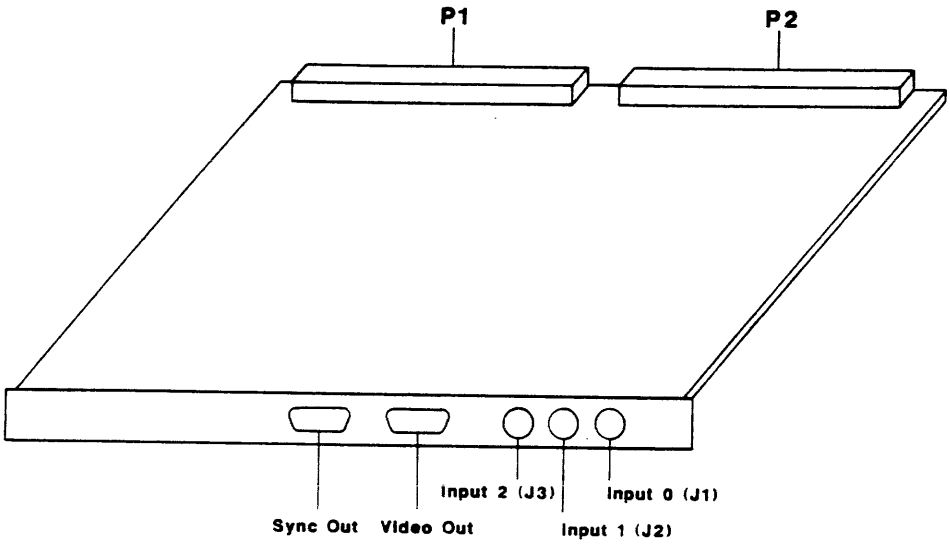


Figure 6.1: CONNECTOR LAYOUT

6.1 External Connectors

6.1.1 Video Input 0 (J1), Input 1 (J2) and Input 2 (J3)

The places for these coaxial connectors are marked at the lower right hand side of the board. They are BNC connectors for RGB input. The following lists the input color for each input connector.

Input 0	Red
Input 1	Green
Input 2	Blue

The following is a diagram of a BNC coaxial connector.

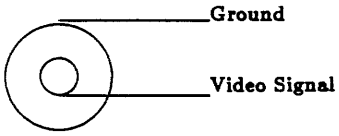


Figure 6.2: INPUT VIDEO CONNECTOR

6.1.2 Video Output (J4)

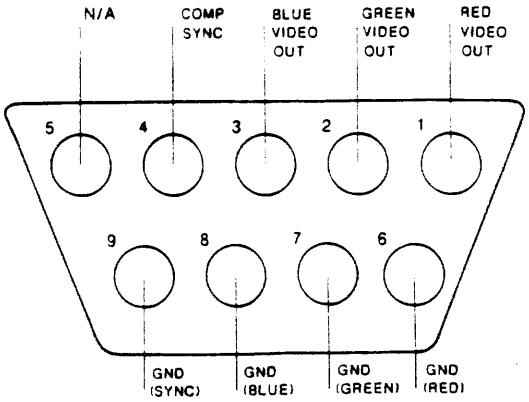


Figure 6.3: OUTPUT VIDEO CONNECTOR

The video output connector is a DB9 female connector for RGB output with separate sync. Composite sync is also available on all channels.

6.1.3 Camera (J5)

The camera output connector is a DB9 male connector with sync and pixel clock for the camera.

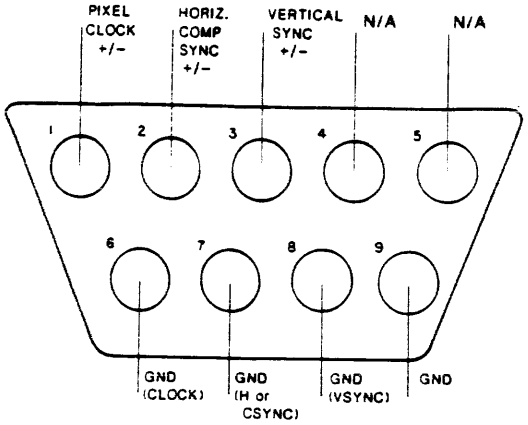


Figure 6.4: OUTPUT CAMERA CONNECTOR

6.2 VMEbus Board Connectors (P1 and P2)

There are two large VMEbus connectors called P1 and P2 on the side of the board opposite the input connectors. Each VMEbus connector consists of three rows of pins labelled A, B, and C.

P1 is a standard VMEbus connector. Signal names for the P1 connector pins can be found in Table 7-1 of the VMEbus Specification Manual.

Row B of P2 is standard. Rows A and C are defined as a Video-Bus. Signal names for row B connector pins can be found in Table 7-2 of the VMEbus Specification Manual. 36 of a possible 64 signals are defined on rows A and C of P2 for expansion or gen-lock. Table 6.1 lists the signal names for the connector pins of rows A and C of P2.

The following defines the signal names used in Connector P2.

- D GND: Digital ground.
- MCLK/: Master clock (input/output).
- MVS/: Master vertical sync (input/output).
- MSIE: Master cycle synchronization (input/output).
- MHS/: Master horizontal sync (input/output).

Pin	ROW A	ROW C
1	MCLK/	D GND
2	MVS/	D GND
3	MSIE	D GND
4	MHS/	D GND
5	MSEPSYNC	D GND
6	S00	S01
7	S02	S03
8	S04	S05
9	S06	S07
10	S40	S41
11	S42	S43
12	S44	S45
13	S46	S47
14	DGND	R0
15	EXTFRG	INTFRG
16	EXPOE	BK/
17	EXPS	D GND
18	Reserved	Reserved
19	Not used	Not used
20	Not used	Not used
21	Not used	Not used
22	Not used	Not used
23	Not used	Not used
24	Not used	Not used
25	Not used	Not used
26	Not used	Not used
27	Not used	Not used
28	Not used	Not used
29	Not used	Not used
30	Not used	Not used
31	Not used	Not used
32	Not used	Not used

Table 6.1: P2 CONNECTOR PIN SIGNAL NAMES

- MSEPSYNC: Master external separated sync (input/output).
- S00-07: Pixel data input to VIP.
- S40-47: Pixel data output from VIP.
- R0: Odd field indicator (output).
- EXTFRG: External frame grab (input).
- INTFRG: Internal frame grab (output).
- EXPOE: Input signal. When EXPOE is asserted then the expansion is enabled.
- BK/: Composite blank (output).
- EXPS: Input signal used to synchronize the VIP with the expansion card once per frame (output).

6.2.1 Sync-Bus

The Sync-Bus consists of 10 signals and is located on P2. These 10 signals occupy the first 5 pins on P2 rows A and C and are used to synchronize multiple VIPs. i.e. they synchronize a master/slave configuration. These must be interconnected to gen-lock two to four VIPs. The next 12 pins of rows A and C on P2 are the Video-Bus. They are used in conjunction with the first 5 to provide connection to an expansion board only. Note that the remaining pins of the Video-Bus (rows 6 to 17) must not interconnect master and slave VIPs.

Chapter 7

MAINTENANCE AND WARRANTY

Matrox products are warranted against defects in materials and workmanship for a period of 1 year from the date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. Matrox is not liable for consequential damages.

To return units for repair:

1. Obtain an RMA number from our Application Engineering Deptment.
2. Fill out the Product Failure Report found at the back of this manual and put the RMA number in the top margin.
3. Return the unit and the completed product failure report to Matrox.

U.S. customers are to return their products to our U.S. office, at the following address:

Matrox International Corporation,
Trimex Building,
Mooers, N.Y. 12958

* * * * *

Appendix A

INSTALLATION

To install the VIP follow these steps:

1. Configure the VIP using the jumpers described in Chapter 5.
2. Firmly press the board into the slot.
3. Ensure proper connections to the P2 connector via your VMEbus backplane. Note that rows A and C of P2 are user defined. Exercise caution with these connections as incorrect connections may damage the system. Also, before changing the slot position of the board ensure that the P2 connections are compatible.
4. Connect the RGB monitor to J4 and the camera(s) to J1, J2, and J3, as well as to J5 if necessary. The removal or insertion of video inputs (BNC connectors) during External Sync operation is not recommended.

Appendix B

DATA SHEETS

The following pages contain the data sheets for the Synertek SY6845E CRT Controller.

Synertek

SY6845E
CRT Controller

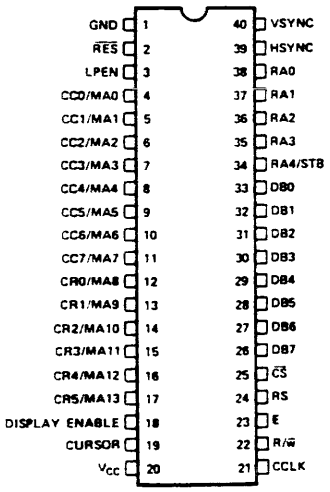
Features

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845R.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6845
- Internal status register.
- 3.7 MHz Character Clock
- Transparent Address Mode

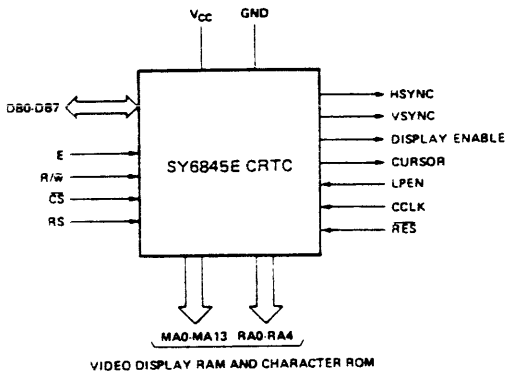
Description

The SY6845E is a CRT Controller intended to provide capability for interfacing any 8 or 16 bit microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Interface Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

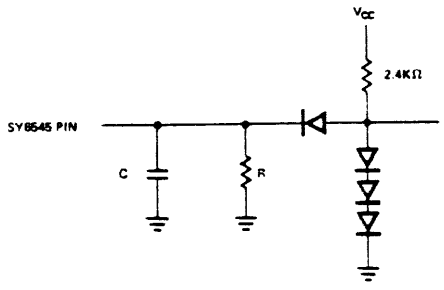
Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0–70° C, unless otherwise noted)

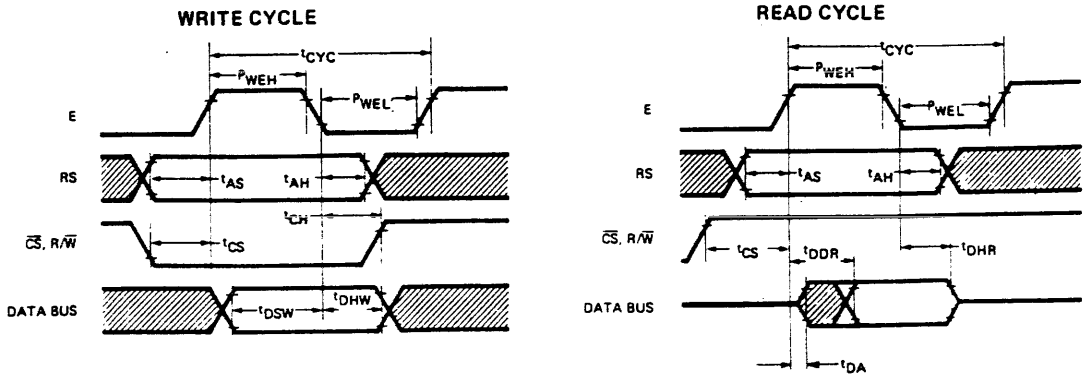
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/W, RES, CS, RS, LPEN, CCLK)	—		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	—		±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		—	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	—		0.4	V
P_D	Power Dissipation	—	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	— —		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	—		10.0	pF

Test Load



R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics



Write Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	0.25	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	115	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	100	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	20	–	ns
t_{CH}	R/W, CS Hold Time	0	–	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	10	–	ns

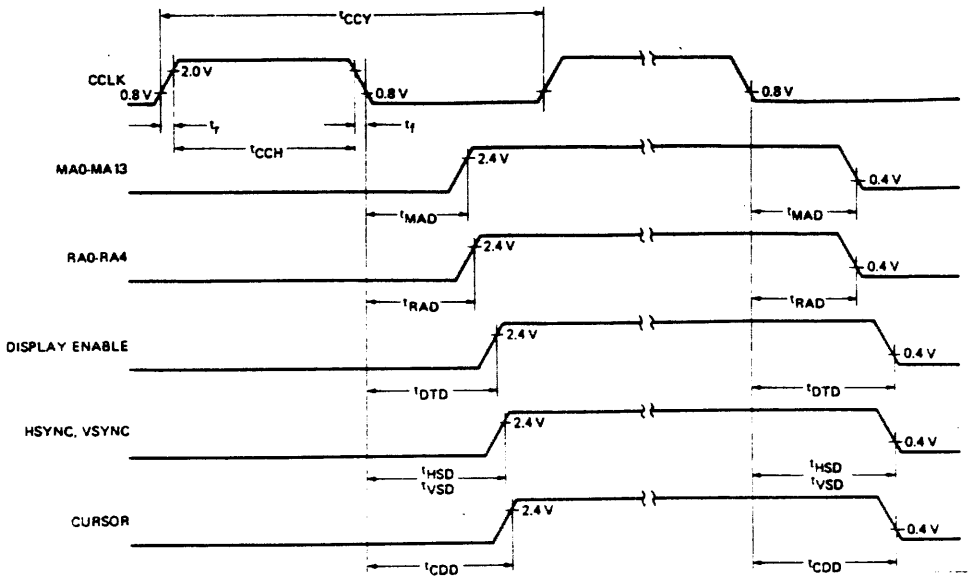
(t_r and t_f = 10 to 30ns)

Read Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	0.25	–	μs
P_{WEH}	ϕ2 Pulse Width, High	440	–	200	–	150	–	115	–	ns
P_{WEL}	ϕ2 Pulse Width, Low	420	–	190	–	140	–	100	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	0	–	ns
t_{CS}	R/W, CS Set-Up Time	80	–	40	–	30	–	20	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	–	85	ns
t_{DHR}	Read Hold Time	10	–	10	–	10	–	10	–	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	20	60	ns
t_{TAD}	MA0-MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	60 typ.	95	ns

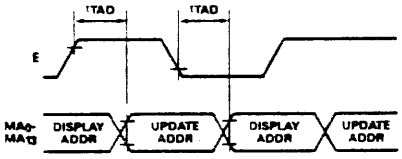
(t_r and t_f = 10 to 30ns)

Memory and Video Interface Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

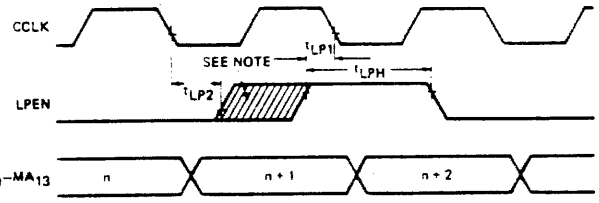


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCY}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (Φ1/Φ2 Interleaving)



Light Pen Strobe Timing



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	–	0	ns

t_r and t_f = 20ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the SY6845. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6845 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6845; a low on the R/$\overline{W}$ pin allows a write to the SY6845.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6845 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6845. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0–MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0–MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0–MA7 function as column addresses CC0–CC7, and MA8–MA13, as row addresses CR0–CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0–CC7 and CR0–CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6845 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0–MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6845 with only a small amount of external circuitry.

Description of Internal Registers

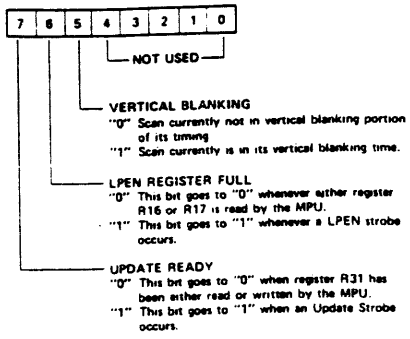
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6845 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6845 data transfers to and from the system MPU. Its contents is the number of the desired register (0–31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

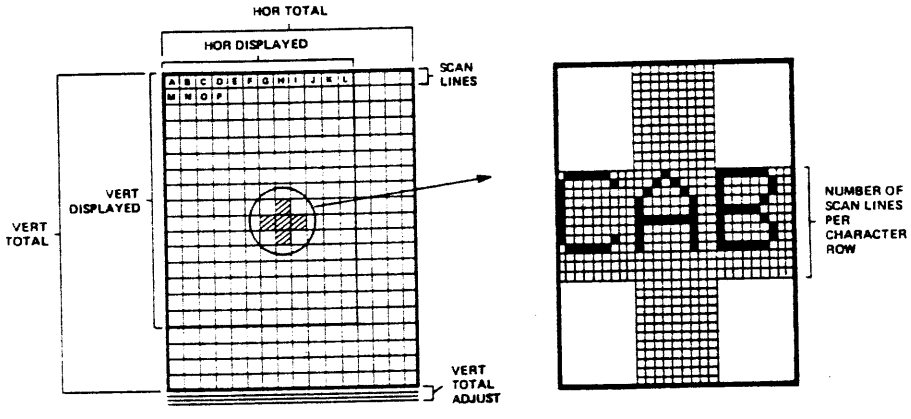


Figure 1. Video Display Format

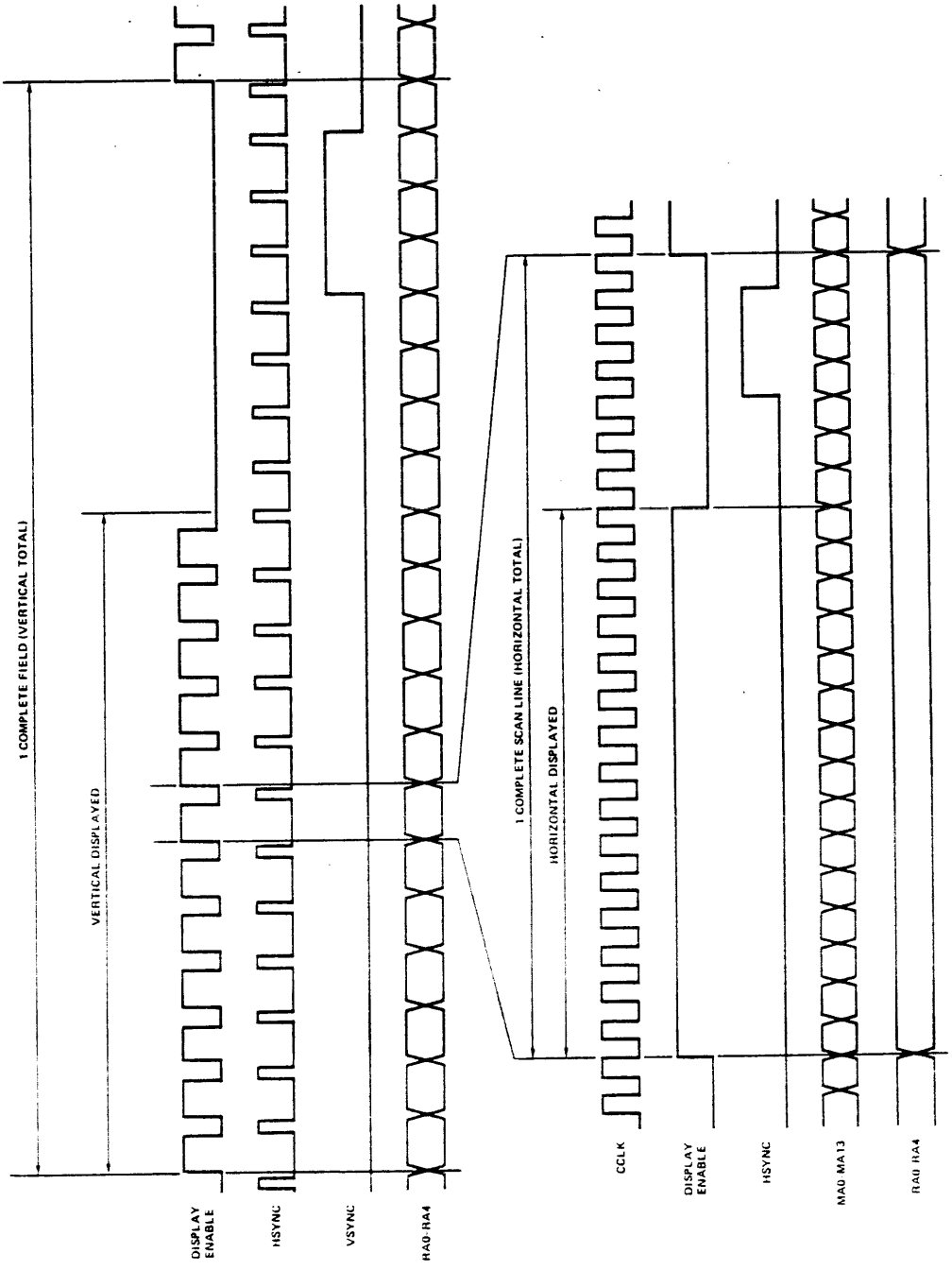
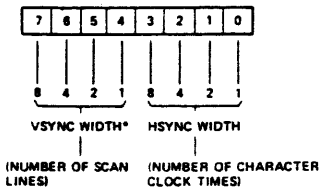


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6845 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		\				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		\		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	= Charac. -1		\	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	= Charac.		\	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	= Charac.		\	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	= Scan Lines and = Char. Times		\	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	= Charac. Row -1		\		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	= Scan Lines		\				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	= Charac. Rows		\		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	= Charac. Rows		\		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			\	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	= Scan Lines -1		\				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		\		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		\				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		\				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		\	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	\	\				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)	Col	\	\	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		\					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		\		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			\				●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			\	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

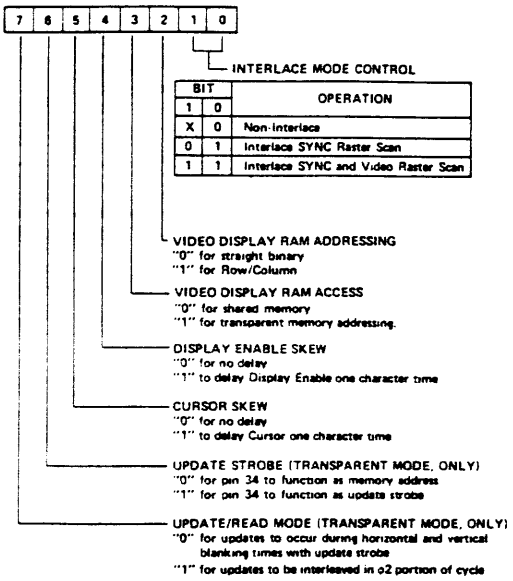
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6845 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	CURSOR MODE
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16x field rate (fast)
1	1	Blink at 32x field rate (slow)

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6845 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

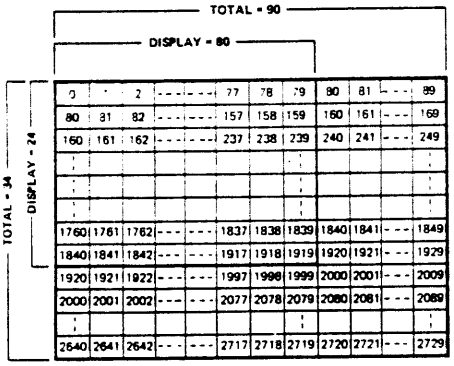
Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

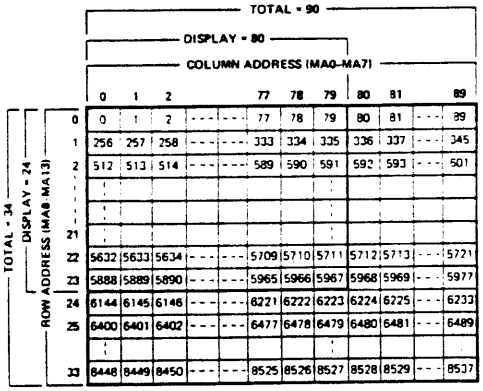
Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.



STRAIGHT BINARY ADDRESSING SEQUENCE



ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6845 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6845 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6845. All MPU accesses are made via the SY6845 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

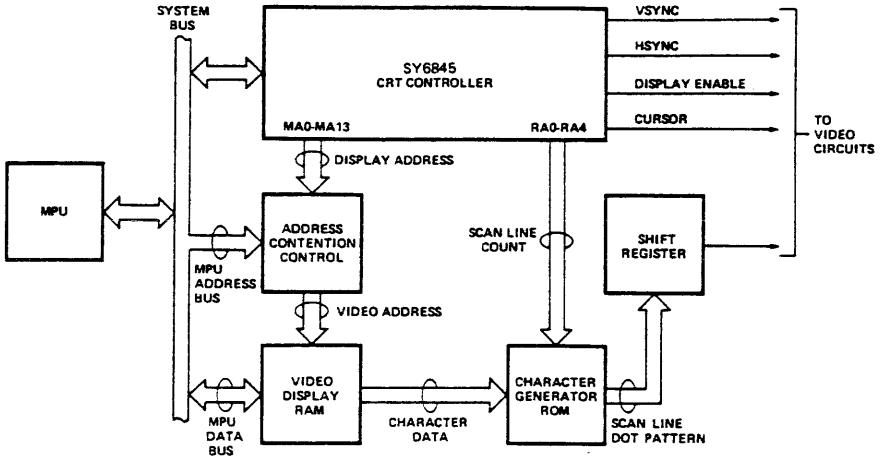


Figure 5. Shared Memory System Configuration

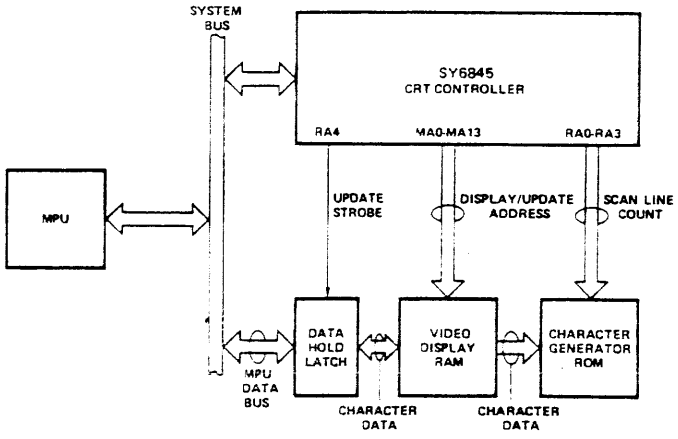


Figure 6. Transparent Memory Addressing System Configuration
(Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the SY6845 and the system MPU must be capable of addressing the video display memory. The SY6845 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6845 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6845 and the MPU has immediate access.

- $\phi1/\phi2$ Memory Interleaving

  This method permits both the SY6845 and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when E is low), the SY6845 address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the SY6845 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

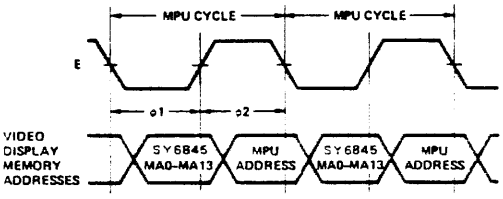


Figure 7. $\phi1/\phi2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6845. In effect, the contention is handled by the SY6845. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi1/\phi2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6845. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi2$. Figure 8 shows the timing.

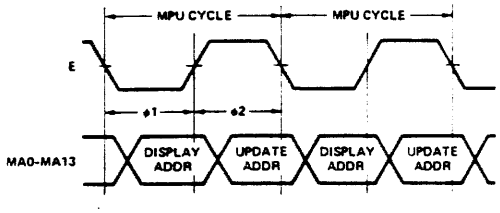


Figure 8. $\phi1/\phi2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in a related Technical Note available from Synertek.

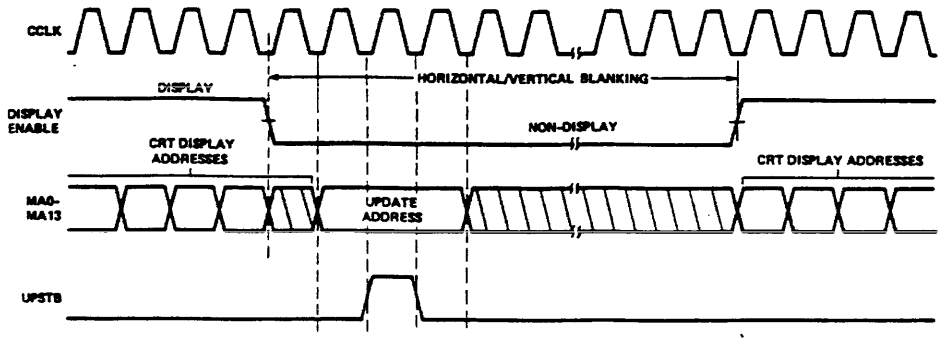


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6845 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

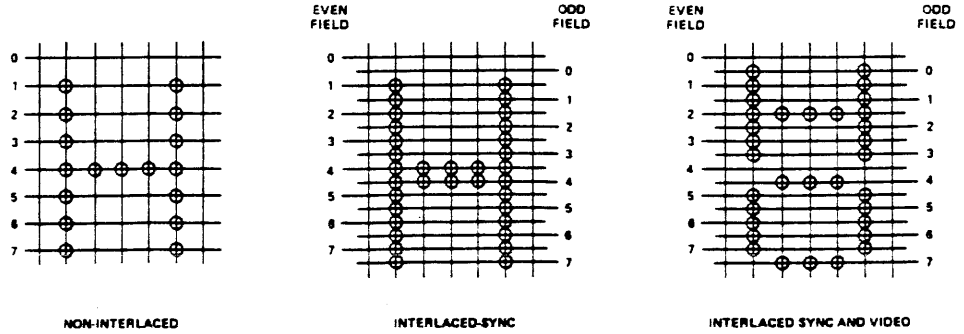


Figure 10. Comparison of Display Modes.

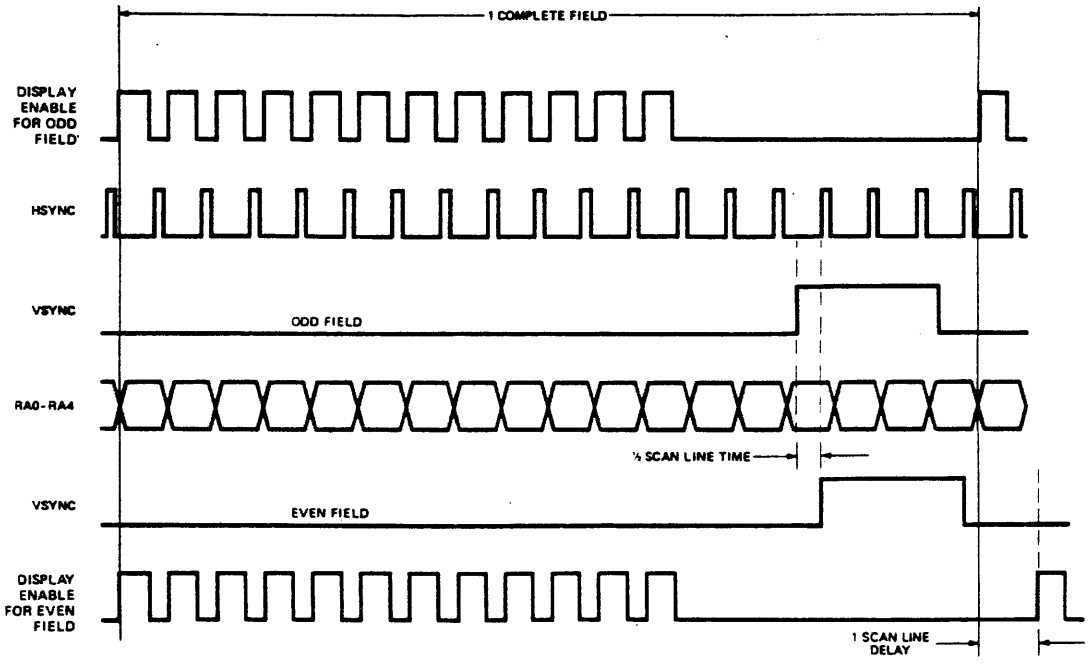


Figure 11. Interlace Sync Mode and Interlace Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

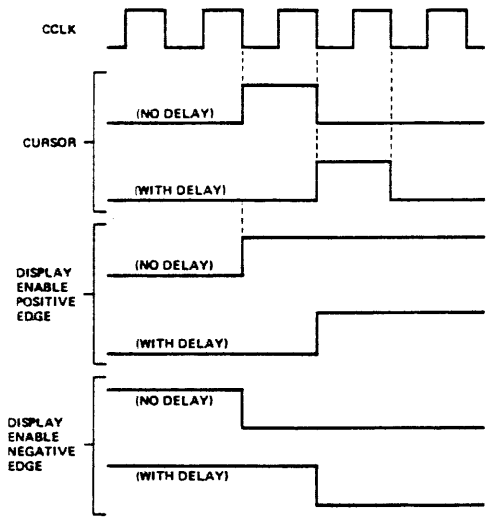


Figure 12. Cursor and Display Enable Skew

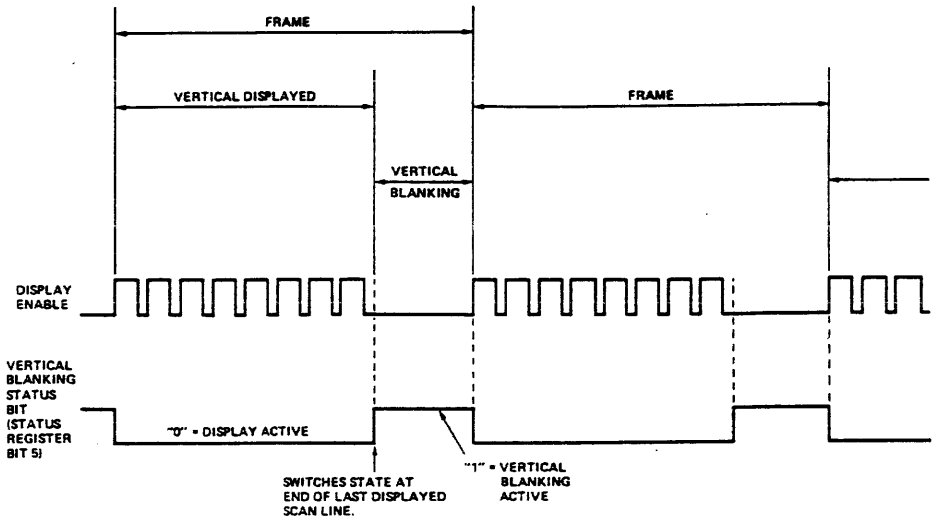


Figure 13. Operation of Vertical Blanking Status Bit

Package Availability 40 Pin Molded DIP

Ordering Information

Part Number	Package	CPU Clock Rate
SYP6845E	Molded DIP	1 MHz
SYP6845EA	Molded DIP	2 MHz
SYP6845EB	Molded DIP	3 MHz

Detailed help in Application Notes 7 and 8 available from Synertek sales offices.

Synertek

CRTC Register Comparison

NON-INTERLACE

REGISTER	SY6845R	MC6845R HD6845R	HD6845S	SY6545-1	SY6845E
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONTAL DISP	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZONTAL AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = (R9H) • X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1
R8 MODE REG BITS 0 AND 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT
BITS 2	–	–	–	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	–	–	–	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	–	–	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	–	–	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	–	–	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	–	–	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	READ/WRITE	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	YES	NO	NO	YES	YES
INTERLACE SYNC					
R0	TOT-1 = ODD OR EVEN	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD OR EVEN
INTERLACE SYNC AND VIDEO					
R4 VERTICAL	TOT-1	TOT-1	TOT-1	TOT/2-1	TOT-1
R6 VERT DISP	TOT	TOT/2	TOT	TOT/2	TOT
R7 VERT SYNC	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL/2	ACTUAL-1
R9 SCAN LINES	TOT-1 ODD/EVEN	TOT-1 ONLY EVEN	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	ODD/EVEN ODD/EVEN	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN
CCLK	2.5 MHz	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz

Appendix C

NOMINAL GAIN AND OFFSET

The following algorithm can used to determine nominal offset and gain.

```
{*
Setting Nominal Offset
*}

offset := nominal_value;
increment := 1;
write_ramp;  {* write a ramp from 0 to 255 in a row
              of pixels *}
feed_back_snapshot;  {* take a snapshot using the
                      feed back channel *}
while (pixel_0 is not the only zero and is a zero)
 begin
   offset := offset + increment;
   write_ramp;
   feed_back_snapshot;
   if (the ramp is written back worse) then
      increment := -increment
 end;


{*
Setting Nominal Gain
*}

gain := nominal_value;
increment := 1;
write_ramp;  {* write a ramp from 0 to 255 in a row of
```

```
              pixels *}
feed_back_snapshot;  {* take a snapshot using the feed
                        back channel *}
while (pixel_255 is not the only value > 253 and is > 253)
 begin
   gain := gain + increment;
   write_ramp;
   feed_back_snapshot;
   if (the ramp is written back worse) then
      increment := -increment
 end;
```

Appendix D

INITIALIZATION EXAMPLE

```
/***************************** init.c ******************************/
/*                                                                 */
/* initialize the VIP                                  BCM         */
/*                                                                 */
/* Program to set all required parameters for operation            */
/*      of VIP-640 and VIP-1024.  Following the initialization     */
/*      the board performs a series of frame grabs at a reduced    */
/*      grab rate.  Note that real-time grabbing can be performed  */
/*      using CONFGR.  Also the green look-up table is inverted    */
/*      demonstrating the pseudo-color capability.  The inverted   */
/*      green LUT results in extreme low intensities being         */
/*      displayed as green and exterme high intensities being      */
/*      displayed as purple (blue + red).  Returning the green     */
/*      LUT to a non-inverted state results in a grey-scale dis-   */
/*      play since all colors are displayed with the same          */
/*      intensity.                                                 */
/*                                                                 */
/*******************************************************************/

#define  V640                   0x01
#define V1024                   0x00
#define MODE                    0x00      /*this is 640
   set to 0x01 for 1024
 */
```

INITIALIZATION EXAMPLE

```
#define MB_PAGE          0x00000000
#define VIP_BASE         0x00200000
#define VRAM_BASE        0x00100000

#define BASE_LEN         0x00010000
#define VRAM_LEN         0x00100000

#define E_VIP_BASE       MB_PAGE + VIP_BASE
#define E_VRAM_BASE      MB_PAGE + VRAM_BASE

#define LUT_LEN          0x800

#define REGLIST          0x0e

unsigned char
*ilut =  E_VIP_BASE + 0x0000,
*rlut =  E_VIP_BASE + 0x0800,
*glut =  E_VIP_BASE + 0x1000,
*blut =  E_VIP_BASE + 0x1800,

*ctrl_0 =       E_VIP_BASE + 0x2800,
*ctrl_1 =       E_VIP_BASE + 0x2900,
*mask   =       E_VIP_BASE + 0x2A00,
*status =       E_VIP_BASE + 0x2B00,
*snpsht =       E_VIP_BASE + 0x2C00,

*crtc_index   = E_VIP_BASE + 0x3000,
*crtc_status  = E_VIP_BASE + 0x3000,
*crtc_data    = E_VIP_BASE + 0x3400,

  *video_gain   = E_VIP_BASE + 0x3800,
*video_offset = E_VIP_BASE + 0x3C00;
```

```
/*    set up CRTC parameter list              */


unsigned char   crtc_1024_parms[REGLIST] =
  { 0x51,0x40,0x42,0x4E,0x1F,0x06,0x1E,0x1E,0x07,0x0f,0,0,0,0 };

unsigned char   crtc_640_parms[REGLIST] =
        { 0x61,0x4f,0x51,0x4f,0x1f,0x06,0x1e,0x1e,0x07,0x0f,0,0,0,0 };



#define SNAP_IT           0         /* dummy value for snapshot  */
#define DEFAULT_GAIN   0x80         /* median value for gain     */
#define DEFAULT_OFFSET 0x80         /* median value for offset   */
#define TRANSPARENT    0x00         /* mask value enabling all bit planes*/
#define RASDIS         0x80         /* value for RAS disable */
#define RASEN          0x00         /* value to enable RAS */
#define EXTERNAL       0x80         /* value for external sync   */
#define INTERNAL       0x00         /* value for internal sync */
#define INPUT_0        0x04         /* input 0, output from FB  */
#define INIT_CTRL_0    0x00         /* LUT map 0, one buffer, no RASDIS */
#define GRABBING       0x02         /* mask for grabbing busy flag   */

#define MAX_ITERS      0x00ff       /* number of snapshots before quitting */
#define MAX_DELAY      0x8000       /* delay before next snapshot   */


/*  ` low byte extraction macro definition      */

#define   LOW(x)       ((unsigned char)(x & 0xff))

/************************** main ***********************************/

main()
{
init();         /*   set up board     */
grab();         /*   do grabbing demo */
}

/*****************************************************************/
```

INITIALIZATION EXAMPLE

```
/************************** init *********************************/


init()
{

/*      make local copies of LUT addresses     */

unsigned char *l_ilut = ilut,
*l_rlut = rlut,
*l_glut = glut,
*l_blut = blut;

unsigned int            loop;


*ctrl_0 = RASDIS;       /*remove RAS and set to internal sync in case
 we were already running  */

*ctrl_1 = INTERNAL;     /*set to internal sync*/

*ctrl_0 = RASEN;        /*continue RAS         */

/*  do CRTC initialization   */

for(loop = 0; loop < REGLIST ; loop++)
{

*crtc_index = LOW(loop);
if(MODE == V640)
     *crtc_data  = crtc_640_parms[loop];
else
        *crtc_data  = crtc_1024_parms[loop];

};
```

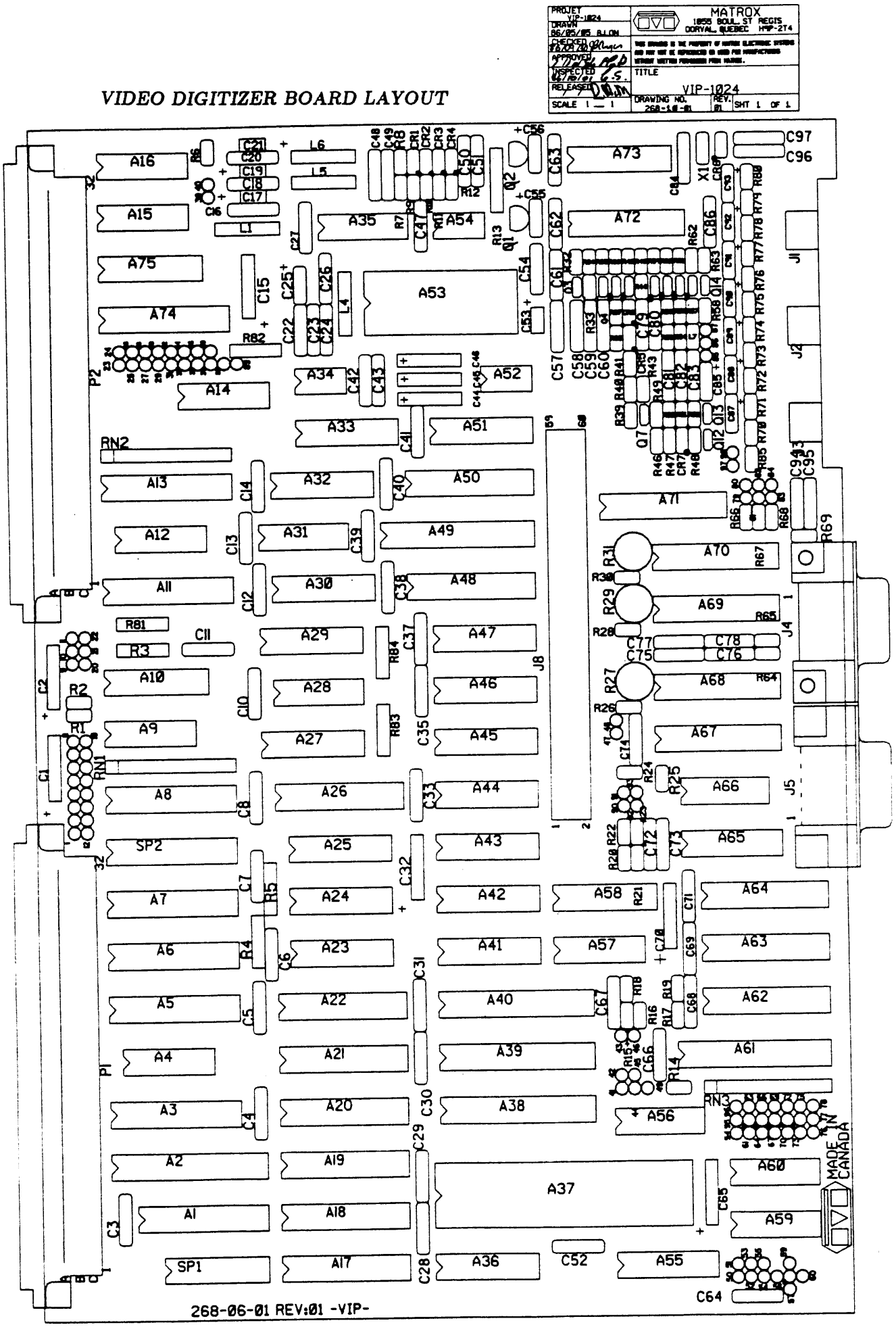
```
/*  do control register  initialization   */


*ctrl_0 = INIT_CTRL_0;

*ctrl_1 = INPUT_0;

*mask   = TRANSPARENT;

*video_gain   = DEFAULT_GAIN;

*video_offset = DEFAULT_OFFSET;


/*  set up the LUTS with ramps   */

for(loop = 0; loop < LUT_LEN ; loop++)
{
*l_rlut++ = LOW(loop);
*l_glut++ = ~LOW(loop);  /*inverted green LUT for demonstration
   of pseudo-color capabilities
 */
*l_blut++ = LOW(loop);
*l_ilut++ = ~LOW(loop);  /*ILUTS loaded with inverve values */
}

}


/*********************************************************************/
```

```
/************************** grab ***********************************/

grab()
{

int loop,loop1;

*ctrl_0 = RASDIS;                    /* disable RAS  */

*ctrl_1 = EXTERNAL;                  /* set to external sync  */

*ctrl_0 = RASEN;                     /*reenable RAS    */

*ctrl_1 = (EXTERNAL | INPUT_0);      /* external sync, input 0  */

for(loop = 0; loop < MAX_ITERS ; loop++)
{

*snpsht = SNAP_IT;                   /* cause a snapshot     */

while(*status & GRABBING);           /*  pause until grab is done   */

for(loop1 = 0; loop1 < MAX_DELAY; loop1++); /* delay before next snapshot
                                                    to give animated effect
    */
}
}

/*****************************************************************/
```

Appendix E

VIDEO DIGITIZER BOARD LAYOUT

VIDEO DIGITIZER BOARD LAYOUT



Appendix F

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