VME-MWS

Hardware Reference Manual

INTEGRATED SOLUTIONS
1140 Ringwood Court
San Jose, California 95131
(408) 943-1902

UNIX is a trademark of Bell Laboratories.

490124 Rev. A

March 1987

Copyright 1987 by Integrated Solutions. All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means (e.g., electronic, mechanical, photocopying, recording) without the prior written permission of Integrated Solutions.

The information in this publication is subject to change without notice.

PREFACE

This manual describes the features, architecture, specifications, configuration, and software interface of the Integrated Solutions VME-MWS.

The manual is divided into four sections:

SECTION 1 - Introduction
A description of the general features and architecture of the VME-MWS.

SECTION 2 - Specifications
This section lists the specifications of the VME-MWS.

SECTION 3 - Configuration
Information regarding the configuration of the VME-MWS is provided.

SECTION 4 - Software Interface
This section describes the VME-MWS software interface.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION 1: INTRODUCTION

1.1 Features

The VME-MWS is a double-wide VME printed circuit board that supports a high-resolution monochrome monitor in an industry standard VMEbus environment. The VME-MWS consists of a frame buffer along with the necessary video display refresh logic.

General features of the VME-MWS include the following:

- Pipelined writes to RAM for low write access time
- Optional interrupt on vertical retrace
- Total display memory — 256 kilobytes (Kbytes)
- Displayable memory size — 1280 x 1024 bits or 1024 x 1440 bits
- Unused video memory available for storing menus, fonts, and display tables

A block diagram of the VME-MWS is shown in Figure 1-1.

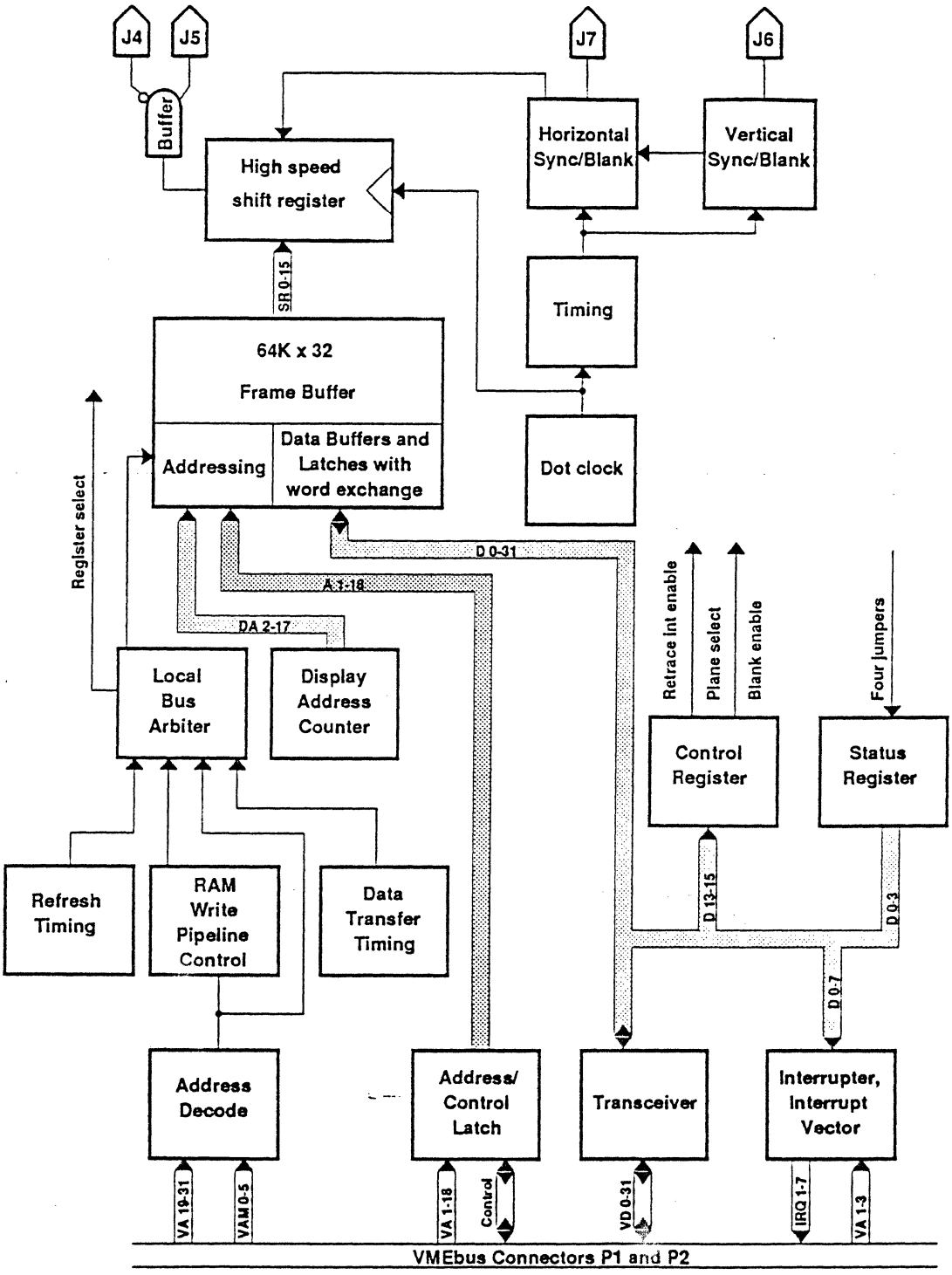


Figure 1-1. VME-MWS Block Diagram

1.2 Architecture

The VME-MWS logic is implemented on a single VME double-wide printed circuit board. Refer to Figure 1-1 for clarification of the function of the blocks discussed in the following subsections.

1.2.1 Address Decode

The address decoding logic recognizes the selected 16- or 32-bit address beginning on any 256 Kbyte boundary.

1.2.2 Address/Control Latch

The address/control latch stores the address and control signal states needed for a pipelined write to RAM. The latch retains data as long as necessary to allow completion of a pipelined write is pending.

1.2.3 Transceiver

The data transceiver is used to buffer data from the VME data lines.

1.2.4 Interrupter

The VME-MWS has a VME interrupter capable of interrupting on any of the seven VME interrupt levels. The interrupt vector used during VME interrupts is software-programmable. Interrupts may be generated at the beginning of vertical retrace.

1.2.5 Refresh Timing

This block requests that the local bus arbiter perform a video RAM refresh cycle every 12.488 microseconds (µs) or less during the active portion of the vertical scan.

1.2.6 Data Transfer Timing

Before a row of video RAM data is displayed, a video RAM data transfer cycle must be performed by the arbiter. The data transfer timing block requests that data transfer cycles occur at the appropriate times during a frame.

1.2.7 RAM Write Pipeline Control

This block is a circuit which causes data and address for RAM writes to be latched, then returns the VME signal DTACK* within 115 nanoseconds (ns) of assertion of the VME data strobes. The latched data is then written to RAM after any active cycles complete.

Pipelining of RAM writes permits the controlling VME master to perform other cycles in parallel with RAM writes, thereby increasing throughput to the RAM.

1.2.8 Local Bus Arbiter

This circuit arbitrates between the RAM write pipeline, the refresh timing circuit, the data transfer timing circuit, and VMEbus masters requesting reads or non-RAM writes. When the arbiter recognizes a request, it turns on the select signal for the addressed on-board slave for the appropriate amount of time. The arbiter prioritizes access requests as shown in Table 1-1, with 1 being the highest priority.

Table 1-1. Arbiter Access Priorities

Priority	Requester
1	Data transfer
2	Refresh
3	RAM write pipeline
4	All other requests

1.2.9 Status Register

The status register allows the user to read the configuration of the on-board jumpers. The maximum status register access time is 1500 ns.

1.2.10 Control Register

The control register permits the user to enable and disable vertical retrace interrupts, and enable and disable video. It also contains the interrupt vector used in VME interrupt acknowledge cycles. The maximum control register access time is less than 1500 ns.

1.2.11 Display Address Counter

The display address counter provides the RAM with refresh and data transfer cycle addresses when requested by the corresponding timing circuits.

1.2.12 Frame Buffer

The frame buffer consists of 256-Kbytes of video RAM with integral shift registers. Data may be accessed from the VME interface simultaneously with data being clocked out of the RAMs shift registers into the high-speed shift register. Average RAM access times from VME data strobe assertion to VME DTACK* assertion are about 94 ns for RAM writes and 400 ns for the 1280 x 1024 and 350 ns for the 1024 x 1440 for RAM reads. The maximum RAM access time is less than 1500 ns.

1.2.13 Timing and Sync Generators

These circuits provide the signals needed to synchronize the video monitor with the video data. They also provide miscellaneous signals needed elsewhere on the card.

1.2.14 VME Interface

The VME-MWS interfaces with the VMEbus as a 24 or 32 address bit, 16 or 32 data bit slave. The VME-MWS host interface logic provides interfacing capability consistent with the VME specification for the following VME-defined functional modules:

- Slave — This is the ability to respond to an access attempt by a master. Determination of an attempt to access is based on recognition of a certain address range and appropriate address modifiers. The VME-MWS responds to a single block of addresses located on any 256 Kbyte boundary.
- Interrupter — The interrupter performs three tasks. It asserts the interrupt request line, supplies a status/ID (vector) byte to the data bus when its request has been acknowledged, and propagates the interrupt acknowledge daisy chain signal. There are seven levels (1-7) of interrupt request priority supported by VME, with Level 7 being the highest. The interrupt priority level of the VME-MWS is jumper selectable from VME interrupt Levels 1 through 7.

For detailed information regarding the VMEbus interface and the associated functional units, refer to the *VMEbus Specification Manual* (Motorola part number MVMEBS/D1).

SECTION 2: SPECIFICATIONS

This section provides performance specifications and operating requirements for the VME-MWS.

2.1 Form Factor

The VME-MWS is a standard double-wide VME board (160mm x 233.33mm).

2.2 Power Requirements

The VME-MWS power requirements are shown in Table 2-1.

Table 2-1. Power Requirements

Voltage	Typical Current	Maximum Current
+5 volts	3.69 amperes (A)	5.85 A
-12 volts	447 milliamperes (mA)	533 mA

2.3 Environmental

The environmental requirements for the VME-MWS are as follows:

Temperatures:

0 to 50 degrees centigrade (operating)
-40 to 65 degrees centigrade (non-operating)

Humidity:

10 to 90 percent (non-condensing)

2.4 System Bus

The VME-MWS interfaces with the VMEbus as defined in *VMEbus Specification Manual* (Motorola part number MVMEBS/D1).

The VME-MWS is attached to the VMEbus via connectors P1 and P2. The pin assignments and signal mnemonics for the VME-MWS P1 and P2 connectors are provided in Tables 2-2 and 2-3, respectively.

Table 2-2. VME-MWS Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*†	D08
2	D01	BCLR*†	D09
3	D02	ACFAIL*†	D10
4	D03	BG0IN*‡	D11
5	D04	BG0OUT*‡	D12
6	D05	BG1IN*‡	D13
7	D06	BG1OUT*‡	D14
8	D07	BG2IN*‡	D15
9	GND	BG2OUT*‡	GND
10	SYSCLK†	BG3IN*‡	SYSFAIL*†
11	GND	BG3OUT*‡	BERR*†
12	DS1*	BR0*†	SYSRESET*
13	DS0*	BR1*†	LWORD*
14	WRITE*	BR2*†	AM5
15	GND	BR3*†	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK†	A17
22	IACKOUT*	SERDAT†	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE

An asterisk following a signal name indicates that the signal is asserted when low.

† VMEbus signals, but no connection on VME-MWS.

‡ Respective *BGIN and *BGOUT signals are tied together.

Table 2-3. VME-MWS Connector P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	n/c†	+5V	n/c
2	n/c	GND	n/c
3	n/c	Reserved‡	n/c
4	n/c	A24	n/c
5	n/c	A25	n/c
6	n/c	A26	n/c
7	n/c	A27	n/c
8	n/c	A28	n/c
9	n/c	A29	n/c
10	n/c	A30	n/c
11	n/c	A31	n/c
12	n/c	GND	n/c
13	n/c	+5V	n/c
14	n/c	D16	n/c
15	n/c	D17	n/c
16	n/c	D18	n/c
17	n/c	D19	n/c
18	n/c	D20	n/c
19	n/c	D21	n/c
20	n/c	D22	n/c
21	n/c	D23	n/c
22	n/c	GND	n/c
23	n/c	D24	n/c
24	n/c	D25	n/c
25	n/c	D26	n/c
26	n/c	D27	n/c
27	n/c	D28	n/c
28	n/c	D29	n/c
29	n/c	D30	n/c
30	n/c	D31	n/c
31	n/c	GND	n/c
32	n/c	+5V	n/c

2.5 Video Interface

The signal interface to the high-resolution monitor is provided by coaxial cables attached to the board connectors J4, J5, J6, and J7. The board connector J4 is unused on the 1280 x 1024. The coaxial cables are numbered J4, J5, J6, and J7. The proper connection sequence is shown in Figure 2-1 for the 1280 x 1024 and in Figure 2-2 for the 1024 x 1440.

† All pins marked "n/c" are not connected on the VME-MWS.

‡ Reserved for future use.

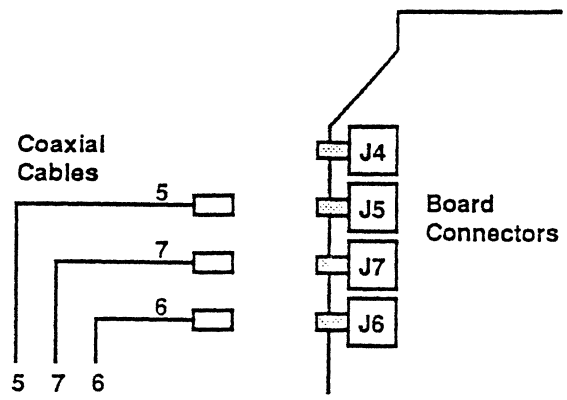


Figure 2-1. Video Cable Connections for 1280 x 1024

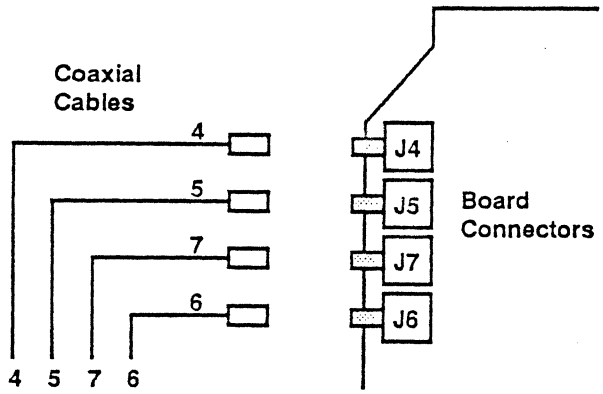


Figure 2-2. Video Cable Connections for 1024 x 1440

The video interface timing specifications are given in Table 2-4 and the Monitor Interface Signals are listed in Table 2-5.

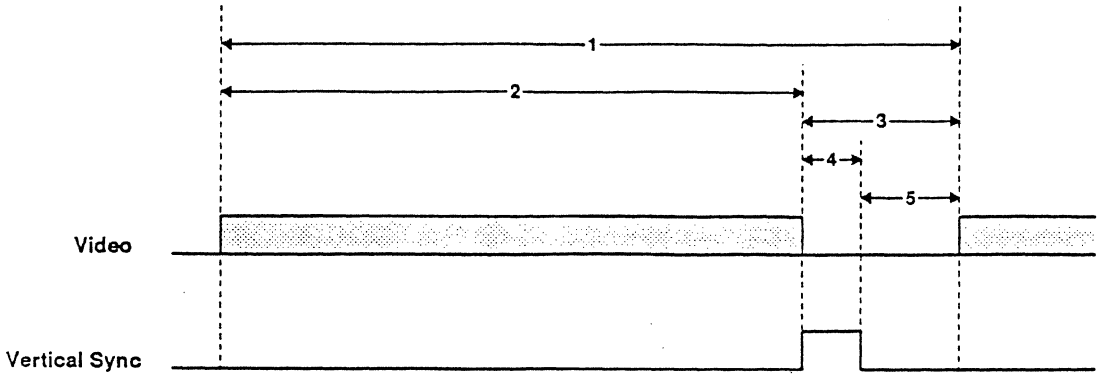
Table 2-4. Video Interface Timing

Description	1280 x 1024	1024 x 1440
Screen Refresh	63.0 Hz	66.0 Hz
Vertical Retrace	682.3 µs	749.3 µs
Horizontal Scan Time	14.83 µs (67.4 KHz)	9.99 µs (100.0 KHz)
Horizontal Retrace	3.845 µs	3.33 µs
Pixel Cell Time	8.6 ns	6.5 ns

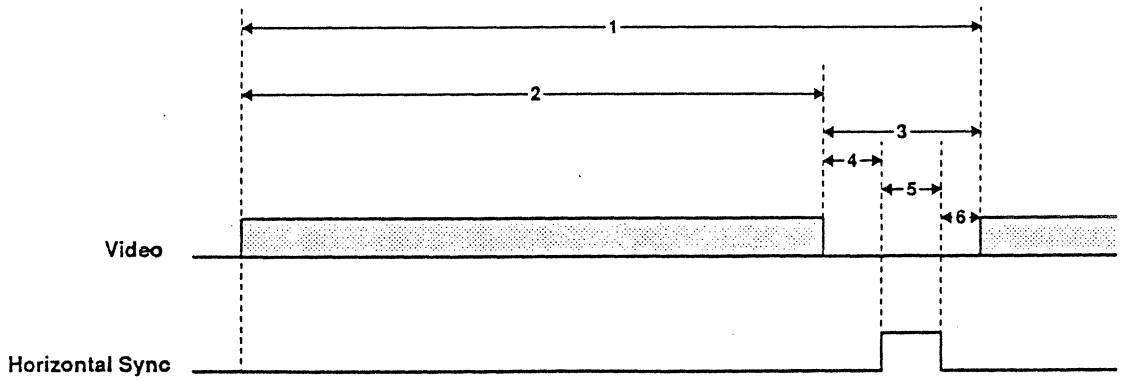
Table 2-5. Monitor Interface Signals

Signal	1280 x 1024	1024 x 1440
J4	N/A	Negative Differential ECL Video
J5	Positive ECL video	Positive Differential ECL Video
J6	Positive TTL Vertical	Positive TTL Vertical
J7	Positive TTL Horizontal	Positive TTL Horizontal

Timing diagrams for the VME-MWS are shown in Figure 2-3.



Vertical Timing Parameters			
		1280 x 1024	1024 x 1440
1.	Vertical Frame Time	15.871 ms	15.136 µs
2.	Vertical Active	15.189 ms	14.387 ms
3.	Vertical Blanking	682.300 µs	749.317 µs
4.	Vertical Sync	237.322 µs	159.854 µs
5.	Vertical Back Porch	444.979 µs	589.463 µs



Horizontal Timing Parameters			
		1280 x 1024	1024 x 1440
1.	Horizontal Scan Time	14.833 µs	9.991 µs
2.	Horizontal Active	10.987 µs	6.661 µs
3.	Horizontal Blanking	3.845 µs	3.330 µs
4.	Horizontal Front Porch	0.824 µs	0.000 µs
5.	Horizontal Sync	1.099 µs	1.353 µs
6.	Horizontal Back Porch	1.923 µs	1.977 µs

Figure 2-3. Video Signal Timing Diagrams

In Figure 2-3, the vertical sync pulse occurs immediately after the vertical active period. There is no

vertical front porch.

2.6 Display Memory

The board provides 256 Kbytes of memory. See Section 4 for more detailed information regarding the display memory address map.

2.7 Addressing

The VME-MWS base address may be positioned on any 256-Kbyte boundary. Refer to Section 3 for address mapping details and the associated jumper configurations.

2.8 VME Specification

The VME-MWS's features are listed in this section, in accordance with the standards specified in the *VMEbus Specification Manual.*

Master Data Transfer Options
N/A

Slave Data Transfer Options
A24 or A32:D16 or D32

Arbiter Options
N/A

Requester Options
N/A

Interrupt Handler Options
N/A

Interrupter Options
Any one of I(1), I(2), I(3), I(4), I(5), I(6), or I(7) (STAT)

Environmental Options
Operating Temperature: 0° C to 50° C
Maximum Operating Humidity: 90% (non-condensing)

Power Options
5.85 A Max (3.69 A typ) at +5 VDC
533 mA Max (447 mA typ) at -12 VDC

Physical Configuration Options
EXP

SECTION 3: CONFIGURATION

This section discusses the various jumper configuration options for the VME-MWS. The default jumpers for the VME-MWS are presented in **boldface** type.

3.1 Base Address Jumpers

Each address jumper on the board corresponds to a VME address bit or an address modifier bit. If a jumper is absent in a given position, the corresponding address bit or address modifier bit is recognized as a one. If a jumper is present, the corresponding address bit or address modifier bit is recognized as a zero. Table 3-1 describes the address bit/jumper correspondences.

Table 3-1. Base Address Jumpers

Jumpers	Address Bit	Address Modifier Bit
W27	31	
W29	30	
W30	29	
W28	28	
W25	27	
W23	26	
W24	25	
W26	24	
W49	23	
W47	22	
W44	21	
W42	20	
W43	19	
W50	18	
W48		3
W45		4
W41		5

The VME-MWS responds to either 32- or 24-bit addresses. It responds only to addresses with AM1 and AM0 equal to "01" or "10," and ignores the state of AM2. When AM5 is equal to one, standard 24-bit addresses are recognized. When AM5 is equal to zero, extended 32-bit addresses are recognized. It responds to the address modifiers shown in Table 3-2.

Table 3-2. Address Modifiers

Jumper States		Hexadecimal Codes and Functions
W41	W45	
Open	Open	0x39 (Standard Non-privileged Data Access) or 0x3A (Standard Non-privileged Program Access) or 0x3D (Standard Supervisory Data Access) or 0x3E (Standard Supervisory Program Access)
Jumper	Jumper	0x09 (Extended Non-privileged Data Access) or 0x0A (Extended Non-privileged Program Access) or 0x0D (Extended Supervisory Data Access) or 0x0E (Extended Supervisory Program Access)

3.2 Default Address Configuration

Default Integrated Solutions' UNIX configurations have the VME-MWS residing at address 0xE00000 in 24-bit Standard Supervisory Data address space.

The default address jumpering is listed in Table 3-3.

Table 3-3. Default Address Configuration

Jumper	Address Bit	Address Modifier Bit	Jumper State
W27	31		Jumper
W29	30		Jumper
W30	29		Jumper
W28	28		Jumper
W25	27		Jumper
W23	26		Jumper
W24	25		Jumper
W26	24		Jumper
W49	23		Open
W47	22		Open
W44	21		Open
W42	20		Jumper
W43	19		Jumper
W50	18		Jumper
W48		3	Open
W45		4	Open
W41		5	Open

Note that the states of jumpers W23-W30 are "don't cares," since the board is accessed using 24-bit addresses, and address bits 24 through 31 are ignored.

3.3 Interrupt Request Level

The VME-MWS is capable of generating interrupt requests at VME priority Levels 1 through 7. Selection of the interrupt request level is a function of jumpers. Table 3-4 gives the jumpering configurations for the various interrupt request levels.

Table 3-4. Interrupt Request Level Selection †

Interrupt Level	W31	W32	W33	W34	W35	W36	W37	W51	W22	W46
1	J	O	O	O	O	O	O	J	J	O
2	O	J	O	O	O	O	O	J	O	J
3	O	O	J	O	O	O	O	J	O	O
4	O	O	O	J	O	O	O	O	J	J
5	O	O	O	O	J	O	O	O	J	O
6	O	O	O	O	O	J	O	O	O	J
7	O	O	O	O	O	O	J	O	O	O

† "O" represents open; "J" represents jumpered

3.4 Other Jumpers

Any jumpers not described in this section are factory set and should not be changed. Installed jumpers include **E8A** and **E9B**.

Note that jumpers **W23-W30** are installed spares.

3.5 Display Configuration

Jumpers, along with some programmable integrated circuits on the board, determine the display format as ordered by the customer. Table 3-5 lists the integrated circuit part numbers, RAM speeds, and jumpers which are required for each display format.

Table 3-5. Display Configuration

Display Format	IC U8 Part Number	IC U9 Part Number	IC U4 Part Number	RAM Speed	Jumpers to Install
1280 x 1024	750129	750128	750134	150 ns or 120 ns	W1, W3, W4, W5, W7, W9, W10, W12, W16, W20, W39, E1B, E2B, E3B, E4A, E5B, E6B, E7A
1024 x 1440	750133	750132	750144	120 ns	W1, W2, W3, W4, W6, W7, W9, W10, W11, W12, W13, W14, W19, W40, E1A, E2A, E3A, E4B, E5B, E6B

3.6 Jumper Locations

Figures 3-1 and 3-2 locate the jumpers on the VME-MWS 1280 x 1024 and 1024 x 1440, respectively. The default jumpers are represented by a shaded rectangle.

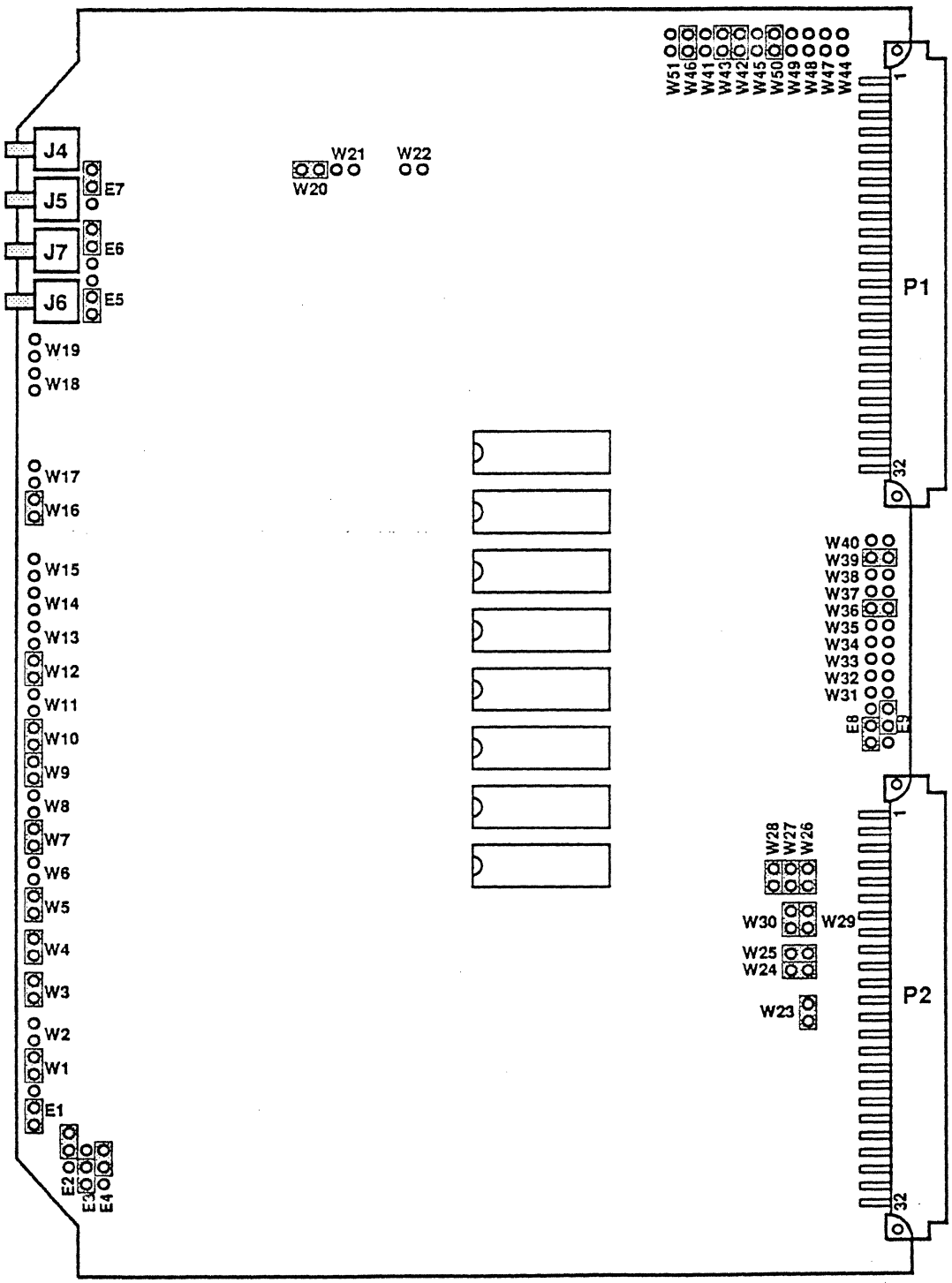


Figure 3-1. VME-MWS 1280 x 1024 Jumper Locations

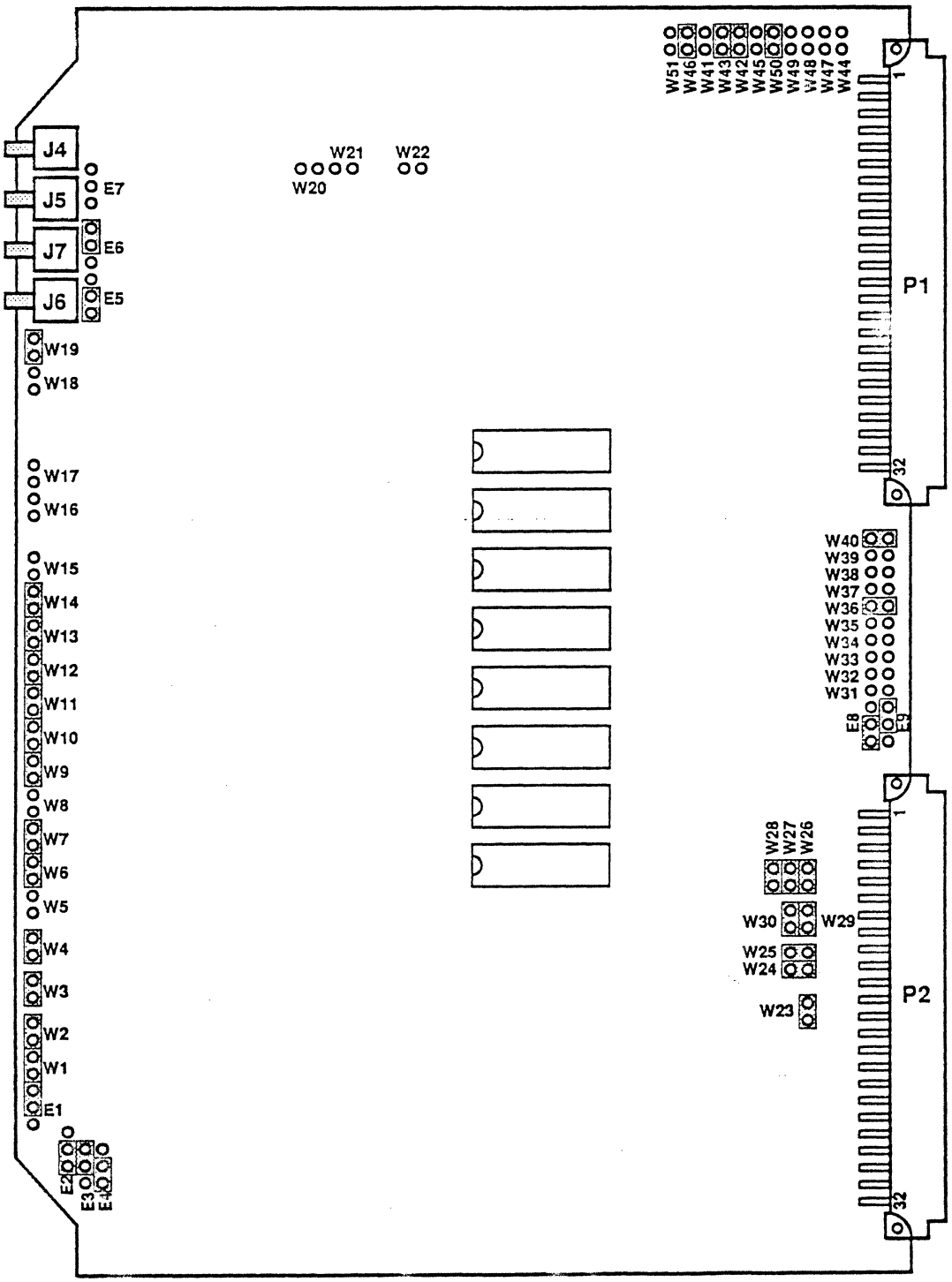


Figure 3-2. VME-MWS 1024 x 1440 Jumper Locations

SECTION 4: SOFTWARE INTERFACE

This section provides information regarding the software interface to the VME-MWS. Specifically, display memory and the control and status registers are discussed in the subsections that follow.

4.1 Address Map

The address map of the VME-MWS begins at the base address of the card. The display memory is 262080 bytes long (256 Kbytes - 64), followed by a 64-byte control space, making a total occupied address space of 256 Kbytes. It will not respond to addresses outside of this 256-Kbyte range.

Table 4-1 summarizes the layout of VME-MWS address map.

Table 4-1. VME-MWS Address Map

Display Format	VME Address (Hexadecimal)	Function
Any	Base Address + 0	Displayed Portion
1280 x 1024	Base Address + 28000	Non-displayed Portion
1024 x 1440	Base Address + 2D000	Non-displayed Portion
Any	Base Address + 3FFC0	Control Space

4.1.1 Display Memory

Display memory consists of a displayed part and a non-displayed part. The displayed part begins at the lowest address. It is

$$\frac{1280 \text{ pixels/line} \times 1024 \text{ lines}}{8 \text{ pixels/byte}} = 163840 \text{ bytes (1280 x 1024 display)}$$

$$\frac{1024 \text{ pixels/line} \times 1440 \text{ lines}}{8 \text{ pixels/byte}} = 184320 \text{ bytes (1024 x 1440 display)}$$

in length. The non-displayed portion of display memory may be used for regular data/program storage purposes, although this is recommended only if faster memory is not available for data/program storage.

Display memory supports byte, word, and longword accesses from the VMEbus. Read-modify-write cycles are also supported.

Mapping from linear address space to the two-dimensional screen address space requires that the user know the pitch of the video system. Pitch is defined as the offset between vertically adjacent words on the screen. For the display resolution of 1280 horizontal pixels, the pitch is 80 words (1280 + 16 = 80) or 160 bytes. Pitch values for the various resolutions are listed in Table 4-2.

Table 4-2. VME-MWS Pitch Values

Display Format	Pitch
1280 x 1024	80 words
1024 x 1440	64 words

4.1.2 Control Space

The 64-byte control space, located as described above, contains the control and status registers. The map of the control space is in Table 4-3.

Table 4-3. Control Space Layout

Byte Offset (Hexadecimal)	Function
0-1	Control/Status Register
2-63	Reserved — do not access

All accesses of the control and status registers **must** be word (16 bit) accesses.

4.1.3 Control Register

At the beginning of control space is a 16-bit write-only register, the Control Register. The bit layout of that register is shown in Table 4-4. The Control Register is write-only, and all writes **must** be word (16 bit) writes.

Table 4-4. Control Register (CR)

Bit Number	Active state	Function
0	N/A	Interrupt vector bit 0
1	N/A	Interrupt vector bit 1
2	N/A	Interrupt vector bit 2
3	N/A	Interrupt vector bit 3
4	N/A	Interrupt vector bit 4
5	N/A	Interrupt vector bit 5
6	N/A	Interrupt vector bit 6
7	N/A	Interrupt vector bit 7
8	1	Vertical Retrace interrupt enable
9	1	Blank enable
10	-	Not used - always write one
11-15	-	Not used - always write zero

On receipt of the VME signal SYSRESET* (usually on power up), bits 8 and 9 of CR are set to their inactive (0) states. The interrupt vector is unaffected by SYSRESET* and has an indefinite state on power up.

Bits 0 through 7 constitute the interrupt vector to be used during a VME interrupt acknowledge cycle.

Bit 8 enables vertical retrace interrupts when set to one.

Bit 9 turns off the video output of the card when set to one.

Bit 10 must always be written with a one.

4.1.4 Status Register

The Status Register is a four-bit read-only register. The bit layout of that register is shown in Table 4-5. The Status Register is read-only, and all reads **must** be word (16 bit) reads.

Table 4-5. Status Register (SR)

Bit Number	Active state	Function
0	0	State of Jumper W39
1	0	State of Jumper W40
2	0	State of Jumper W38
3	0	State of Jumper W18
4-15	-	Indeterminate - mask off after reading

Bits 0 through 3 return the state of the four software jumpers, with a zero representing the presence of a jumper.

The states of SR bits 0-3 identify a particular board configuration. Table 4-6 lists the SR values for each configuration supported.

Table 4-6. SR Values

Configuration	SR bits 0-3 (hexadecimal)
1280 x 1024	E
1024 x 1440	D

Integrated Solutions

DOCUMENTATION COMMENTS

Please take a minute to comment on the accuracy and completeness of this manual. Your assistance will help us to better identify and respond to specific documentation issues. If necessary, you may attach an additional page with comments. Thank you in advance for your cooperation.

Manual Title: *VME-MWS Hardware Reference Manual*	Part Number: *490124 Rev. A*

Name: _____ Title: _____

Company: _____ Phone: ( ) _____

Address: _____

City: _____ State: _____ Zip Code: _____

1. Please rate this manual for the following:

	Poor	Fair	Good	Excellent
Clarity	☐	☐	☐	☐
Completeness	☐	☐	☐	☐
Organization	☐	☐	☐	☐
Technical Content/Accuracy	☐	☐	☐	☐
Readability	☐	☐	☐	☐

Please comment: _____

_____

2. Does this manual contain enough examples and figures?

Yes ☐ No ☐

Please comment: _____

_____

3. Is any information missing from this manual?

Yes ☐ No ☐

Please comment: _____

_____

4. Is this manual adequate for your purposes?

Yes ☐ No ☐

Please comment on how this manual can be improved: _____

_____

_____

_____

_____

_____

_____

i Down First Fold Down

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

First-Class Mail Permit No. 7628 San Jose, California 95131

Postage will be paid by addressee

Integrated Solutions

ATTN: Technical Publications Manager
1140 Ringwood Court
San Jose, CA 95131

d Up Second Fold Up

Staple Here