VME-QIC2/R SPECIFICATION/CONFIGURATION SUMMARY

(490005 Rev. B)

This paper provides the specification and configuration information that you may require upon receipt of your Integrated Solutions' VME-QIC2/R tape controller board (see Figure 1-1).

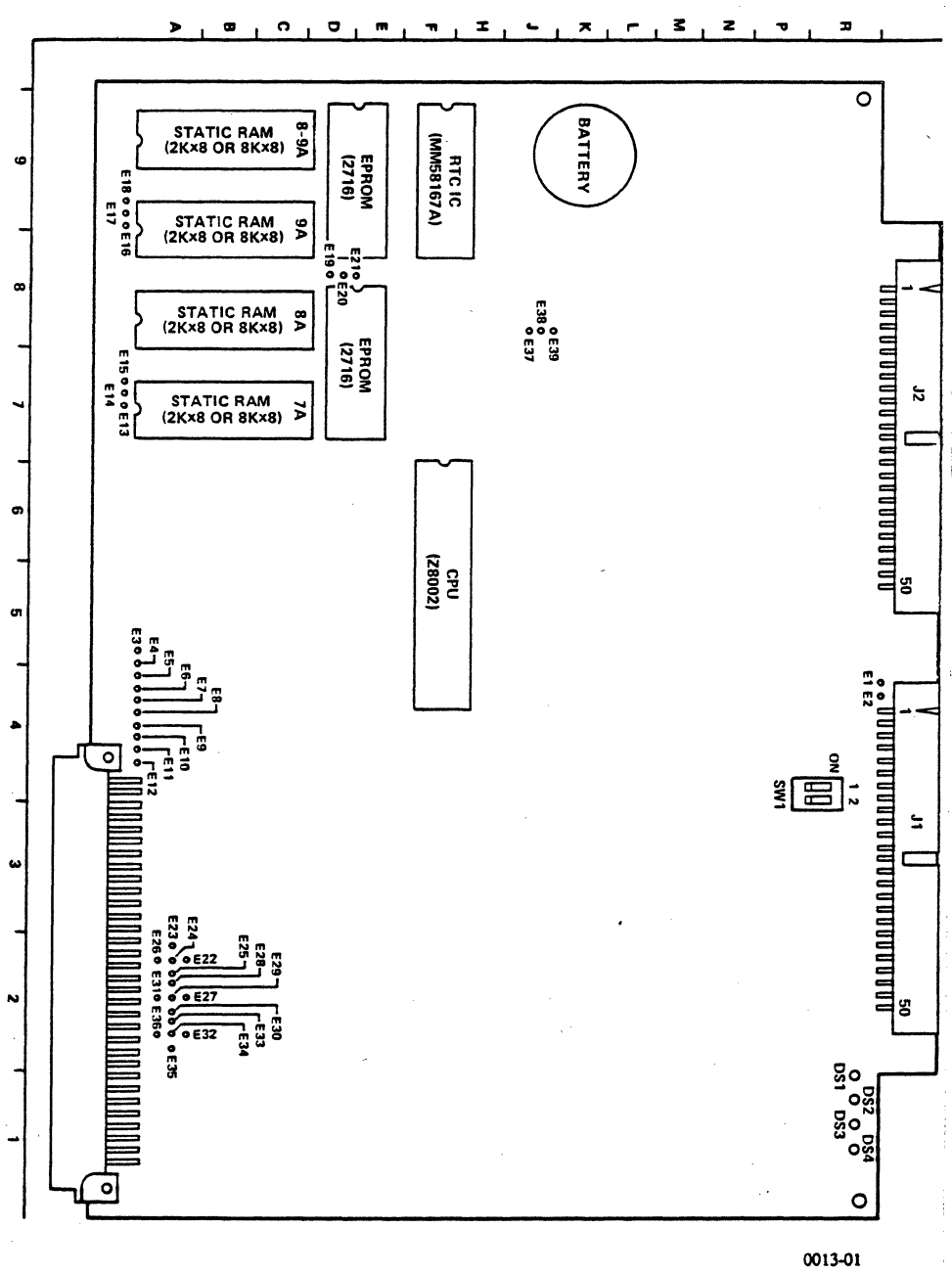

Figure 1-1. VME-QIC2/R Board Layout

SPECIFICATIONS

Form Factor

The VME-QIC2/R form factor is standard double-sized VME - 160mm x 233.33mm.

Compatibility

The VME-QIC2/R controller board supports all standard QIC02 interface drives. Tape capacity is up to 100 megabytes per 600-foot tape cartridge when using twelve track QIC02 standard interface drives. The tape drive supplied by Integrated Solutions is a nine track quarter-inch cartridge tape unit with a tape capacity up to 75 megabytes.

NOTE

The terms VME-QIC2/R and QIC02 are used throughout this paper. VME-QIC2/R is the name of the Integrated Solutions' cartridge tape controller. QIC02 is a streaming cartridge tape unit interface specification and is used to designate those units that meet the specification.

The VME-QIC2/R plugs into a VME bus based system and supports a QIC02-compatible quarter-inch cartridge tape drive. The VME-QIC2/R interfaces with the VME bus as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1. Table 1-1 provides the pin assignments and signal mnemonics for the VME-QIC2/R VME bus connector, P1.

The VME-QIC2/R controller attaches to the quarter-inch cartridge tape drive via a 50-pin connector, J1. Table 1-2 provides the J1 connector pin assignments.

Addressing

The VME-QIC2/R uses three one-word control registers. These registers may be located as the first three words on any sixteen-word boundary within the address range of FFF000 (hex) to FFFFF0 (hex). The first two words function as tape controller device registers, while the third word is the control register for the real time clock.

Address Modifiers

The VME-QIC2/R responds to all standard supervisory and non-privileged accesses. It does not respond to short I/O or extended accesses.

Tape Controller Interface

With regard to programming interface, the VME-QIC2/R corresponds closely to the DEC TS11 interface. Consequently, UNIX or other operating system TS11 drivers can be easily modified for use with the VME-QIC2/R. The real time clock register is defined to handle all commands and data necessary for implementing the clock function.

Interrupt Vector

The VME-QIC2/R can request an interrupt at VME Interrupt Levels 4, 5, 6, or 7. The priority level is selectable (see "Configuration").

Transfer Rate

The VME-QIC2/R controller supports 30 or 90 inch per second QIC02-compatible tape units. The effective data transfer rates for these tape drives are provided in Table 1-3.

Real Time Clock

The Real Time Clock (RTC) consists of a CMOS real time clock, calendar clock chip, rechargeable NICAD battery, micropower crystal oscillator, and power failure detection and cutover circuits. In addition, a trickle charge circuit continuously charges the battery while the power is on. A fully charged battery will reliably power the clock for approximately 500 hours.

Table 1-1. VME Bus Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	VMED0	BBUSY*	VMED8
2	VMED1	BCLR*†	VMED9
3	VMED2	ACFAIL*†	VMED10
4	VMED3	BG0IN*	VMED11
5	VMED4	BG0OUT*	VMED12
6	VMED5	BG1IN*	VMED13
7	VMED6	BG1OUT*	VMED14
8	VMED7	BG2IN*	VMED15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	VMEBERR*
12	VMEDS1*	BR0*	SYSRESET*
13	VMEDS0*	BR1*	LWRD*†
14	VMEWR*	BR2*	VMEAM5
15	GND	BR3*	VADD23
16	VMEDTACK*	VMEAM0†	VADD22
17	GND	VMEAM1†	VADD21
18	VMEAS*	VMEAM2†	VADD20
19	GND	VMEAM3	VADD19
20	VMEIACK*	GND	VADD18
21	IACKIN*	SERCLK†	VADD17
22	IACKOUT*	SERDAT†	VADD16
23	VMEAM4	GND	VADD15
24	VADD7	IRQ7*	VADD14
25	VADD6	IRQ6*	VADD13
26	VADD5	IRQ5*	VADD12
27	VADD4	IRQ4*	VADD11
28	VADD3	IRQ3*†	VADD10
29	VADD2	IRQ2*†	VADD9
30	VADD1	IRQ1*†	VADD8
31	-12V†	+5V STDBY†	+12V
32	+5V	+5V	+5V

† VME bus signals, but no connection on VME-QIC2/R board.

Table 1-2. I/O Port Connector J1 Pin Assignments†

Pin Number	Signal Mnemonic	Signal Name
2	Spare	(not used)
4	Spare	(not used)
6	Spare	(not used)
8	Spare	(not used)
10	HBP*	Host Bus Parity (not used)
12	DB7	Data Bus 7
14	DB6	Data Bus 6
16	DB5	Data Bus 5
18	DB4	Data Bus 4
20	DB3	Data Bus 3
22	DB2	Data Bus 2
24	DB1	Data Bus 1
26	DB0	Data Bus 0
28	ONL*	On Line
30	REQ*	Request
32	QICRES*	Controller Reset
34	XFER*	Transfer
36	ACK*	Acknowledge
38	RDY*	Ready
40	EXC*	Exception
42	DIR*	Direction
44	Spare	(not used)
46	Spare	(not used)
48	Spare	(not used)
50	Spare	(not used)

Table 1-3. Data Transfer Rates

Tape Speed	Disk Image Backup Rate††	File by File Transfer Rate††
90 ips	85Kbytes	40Kbytes
30 ips	28Kbytes	15Kbytes

† With the exception of Pin 1 all odd pins on the J1 connector are connected to ground.

†† The data transfer rate is a function of many variables including the backup program, disk access time, file system structure on the disk, memory speed, and the efficiency of the disk controller. Consequently, these numbers represent only general approximations. In the case of the disk image backup, it is assumed that the disk controller can provide continuous data at a rate fast enough to maintain these backup rates.

Diagnostics

The VME-QIC2/R board has automatic self test at power on with LED indication upon successful completion.

Electrical Requirements

The VME-QIC2/R electrical requirements are as follows

+5 volts at 2.6 amps
+12 volts at 0.1 amp

Environmental Requirements

The VME-QIC2/R environmental requirements are as follows

Temperature:

0°C to 50°C (operating)
-40°C to 65°C (non-operating)

Humidity:

10% to 95% (non-condensing)

CONFIGURATION

Jumper Positions E1 and E2

This position must be set to open (no jumper installed).

Address Jumpers (E3-E12)

Jumpers E3 through E12 set the VME-QIC2/R address location on the VME bus within the address range of FFF000 (hex) and FFFFF0 (hex). (Figure 1-2 shows the address bits that are selectable within the 24-bit address.) Jumper post E12 is tied to ground, while E3 is tied to +5 volts. Positions E4 through E11 must be jumpered to either E3 or E12 to produce a logical 1 or 0, respectively. E4 corresponds to Bit 4, E5 to Bit 5, etc. For the factory default setting (FFF550 hex), posts E4, E6, E8, and E10 are tied to E3 (+5 volts), while posts E5, E7, E9, and E11 are tied to E12 (ground).

Bits 23 - 12	Bits 11 - 4	Bits 3 - 0
1 1 1 1 1 1 1 1 1 1 1 1	X X X X X X X X	0 0 0 0

Note: X = logic level jumper selectable

Figure 1-2. Jumper Selectable Address Bits

Static RAM Socket Configuration (E13-E18)

Jumpers E13 through E18 configure the static RAM sockets for the 8K x 8 static RAMs. The jumper setting is shown in Table 1-4.

Table 1-4. Static RAM Jumpers

RAM	Jumper Setting
8K x 8	E13 to E14 E16 to E17

EPROM Socket Configuration (E19-E21)

Jumpers E19 through E21 configure the EPROM sockets to accommodate either 2K x 8 (2716) or 4K x 8 (2732) EPROMs. Integrated Solutions' firmware is resident on 2K x 8 EPROMs (2716) so the factory setting is E20 to E21. The jumper settings are provided in Table 1-5.

Table 1-5. EPROM Jumpers

EPROM	Jumper Setting
2716	E20 to E21
2732	E19 to E20

VME Bus Requestor Jumpers (E22-E36)

Jumpers E22 through E36 control the VME bus request/grant level of the VME-QIC2/R requestor. There are four levels of bus request/grant, Levels 0 through 3. The jumper configurations for each request/grant level are shown in Table 1-6. The factory default setting is for Level 3.

Table 1-6. Bus Request/Grant Level Jumper Settings

Level 0	Level 1	Level 2	Level 3
E22 to E24	E25 to E24	E26 to E24	E23 to E24
E33 to E28	E33 to E28	E33 to E28	E33 to E34
E36 to E31	E36 to E31	E36 to E34	E36 to E31
E35 to E30	E35 to E34	E31 to E29	E28 to E29
E32 to E34	E30 to E29	E35 to E30	E35 to E30
E27 to E29	E32 to E27	E32 to E27	E32 to E27

Jumper Positions (E37-E39)

These jumper positions are factory set (E37 to E38) and must remain in this configuration.

Switch SW-1 Configuration

SW-1 controls the DMA burst size on the VME bus. If the switch is off, DMA bursts occur at 256 words per burst, which gives very efficient bus utilization. However, this DMA burst size may cause problems with some other non-buffered DMA devices on the VME bus, which may require the bus more frequently than every 150 microseconds. If SW-1 is on, DMA bursts occur at 16 words per burst.

Switch SW-2 Configuration

SW-2 controls the interrupt request level. The VME-QIC2/R can request an interrupt at interrupt Levels 4, 5, 6, or 7 of the seven interrupt levels that are implemented on the VME bus. If SW-2 is off, the default level, Level 4, is used. If SW-2 is on, the level is taken from the low order two bits of Location 0 of the low order PROM. These bits are default programmed for Level 5 at the factory, but they can be changed by the user to either Level 6 or 7 by reprogramming the EPROM.

LED DS1

DS1 is under program control. DS1 can mean any one of the five following things depending on its signal pattern:

1. After a power up when the tape unit is idle, DS1 flashes with a 1/2-second on, 1/2-second off signal pattern.
2. When the tape unit is rewinding the tape or executing the tape retension command, DS1 flashes with a faster rate of 1/5-second on, 1/5-second off signal pattern.
3. When the tape is in the Write sequence, DS1 is on continuously.
4. When the tape is in the Read sequence, DS1 is off continuously.
5. When the tape controller has detected a fatal error condition either at power on or while operating, it continuously flashes a fatal error signal pattern. The patterns (a combination of short and long flashes) and their corresponding definitions are provided in Table 1-7. The tape controller remains in the fatal error status until a Reset command is issued to the tape unit.

Table 1-7. DS1 Fatal Error Signal Patterns

Code	LED Failure Indication	Failure Location
0000	short, short, short, short	Memory Bank 0 (RAMs at 7A, and 8/9A)
0001	short, short, short, long	Memory Bank 1 (RAMs at 8A, and 9A)
0011	short, short, long, long	No RAM in Bank 0.
0101	short, long, short, long	The VME-QIC2/R is active but there are no drives attached to it. The controller will never come ready in this case.
0110	short, long, long, short	An error occurred in the tape unit on a Write File Mark command
0111	short, long, long, long	A sequencing error occured while reading records off the tape; a tape record was encountered that was not the same length as the 512-byte header block indicated it was.
1000	long, short, short, short	A sequencing error on reads; the first tape block in a logical record was not a valid header block.
1100	long, long, short, short	A full or empty queue problem; an attempt was made to read from an empty queue or write to a full queue.