Publication Number H29-335R06

METRIC

M46-416
REMOVABLE CARTRIDGE DISC SYSTEM
MAINTENANCE MANUAL

Consists of:

Installation Specification	02-314R01A20
Maintenance Specification	02-314R02A21
Information Drawing	02-314D12
Schematic	02-314R07D08
Component Locator	35-438M01R12E03

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PAGE REVISION STATUS SHEET

PUBLICATION NUMBER H29-335
TITLE M46-416 Removable Cartridge Disc System Maintenance Manual
REVISION R06 DATE May 1979

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/i	R05	10/78						
02-314A20 Installation Specification 1-7/8	R01	1/74						
02-314A21 Maintenance Specification 1	R02	10/78						
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PREFACE

This manual contains an installation specification and a maintenance specification for the M46-416 Removable Cartridge Disc System. The installation specification provides configuration, unpacking, and mounting information and power requirements. The maintenance specification provides a block diagram, a functional schematic analysis, device address strapping details, adjustment procedures, and a mnemonics list.

For additional information, refer to the following publication:

29-337 Diablo 44 Disc Maintenance Manual

METRIC

M46-416
REMOVABLE CARTRIDGE DISC SYSTEM
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides system installation and system configuration information for the Perkin-Elmer Removable Cartridge Disc System.

The following is the relationship between Product Numbers and Part Numbers for the hardware components required for different configurations of the Removable Cartridge Disc System.

Marketing Number	Part Number	Contents	Description
M46-416	02-314	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
		1 each 27-056	Cartridge
		1 each 27-055	Series 44 Disc
M46-418	02-316	1 each 27-055	Series 44 Disc
		1 each 17-279	Expansion Cable
		1 each 27-056	Cartridge
M46-421	02-318	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
M46-417	02-315	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
		1 each 27-056	Cartridge
		1 each 27-055	Series 44 Disc
M46-419	02-317	1 each 27-055	Series 44 Disc
		1 each 27-056	Cartridge
		1 each 17-279	Expansion Cable

The Removable Cartridge Disc System consists of a single 381mm (15") printed circuit controller (Part Number 35-438F01M01R02), interconnecting cables (17-278 or 17-279), Power Supply (34-021), and one to four disc drives. The dimensions and weights of the disc drive and the Power Supply are shown in Information Drawing 02-314D12 which is provided in the Removable Cartridge Disc System Instruction Manual, Publication Number 29-335.

All Removable Cartridge Disc Drives are normally equipped for 115V, 50/60 Hz operation. For operation with 230V, 50/60 Hz, a wiring change is required in the transformer primary winding of the disc power supply. There are two alterations which may have to be made to the 34-021 to match it to the primary power source being used. The first involves earth ground, and the second involves input voltage and frequency. Prior to use of the 34-021, a voltmeter should be used to verify which contact on the AC power receptacle is at earth ground. It should then be determined if the white AC lead coming from the power plug will be connected to earth ground when the unit is plugged in. If not, that side of the line must be fused. Fusing the line is accomplished by removing a jumper on the AC Filter PCB and insetring a fuse in the fuse holder. Figure 1 shows the AC Filter PCB. Remove the power supply cover to expose the PCB on the AC power cord end of the unit. Clip the jumper and insert a fuse of the proper size for the primary power being used -- 3AG7A for 115VAC and 3AG5A for 220VAC.

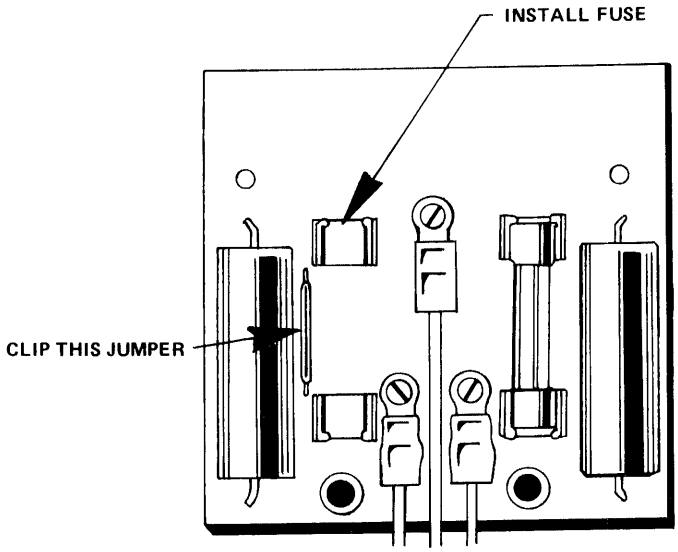


Figure 1. AC Filter PCB

To allow the 34-021 to operate from either 115VAC or 220VAC, at either 50 Hz or 60 Hz, both the primary and secondary windings of the power transformer are tapped. The unit is connected at the factory for an input of 115V 60 Hz. If operation from a different power source is desired, it will be necessary to remove the cover and change the transformer connections.

> CAUTION
>
> Transformer leads are not identification coded other than by their location on the terminal strips. When changing connections, ensure that the transformer leads remian on the proper terminal.

Figure 2 shows the connections for the four possible input power sources. As shown in the figure, 220V 60 Hz operation requires a jumper between terminals 2 and 6 of the transformer. This jumper is stored on a clip attached to the inside of the power supply cover. Other jumpers are of the metal barrier-strip type, and are already on the terminal strips.

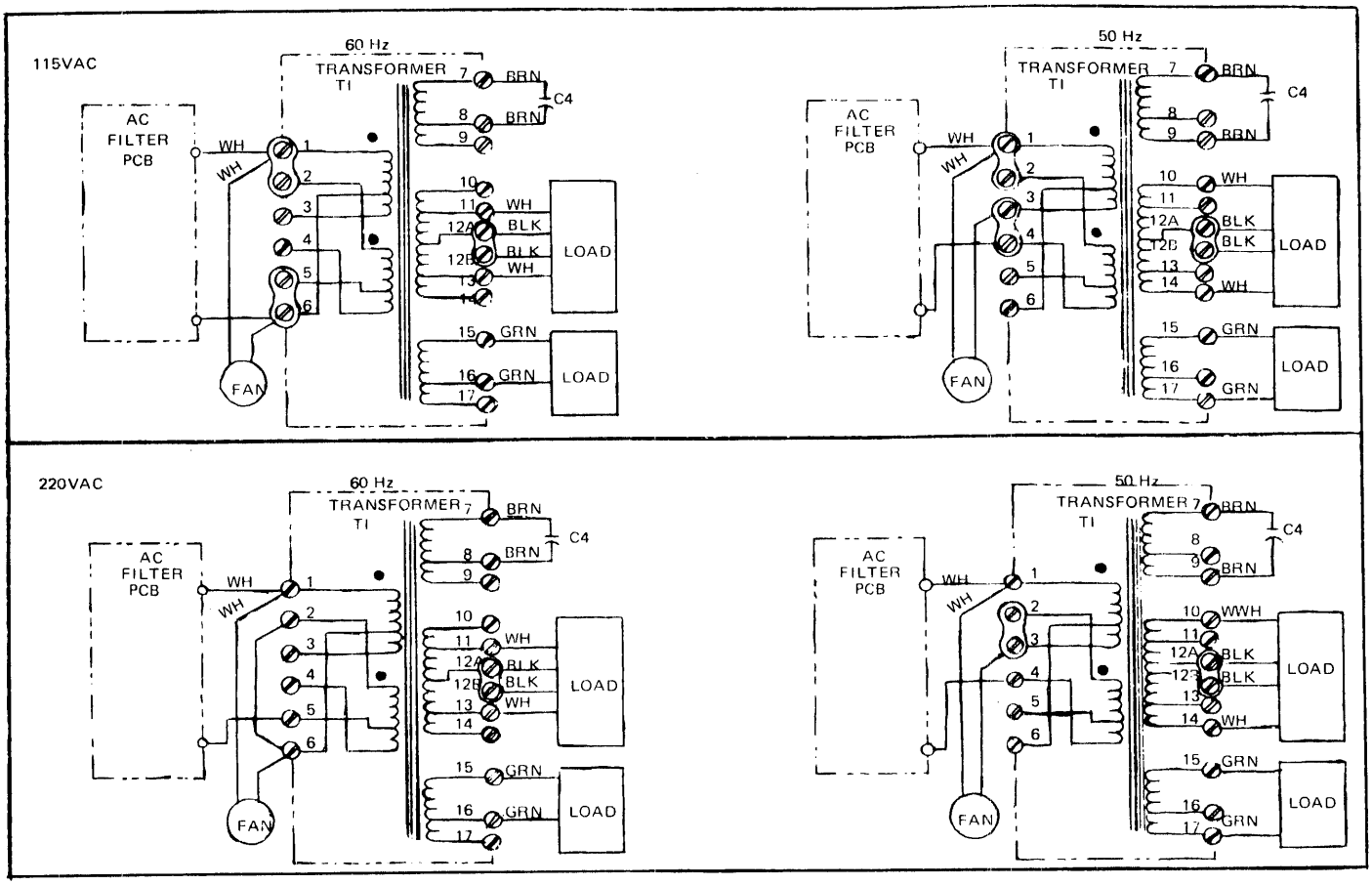


Figure 2. Power Transformer Connections

4. VOLTAGE ADJUSTMENT AND OUTPUT CONNECTIONS

To facilitate use and handling, the DC power cable assembly furnished with the 34-021 has been made very thin and flexible. As a result, the voltage drop in the cable under nominal load is larger than would normally be encountered in similar applications. In the case of the 24-volt outputs, the drop is still a negligible percentage of the output voltage. In the case of the 5-volt output, however, the drop is 0.3 volts. The Power Supply is factory adjusted so that the voltage present at the output connector is 5 volts under nominal load. If the cable assembly furnished with the 34-021 is shortened or if a different cable is used, the 5 volt output may have to be adjusted. This is accomplished by means of a 500 ohm potentiometer at B62 on the regulator PC assembly. Access to this control is by loosening the two screws holding the DC output end of the power supply cover, and lifting the cover. An adjustment range of approximately 4.8V to 6.4V is available at the terminal posts on the PCB. The adjustment should be made under conditions simulating the expected nominal load.

The cable assembly furnished with the 34-021 provides separate ground conductors for the 24-volt and 5-volt outputs. If a different cable is used, care must be exercised to maintain these separate ground systems. Failure to maintain this separation may cause large ground currents which can damage a disc drive connected to the power supply. The DC power cable is removed by unscrewing the terminal post clamps and the cable clamp. Connector pin assignments are as shown in Figure 3. DC ground should not be tied to chassis ground.

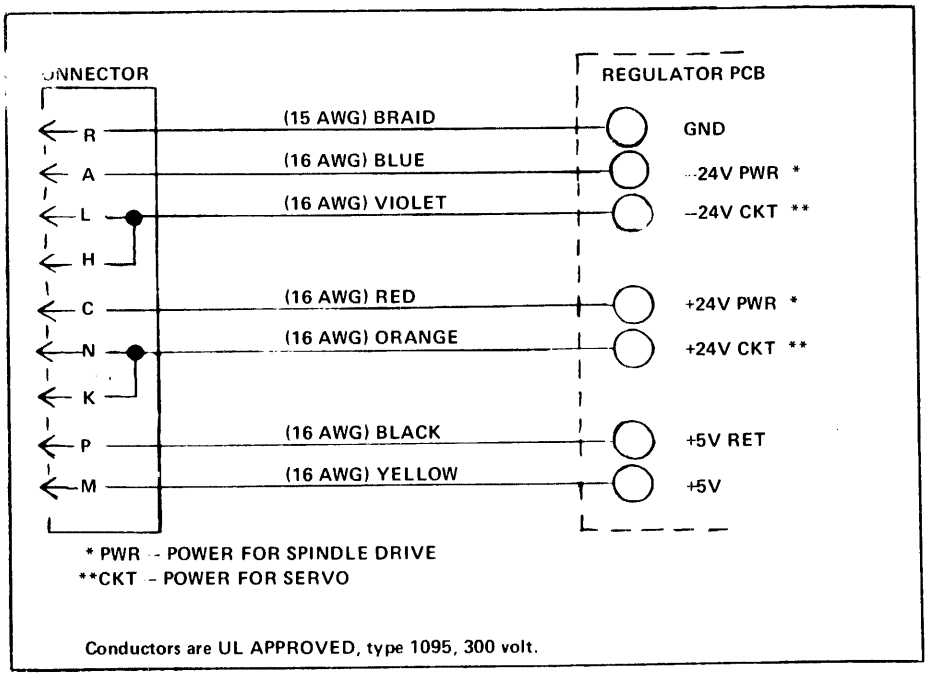


Figure 3. Connector Pin Assignments

5. UNPACKING INSTRUCTIONS

There are no special unpacking instructions for the Removable Cartridge Disc System. Be cautious when handling the Disc Drive after it has been uncrated.

6. MOUNTING INSTRUCTIONS

The Removable Cartridge Disc Drive can be mounted in any standard 483mm (19") Retma cabinet or rack. All hardware is included to mount the disc or power supply in a Perkin-Elmer rack. For mounting instructions and procedures, refer to Vendor Maintenance Manual 29-337 and Information Drawing 02-314D12 provided in the Removable Cartridge Disc System Instruction Manual, Publication Number 29-335.

7. SYSTEM CONFIGURATION

The Removable Cartridge Disc Controller may be installed in any standard 381mm (15") I/O Slot of a Perkin-Elmer Processor or Expansion Card File. Remove the RACK0/TACK0 Strap between back panel Terminal 122-1 and 222-1 at the Controller location. The Controller device addresses are normally wired for X'B6', X'C6', X'D6', X'E6' and X'F6'. If a set other than the normal set is desired, the address strapping at the controller must be altered. Information for changing the addresses is provided in Maintenance Specification 02-314A21.

NOTE

There are special considerations for adapting the Removable Cartridge Disc System to a Model 4 or 5 Processor. For information, contact Perkin-Elmer, Oceanport, New Jersey.

7.1 Cables

There are two different cables for the system. The cables required are a function of the number of disc drives per system.

Disc Drives Per System	Cables Per System
1	1 each 17-278
2	1 each 17-278 1 each 17-279
3	1 each 17-278 2 each 17-279
4	1 each 17-278 3 each 17-279

7.2 Power Supply

Each Power Supply can drive one disc drive.

8. 1 X 1 REMOVABLE CARTRIDGE DISC SYSTEM CONFIGURATION

Figure 4 shows the Configuration and Inter-connecting cable connections for a 1 x 1 Removable Cartridge Disc System.

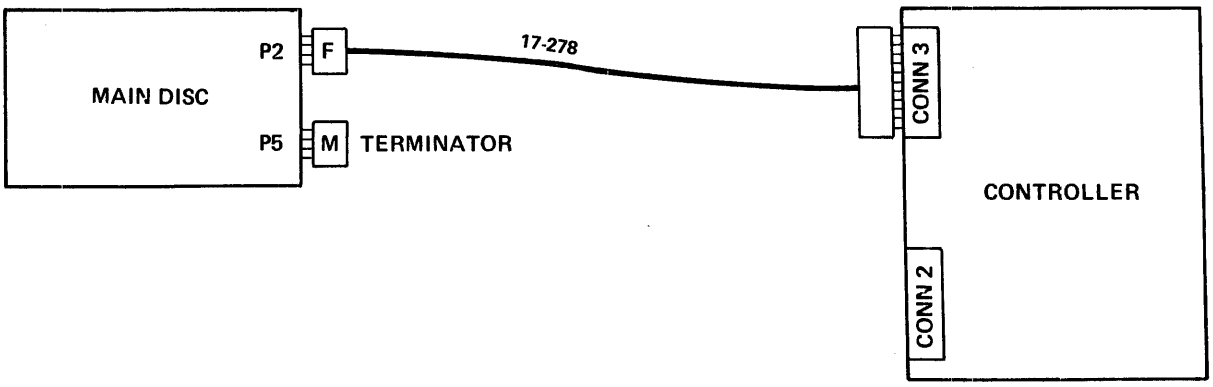


Figure 4. 1 x 1 Removable Cartridge Disc System Configuration

9. 1 X 2 REMOVABLE CARTRIDGE DISC SYSTEM CONFIGURATION

Figures 5 and 6 show the Configuration and Inter-connecting cable connections for a 1 X 2 Removable Cartridge Disc System. The terminator must be moved to the last disc drive.

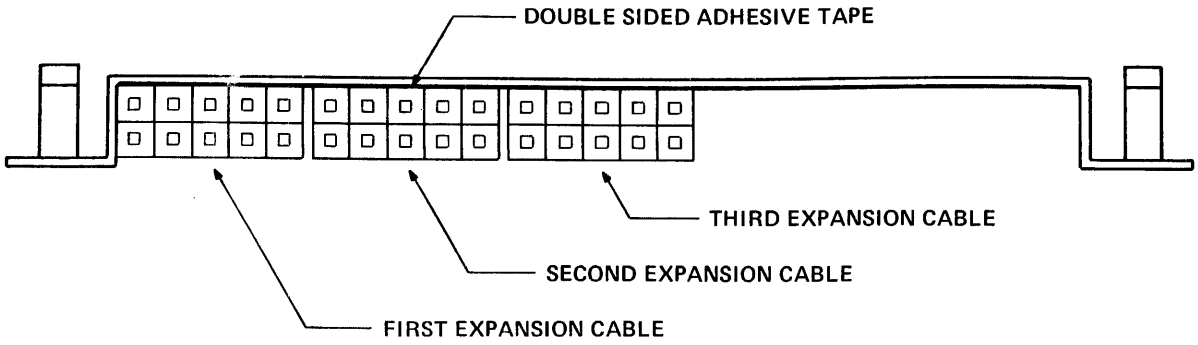


Figure 5. Expansion Cable Connections

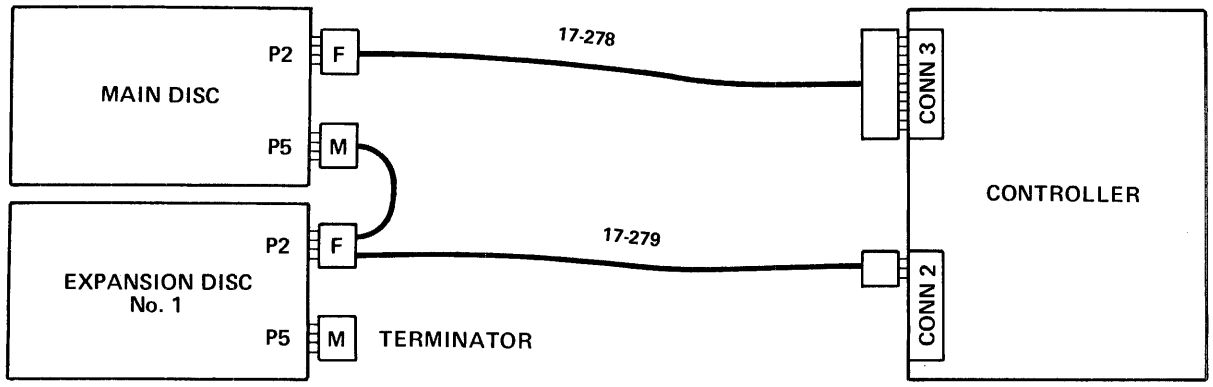


Figure 6. 1 x 2 Removable Cartridge Disc System Configuration

10. 1 X 3 REMOVABLE CARTRIDGE DISC SYSTEM CONFIGURATION

Figures 5 and 7 show the Configuration and Inter-connecting cable connections for a 1 X 3 Removable Cartridge Disc System. The terminators must be removed from the first and the second disc drives.

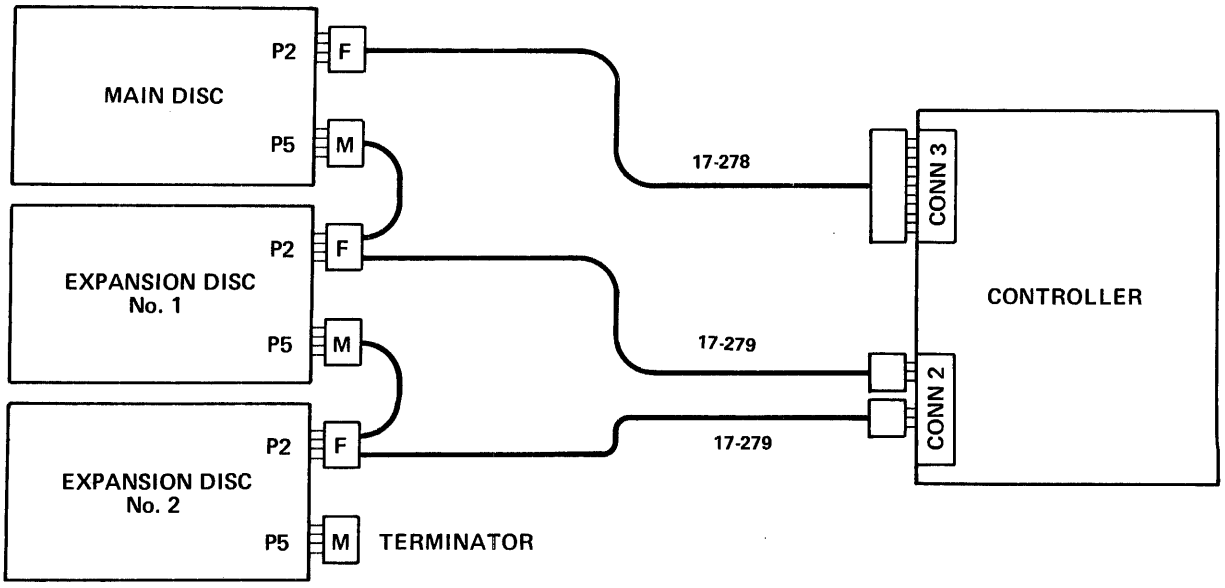


Figure 7. 1 x 3 Removable Cartridge Disc System Configuration

11. 1 X 4 REMOVABLE CARTRIDGE DISC SYSTEM CONFIGURATION

Figure 8 shows the Configuration and Inter-connecting cable connections for a 1 X 4 Removable Cartridge Disc System. The terminators must be removed from the first, second, and third disc drives.

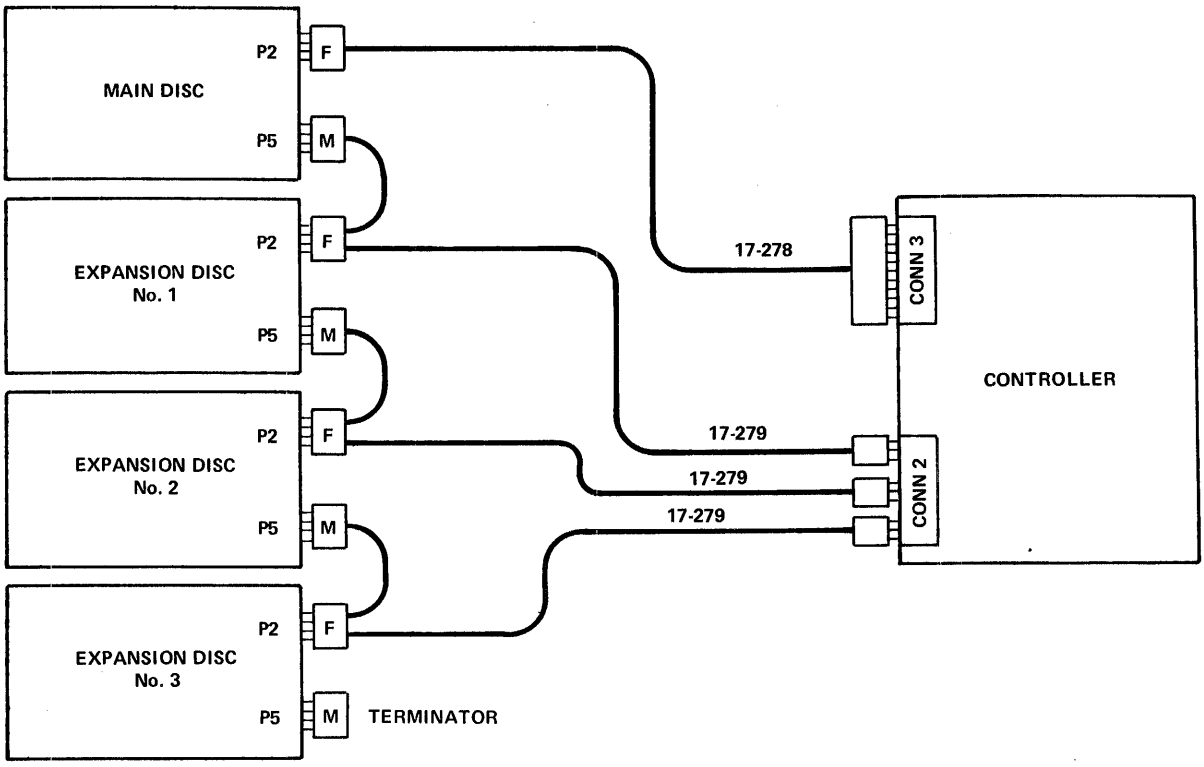


Figure 8. 1 x 4 Removable Cartridge Disc System Configuration

12 TESTING

Load Test Program 06-122 and run the tests as described in 06-122A15.

WARNING

The Model 44 disc weighs 61.69kg (136 lbs.). When mounted in a RETMA cabinet or rack, the leveling feet of the rack must be lowered to the floor. The disc should be mounted in rack no higher than 1.08m ($42\frac{1}{2}$'') above the floor (from disc top to floor). If more than one disc is mounted in the rack, only one disc can be pulled out at a time. If any other rack mounting peripherals are pulled out, be sure to push them back into the rack before pulling out the disc.

METRIC

M46-416
REMOVABLE CARTRIDGE DISC SYSTEM MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Perkin-Elmer Removable Cartridge Disc System consists of a single 381mm (15'') Controller, interconnecting cables, and from one to four disc drives.

The Controller, which is used on the SELCH Bus, handles all communication between the Processor and the disc drives. Each Controller can support from one to four disc drives with overlapping Seek and Restore.

The following is the relationship between Product Numbers and Part Numbers for hardware components required for different Configurations of the Removable Cartridge Disc System.

Product Number	Part Number	Contents	Description
M46-416	02-314	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
		1 each 27-056	Cartridge
		1 each 27-055	44 Series Disc
M46-418	02-316	1 each 27-055	44 Series Disc
		1 each 17-279	Expansion Cable
		1 each 27-056	Cartridge
M46-417	02-315	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
		1 each 27-056	Cartridge
		1 each 27-055	44 Series Disc
M46-421	02-318	1 each 35-438F01M01R03	Controller
		1 each 17-278	Main Cable
M46-419	02-317	1 each 27-055	Series 44 Disc
		1 each 27-056	Cartridge
		1 each 17-279	Expansion Cable

A simplified block diagram of the system is shown in Figure 1.

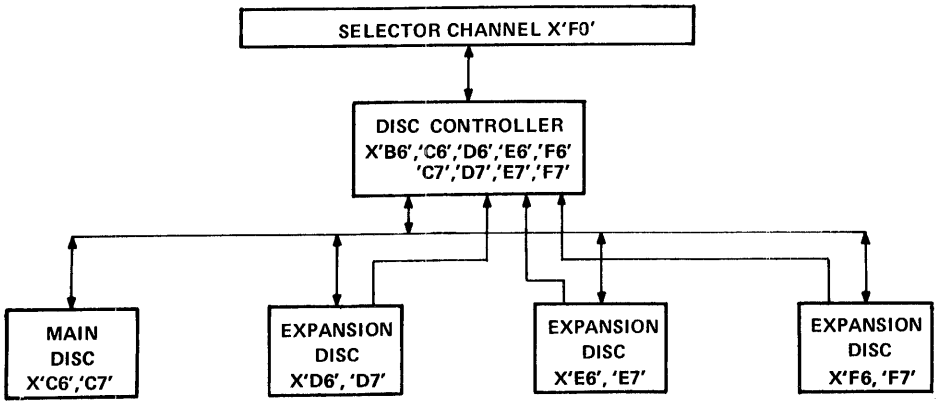


Figure 1. Simplified Block Diagram

2. SCOPE

This specification provides the information necessary to maintain the Removable Cartridge Disc Controller. Included in this specification are a simplified block diagram, device address strapping, timing information, functional schematic analysis, and a mnemonics list.

3. FUNCTIONAL SCHEMATIC ANALYSIS

3.1 Introduction

The Perkin-Elmer Disc Controller is designed to connect one to four disc drives to a Perkin-Elmer Computer equipped with a Selector Channel.

Refer to the timing diagrams in Figures 1 through 9 during this discussion.

The location shown for a signal or device may refer to the location on the P. C. board or to the location on the drawings. In this manual, references are primarily to schematics. Occasionally, when further refinement is necessary, the board pin number is also given. A reference such as 2A6 refers to drawing Sheet 2, coordinate block A6. A particular pin would be referred to as A19-8, shown at 2A6. Look on Sheet 2 at grid square A6 and find pin 8 of the logic element A19.

3.2 Computer Interface and File Control Section

3.2.1 Controller Addresses. Each disc file has a unique address, and the controller has its address. These addresses must be consecutive. Of the eight address bits, five bits must be identical for the files and the data controller. The three remaining bits must be as follows:

Bit 123	
011	Data Controller
100	Disc File 0
101	Disc File 1
110	Disc File 2
111	Disc File 3

For example:

	Bits			
Data Lines	0	123	4567	
X'B 6'	1	011	0110	Data Controller
X'C 6'	1	100	0110	Disc File 0 , Removable DISC
X'D 6'	1	101	0110	Disc File 1 , Removable DISC
X'E 6'	1	110	0110	Disc File 2 , Removable DISC
X'F 6'	1	111	0110	Disc File 3 , Removable DISC
X'B6'	1	011	0110	Data Controller
X'C7'	1	100	0111	Disc File 0, Fixed DISC
X'D7'	1	101	0111	Disc File 1, Fixed DISC
X'E7'	1	110	0111	Disc File 2, Fixed DISC
X'F7'	1	111	0111	Disc File 3, Fixed DISC

Controller addressing logic is shown on Schematic Sheet 2.

The Data Lines from the computer enter at 2G1 to 2M1 and go to the address straps. The three Data Lines which distinguish between the five addresses of this controller are not strapped.

The ADRS0 signal from the computer enters at Sheet 2F1. If the Controller or the File is addressed, CNTAD or FLAD (2M8) is set at the trailing edge of ARDS1, otherwise, both are reset. If the Controller or the File is addressed, the decoded address gates ADRS1 to produce SYN0 (2E9).

The Controller I/O function lines, SR, DA, DR, and CMD, enter Sheet 2 at C1 and D1. If CTLGT (2N8) is on, indicating that the data controller or one of the files was the last I/O device addressed, these I/O functions are gated into the controller as SRG (Gated Status Request), DAG (Gated Data Available), DRG (Gated Data Request), or CMG (Gated Command).

3.2.2 General Clear. System Clear (SCLR) enters Sheet 2 at E1 and is ORed with data controller CMD RESET to produce General Clear (GCLR) at 2S6.

3.2.3 File Addressed and File Selected. The File Addressed (FA) flip-flops are shown at 4C1. At every ADRS when the File is addressed and Write Gate is not on or the Controller is not BUSY, D101 and D111 are gated into FA0 and FA1. FAs are decoded into FLSEL 0-3, which go to the files and select one of the four.

3.2.4 Sense Status of File. The Multiplexors at 3K6 and 3K8 have two control inputs: Enable (E) and Select (S). E is always Enabled (Grounded). S is driven by CNTAD0. Thus, a Status Request to any file reads File Status to the Data Lines and to the Processor. DDGRK (2D4) enables the buffer gates of the Data Lines, thus returning the address of the interrupting unit to the computer during an Acknowledge Interrupt instruction. Notice that some Status Lines from the files are gated in the files by File Select, while File Ready, File Ready to Seek, Read, or Write, and Seek Incomplete come on separate lines from each file. Illegal Address is stored in this controller in a separate flip-flop for each file (3H2 to 3H4). Those signals gated in the file go directly to the Multiplexor at 3K6 and 3K8, while the four signals which exist as a separate line for each file are gated by the Multiplexor at 3G6 to 3G9, which are controlled by File Address (FA). Thus, a Sense Status instruction addressed to any of the four files reads the status of the file addressed to the Data Lines and then to the computer. Note that Not File Ready and Not File Ready to Seek, Read, and Write are the signals actually sent to the Multiplexors; the Status bits are named "File Not Ready" and "File Not Ready to Seek, Read, or Write".

3.2.5 Seek and Restore Commands. The Seek and Restore controls are located between A and H of Sheet 3. When a CMD is addressed to one of the files, FLAD is set during the ADRS portion of the I/O operation. Then, when CMD is generated, D141 and D151 are gated into the Restore and Seek flip-flops, respectively (3B2 and 3B3.) The Restore flip-flop sends Restore and Strobe to the file, while Seek sends Strobe only. Thus, if Restore and Seek are both commanded, Restore will govern. Strobe is delayed by a one shot at 3F2 to enable Restore to settle. Strobe is gated by Write Gate, so that if head motion is commanded during Write Zero Fill, motion does not begin until zero fill is over. The Restore and Seek flip-flops also set Busy, which caused the status "Controller Not Idle". Address Acknowledge or Logical Address Interlock (Illegal Address) resets Restore and Seek, indicating that Seek set-up is over. If the file is RSRW at this time, Seek is over. If the file is Not RSRW, Seek is going on.

3.2.6 Illegal Address Storage. An Illegal Address (attempt to Seek to a cylinder greater than 407) is indicated by a Logical Address Interlock (LAI) pulse (3A5) from the file currently selected. The LAI pulse sets the IA flip-flop of the selected file. The Address Acknowledge signal (ADAWK), which indicates a good Seek (or Restore) address, resets the Illegal Address flip-flop. Thus, Illegal Address is reset by a legal address, or by General Clear.

3.2.7 Interrupt Controls. Each file has its own Interrupt controls, and can be disarmed, enabled or disabled independently of the other files.

3.2.8 Disable and Disarm Storage. Enable (Disable) and Disarm are stored in the flip-flops shown at Sheet 4, area G-H. Note the signals: Enable, a positive signal: and Disarm, a ground signal.

If the file is addressed with an Output Command, Data Line Bits 8 and 9 control these functions as follows:

DATA LINE BITS	9	8	7475 INPUTS		FUNCTION
			ENABLE	ARM	
BINARY BITS	0	0	-	-	no change
	0	1	H	H	Disable, Arm
	1	0	L	H	Enable, Arm
	1	1	H	L	Disable, Disarm

Where Enable permits an Interrupt "attention", Disable prevents an Interrupt "attention"; Arm permits queuing Interrupt requests, Disarm prevents queuing Interrupt requests. Thus, Arm and Enable enable the Interrupt for the File, Disable and Disarm prevent Interrupts from the file, and Disable and Arm prevent Interrupts, but allow storage of Interrupt requests in the Queue flip-flop. General Clear forces all Enable and Arm storage flip-flops to Disable, Disarm, which is the reset condition.

3.2.9 File Interrupt. Each file can interrupt if:

1. The file goes Not Ready.
2. The file goes Ready to Seek, Read, or Write.
3. Seek ends.
   Seek end is signaled by:
   1. FRSRW going to 0, then back to 1.
   2. Address Acknowledge if FRSRW stays 1 (seek the same address).
   3. Illegal Address (FRSRW stays 1).
   4. FRSRW going to 0 followed by Seek Incomplete (FRSRW stays 0).

Taking File 0 as typical of all four, when the file goes Not Ready, the signal FRDY01 (3K1) goes to ground which sets the QF0 flip-flop at 3M1. If the file goes Ready to Seek, Read or Write, signal FRSRW01 (3J1) goes high, which sets the QF0 flip-flop. Before head motion begins in a Seek or Restore operation, FRSRW01 goes to ground. When head motion stops normally, FRSRW01 goes high and QF0 sets as described above. If head motion stops improperly and a Seek Incomplete occurs, signal SKINC01 (3J1) goes high and QF0 sets. If the Seek called for does not involve head motion, FRSRW01 stays high. An Address Acknowledge (ADAWK0) pulse (3A6) or a logical address interlock (LAI0) (3A5) occurs. These pulses are distributed to the IA flip-flops, 3H2-3H5. LAI for File 0 is ORed with ADAWK for File 0 by gate A35 shown at 3F3. The pulse from this gate goes to Pin 12 of gate A36 at 3K1. If Pin 13 of A36 is low, indicating head motion will occur, Pin 1 of A47 (3M1) stays high and the QF01 flip-flop does not set. If Pin 13 of A36 is high, indicating that the same address is seeking and head motion does not occur, Pin 1 of A47 goes low and the QF01 flip-flop sets.

A flip-flop does ,et set if held reset and pulsed at the set input, so if DSARM00 is low, (3K1), QF01 flip-flop does not get set.

If ENBL01 (3M1) is high, the QF0 signal becomes Interrupt Request File 0 (NTRQF01) (3N1). If ENBL01 is low, the QF0 output is blocked. When the internal RACKO-TACKO circuits (Sheet 6) respond with an Interrupt Acknowledge (INAKF00) (6N2) QF0 is reset. General Clear resets all QF flip-flops.

3.2.10 Internal Racko-Tacko. If a RACKO (2B1) signal occurs and no Interrupt Request from the files or the Data Controller is pending, the RACKO enters at 2B1, passes through the contention circiut at 2A4 and leaves as TACKO at 2A6.

An Interrupt Request from a file (NTRQFX1) or from the Data Controller (NTRQC1) enters at 6K1-6K4. If RACK0 is not present, the T inputs to the 7475s (6K1-6K4) are high, and the Interrupt Request sets the appropriate 7475. The "zero" outputs from the 7475s are ORed together (6N1-6N3) to produce Attention (ATEN0) to the Processor and to furnish an input to the contention circuits (2A3).

When a RACKO occurs and attention from this unit is present, TACKO does not occur. Instead, the "T" inputs to the 7475s go low to prevent any more Interrupt Requests from disturbing the pulse gating. After a short delay (6G1), gated RACKO pulses a priority circuit (6M1-6M4). When the delayed gated RACKO encounters the first gate who's 7475 is set, delayed gated RACKO becomes Interrupt Acknowledge (INAKC0 or INAKFX0) which resets the flip-flop for that device (3L1-3L5). Interrupt Acknowledge also indicates which device is being acknowledged by sending signals IAD1, IAD2 (6S5) and INAKC0 (6R1) to the Multiplexors shown at 2K5-2M5. Delayed gated RACKO is delayed again producing double-delayed gated RACKO (DDGRK0) (6J2) which produces SYN0 (2E4-2E9) and gates the device address (2E2-2M2) to the Processor.

3.3 Data Transfer Section

3.3.1 Data Controller Commands. Data controller commands are sent to the controller via CMD I/O instruction addresses to the data controller with the function desired as the output data. The command is set up in the command registers, shown at 4B5-4B7. The command is decoded and command functions are generated by subsequent gating (4E5) (4E7). Note that the format commands are disabled unless the format (FMT) switch is closed (handle towards right). The CNTCM signal also sets the Data Controller Busy (CBSY) flip-flop (5L1).

3.3.2 Normal Mode Instructions. The normal mode instructions are: Read, Read-Check, and Write. Read and Read-Check are very similar and are discussed together. Normal Mode assumes that the disc has been formatted. The Format Instructions are used to format the disc.

3.3.3 Track Addresses. In the process of setting up for a Normal Mode Data Transfer, the program Writes Data to the file, giving the cylinder address. This operation sets the file address (4C1) and loads the cylinder address into the Data Input Register (DIR) (6K6-6K9). Next, the program writes data to the data control section, giving the sector address and head. This operation transfers the cylinder address from DIR to the Data Output Register (DOR) (6M6 and 6R8) and then loads the sector number and head into the DIR. Note that Cylinder Address Bit 256 is stored in Bit 7 of DOR and is enabled by Flip-flop A149 at 6J5. Two DAGs are needed to enable Cylinder Address Bit 256.

3.3.4 Read Operation. The program executes an Output Command to the data control section, with the data defining the function. Assume a Read function. The Output Command sets CBSY (5L1). The sector comparitor gates (5B8-5B9) are always operating, comparing the data from the file's internal sector counter with data from the DIR. (CONT0 (5D9) will be described under "Multi-sector Operations" later; assume it is high now). If the selected file is ready to Seek, Read, or Write (5E3) and if the data controller is Busy (5M2), then a one-shot (5G3) is triggered on the trailing edge of each sector mark. Since the file's internal sector counter stops on the leading edge of sector mark, the counter has settled down by the trailing edge. This one-shot tests the output of the sector comparison gates, and if the sector counter and DIR agree, the sector comparison (SCCMP) (5H9) signal is generated. See Figure 2 for the Sector Timing.

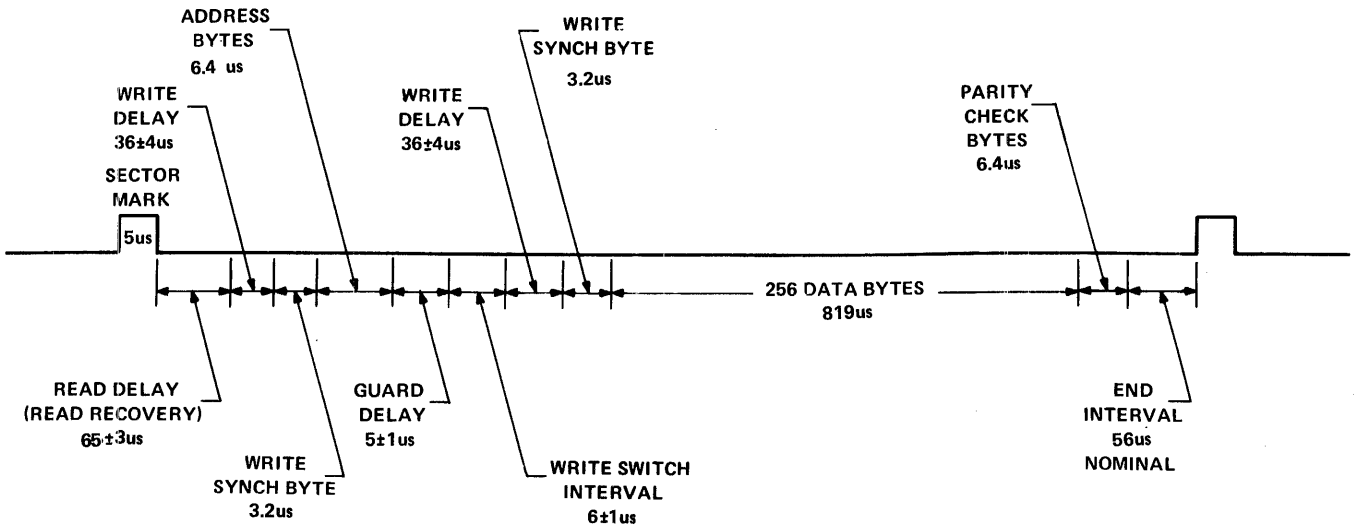


Figure 2. Sector Timing

3.3.5 Address Read. The operations Read, Read-Check, and Write should begin with an address Read in order to verify that the sector selected is correct.

Data from the disc is received by the INDTA flip-flop (5M9). Read Data (RDTA) from the disc first passes through a non-inverting amplifier (5K9) and then direct sets the INDTA flip-flop (5M9). The trailing edge of Read Clock, slightly delayed, resets INDTA. INDTA is the source of data from the disc to the controller.

If Read or Write (RDWT) is true and Sector Compare (SCCMP) occurs, the Address Read Gate (ARDGT) flip-flop (6B6) sets at the end of SCCMP (65 microseconds). ARDGT turns on Read Gate (RDGT) (5R5), and clock pulses start coming from the disc. The pattern 011 is the SYNCH pattern and is written at the beginning of each sector. The SYNCH detector gates (6A6) detect this pattern and set the address compare (ADCMP) (6D6) flip-flop at the trailing edge of the next Read Clock. ADCMP and Read Clock are gated together to produce Read Count Bit Counter (RCBCT) (6G5). The reset side of the compare counter flip-flop at 6E6 is gated by ADCMP and is called Compare First Byte (CMP1) (6G6). At the end of the first byte of address comparison, the trailing edge of the Bit 7 signal compliments the compare counter, removing CMP1. At the end of the second byte of address compare, the Compare Counter is complimented again, triggering the Address Read Complete (ARDCM) one-shot 6H7, which resets ARDGT and ADCMP, ending the address read operation.

The address comparison is accomplished with an Exclusive-OR, shown at 6F4. One input to this comparison is from the Data Auxiliary Register Bit 7 (DAR7), (4N8), which is the data just received from the disc. The other input, Check Data (CKDA) (6R6) comes from the DIR and the DOR. Two 8-bit multiplexors are shown on Sheet 6. One of them, shown at 6M9, takes data from the DIR. The other, at 6R6, takes data from the DOR. The multiplexor at 6R6 is selected at all times except during the first byte of address compare. Compare First Byte (CMP1) enters at 6N5 and cuts off one multiplexor at 6R6 and turns on the multiplexor at 6M9. Since the Data Input Register contains the sector number and head, this data is compared against data from the disc during the first byte of Address Read. During the second byte, CMP1 goes to 0, and the multiplexor at 6R6 is selected. Since the DOR contains the cylinder address, data from the disc is compared with the cylinder address during the second byte of Address Read. If the data differs, the Address Compare Error flip-flop (6F4) is set.

In addition, during the first byte of Address Read, the head and defective track bits from the disc are tested. At Bit 3 time of CMP1 (6G6), the defective track bit is in DAR5 (4N8). If this bit is a 1, the defective track flip-flop (6D3) becomes set. Also at Bit 3 time of CMP1, the head bit is in DAR6 (4N8). This bit is checked against the current Head Select flip-flop (HD) (4C4). If these bits differ, the Head Comparison Error flip-flop (6G4) becomes set. Note that these errors set Examine (6H3) and that Examine prevents writing on the disc (3E1). See Figure 3 for Address Read and Compare Timing.

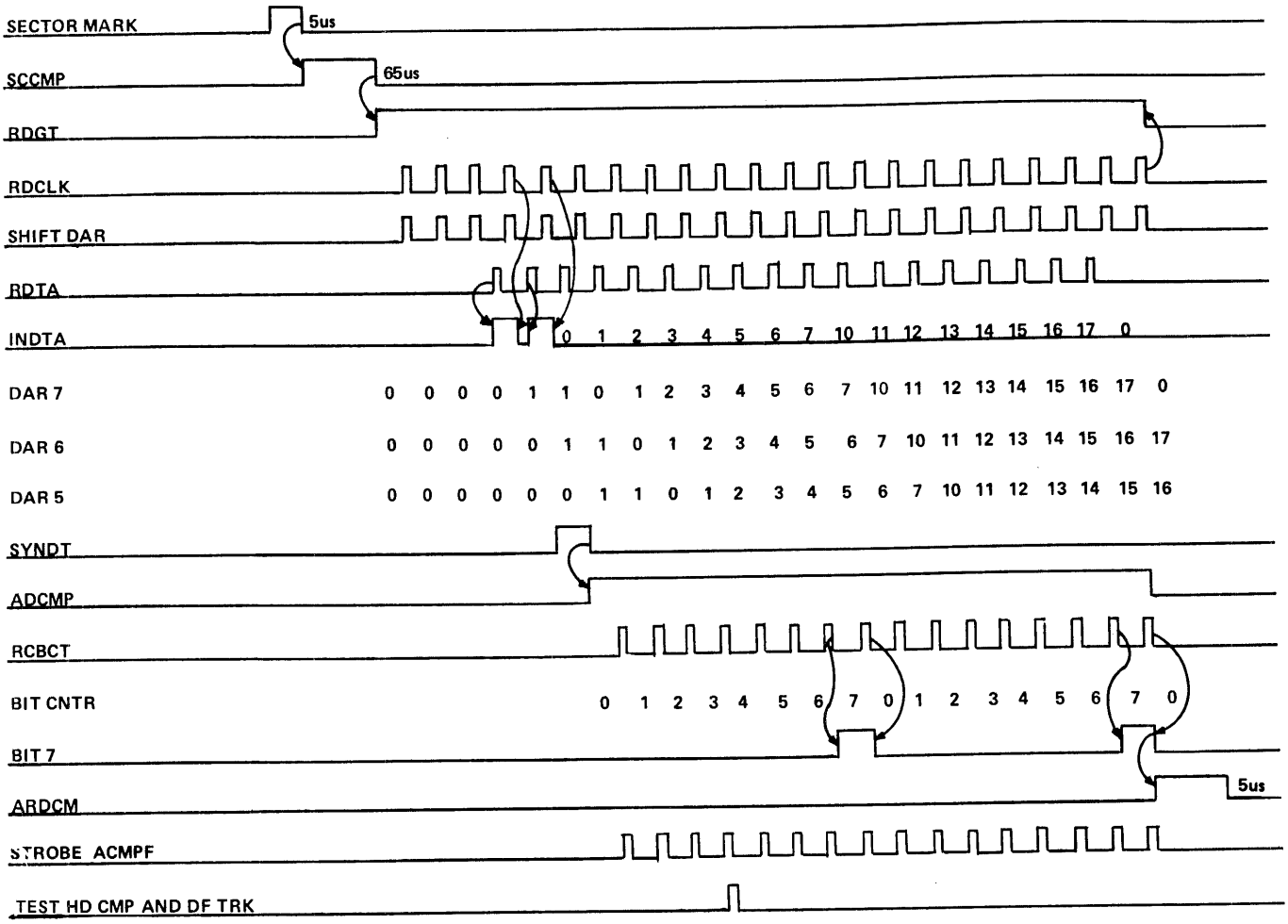


Figure 3. Address Read and Compare

3.3.6 Read Data. An Address Read ends with ARDCM (6H6); the trailing edge of ARDCM triggers the Data Start (DTST) one-shot (5H7) which starts Read Data. If Combined Read (Read or Read-Check) (CRD) is present, DTST sets the Data Read Gate (DRDGT) flip-flop (5J6) which turns on the Read Gate in the selected file (5R5). Once Read Gate is on, the controller waits for SYNCH Detected (SYNDT) (6B6) which sets the Data Read Bit Counter Gate (DRBCG) flip-flop (5N8) which gates Read Clock to count the Bit Counter (6F6, 4G5).

DRDGT gates Read Clock to produce Shift Data Input Register (SHDIR) (5N7) which shifts data from disc to the Data Input Register (DIR) (6K6, 6K8). At the end of each byte of data, Bit 7 and RDGT generate Read Load Data Output Register (RLDD01) (5N6) which shifts data from DIR to DOR (6R9, 6M6) and sets the Data Request (DTRQ) flip-flop (4F8). If this is a Read operation, DTRQ passes through a gate at 4G6 and becomes DTARQ which is Busy on the selector bus (3K6). If the operation is Read Check, the gate at 4G6 is closed, in which case, no Data Request occurs.

The Byte Counter (4K5) has been counting the bytes and at the 256th byte (Byte Number 255), produces the signal End Byte (BYEND) (4R3). The RLDD0 at the end of the last byte sets the Cyclic Check (CKCY) flip-flop (5K6). The next RLDD0 sets the Cyclic Check 2 (CKCY2) flip-flop (5L6), and the next RLDD0 triggers the Read End (RDEND) one-shot (5R6).

RDEND triggers the Operation End (OPEND) one-shot (4M6). The OPEND pulse resets the five Read Control flip-flops (5J6-5N8). CKCY0 prevents RLDD0 from making a Data Request (4C9). If this is a single sector record, the Data Request flip-flop (4F8) should now be set, since the Selector Channel (SELCH) will not have answered the last Data Request. The OPEND pulse then passes through the gate shown at 4N7 and becomes the Operation Complete (OPCMP) pulse (4R7), which in turn becomes the Complete or General Clear (CMPCL) pulse (4R7), which resets CBSY (5L1), ending the Read or Read-Check operation. See Figure 4 for Read and Read Format Timing.

For the Multi-sector Record case, see "Multi-Sector Records", Section 3.3.12.

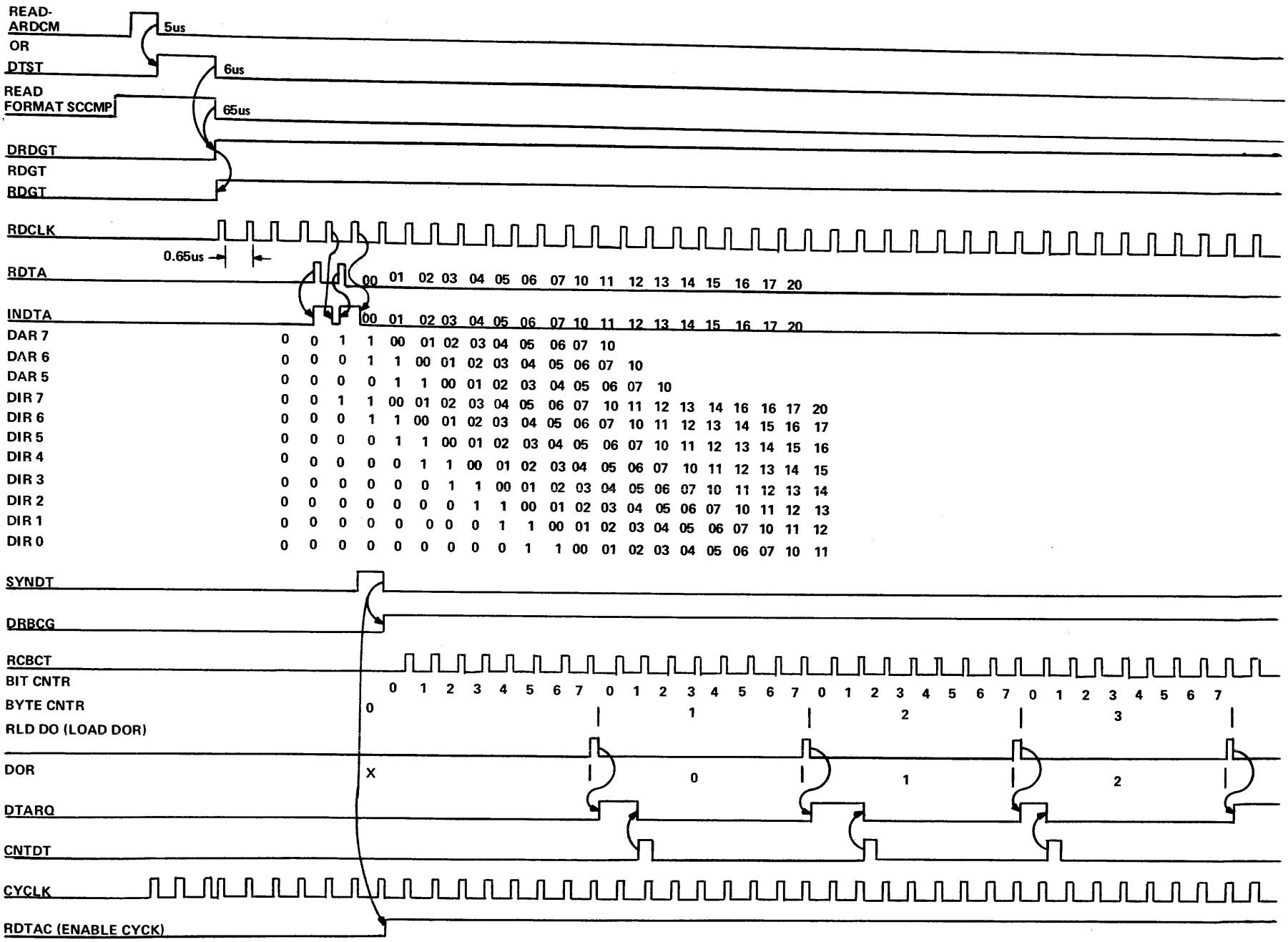
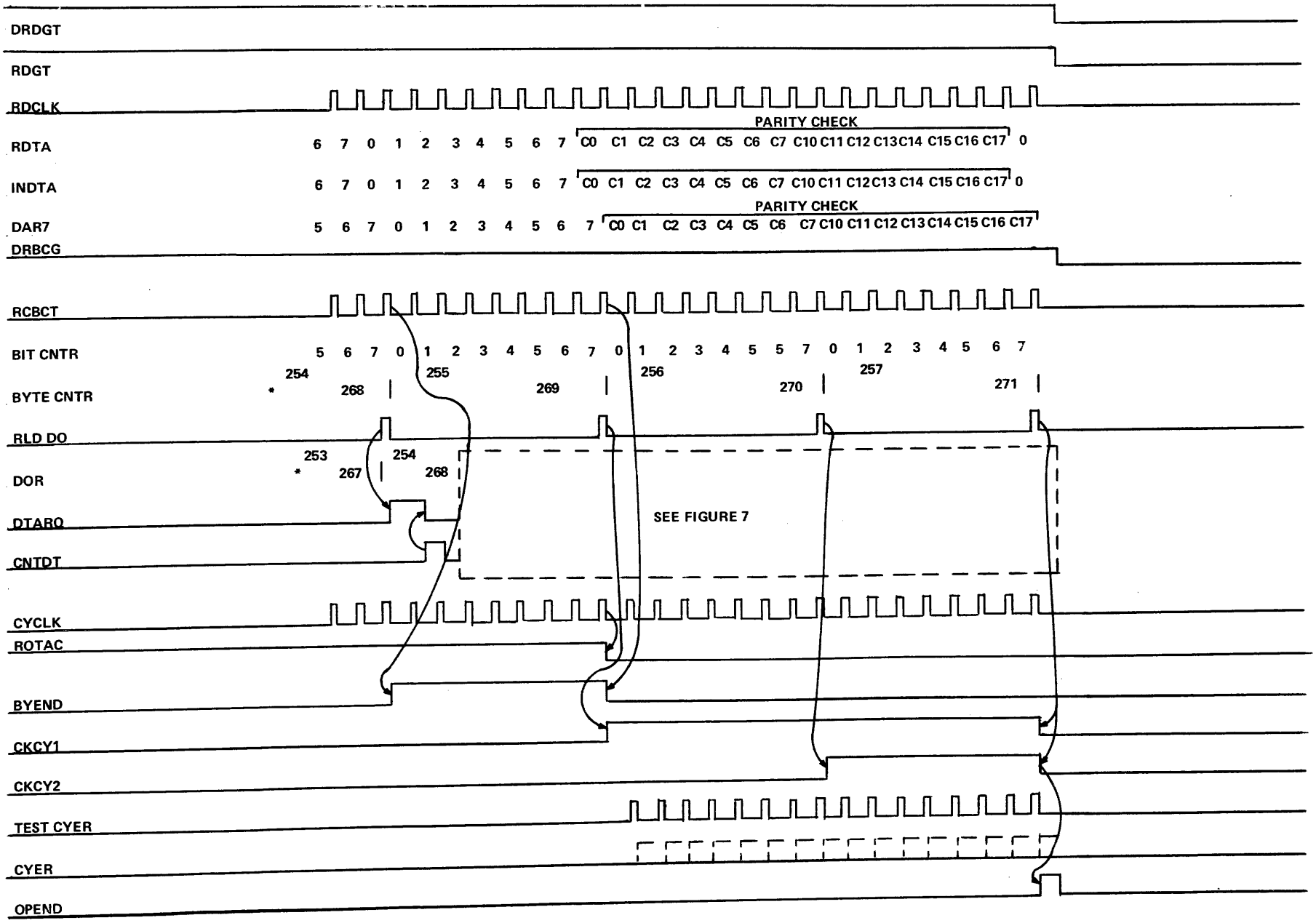


Figure 4. Read and Read Format



*NOTE: UPPER NUMBER IS FOR READ;
LOWER NUMBER IS FOR READ FORMAT.

Figure 4. Read and Read Format (Continued)

3.3.7 Longitudinal Parity Check. During a Read or Read-Check, the Longitudinal Parity Check circuits are operating. The Longitudinal Parity Check Shift Register (6D8-6F8), is always being shifted by Write Cyclic Check (WCYCK) (6B8) except during Read Data, when it is shifted by the Shift Data Input Register (SHDIR) (6B8). Normally, zero is shifted through the Register. During the Read Data Control (RDTAC) (6B8) time, which is between SYNCH detected and Longitudinal Parity Check time, data from the disc, via Data Auxiliary Register 7 (DAR7) is gated into the Exclusive-OR at 6C7 and then to the Shift Register. The other input to the Exclusive-OR is the Q output of the Shift Register. Through shift operations, two Longitudinal Parity Bytes are generated. The first Parity byte is an even Longitudinal Parity Byte of odd-number data bytes and the second Parity Byte is an even Longitudinal Parity Byte of even-number data bytes. See Figure 5, for derivation of Longitudinal Parity Bytes.

During Read Longitudinal Parity Check time, the data from the disc is compared with the data from the Shift Register; they should agree. If they do not agree, the "J" input to the Longitudinal Parity Check Error (CYER) flip-flop (6C9) goes high. This flip-flop is clocked by each Read Clock during Parity Check time, so that the flip-flop sets on Longitudinal Parity Check Error.

During Write or Write Format operations, Longitudinal Parity Check operates in a similar manner except that the data source is WTDTA (6B7); the Shift Register is shifted by WCYCK (6B8); the Longitudinal Parity Check Error (CYER) flip-flop (6C9) cannot set; and during Write Parity Check time the Longitudinal Parity Check Shift Register Out (CYOUT) (6F9) is written on the disc.

3.3.8 Write Data. Write Data begins with Address Read. Address Read ends with Address Read Complete (ARDCM) which triggers the Data Start (DTST) one-shot (5G7).

DTST and Write (WT) become Write Start (WTST) (5H8). WTST sets the Write Gate (WTGT) flip-flop (5K3) and produces a Write Load Data Output Register (WLDOR) pulse (5S4) which generates a Data Request (4G6), requesting the first byte from SELCH and loading it into the Data Input Register (DIR) (6K6-6K8).

The Write Gate flip-flop turns on Write Gate (WTGT) to the file (3F1) and enables Write Zeros (5S4), thus writing a string of zeros on the disc.

The Write Oscillator (2F8) produces pulses at 10.163 MHz. These pulses toggle a flip-flop at 2G8, which produces a 5.081 MHz square wave. This square wave (WTOSC) (2K8) toggles the Phase flip-flop (5J4). This flip-flop is reset during the Write Clock phase and set during the Write Data phase. Each phase is 197 nanoseconds long, and a bit cell is 394 nanoseconds long. WTGT enables Write Phase to Write Clock and Data which is gated with WTOSC (5R4), producing pulses 98 nanoseconds long which are sent to the file.

WTST also triggers the Write Delay (WTDLY) one-shot (5G4). The trailing edge of WTDLY sets the Write Bit Counter Gate (WBTCG) flip-flop (5L3).

WBTCG turns Erase Gate on (3E2) and gates Write Clock to form Write Count Bit Counter (WCBCT) (5S3) which is counted by the bit counter (4J5).

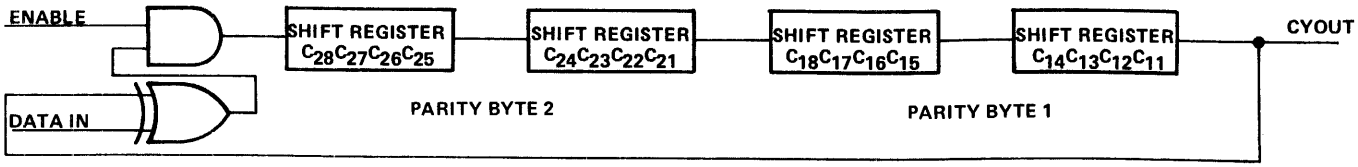
Write Bit Counter Gate also enables the Enable SYNCH (ENSYN) signal (5S3). ENSYN and Bit Counter Bit 2 and B4 (5J5), which is true only during Bit Counter time 6 and 7, passes through an OR Gate (5M5), is gated by Data Phase (5N5), and ORed with Clock to produce Write Clock and Data which is gated by WTOSC to produce Write Data and Clock (WTDAC) (5S4) for the file. This signal, present only during bit time 6 and 7 of Enable SYNCH, writes the ones of the SYNCH Byte.

During Bit Counter 7 time, the Bit 7 signal occurs. This signal is gated with WTCLK to produce Write Gated Bit 7 (WGBT7) (5N4). WGBT7 shifts the Shift Register shown at 4B9, which is now shifting zeros. WGBT7 and WBTCG (5M2) produces Write Load Data Output Register (WLDOR) (5S4); WGBT7 and WBTCG also set the Data Out flip-flop (5N3) which removes ENSYN (5S3) and produces Enable Data (ENDTA) (5S2).

WLDOR (5S4) shifts the byte in DIR to DOR (6M6-6R9) and sets Data Request (4F8). Data Request is sent to SELCH as Not Busy (3K6). SELCH responds with the next byte on the Data Lines and sends a DA signal. DA is accepted as DAG and generates SYN (2E9). DAG also becomes CNTDT (2S7) which resets Data Request (4G6).

The content of DOR is multiplexed to become Data Output Register Out (DOROT) (6R7). The multiplexor is driven by the Bit Counter bits (B1, B2 and B4) (6S9). DOROT is gated by ENDTA (5J6) to produce Write Data (WTDTA) (5L6), which becomes Data to the disc.

This process continues. Data is continually multiplexed from DOR to the disc. At the end of each byte, the next byte is moved from DIR to DOR, and SELCH furnishes the third byte to DIR.



INITIAL CONDITION: ZERO IS SHIFTED THROUGH THE REGISTERS.
AFTER ENABLE:

BIT COUNT 1: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = C_{21} = C_{22} = C_{23} = C_{24} = C_{25} = C_{26} = C_{27} = 0$;
$C_{28} = B_{11} \oplus 0 = B_{11}$

BIT COUNT 8: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = 0$.
$C_{21} = B_{11} \oplus 0 = B_{11}$
$C_{22} = B_{12} \oplus 0 = B_{12}$
$C_{23} = B_{13} \oplus 0 = B_{13}$
$C_{24} = B_{14} \oplus 0 = B_{14}$
$C_{25} = B_{15} \oplus 0 = B_{15}$
$C_{26} = B_{16} \oplus 0 = B_{16}$
$C_{27} = B_{17} \oplus 0 = B_{17}$
$C_{28} = B_{18} \oplus 0 = B_{18}$

BIT COUNT 16:
$C_{11} = B_{11}$ $C_{21} = B_{21}$
$C_{12} = B_{12}$ $C_{22} = B_{22}$
$C_{13} = B_{13}$ $C_{23} = B_{23}$
$C_{14} = B_{14}$ $C_{24} = B_{24}$
$C_{15} = B_{15}$ $C_{25} = B_{25}$
$C_{16} = B_{16}$ $C_{26} = B_{26}$
$C_{17} = B_{17}$ $C_{27} = B_{27}$
$C_{18} = B_{18}$ $C_{28} = B_{28}$

BIT COUNT 17:
$C_{28} = B_{11} \oplus B_{31}$ $C_{18} = B_{21}$
$C_{27} = B_{28}$ $C_{17} = B_{18}$
$C_{26} = B_{27}$ $C_{16} = B_{17}$
$C_{25} = B_{26}$ $C_{15} = B_{16}$
$C_{24} = B_{25}$ $C_{14} = B_{15}$
$C_{23} = B_{24}$ $C_{13} = B_{14}$
$C_{22} = B_{23}$ $C_{12} = B_{13}$
$C_{21} = B_{22}$ $C_{11} = B_{12}$

BIT COUNT 32:
$C_{28} = B_{28} \oplus B_{48}$ $C_{18} = B_{18} \oplus B_{38}$
$C_{27} = B_{27} \oplus B_{47}$ $C_{17} = B_{17} \oplus B_{37}$
$C_{26} = B_{26} \oplus B_{46}$ $C_{16} = B_{16} \oplus B_{36}$
$C_{25} = B_{25} \oplus B_{45}$ $C_{15} = B_{15} \oplus B_{35}$
$C_{24} = B_{24} \oplus B_{44}$ $C_{14} = B_{14} \oplus B_{34}$
$C_{23} = B_{23} \oplus B_{43}$ $C_{13} = B_{13} \oplus B_{33}$
$C_{22} = B_{22} \oplus B_{42}$ $C_{12} = B_{12} \oplus B_{32}$
$C_{21} = B_{21} \oplus B_{41}$ $C_{11} = B_{11} \oplus B_{31}$

BIT COUNT 33:
$C_{28} = B_{11} \oplus B_{31} \oplus B_{51}$ $C_{18} = B_{21} \oplus B_{41}$
$C_{27} = B_{28} \oplus B_{48}$ $C_{17} = B_{18} \oplus B_{38}$
$C_{26} = B_{27} \oplus B_{47}$ $C_{16} = B_{17} \oplus B_{37}$
$C_{25} = B_{26} \oplus B_{46}$ $C_{15} = B_{16} \oplus B_{36}$
$C_{24} = B_{25} \oplus B_{45}$ $C_{14} = B_{15} \oplus B_{35}$
$C_{23} = B_{24} \oplus B_{44}$ $C_{13} = B_{14} \oplus B_{34}$
$C_{22} = B_{23} \oplus B_{43}$ $C_{12} = B_{13} \oplus B_{33}$
$C_{21} = B_{22} \oplus B_{42}$ $C_{11} = B_{12} \oplus B_{32}$

FINAL:
$C_{11} = B_{11} \oplus B_{31} \oplus B_{51} \oplus B_{71} \oplus \cdots\cdots \oplus B_{2551}$
$C_{12} = B_{12} \oplus B_{32} \oplus B_{52} \oplus B_{72} \oplus \cdots\cdots \oplus B_{2552}$
$C_{13} = B_{13} \oplus B_{33} \oplus B_{53} \oplus B_{73} \oplus \cdots\cdots \oplus B_{2553}$
$C_{14} = B_{14} \oplus B_{34} \oplus B_{54} \oplus B_{74} \oplus \cdots\cdots \oplus B_{2554}$

$C_{15} = B_{15} \oplus B_{35} \oplus B_{55} \oplus B_{75} \oplus \cdots\cdots \oplus B_{2555}$
$C_{16} = B_{16} \oplus B_{36} \oplus B_{56} \oplus B_{76} \oplus \cdots\cdots \oplus B_{2556}$
$C_{17} = B_{17} \oplus B_{37} \oplus B_{57} \oplus B_{77} \oplus \cdots\cdots \oplus B_{2557}$
$C_{18} = B_{18} \oplus B_{38} \oplus B_{58} \oplus B_{78} \oplus \cdots\cdots \oplus B_{2558}$

$C_{21} = B_{21} \oplus B_{41} \oplus B_{61} \oplus B_{81} \oplus \cdots\cdots \oplus B_{2561}$
$C_{22} = B_{22} \oplus B_{42} \oplus B_{62} \oplus B_{82} \oplus \cdots\cdots \oplus B_{2562}$
$C_{23} = B_{23} \oplus B_{43} \oplus B_{63} \oplus B_{83} \oplus \cdots\cdots \oplus B_{2563}$
$C_{24} = B_{24} \oplus B_{44} \oplus B_{64} \oplus B_{84} \oplus \cdots\cdots \oplus B_{2564}$
$C_{25} = B_{25} \oplus B_{45} \oplus B_{65} \oplus B_{85} \oplus \cdots\cdots \oplus B_{2565}$
$C_{26} = B_{26} \oplus B_{46} \oplus B_{66} \oplus B_{86} \oplus \cdots\cdots \oplus B_{2566}$
$C_{27} = B_{27} \oplus B_{47} \oplus B_{67} \oplus B_{87} \oplus \cdots\cdots \oplus B_{2567}$
$C_{28} = B_{28} \oplus B_{48} \oplus B_{68} \oplus B_{88} \oplus \cdots\cdots \oplus B_{2568}$

THE FIRST LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF ODD-NUMBER DATA BYTE.
THE SECOND LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF EVEN-NUMBER DATA BYTE.

Figure 5. Derivation of Longitudinal Parity Bytes

The Byte Counter counts the bytes (4K5-4N5) and, at the 256th byte, (Byte Number 255) generates the signal BYEND into the last byte (LSTRBY) flip-flop, which is the first flip-flop of the Shift Register shown at 4B9. The last byte circulates back to the input to the Shift Register so that ones will now be shifted down the Shift Register.

At the end of the next byte, Write Last Byte (WLSBY) (4C7) goes to one. WLSBY turns off ENDTA (5S2) stopping data output to the disc, and turns on Enable Longitudinal Parity Check (ENCY), which feeds the output of the Longitudinal Parity Check Shift Register (CYOUT) (5J5) to the disc.

The next WGBT7 pulse shifts a one to the next flip-flop (4B9), whose output is not used. This flip-flop provides for two bytes of Longitudinal Parity Check Data.

The next WGBT7 sets the Write End (WTED) flip-flop (4B8). WTED turns off ENCY, therefore no more data is sent to the disc. Clock pulses continue to be written, however, filling the sector with zeros.

WTED also triggers the Operation End (OPEND) one-shot (4L6) which results in CMPCLR (4R7) as explained in "Read Data" above, and in Sector Mark, End, or General Clear (SECLR) (5K3), which resets all Write Control flip-flops except Write Gate, which is reset by Sector Mark or General Clear (SMCLR) (5H2). Since the Write Gate flip-flop stays on, Zero Fill continues until the next Sector Mark. See Figure 6 for Write and Write Format Timing.

3.3.9 Read Format. Read Format is identical to Read Data except for starting and ending. Since Read Format does not include an Address Read operation, Read Format is started by Sector Compare (SCCMP) (5H9). SCCMP sets the flip-flop shown at 5J7 while the Read format (RDFOT) signal is present. The output from this flip-flop becomes Data Read Data Gate (DRDGT) (5L7). From this point, Read Format is the same as Read except that BYEND (5S2) occurs at the 270th byte (Byte Number 269). See Figure 4 for Read and Read Format Timing.

3.3.10 Write Format. Write Format is identical to Write Data except for starting and ending. Since Write Format does not include an Address Read operation, Write Format is started by Sector Compare (SCCMP) (5H9). The Write Format command (WTFOT) (5G9) and SCCMP are ANDed together (5G9) and then ORed with the Write Normal Start to form the Write Start (WTST) signal (5G7). The remainder of Write Format is identical to Write, except that BYEND (5S2) is generated by the 270th byte (Byte Number 269). See Figure 6 for Write and Write Format Timing.

3.3.11 Format Mode Errors. Since Format Mode operations do not include the Address Read operation, the errors associated with Address Read, Address Compare Error, and Defective Track, cannot occur but Longitudinal Parity Error can occur.

3.3.12 Multi-Sector Records. The Disc Controller can transfer data into Records which extend over more than one sector.

The end of Data Transfer is determined by the SELCH. The only way to determine if the SELCH has finished is by trying to transfer another byte. If the SELCH responds with DA or DR, it has not ended.

There are three cases:

- SELCH stops before the sector ends.
- SELCH stops at the same time the sector ends.
- SELCH has more data to transfer when the sector ends.

The last case is the continue case; data remains after the sector is over and the data transfer operation must continue into the next sector.

3.3.13 Read Multi-Sector. At the beginning of Read Longitudinal Parity Check, near the end of a Read operation, CKCY1 (5L6) is set by RLDD01 (5N6). That same RLDD0 sets Data Request (4F8) and also sets CKCY2 (5M7). CKCY0 (4C9) prevents further Data Requests (4G6). If SELCH responds with DR, CNTDT resets Data Request (4F8). The 0 output of Data Request remains low until passing the Sector boundry, so the J input of the CONTINUE flip-flop (4H7) stays high. On the leading edge of CKCY20 (4C7), the CONTINUE flip-flop is set, indicating that more data remains to be transferred.

If CONT is set, Sector Compare is forced (5D9), Address Compare is disabled (6E5), and a Read or Read Format operation is started for the next sector. Operation continues in the new sector in the same manner as described for a one sector operation. See Figure 7 for Read Multi-Sector Timing.

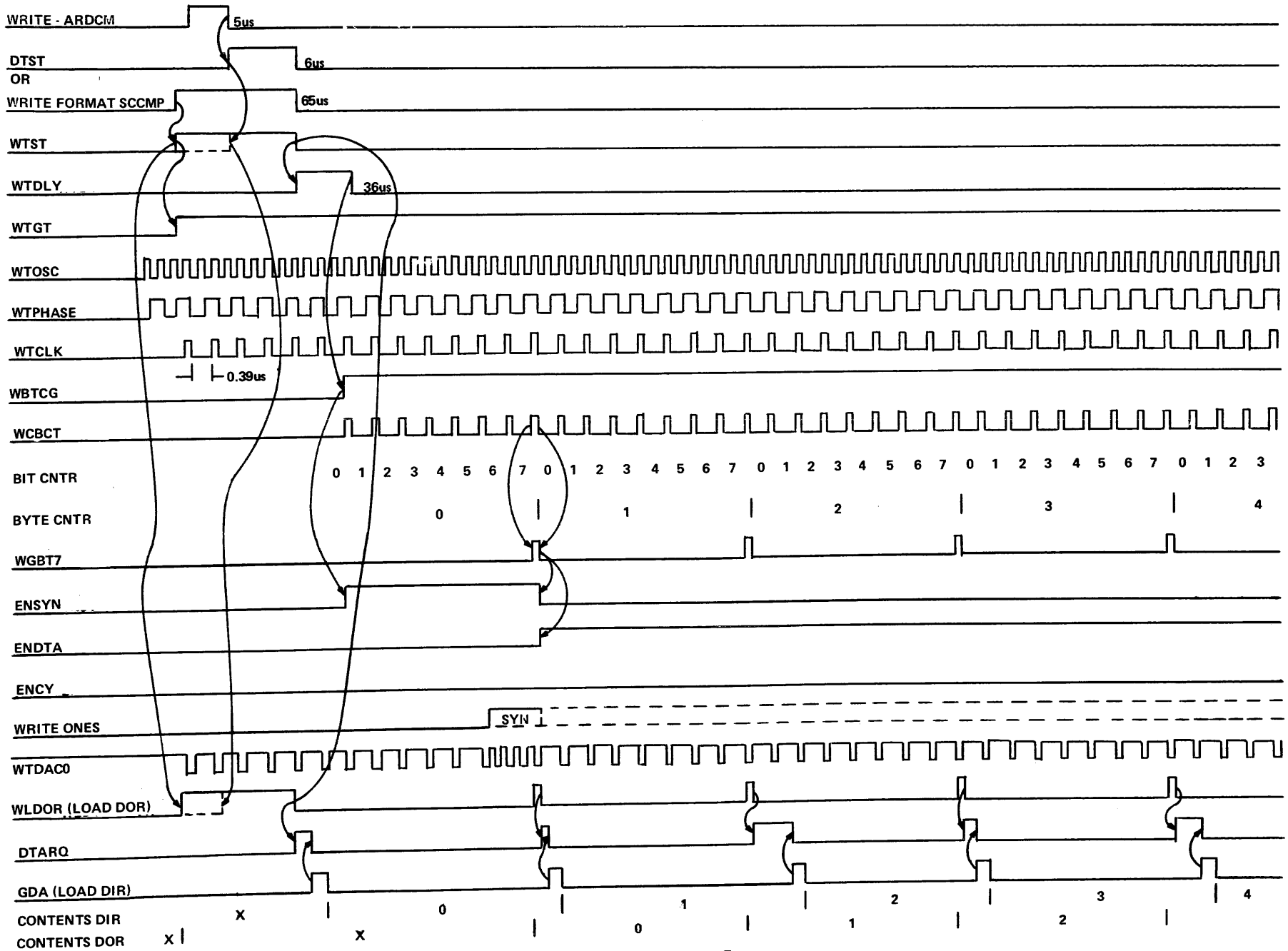
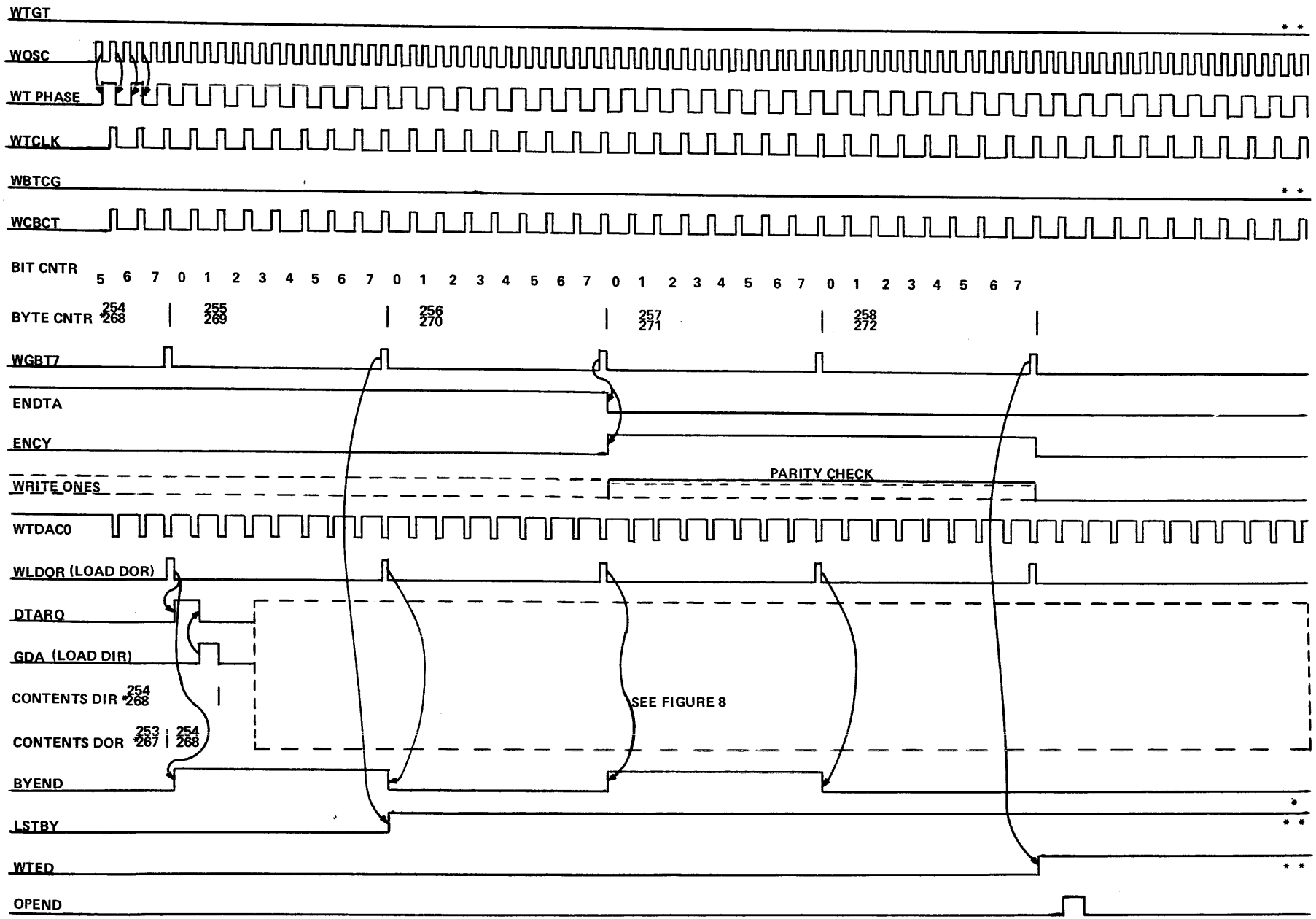


Figure 6. Write and Write Format



NOTES:

* UPPER NUMBER IS FOR WRITE
LOWER NUMBER IS FOR WRITE FORMAT

** RESET BY NEXT SECTOR MARK

Figure 6. Write and Write Format (Continued)

3.3.14 Write Multi-Sector. Near the end of a Write or Write Format operation, the signal Last Byte (LSTBY) (4C8) occurs during the last data byte before the Parity Check is written. It is set on the leading edge of WGBT71 (4A9). LSTBY1, ANDed with BYEND0 (4C8) blocks further data requests. Data Request is set on the trailing edge of WLDOR (4D7).

If SELCH has ended, it will not send a DA, so DTRQ (4F7) will not reset. WTED (4K6) triggers OPEND (4M6) which, if DTRQ is set, becomes OPCMP (4R7), ending the operation.

If SELCH has not ended, it responds with DA, which clears DTRQ (4F7). END1 (4K7) stays low and blocks OPEND (4N7) and CMPCL (4R7) does not occur. In this case WLSBY (4C7) sets Continue (CONT) (4H7). At the beginning of the next sector, SCCMP is forced (5H9) and address comparison is inhibited (6E5). Write or Write Format continues as described previously. See Figure 8 for Write Multi-Sector Timing.

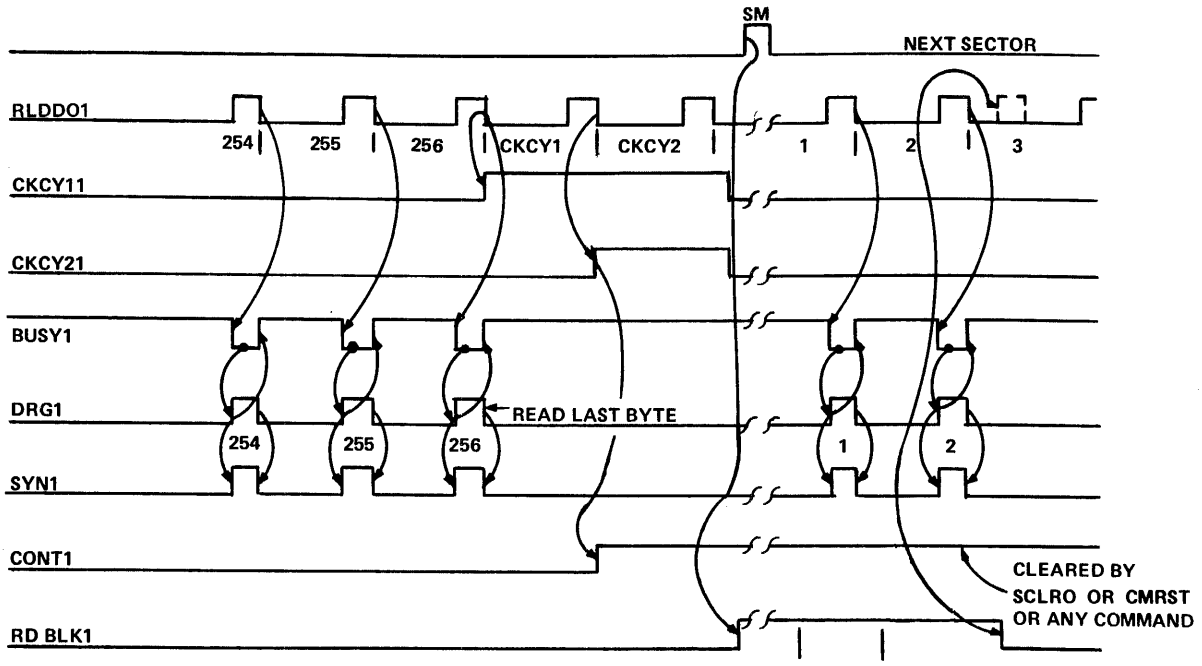


Figure 7. Multi-Sector Operation Timing Chart Read and Read Format

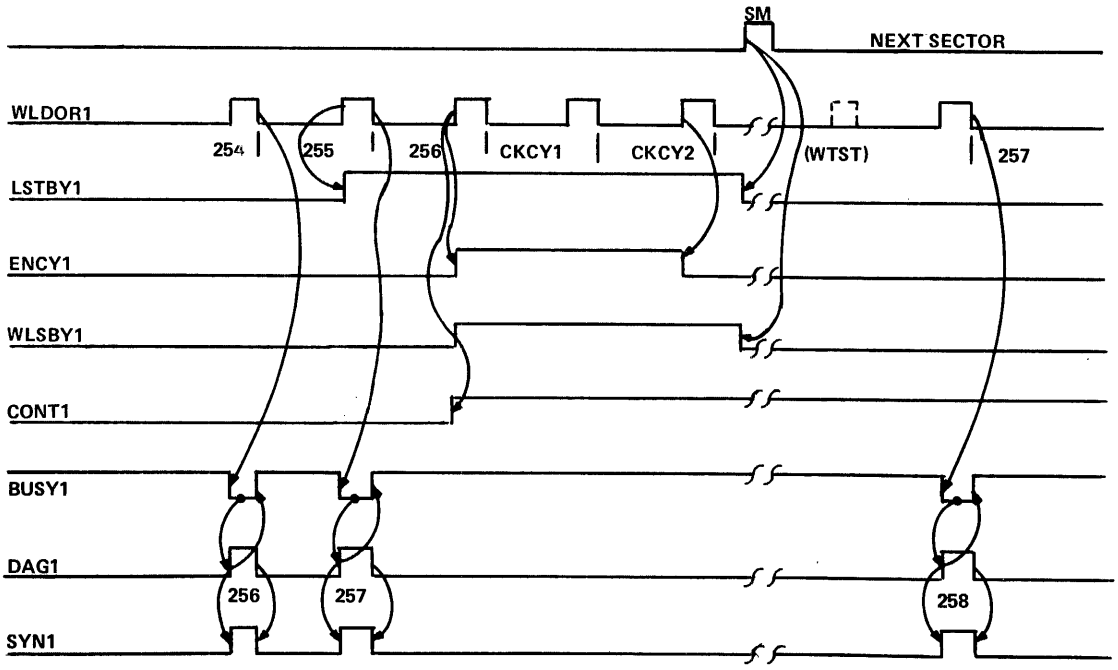


Figure 8. Multi-Sector Operation Write and Write Format

3.3.15 Automatic Head Switch. When in a multi-sector record, it may be necessary to switch from Head 0 to Head 1.

The Index Store (IDXST) flip-flop (5F1) is set by the Index Mark and reset by the trailing edge of the first Sector Mark (SM) after Index (5F2). The AND of IDXST, Sector Mark and Continue (XSMC) (4K8), sets the Head (HD) flip-flop (4C4). This can only occur if Continue is set, indicating more data, and at the first Sector Mark after Index. If HD was already set, it does not change. Instead, the signal Index Store, Sector Mark, and Continue (IXSMC) (6A2) set the Cylinder Overflow (CYLOF) flip-flop (6D2). CYLOF appears as an error and sets Examine (6H2). Examine inhibits Write (3E1), so that data on the disc is not changed.

3.3.16 Bit and Byte Counters. The Bit and Byte Counters are actually one combined 12 bit counter. The three least significant bits are the Bit Counter; the remainder is the Byte Counter. The counters are cleared by General Clear, Sector Mark, and Data Start (4G6); they count Write Count Bit Counter (WCBCT) and Read Count Bit Counter (RCBCT) (4G5) pulses. The outputs of the Bit Counter flip-flops are named B1, B2, and B4 (4J2). The Bit Counter is decoded to give two signals, Bit 3 (4L2) and Bit 7 (4L2). The Byte Counter is decoded to give two signals, Byte 269 (BY 269) (4L3) and Byte 255 (4N3). These signals are used to signal the end of a sector. CNT5 (4M3), which indicates that a Format Command is being executed, selects BY 269. Otherwise, BY 255 is selected.

3.3.17 Track Address. The Track Address (TA) drivers are shown at 5C5-5C7. Track Address comes from DIR (6K6-6K9) and Bit 7 of DOR (6R7).

3.3.18 Errors. Errors associated with Address Read are discussed in Section 3.3.5; Cylinder Overflow is discussed in the Section 3.3.15, "Automatic Head Switch". Overrun is the only other error. Overrun (6D4) is set whenever at least one full disc revolution has passed since a Data Controller Command and no Sector Compare (SCCMP) has occured. The two Counter flip-flops (6D4) are held reset when the Data Controller is Not Busy (CBSY) (6B5). When the Data Controller goes Busy, the Counters count Index Store (IDXST) (6C5), which goes true at Index and false at the end of the first Sector Mark after Index. If Sector Compare occurs, it resets the counters. The second flip-flop can be set by the first, but not reset. The usual cause of Overrun is calling for a Sector Number which is too large for the disc. See Figure 9 for Read and Write Gate ON-OFF Timing.

4. DEVICE ADDRESS STRAPPING

The preferred addresses for the Removable Cartridge Disc Controller are X'B6', X'C6', X'D6', X'E6', X'F6'. Wire-wrap stakes are available on the controller for address strapping. Refer to Functional Schematic 02-314D08 for details.

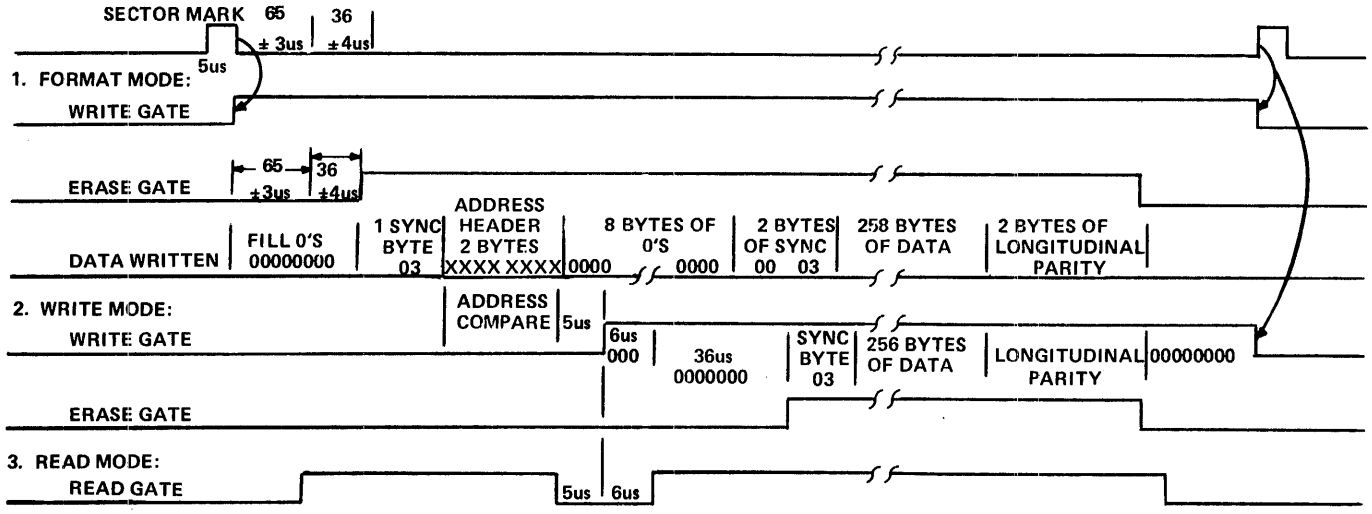


Figure 9. Read and Write Gate ON-OFF Timing Chart

5. ADJUSTMENTS

There are five adjustments required on the Controller. They are:

1. Read Delay
2. Write Delay
3. Guard Delay
4. Write Switching Delay
5. Sector Mark

Adjustment Procedures are:

1. Load test program 06-122 and run Test 8 (Spiral Data Test). Set the LOOP option to FFFF and turn off the TELETYPE while Test 8 is running.
2. Adjust Potentiometer R59, associated with the Sector Mark, for a time period of 5±1 microseconds. (Pin 5 of A56)
3. Adjust Potentiometer R61, associated with the Read Delay, for a time period of 65 ± 3 microseconds. (Pin 6 of A97)
4. Adjust Potentiometer R63, associated with the Write Delay, for a time period of 36±4 microseconds. (Pin 6 of A95)
5. Adjust Potentiometer R79, associated with the Guard Delay, for a time period of 5±1 microseconds. (Pin 13 of A139)
6. Adjust Potentiometer R66, associated with the Write Switching Delay, for a time period of 6±1 microseconds. (Look at Pin 5 of A107).

All Potentiometers decrease in value while turning counterclockwise.

6. MAINTENANCE

There is no maintenance required on the controller, however, there is preventive maintenance required on the disc drive. Refer to the Vendor Maintenance Manual 29-337 for maintenance procedures.

7. MNEMONICS

The following is a list of the Mnemonics found in the Removable Cartridge Disc system. The meaning and 02-314D08 Schematic source of each signal are provided.

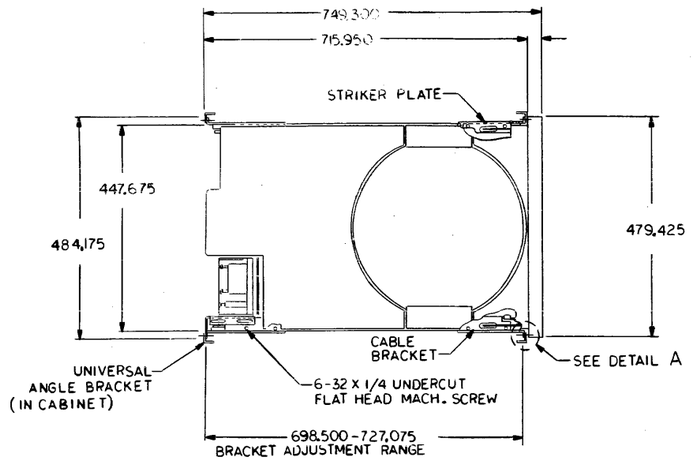
MNEMONIC	MEANING	LOCATION
ACMPF1	Address Compare Failure	6H4
ADAWK0	Address Acknowledge	3A6
ADAWK1	Address Acknowledge	3C6
ADRS0	Address	2F1
ADRS1	Address	2F3
ARDCM0	Address Read Complete	6H7
ARDGT0	Address Read Gate	6B6
ATEN1	Attention	6N1
ATN0	Attention	2A1
B11	Bit Counter Bit 1	4J2
B21	Bit Counter Bit 2	4J2
B41	Bit Counter Bit 4	4J1
BIT 31	Bit Counter Equals 3	4L2
BIT 71	Bit Counter Equals 7	4L2
BUSY0	Busy	3G3
BUSY1	Busy	3E3
BYEND0	Byte End	5S2
BYEND1	Byte End	4R3
CBSY1	Controller Busy	5M2
CEXAM0	Controller Examine	6H2
CEXAM1	Controlelr Examine	6H3
CKCY0	Cyclic Check	5S7

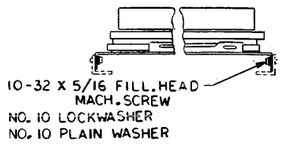
MNEMONIC	MEANING	LOCATION
CKCY1	Cyclic Check	5L6
CKCY20	Cyclic Check Two	5M7
CKDA1	Check Data	6R6
CL070	Power Failure Clear	3E1
CMD0	Command	2C1
CMG0	Gated Command	2C9
CMP11	Compare Byte 1	6G6
CMPCL0	Completed or General Clear	4R7
CNT50	Control 5 (A Format Command)	4C5
CNT51	Control 5 (A Format Command)	4D5
CNTAD0	Controller Addressed	2M8
CNTAD1	Controller Addressed	2M7
CNTCM0	Controller Command	2S8
CNTCM1	Controller Command	5M1
CNTDT0	Controller Data Transfer	2S7
CONT0	Continue	4H8
CRD1	Combined Read Command (Read or Read Check)	4E6
CTLGT1	Control Gate	2N8
CY2561	Cylinder Address 256	6K5
CYLOF1	Cylinder Overflow	6E2
CYOUT1	Cyclic Out	6G9
D080-D150	Data Lines 8-15	2M1-2G1
D080A-D150A	Data Lines 8-15	2M4-2G4
D081-D151	Data Lines 8-15	2M4-2G4
DA0	Data Available	2C1
DAG0	Gated Data Available	2C9
DAR41	Data Auxiliary Register Bit 4	4N9
DAR51	Data Auxiliary Register Bit 5	4N8
DAR61	Data Auxiliary Register Bit 6	4N8
DAR71	Data Auxiliary Register Bit 7	4N8
DAT081-DAT151	Data Bits 8-15	3S6-3S8
DATAOV1	Data Overflow	4H9
DDGRK0	Double Delayed Gated RACK0	6J2
DFTRK1	Defective Track	6E3
DIR001-DIR031	Data Input Register Bits 0-3	6L8
DIR041-DIR071	Data Input Register Bits 4-7	6M8
DISARM00	Disarm Disc 0	4H1
DISARM10	Disarm Disc 1	4H2
DISARM20	Disarm Disc 2	4H3
DISARM30	Disarm Disc 3	4H3
DOR001-DOR031	Data Output Register Bits 0-3	6N7
DOR041-DOR071	Data Output Register Bits 4-7	6R8
DOROT1	Data Output Register Out	6R7
DR0	Data Request	2D1
DRBCG0	Data Read Bit Counter Gate	5S8
DRBCG1	Data Read Bit Counter Gate	5S8
DRDGT0	Data Read Gate	5L7
DRDGT1	Data Read Gate	5L8
DRG0	Gated Data Request	2D9
DSKSEL0	Disc Select	4C2
DTARQ0	Data Request	4G6
DTST0	Data Start	5H7
DTXFER1	Data Transfer Error	6C1
ENBL01	Interrupt Enable Disc 0	4H1
ENBL11	Interrupt Enable Disc 1	4H2
ENBL21	Interrupt Enable Disc 2	4H4
ENBL31	Interrupt Enable Disc 3	4H3
END1	End	4G8
ENDTA0	Enable Data	5S2

MNEMONIC	MEANING	LOCATION
ENSYN1	Enable Sync	5S3
ERSGT0	Erase Gate	3F1
FA00	File Address	4C1
FA01	File Address	4C1
FA10	File Address	4C1
FA11	File Address	4C1
FILE1	File	2K9
FLAD1	File Addressed	2M8
FLSEL00	File Selected Disc 0	4E1
FLSEL10	File Selected Disc 1	4E1
FLSEL20	File Selected Disc 2	4E1
FLSEL30	File Selected Disc 3	4E2
FRDY00	File Ready Disc 0	3A7
FRDY10	File Ready Disc 1	3A7
FRDY20	File Ready Disc 2	3A8
FRDY30	File Ready Disc 3	3A8
FRDY0	File Ready	3H7
FRDY01	File Ready Disc 0	3C7
FRDY11	File Ready Disc 1	3C7
FRDY21	File Ready Disc 2	3C8
FRDY31	File Ready Disc 3	3C8
FRSRW00	File Ready to Seek, Read or Write Disc 0	3D6
FRSRW10	File Ready to Seek, Read or Write Disc 1	3D6
FRSRW20	File Ready to Seek, Read or Write Disc 2	3D6
FRSRW30	File Ready to Seek, Read or Write Disc 3	3D7
FRSRW01	File Ready to Seek, Read or Write Disc 0	3F6
FRSRW11	File Ready to Seek, Read or Write Disc 1	3F6
FRSRW21	File Ready to Seek, Read or Write Disc 2	3F6
FRSRW31	File Ready to Seek, Read or Write Disc 3	3F7
FRSRW1	File Ready to Seek, Read or Write	3H6
GCLR0	General Clear	2S6
GCMD1	Gated Command	2R8
HD0	Head 1 Selected	4C4
HD1	Head 1 Selected	4C3
HDSEL0	Head Select	3C1
HIDEN0	High Density	5F5
HIDEN1	High Density	5G5
IA01	Illegal Address Disc 0	3H2
IA11	Illegal Address Disc 1	3H3
IA21	Illegal Address Disc 2	3H3
IA31	Illegal Address Disc 3	3H4
IAADWK00	Illegal Address or Address Acknowledge Disc 0	3F3
IAADWK10	Illegal Address or Address Acknowledge Disc 1	3F3
IAADWK20	Illegal Address or Address Acknowledge Disc 2	3F4
IAADWK30	Illegal Address or Address Acknowledge Disc 3	3F4
IAD11	Interrupt Address 1	6S5
IAD21	Interrupt Address 2	6S5
IDXST1	Index Pulse Store	5G1
INAKC0	Interrupt Acknowledge Controller	6R1
INAKF00	Interrupt Acknowledge Disc 0	6N2
INAKF10	Interrupt Acknowledge Disc 1	6R3
INAKF20	Interrupt Acknowledge Disc 2	6N3
INAKF30	Interrupt Acknowledge Disc 3	6R4
INDTA1	In Data	5S9
INDTA1A	In Data	5N9
INDX0	Index Mark	5A1
INDX0A	Index Mark	5F1

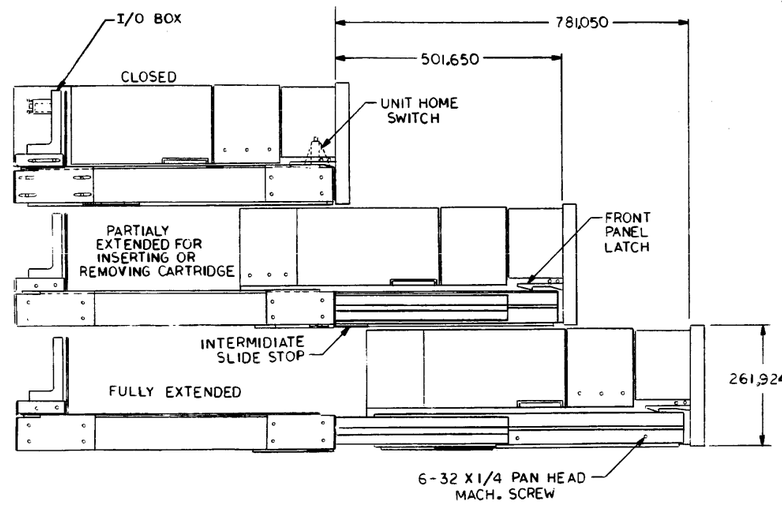
MNEMONIC	MEANING	LOCATION
IXSMC	Index • Sector Mark • Continue	4K8
IXSMC0A	Index • Sector Mark • Continue	6C2
LAI0	Logical Address Interlock	3A5
LSTBY1	Last Byte	4C8
NTROC1	Interrupt Request Controller	5R1
NTRQF01	Interrupt Request Disc 0	3N1
NTRQF11	Interrupt Request Disc 1	3N2
NTRQF21	Interrupt Request Disc 2	3N4
NTRQF31	Interrupt Request Disc 3	3N5
OPCMP0	Operation Completed	4R7
OPEND0	Operation End	4M7
OVERRUN	Overrun	6D4
PREAM	Preamble	5H3
RACK0	Receive Acknowledge	2B1
RACK0A	Receive Acknowledge	2B6
RCBCT0	Read Count Bit Counter	6G5
RD256END0	Read 256 Byte Ended	4J9
RDBLK0	Read Block	4K6
RDCLK0	Read Clock	5J9
RDCLK1	Read Clock	5J9
RDEND0	Read End	5S6
RDFOT1	Read Format	4F4
RDGT0	Read Gate	3C1
RDGT1	Read Gate	5R5
RDRFT1	Read or Read Format	4F5
RDTA0	Read Data	5J9
RDTAC0	Read Data Control	5S7
RDWT1	Read or Write	4F7
RLDD00	Read Load Data Output Register	6K5
RLDD01	Real Load Data Output Register	5N6
RSTR0	Restore	3D2
SCCMP0	Sector Compare	5H9
SCCMP1	Sector Compare	5H9
SCLR0	System Clear	2E1
SCLR0A	System Clear	2E4
SEC10	Sector Counter Bit 1	5A2
SEC20	Sector Counter Bit 2	5A2
SEC40	Sector Counter Bit 4	5A3
SEC80	Sector Counter Bit 8	5A3
SEC160	Sector Counter Bit 16	5A4
SEC320	Sector Counter Bit 32	5A4
SEC11	Sector Counter Bit 1	5C2
SEC21	Sector Counter Bit 2	5C2
SEC41	Sector Counter Bit 4	5C3
SEC81	Sector Counter Bit 8	5C3
SEC161	Sector Counter Bit 16	5C4
SEC321	Sector Counter Bit 32	5C4
SECLR0	Sector Mark + Operation Completed + General Clear	5K3
SHDIR0	Shift Data Input Register	5N7
SKINC00	Seek Incomplete Disc 0	3D7
SKINC10	Seek Incomplete Disc 1	3D8
SKINC20	Seek Incomplete Disc 2	3D8
SKINC30	Seek Incomplete Disc 3	3D8
SKINC01	Seek Incomplete Disc 0	3F7
SKINC11	Seek Incomplete Disc 1	3F8
SKINC21	Seek Incomplete Disc 2	3F8
SKINC31	Seek Incomplete Disc 3	3F8
SKINC1	Seek Incomplete	3K7
SM0	Sector Mark	5A2

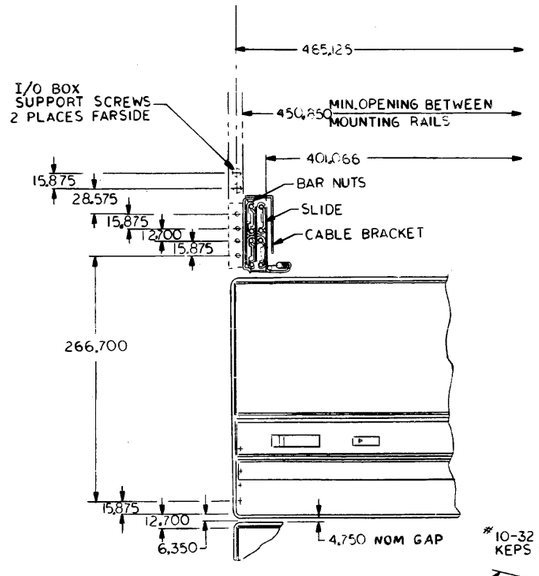
MNEMONIC	MEANING	LOCATION
SM1	Sector Mark	5E3
SMCLR0	Sector Mark + General Clear	5H2
SR0	Status Request	2D1
SREQ0	Selch Request	2A1
ST081-ST151	Status Bits 8-15	3M8-3M6
STCLR0	Controller Start or General Clear	5K1
STRB0	Strobe	3H1
SYN0	Sync to Computer	2E9
SYNDT1	Synch Character Detected	6B6
TA10	Track Address 1	5C4
TA20	Track Address 2	5C5
TA40	Track Address 4	5C5
TA80	Track Address 8	5C5
TA160	Track Address 16	5C6
TA320	Track Address 32	5C6
TA640	Track Address 64	5C7
TA1280	Track Address 128	5C7
TA2560	Track Address 256	5C7
TACK0	Transmit Acknowledge	2A6
TERM0	Terminate	2B1
WAWFT1	Write or Write Format	4F6
WBTCG1	Write Bit Counter Gate	5M2
WCBCT0	Write Count Bit Counter	5S3
WCYCK	Write Clock	5S5
WGBT71	Write Gated Bit 7	5N4
WLDOR	Write Load Data Output Register	5S4
WLDOR0	Write Load Data Output Register	5G8
WLSBY1	Write Last Byte	4C7
WRTCK0	Write Check	3A6
WRTCK1	Write Check	3C6
WT1	Write Command	4F6
WTCLK1	Write Clock	5M3
WTDAC0	Write Data and Clock	5S4
WTDTA0	Write Data	5L6
WTED0	Write End	4D8
WTFOT1	Write Format	4F5
WTGT0	Write Gate	3F1
WTGT0A	Write Gate	3G1
WTGT0A + CBSY0	Write Gate + Controller Busy	3K9
WTGT1	Write Gate	5L2
WTPT0	Write Protect	3A6
WTPT1	Write Protect	3C6
WTST0	Write Start	5H8
XFER1	Transfer	2C7
Y11	Byte Counter Bit 1	4K3
Y21	Byte Counter Bit 2	4K4
Y41	Byte Counter Bit 4	4K4
Y81	Byte Counter Bit 8	4K4
Y161	Byte Counter Bit 16	4M4





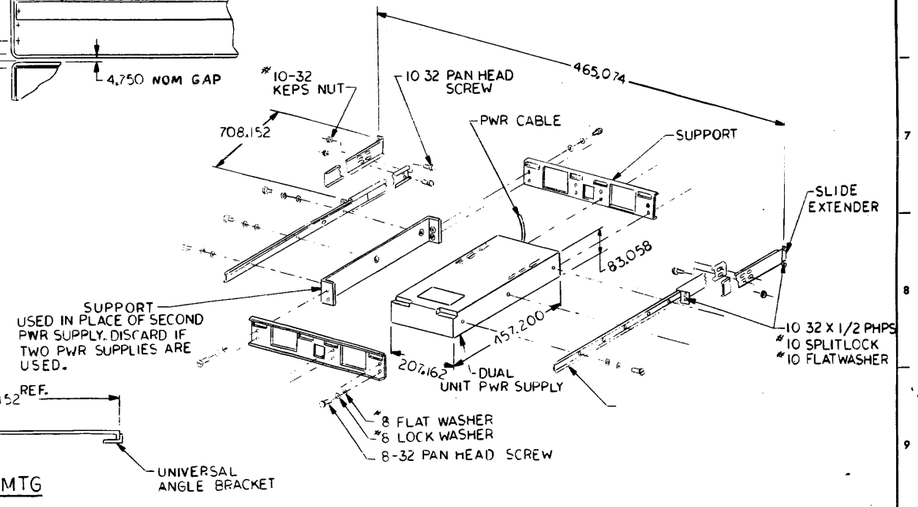
DETAIL A





MILLIMETER	INCH
749.300	29.500
715.950	28.187
447.675	17.625
484.175	19.062
479.425	18.875
698.500	27.500
727.075	28.625
781.050	30.750
501.650	19.750
15.875	.625
28.575	1.125
12.700	.500
266.700	10.500
6.350	.250
4.750	.187
465.125	18.312
450.850	17.750
401.066	15.790
465.074	18.310
708.152	27.880
83.058	3.270
457.200	18.000
207.162	8.156
479.425	18.875
749.300	29.500
261.924	10.312
40.823 kg	90 lb.

METRIC



SLIDE MTG

PHYSICAL DATA

WIDTH —— 479.425
DEPTH —— 749.300
HEIGHT —— 261.924
WEIGHT —— 40.823 kg

NOTES:

1. IF ELECTRONIC CABINET SIDE PANELS ARE DETACHABLE, SLIDE MOUNTING AS SHOWN IN DETAIL "A" IS RECOMMENDED.
2. BEFORE MOUNTING SLIDES IN CABINET AS SHOWN IN DETAIL "A", SLIDES SHOULD BE DETACHED FROM DISK FILE IN THE FOLLOWING MANNER:
   A. BY DEPRESSING INTERMEDIATE SLIDE STOPS LOCATED UNDER SLIDES MOVE SLIDES TO FULLY EXTENDED POSITION.
   B. REMOVE 6-32 X 1/4 PAN HEAD MACH SCREW FROM SLIDES (4 PLACES)
   C. REMOVE 6-32 X 1/4 UNDERCUT FLAT HD MACH SCREW FROM CABLE BRACKET (4 PLACES) (SAVE BAR NUTS)
   D. MOVE CABLE BRACKET BACK INTO DISK FILE.
   E. DISK FILE CAN NOW BE LIFTED FROM SLIDES.
3. SECURE SLIDES INTO CABINET.
   A. BRING SLIDES TO FULLY EXTENDED POSITION.
   B. PLACE DISK FILE ON SLIDES AND FASTEN WITH 6 32 X 1/4 UNDERCUT FLAT HD. MACH. SCREW.
   C. PLACE CABLE BRACKET ON SLIDES AND FASTEN WITH 6-32 X 1/4 UNDERCUT FLAT HD. MACH SCREW.
   D. ADJUST SLIDE MOUNTINGS SO FRONT PANEL FITS IN PROPER POSITION WITHIN CABINET.
4. ADJUST STRIKER PLATE (RIGHT) AND CABLE BRACKET (LEFT) SO THAT FRONT PANEL LATCH WILL ENGAGE WHEN LIGHT PRESSUR IS APPLIED TO FRONT PANEL.
5. AFTER FRONT PANEL LATCH, CABLE BRACKET, AND STRIKER PLATE ARE ADJUSTED; ADJUST UNIT HOME SWITCH. LOOSEN 4-40 X 1/4 PAN HEAD MACH. SCREWS AND ADJUST SWITCH FOR .030 TO .090 OVERTRAVEL, THEN TIGHTEN SCREWS.

NOTES

NAME	TITLE	DATE	TITLE INFORMATION DWG
REDWARDS	DRAFT		DISK FILE & POWER SUPPLY DISK CONTROLLER
K. HUNTER	CHK		
J. YANG	ENGR	1/	TASK NO. 03042 SHEET OF
H. [illegible]	O.C.		DWG NO. 02-314 D12 1-1
J. PISARCIN	ENG		

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

SHEET LOCATION	ROW 2	TERM. NO.	ROW 1	SHEET LOCATION
3A6	WTPTO	24	SKINC00	3D7
3A6	WRTCKO	23	FRDY00	3A7
	GND	22	RDGTO	3C1
	GND	21	FRSRW00	3D6
3A6	ADAWKO	20	LAIO	3A5
	GND	19	RSTRO	3D2
	GND	18	HDSELO	3C1
3F2	ERSGTO	17	WTGTO	3F1
	GND	16	STRBO	3J1
	GND	15	RDTAO	5J9
	GND	14	INDXO	5A1
	GND	13	SMO	5A2
	GND	12	SEC4O	5A3
5A2	SEC1O	11	SEC2O	5A2
5A4	SEC32O	10	SEC8O	5A3
	GND	09	SEC16O	5A4
	GND	08	RDCLKO	5J9
	GND	07	WDTACO	5S4
	GND	06	TA64O	5C7
5C7	TA256O	05	TA128O	5C7
5C5	TA2O	04	TA4O	5C5
5C5	TA8O	03	TA1O	5C4
	GND	02	TA16O	5C6
5F5	HIDENO	01	TA32O	5G6
4C2	DSKSELO	00	FLSELO	4E1

CONN 3

CABLE CONNECTOR

SHEET LOCATION	ROW 2	TERM NO.	ROW 1	SHEET LOCATION
	GND	00	FRSRW10	3D6
		01	FRDY10	3A7
		02	SKINC10	3D8
		03	FLSEL10	4E2
		04	GND	
		05	FR6RW20	3D6
		06	FRDY20	3A8
		07	SKINC20	3D8
		08	FLSEL20	3D8
		09	GND	
		10	FRSRW30	3D7
		11	FRDY30	3A8
		12	SKINC30	3D8
		13	FLSEL30	4E2
	GND	14	GND	

CONN 2

CABLE CONNECTOR

BACK PANEL MAP

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
	P5	41	GND	
	GND	40	GND	
		39		
		38		
		37		
		36		
		35		
		34		
		33		
		32		
		31		
		30		
		29		
		28		
		27		
2E1	SCLRO	26		
		25	SREQO	2A1
2D1	XFERO	24	TERMO	2B1
2E9	SYNO	23	ATNO	2A1
2B1	RACKO	22	TACKO	2B7
3E1	CLO7O	21	DAO	2C1
2D1	DRO	20	CMDO	2C1
2D1	SRO	19	ADRSO	2F1
2H1	DI4O	18	DI5O	2G1
2J1	DI2O	17	DI3O	2H1
2L1	DI1OO	16	DI1O	2K1
2M1	DO8O	15	DO9O	2L1
		14		
		13		
		12		
		11		
		10		
		09		
		08		
		07		
		06		
		05		
		04		
		03		
		02		
	GND	01	GND	
	P5	00	GND	

CONN 1

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
	P5	41	GND	
	GND	40	GND	
	GND	01	GND	
	P5	00	GND	

CONN 0

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. ____ DATE 4/1/73

REVISED SHT'S 4 & 5
35-438 M01 WAS R01
BG [illegible] 1963 [illegible] R01

REVISED SHT'S 4 & 5
35-438 M01 WAS R03
BG [illegible] 2203 ✓ 9-5-74 R02

REVISED SHT'S 2,3,5 & 6
35-438 M01 WAS R04
35-438 F01/M01 WAS R03
JC WC 2613 ✓ 10-1-75 R03

REVISED SHTS 1 THRU 6.
35-438 F01/M01 WAS R04
REMOVED 35-438 M01 R06 FROM TABLE BELOW
TITLES ON ALL SHTS. WAS 44 SERIES D.I.C.
PE JC 2614 — 10-15-75 R04

REVISED SHT'S 1, 2 AND 5.
35-438 F01 M01 WAS R05.
FM MJ 3443 10-25-77 R05

REVISED SHT'S 1 THRU 6.
35-438 F01/M01 WAS R06.
AREA M9. ADDED MANUAL NO. 29-335.
WH MJ 3613 M 10-6-78 R06

REVISED SHT'S. 1 & 5
SHT. 1 AREA S9 35-438 F01 M01 WAS R07
BP MJ 3886 R 5-16-79 R07

PRINTED CIRCUIT BOARDS BEARING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

DISK CONTROLLER	35-438 F01/M01 R08

USED IN MANUAL 29-335

NOTE
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX							
	REV. LEVEL	7	1			7	
	SHEET NO.	1	2	3	4	5	6

NOTES
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, ±5%.

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-30-73
H. MATTER	CHK	7-23-73
J. YANG	ENGR	7-31-73
N. MASSI	TEST	7-31-73
J. PISARCIK	MGR	7-31-73

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER
10 MEGABYTE DISC
TASK NO. 03042
DRAWING NO. 02-314 R07 D08
SHEET 1 OF 6

DRAWING 66 233 10063

PERKIN-ELMER
Computer Systems Division

REVISIONS				
AREA R5, GATES A112 & A103 AND RELATED CIRCUITRY WERE NOT SHOWN.				
PM	2613	—	10-1-75	R01
TITLE WAS 44 SERIES DISC				
PM	2614	—	10-15-75	R02
AREA E7, REMOVED 2 A19DPS, WHICH WAS CONN BETWEEN A21-08 & A10-09 AREA E8 A9-10 WA. CONN. TO A9-09. AREA F2 TO A22 & A21 WERE 19-036 HPO (8 PLS.)				
PM	3443		10-25-77	R03
AREA G7; A18, 19-024 WASN'T SPEC. A29-13 WAS CONN. TO A18-01				
PM	3613	M	10-6-68	R04

P5 — GND
15MF, 20V TANTULUM
C17-C25

P5 — GND
1000PF, 50V
C26-C122

DECOUPLING CAPACITORS

NOTES
1. NORMALLY STRAPPED FOR X'86', X'C6', X'DC', X'E6', X'F6'.
2. STRAPPED FOR 2800 BPI DISC.

NAME	TITLE	DATE
K LAFFERTY	DRAFT	5-30-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER
10 MEGABYTE DISC
TASK NO 03042
DWG NO 02-314 REV: D08
SHEET OF 2 —

BRUNING 44 231 18042

PERKIN-ELMER
Computer Systems Division

REVISIONS				
AREA E1, CONN. ENS WAS NOT SPECD.				
SF	RC	2613	10-9-75	R01
TITLE WAS 44 SERIES DISC				
PC	RC	2614	10-15-75	R02
AREA E2, F2, G2 & G4: ADDED A170, A172 & A169, R84-R88, C124. REMOVED A2 & C4. SEE R02 MICRO-FILM FOR PREVIOUS CONFIGURATION.				
WT A		3613	M 10-6-78	R03

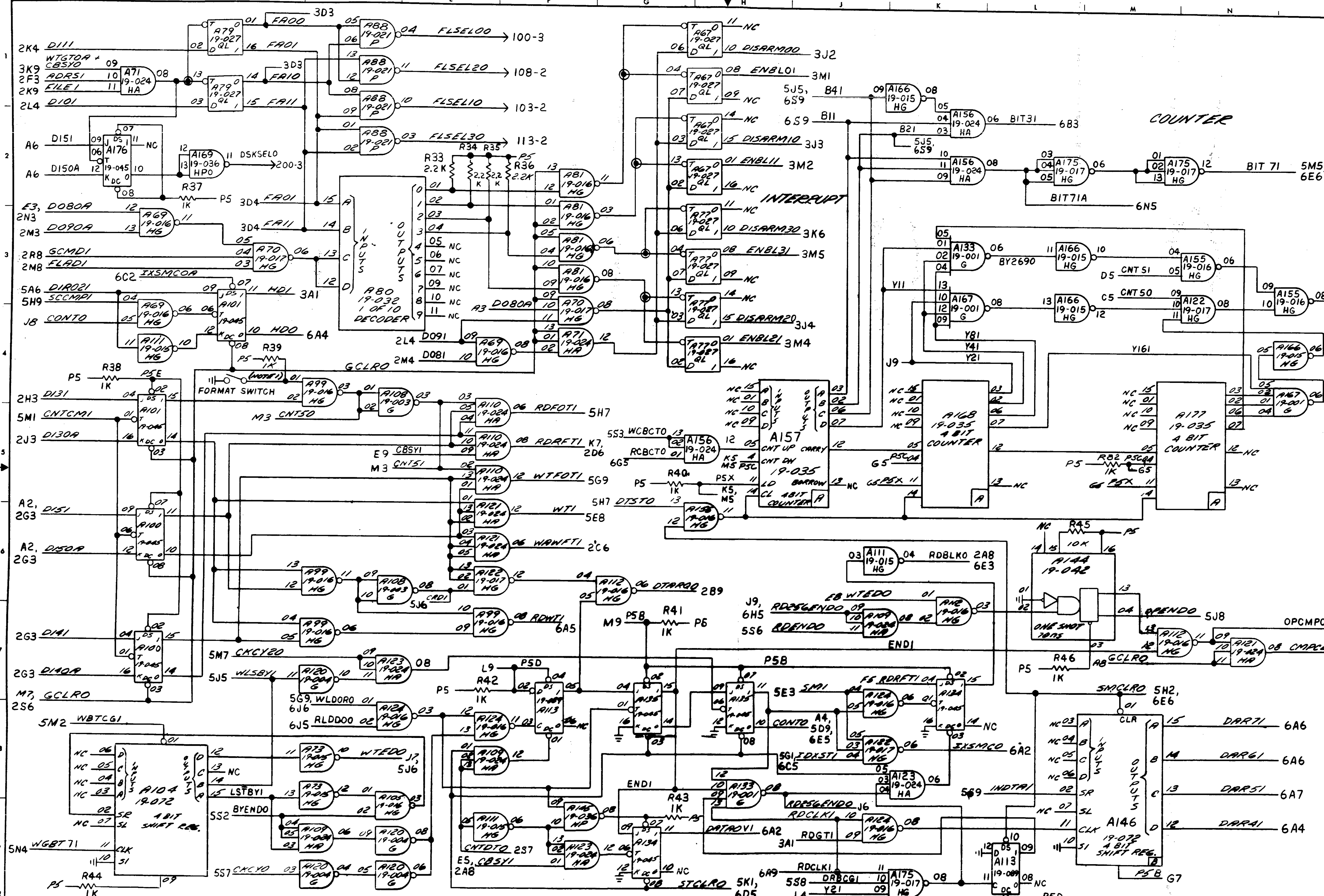
NOTES

NAME		
DRAWN	FLOWARDS	5-30-73
CHECKED		
ENGR		
MFG		

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER
10 MEGABYTE DISC
03042
02-314 203 D08 3

RUNNG 44-231 16042

PERKIN-ELMER
Computer Systems Division



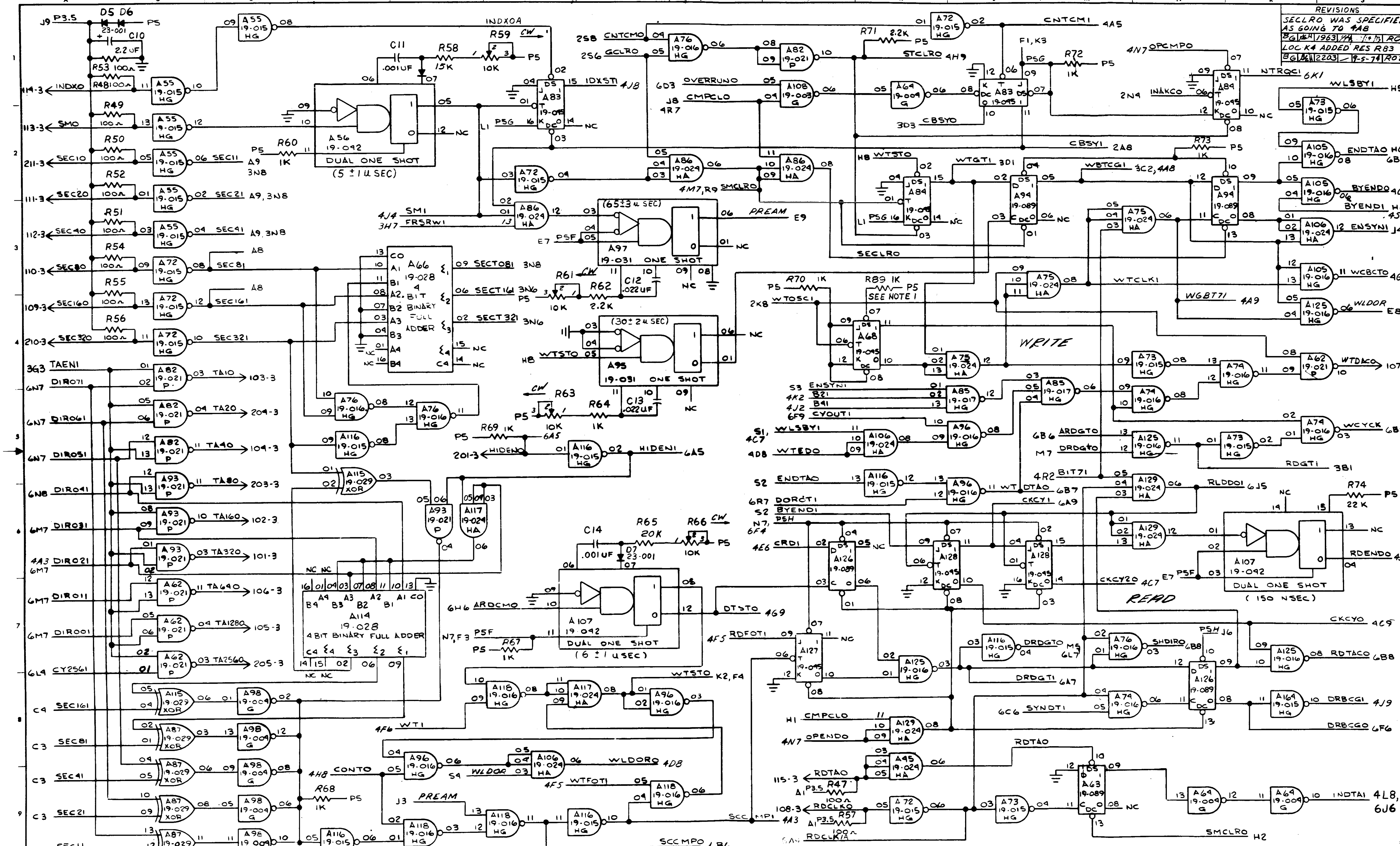
REVISIONS
LOC A8 WBTCG1 WAS SECLR0; LOC C8 DASH WAS NOT SPECIF OVER LSTBY1 — 1963 — 8/10/73 — R01
LOC M5 ADDED RES R82 — 2E03 — 4-5-74 — R02
TITLE WAS 44 SERIES DISC — 2614 — 10-15-75 — R03
AREA J9: REMOVED SHT LOC. 5J9 FROM MNEMONIC "RDCLK1" — 3613 — M — 10-6-76 — R04

NOTES
1. FORMAT SWITCH OPEN — FORMAT MODE
FORMAT SWITCH CLOSED — NORMAL MODE

NAME	TITLE	DATE
P. EDWARDS KL	DRAFT	5-30-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC DISK CONTROLLER 10 MEGABYTE DISC
03042
02-314 R04 D08 — SHEET 4 OF —

PERKIN-ELMER
Computer Systems Division



REVISIONS				
SECLRO WAS SPECIFIED AS GOING TO 4A8				
BG	1963			R01
LOC K4 ADDED RES R83				
BG	2203		9-5-74	R02

REVISIONS
AREA E1, R58 WAS 10K.
AREA G6, R65 WAS 15K.
2615 10-1-75 R03
AREA G3: A95 WAS 36 ± 4 u SEC. AREA K3:

A94-01 WAS TO A86-08
TITLE WAS 44 SERIES DISC
2614 10-15-75 R04
AREA A4, ADDED GATE A08-08 & 09. AREA M2 ADDED A4 TO CBSY1. AREA B4-B7

A62-06 WAS CONN TO A62-05
A62-02 WAS CONN TO A62-01
A62-01 WAS A62-02
A62-02 WAS A62-01
PM 3443 10-24-77 R05
AREA A4, REMOVED A08 FROM A22-01 A08-07 FROM A94-05

"TAENI" & SHT LOC 3G3 WAS NOT SPEC'D AREA M2: MNEM WBTCG1" SHT LOC 3C2 WAS 3F2
A68-09. AREA J9. RDCLK1A, 6A9 WAS SPEC AS RDCLK1, 4J9.

TA 3613 M 10-6-78 R06
A68-07 WAS CONN TO A
ADDED R89 TO A
ADDED NOTE 1.

NOTE 1. A68-07 ISOLATE TO FACILITATE AUTOMATIC TESTING.

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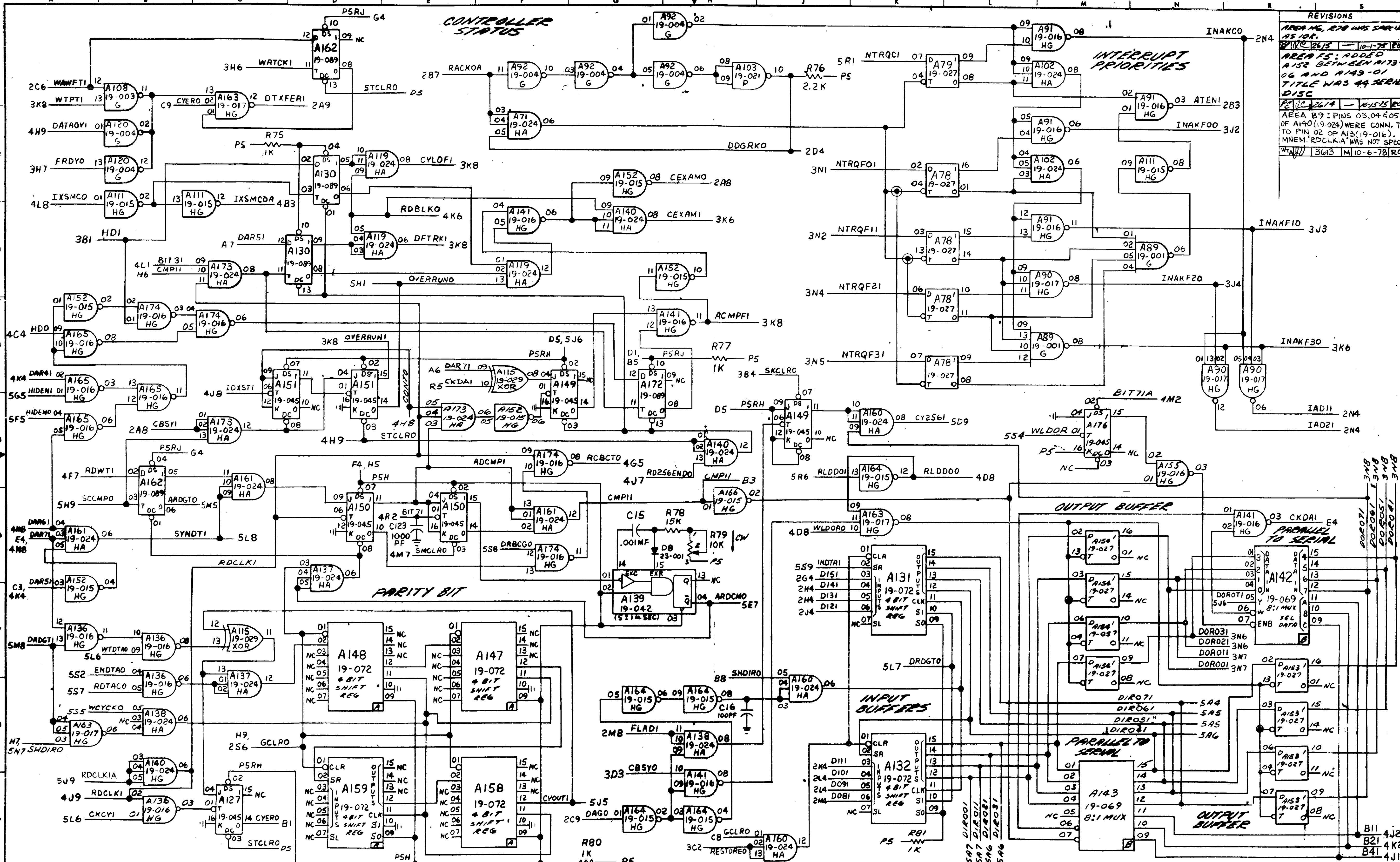
NAME: C. JENSEN KL
DRAFT DATE 5-30-73

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER
10 MEGABYTE DISC
TASK NO. 03042
02-314 R07 D08
SHEET 5 OF 6

PERKIN-ELMER

Computer Systems Division



REVISIONS					
AREA H6, R78 WAS SPEC'D AS 10K.					
		2615	—	10-1-75	R01
AREA F5: ADDED A152 BETWEEN A173-06 AND A149-01 TITLE WAS 44 SERIES DISC					
PE		2614	—	10-15-75	R02
AREA B9: PINS 03,04 & 05 OF A140(19-024) WERE CONN. TO TO PIN 02 OF A13(19-016). MNEM. "RDCLKIA" WAS NOT SPEC'D					
		3613	M	10-6-78	R03

NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	2-26-73
	CHK	
	ENGR	
	DIR ENG	

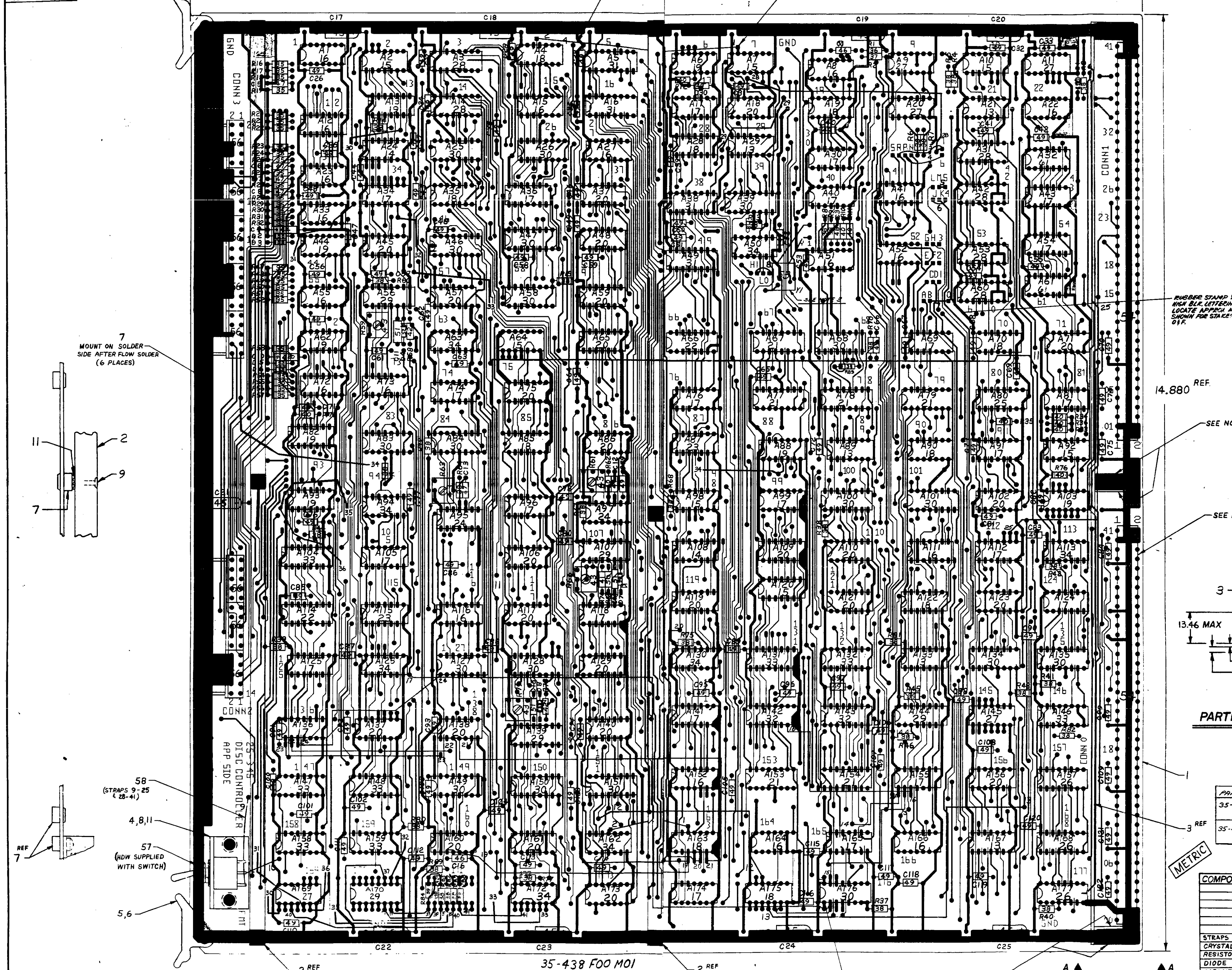
TITLE FUNCTIONAL SCHEMATIC DISK CONTROLLER 10 MEGABYTE DISC

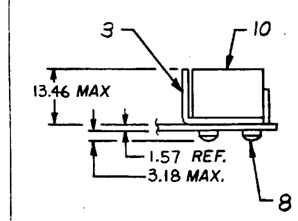
NO. 03042

02-314 R03 D08

SHEET OF 6-6

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530





PARTIAL VIEW A-A

REVISIONS

UNDER A107 - CHANGED SIZE OF R65 & C14 WAS SPECIFIED AS ITEM 50, ADDED C123 NEAR A150.				
KL		3021-02	5-1-73	R01
ADDED STRAPS 11 THRU 24; ON ITEM 57, MOVED LOCKWASHER TO HEX NUT SIDE OF SWITCH.				
BG		3021-004	6-8-73	R02
RELEASED FOR PRODUCTION MFG. ENG. DATE				
REVISED TO REFLECT NEW COPPER				
BG		1963	10/29/73	R03
STRAP 15 WAS WIRED TO A176-14.				
GJH		2004	1-2-74	R04
MOVED CRYSTAL TO RELIEVE STRESS ON LEADS. CHANGED NOTE 3.				
GJH		2025	1-2-74	R05
ADDED R82 & R83				
BG		2203	9-10-74	R06
STRAP 25 WAS NOT SPEC'D, REVISED TO REFLECT NEW COPPER, AREA A56, R58 WAS SPEC'D AS ITEM 39, AREA A107, R65 WAS SPEC'D AS ITEM 42, & AREA A139, R78 WAS SPEC'D AS ITEM 39				
		2615	10-7-75	R07
SHT 2 & VARIATION BLOCK WERE NOT SPEC'D				
		2636		R08
SHT 2, AREA A94: CUT UNDERNEATH A94 WAS SHOWN INCORRECTLY				
TA		2831	10-8-76	R09
SHT 1 & 2 REMOVED C2 ITEM 59 & REVISED TO REFLECT NEW (R06) COPPER, SHT 1 - ADDED STRAP # 26 & 27 SHT 2 ADDED STRAP # 30 & 31 SHT 1 & 2 - I.C. A32 WAS ITEM 27 AND I.C. A61 WAS ITEM 27.				
PM		3443	11-5-77	R10
REVISED CIRCUITRY TO REFLECT NEW COPPER. SHT 1, REMOVED STRAP # 26 FROM A8-08 TO A62-13. SHT 2, REMOVED STRAP # 30 FROM A8-08 TO A62-13. SHTS. 1 & 2: ADDED I.C A170. AREA A171; ADDED RES. R84 - R88, CAP C124. REMOVE R83 BELOW A68 & A69. SHT. 1, ADDED STRAPS 28 - 41. SHT 2, ADDED STRAPS 32-45. ADDED METRIC DIM. & TABLE. REMOVED STRAP # 27 FROM A8-09. SHT. 2 REMOVED STRAP # 31 FROM A8-09.				
		3613	M 10-4-78	R11
ADDED RESISTOR R89 TO A68				
BFP		3886 R	5-4-79	R12

PART NO.	VARIATION	
35-438M01	F00	PER SHT 1
35-438M01	F01	PER SHT 2

SCALE 2:1

COMPONENT	REF DESIGNATION
STRAPS	1-25, 28-41
CRYSTAL	Y1
RESISTOR	R1-R82, R84-R89
DIODE	D1-D82,
CAPACITOR	C1, C3, C5-C124
INT CIRCUIT	A1-A170, A172-A177

NOTES:

1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. CRYSTAL (ITEM 53) MUST BE SECURED TO BOARD WITH TWO-SIDED TAPE. THE LEADS MUST BE SLEEVED

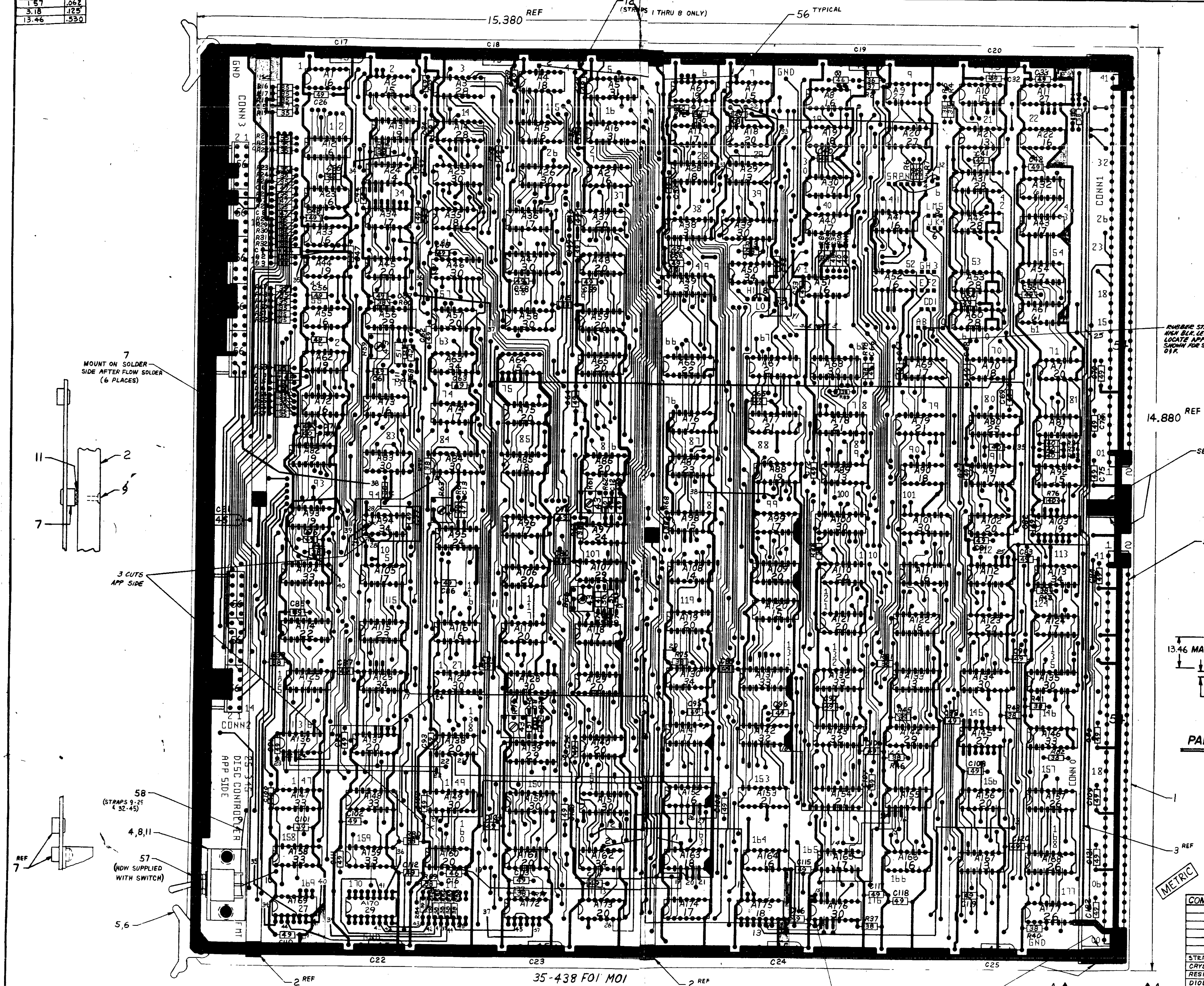
	TITLE	DATE
K. LAFFERTY	DRAFT	3-7-73
H. MATTER	CHK	3-29-73
J. YANG	ENG	3-19-73
H. ROSS	Q.C.	7-2-73
J. PISARCIK	MGR	7-2-73

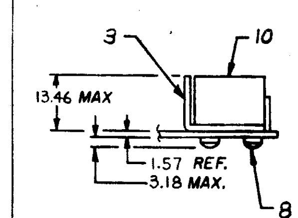
ASSEMBLY CARTRIDGE DISK CONTROLLER

TASK NO. 03021 — DWG NO. 35-438M01 R12 E03 — SHEET 1 OF 2

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530

REVISIONS





PARTIAL VIEW A-A

METRIC

SCALE 2:1

COMPONENT	REF DESIGNATION
STRAPS	1-29, 32-45
CRYSTAL	Y1
RESISTOR	R1-R82, R24-R89
DIODE	D1-D82,
CAPACITOR	C1, C3, C5-C124
INT CIRCUIT	A1-A170, A172-A177

	TITLE	DATE	
K. LAFFERTY	DRAFT	3-7-73	ASSEMBLY CARTRIDGE DISK CONTROLLER
H. MATTER	CHK	3-29-73	
J. YANG	ENG	3-29-73	
H. ROSS	Q.C.	7-2-73	TASK NO. 03021
J. F. [illegible]	M.F.R.	7-2-73	DWG NO. 35-438M01RK E03 — SHEET 2 OF 2

NOTES:

1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. CRYSTAL (ITEM 53) MUST BE SECURED TO BOARD WITH TWO SIDED TAPE. THE LEADS MUST BE SLEEVED.

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