

**HIGH SPEED
PAPER TAPE READER/PUNCH
PROGRAMMING MANUAL**

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HIGH SPEED PAPER TAPE READER/PUNCH PROGRAMMING MANUAL

INTRODUCTION

This manual provides information on the operation and programming of the M46-250 combination High Speed Paper Tape Reader/Punch Interface, which supports the M46-240 Paper Tape Reader or the M46-242 Paper Tape Reader/Punch. Note that with this Interface, the PTR/P cannot read and punch tapes simultaneously.

Table 1 lists the general characteristics of the Reader and Punch.

TABLE 1. READER AND PUNCH CHARACTERISTICS

CHARACTERISTICS	READER	PUNCH
Type	Photo-electric	Electro-mechanical
Tape Width	Fixed width of 1 inch	Fixed width of 1 inch
Speed	Maximum of 300 characters-per-second	Maximum of 75 characters-per-second
Tape handling	Oiled or unoled paper, paper-mylar, mylar, and aluminum mylar	Same as the Reader
Stop time	Capable of stopping on a character	Punches character and stops
Read/Load Switch	Allows loading or changing of tapes	Same as the Reader
Power Switch	Applies AC power to Reader motor	Applies AC power to Punch motor

CONFIGURATION

The M46-242 High Speed Paper Tape Reader/Punch, and the M46-240 Paper Tape Reader only, with the M46-250 Interface, require any basic new series Processor configuration. No particular Processor options are necessary. The device is normally used on the Multiplexor Bus.

The HSPTR/P operates in two separate modes (Reader, Punch) and should be programmed as such. The mode (Reader, Punch) is determined by the last OC instruction given.

OPERATING PROCEDURES

Punch Front Panel

The Punch front panel contains three control switches. They are:

1. **POWER.** This rocker switch turns power ON or OFF to the Punch. It lights in the ON position.
2. **FEED.** This momentary rocker switch causes the unit to feed tape through the punch mechanism, sprocket holes are punched, but data is inhibited. Note that operation of this switch in conjunction with external input on the punch line is not allowed and can cause erratic punching.
3. **RUN/LOAD.** This lever, when in the RUN position, allows operation of the punch mechanism. When in the LOAD position, it disengages the pinch roller from the capstan on the punch mechanism.
4. **DELETE.** This momentary rocker switch causes the unit to punch holes in all channels.

Reader Control Switches

The reader mechanism contains three control switches. They are:

1. **POWER.** This switch turns power ON or OFF to the reader.
2. **RUN/LOAD.** This switch, which is activated by the tape access door, allows the Reader to operate when the door is closed and inhibits Reader operation when the door is open.
3. **DIRECTION CONTROL.** This momentary rocker switch enables the user to manually back up or advance the paper tape. Note that the operation of this switch, in conjunction with external input on the Punch line, is not allowed and can cause erratic punching.

DATA FORMAT

Reader

The High Speed Paper Tape Reader is a byte buffered device capable of reading up to eight channels on a paper tape.

Punch

The High Speed Paper Tape Punch is a byte buffered device capable of punching up to eight channels in a paper tape. See Figure 1.

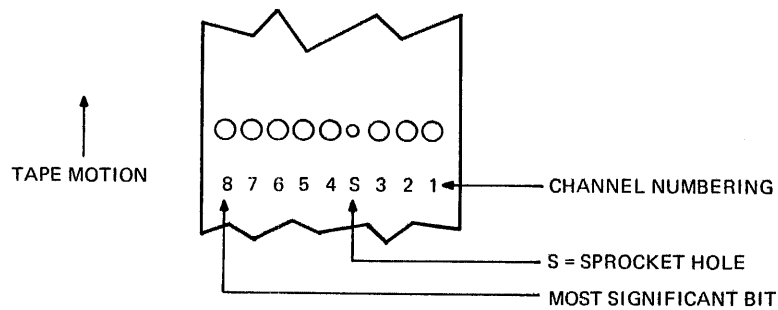


Figure 1. Channel Designations

PROGRAMMING INSTRUCTIONS

Status and Command Bytes

The status and command bytes for the High Speed Paper Tape Reader/Punch Interface are shown in Table 2.

TABLE 2. HSPTR/P INTERFACE STATUS AND COMMAND

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE	OV			NMTN	BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ

Status

BIT

OV

The Overflow bit is ONE when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW Mode. It is ZERO by:

1. Initialization.
2. The HSPTR/P changes from Read Mode to Write Mode.
3. The HSPTR/P changes from Write Mode to Read Mode.
4. The Reader changes from STOP to RUN if BSY=1.

DISARM = DISABLE•ENABLE

READER

PUNCH

The Overflow bit is always ZERO in the Write Mode.

BIT	READER	PUNCH
DU	The Device Unavailable bit is ONE when the power to the Reader is OFF or the power is not stabilized, or the Reader lever is in the LOAD position, or if the drive signal is received and new feed hole is not sensed within 10ms. It indicates either no tape or torn tape and serves as the Out-Of-Tape signal. It is ZERO when the above conditions are not true.	The Device Unavailable bit is ONE when the power to the punch is OFF or internal voltages have not stabilized, or RUN-LOAD Switch is in LOAD or the chad box is full. It is ZERO when the above conditions are not true. Note that CHAD ERROR becomes ZERO by depressing the PERF STATUS Switch.
NMTN	The No Motion Bit is ONE when the Reader has issued a Stop command and the tape has been stopped on the character. It is ZERO when tape starts moving.	The No Motion bit is always ZERO in the Write Mode.
BSY	The Busy bit is ONE when the Buffer Register is empty, waiting for an output from the Reader or the Reader power is not stabilized. It is ZERO when the above conditions are not true.	The Busy bit is ONE when the tape is advancing and in the Punch cycle. It is ZERO when the Punch is ready to accept a punch command.
EX	The Examine bit is ONE whenever OV=1 or NMTN=1. It is ZERO when they are both ZERO.	The Examine bit is always ZERO in the Write Mode.

NOTE

The DU status bit is shared by the Reader and the Punch. The HSPTR/P must be in the Read Mode to sense status on the Reader and must be in the Write Mode to sense status on the Punch. The mode is determined by the last OC instruction.

Commands

BIT	READER	PUNCH
DISABLE	This command inhibits interrupts from the Device Controller from interrupting the Processor. Interrupts are queued if ENABLE is reset.	Same as Reader.
ENABLE	This command bit set with DISABLE reset permits interrupts from the Device Controller to interrupt the Processor.	Same as Reader.
DISARM	This command prevents the device from interrupting or queuing the interrupts.	Same as Reader.
STOP	This command bit halts the motion of the tape. The next character to be read is positioned over the sense light when the tape stops.	Not used.
RUN	This command leaves the controller in the Run Mode, and if in the Slew Mode, starts the tape moving.	Not used.
INCR	In this mode of operation, the tape is advanced one character when the controller is in the Run Mode and a Read Data instruction is executed. The tape stops after encountering the next character. The tape remains stopped until a Read Data Instruction, which starts the tape moving again.	Not used.
SLEW	In this mode of operation, the tape is advanced continuously until stopped.	Not used.
WRITE	Not used	Designates the High Speed Paper Tape Punch.
READ	Designates the High Speed Paper Tape Reader.	

INSTRUCTIONS

Output Command (OC or OCR)	This instruction is used to send a command byte to the Reader/Punch from the Processor.
Sense Status (SS or SSR)	This instruction enables the status byte of the Interface to be examined.
Write Data (WD or WDR)	This instruction is used to output a data byte to the Punch.
Read Data (RD or RDR)	This instruction is used to input a data byte from the Reader when in the Read Mode.
Acknowledge Interrupt (AI or AIR)	This instruction enables the user to examine the Device Address and Status Byte when the Interface generates an interrupt. (This instruction is valid only on 16-bit Processors.)

NOTE

Read Block (RB or RBR) and Write Block (WB or WBR) instructions can be used with the Reader/Punch. Halfword I/O instructions (RH, RHR, WH, WHR) are not used with the Reader/Punch.

PROGRAMMING SEQUENCES

The following three sections briefly describe the different modes of operation. See 16-Bit Reference Manual, Publication Number 29-398 and the 32-Bit Reference Manual, Publication Number 29-365 for general programming procedures.

Sense Status I/O Control

This form of I/O Programming uses loops to continually interrogate the status of a device until a specified condition is met. See Appendices 2 and 3 for programming examples.

Interrupt I/O Control

16 Bit Processor

When using immediate interrupts on a 16 Bit Processor, the appropriate service pointer table must be set up to accommodate a PSW swap. Refer to Appendix 2 for programming examples.

32-Bit Processor

Interrupts are handled through the Interrupt Service Pointer Table. See Appendix 3 for programming examples.

Auto Driver Channel I/O (32-Bit Processor Only)

The purpose of the Auto Driver Channel is to free the user from handling every interrupt. The Auto Driver Channel function is controlled by the set up of the Channel Command Block. See Appendix 3 for programming examples.

INTERRUPTS

When enabled, interrupts are generated by the Interface when:

1. The Reader goes Not Busy. (A character is copied into the Buffer Register from the HSPTR.)
2. The Punch goes Not Busy. (A character has been output to the HSPTP and the Interface is ready for more data.)
- *3. Change from Read Mode to Write Mode provided the Punch is Not Busy.
- *4. Change from Write Mode to Read Mode provided the Reader is Not Busy.
5. Device becomes Unavailable (DU bit goes from 0 to 1).

*When changing from Read Mode to Write Mode, or from Write Mode to Read Mode, pending interrupts are cleared, then the Busy status of the appropriate side of device is checked. If the appropriate side of the device is Busy, no interrupt is generated until the device goes Not Busy. If the appropriate side of the device is already Not Busy upon changing mode, an interrupt is generated at the time of changing mode. The programmer can ignore the last interrupt and change mode directly.

Processor Pending Interrupts are cleared by:

1. Initialization.
2. Disarm command.
3. Acknowledge interrupt instruction. (16-Bit only)
- *4. Changing from Read Mode to Write Mode.
- *5. Changing from Write Mode to Read Mode.

When disabled, interrupts are queued.

When disarmed, interrupts are not generated or queued.

NOTE

To maintain programming compatibility with the 02-031 High Speed Paper Tape Reader/Punch a test for Busy=0 must be performed before changing modes.

INITIALIZATION

Initialization occurs on power up or when the Initialize Switch on the Processor is depressed, provided the Reader power is ON and the RUN/LOAD Switch is in the RUN position.

When initialized, the following occurs:

1. Interrupts of all kinds are disarmed.
2. The NMTN and EX status bits are set.
3. The Disarm, Stop, INCR and Read command functions are set.
4. The BSY status bit is set or reset depending on the state of the Reader.

DEVICE NUMBER

The High Speed Paper Tape Reader/Punch, using Device Controller 35-439, has a preferred address of X'13'. The device number is easily changed by a minor modification to the Device Controller. Refer to the HSPTR/P Interface Maintenance Manual, Publication Number 29-290, for details. For preferred addresses, see the appendices in the 16 Bit 32 Bit Reference Manuals, Publication Numbers 29-398 and 29-365.

SAMPLE PROGRAMS

Appendix 2 is a sample program for use on any 16-Bit Processor. The program combines three types of I/O programming. In section one, the program sets the HSPTR/P in the Increment Mode to read a character and then punches it using programmed sense status loops. At Start 2, the data transfer is done under interrupt control. The third part of the program demonstrates the generation of an interrupt through change of mode.

Appendix 3 is a sample program and flowchart for use on any 32-Bit Processor. The first section of this program handles transfer of data through the Auto Driver Channel with the Reader in the Slew Mode. The second section puts the Reader in the Increment Mode and transfers data under interrupt control.

*When changing from Read Mode to Write Mode, or from Write Mode to Read Mode, pending interrupts are cleared, then the Busy status of the appropriate side of device is checked. If the appropriate side of the device is Busy, no interrupt is generated until the device goes Not Busy. If the appropriate side of the device is already Not Busy upon changing mode, an interrupt is generated at the time of changing mode. The programmer can ignore the last interrupt and change mode directly.

APPENDIX 1

COMPARISON BETWEEN 10 INCH AND 15 INCH HIGH SPEED PAPER TAPE READER/PUNCH

02-031 (10 inch)

When Punch power turns ON, there is a one second delay to allow the AC motor to come up to speed.

When the Reader receives a Run command, the tape is moved first and then the data is loaded into the Buffer Register. Therefore the first data is always missing.

The Reader Busy bit is ONE when the Buffer Register is empty, waiting for an output from the Reader.

The Reader Device Unavailable bit is ONE when the power to the Reader motor is OFF, or the Reader lever is in the LOAD position.

The interrupt can be enabled, disabled, and kept unchanged.

There are four conditions to generate interrupts.

Initialization sets Busy and clears all other status bits.

02-265 (15 inch)

The Punch power is always ON.

When the Reader receives a Run command, the data is loaded into the Buffer Register first and then the tape is moved. Therefore, the first data is not missing.

Same as 02-031, or the Reader is in the load condition, or the Reader power is not stabilized.

The Reader Device Unavailable bit is ONE when the power to the Reader is OFF, or the Reader lever is in the LOAD position, or the power is not stabilized, or if the drive signal is received and a new feed hole is not sensed within 10 ms, indicates either no tape or torn tape and serves as the out of tape signal.

The interrupt can be enabled, disabled, kept unchanged, and disarmed.

Same as 02-031 plus Device Unavailable.

Initialization clears all status bits.

NOTES

1. To insure proper Reader (Digitronics) operation, a Sense Status for Busy = 0 must be performed before transferring to the Write Mode. Many existing programs do not require this sense status because 2 ms or more has elapsed before mode change. With fast Processors or tight programs, transfer to the Write Mode occurring less than 2 ms from the last read data causes the tape to stop in the wrong place.
2. 32 bit operating systems do not support 02-031 (10") Controller.

APPENDIX 2
PROGRAMMING EXAMPLES AND FLOW CHARTS FOR 16-BIT PROCESSORS

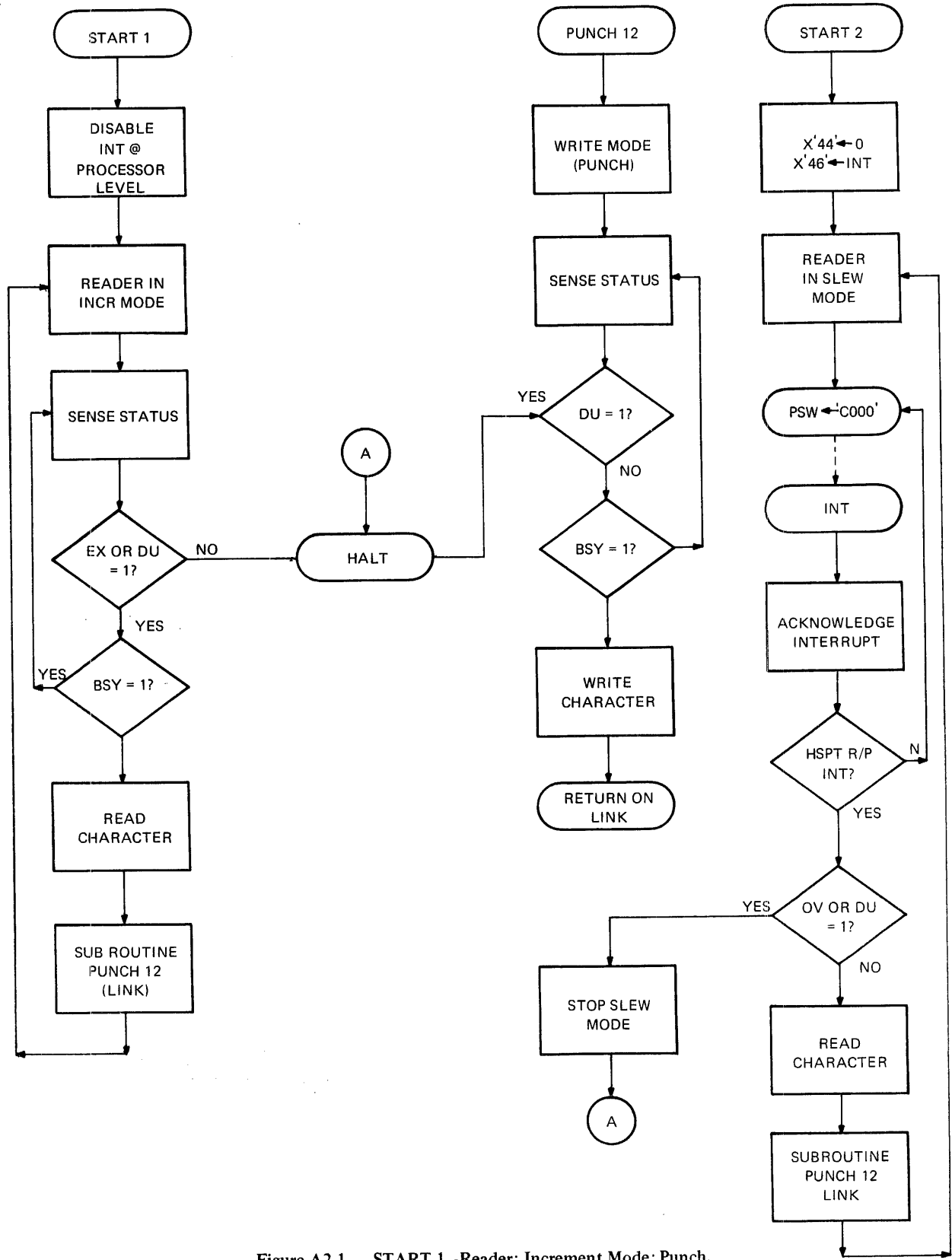


Figure A2-1. START 1—Reader: Increment Mode; Punch.
START 2—Reader: Slew Mode; Punch.
Read Under Interrupts.

APPENDIX 2 (Continued)

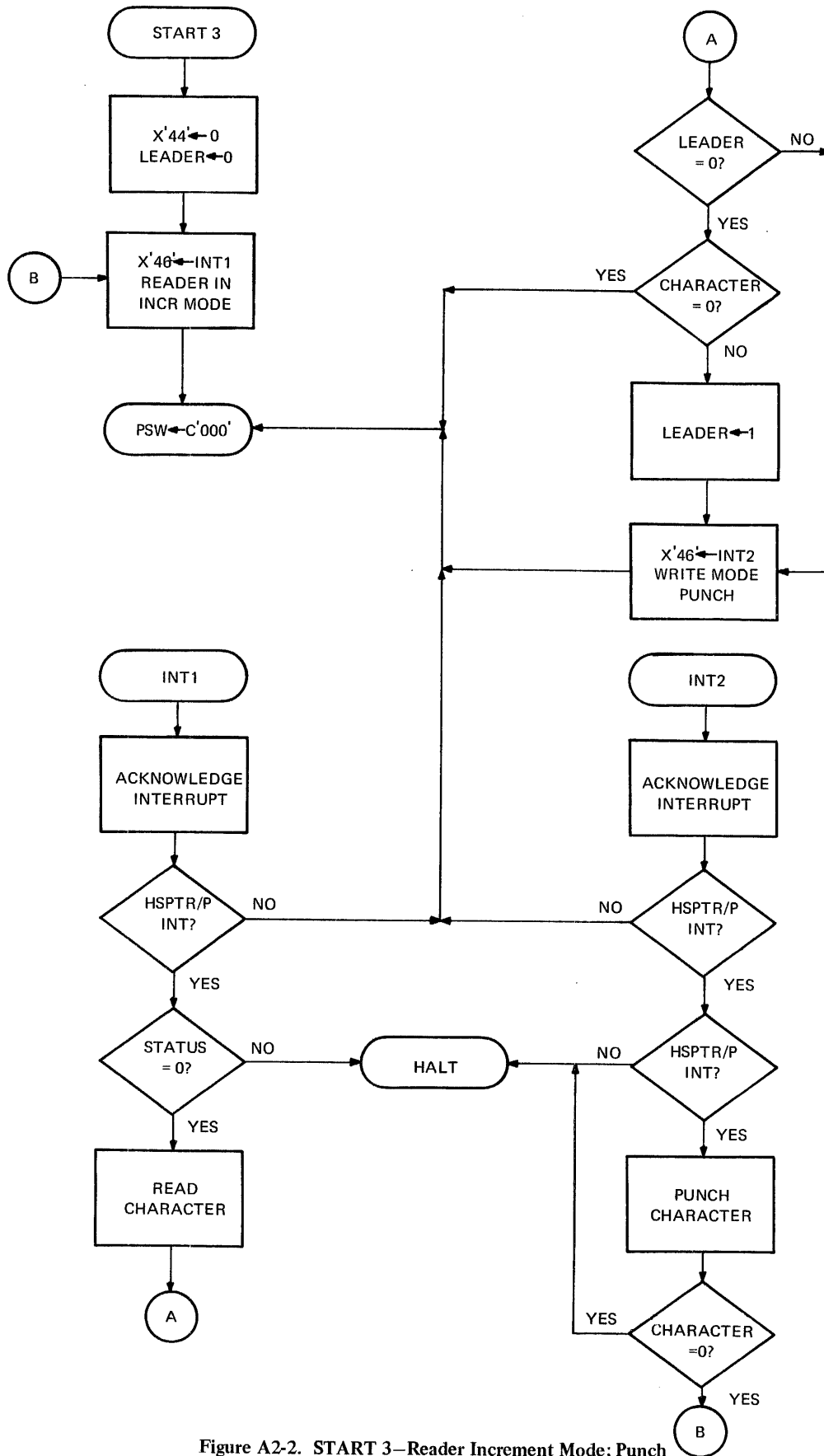


Figure A2-2. START 3—Reader Increment Mode; Punch

PROG= *NONE* ASSEMBLED BY CAL 03-066R04-01 (32-BIT)

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		1	SCRAT			HP210010
		2	CROSS			HP210020
		3	WIDTH 120			HP210030
		4	TARGT 16			HP210040
		5	*			HP210050
		6	* IF HSPTR/P DEVICE ADDRESS IS DIFFERENT THAN X'13', CHANGE			HP210060
		7	* THE HALFWORD LABELED 'DEVADR'.			HP210070
		8	*			HP210080
		9	*			HP210090
		10	* TO READ A CHARACTER FROM PAPER TAPE READER IN INCREMENT			HP210100
		11	* MODE & THEN PUNCH IT, BOTH OPERATIONS ARE DONE USING			HP210110
		12	* SENSE STATUS LOOP. START @ START1			HP210120
		13	*			HP210130
		14	* FOR OPERATION WITH READER IN SLEW MODE (DATA XFER UNDER			HP210140
		15	* INTERRUPT CONTROL) & PUNCH OPERATION USING SENSE STATUS			HP210150
		16	* LOOP, START @ START 2			HP210160
		17	*			HP210170
		18	* THIS PROGRAM RUNS ON INTERDATA 16 BIT PROCESSOR.			HP210180
		19	*			HP210190
		20	R0 FQU 0	WORK REGISTER		HP210200
	0000 0000	21	R1 FQU 1	WORK REGISTER		HP210210
	0000 0001	22	R2 FQU 2	HOLDS EXAMPLE START ADDRESS		HP210220
	0000 0002	23	DEV FQU 3	HOLDS HSPTR/P DEVICE ADDRESS		HP210230
	0000 0003	24	CHAR FQU 4	HOLDS CHARACTER BEING TRANSFERRED		HP210240
	0000 0004	25	STAT FQU 5	HOLDS HSPTR/P STATUS		HP210250
	0000 0005	26	LEADER FQU 6	HOLDS LEADER FLAG		HP210260
	0000 0006	27	LINK FQU 15	LINK REGISTER		HP210270
	0000 000F	28	*			HP210280
		29	*			HP210290
		30	DU FQU 1	DU = 1		HP210300
	0000 0001	31	EX FQU 4	EX = 1		HP210310
	0000 0004	32	BSY FQU 8	BSY = 1		HP210320
	0000 0008	33	*			HP210330
		34	* READER : INCREMENT MODE, READ SENSING STATUS			HP210340
		35	* PUNCH : PUNCH SENSING STATUS			HP210350
		36	*			HP210360
		37	*			HP210370
		38	* THIS PROGRAM DOES NOT IGNORE LEADER AND HALTS ON STATUS ERROR			HP210380
		39	* OR WHEN READER DETECTS END OF TAPE; THUS DUPLICATING			HP210390
		40	* THE ENTIRE TAPE.			HP210400
		41	*			HP210410
		42	*			HP210420
		43	*			HP210430
		44	START1 IH R0,PSW1	PSW = '0000'		HP210440
	0000R 4A00 007ER	45	FPSR R1,R0	R2 = START ADDRESS		HP210450
	0004R 9510	46	IHI R2,START1	GET DEVICE ADDRESS		HP210460
	0006R CA20 000QR	47	IH DEV,DEVADR	READER IN INCREMENT MODE		HP210470
	000AR 4B30 0082R	48	READ1 OC DEV,INCR			HP210480
	000ER DE3C 0084R	49	SSR DEV,STAT			HP210490
	0012R 9D35	50	RTC EX+DU,HALT	OV,NMTN,DU INDICATE PROBLEM		HP210500
	0014R 4250 0038R	51	*	HALT @ END OF TAPE; DU = 1		HP210510
		52	RTES RSY:3	LOOP ON BUSY		HP210520
	0018R 2083	53	RDR DEV,CHAR	READ A CHARACTER WHEN BSY DROPS		HP210530
	001AP 9B34	54	RAL LINK,PUNCH12			HP210540
	001CR 41F0 0024R					

APPENDIX 2 (Continued)

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0020R 4300 000ER          55      R      READ1          READ/PUNCH TILL END OF TAPE          HP210550
                                56 *
0024R DE30 0086R          57 PUNCH12 OC      DEV,WRITE          HP210560
0028R 9035                58      SSR      DEV,STAT          HP210570
002AR 4210 003AR          59      RTC      DU,HALT          DU INDICATES OFF/IN LOAD/CHAD          HP210580
002ER 2083                60      RTBS     BSY,3          LOOP ON BSY          HP210590
0030R 9A34                61      WDR      DEV,CHAR          PUNCH A CHARACTER WHEN BSY DROPS          HP210600
0032R 030F                62      RR       LINK          READ NEXT CHARACTER          HP210610
                                63 *
0034R DE30 0089R          64 STOP      OC      DEV,STOPSLEW          HP210620
0038R CA00 6000           65 HALT      LHI     R0,X'8000'          HP210630
003CR 9510                66      EPSR     R1,R0          HALT PROCESSOR          HP210640
003ER 0302                67      RR       R2          START OVER          HP210650
                                68 *
                                69 *
                                70 *
0040R 0700                71 * READER   : SLEW MODE, READ UNDER INTERRUPT CONTROL          HP210660
0042R 4000 0044           72 * PUNCH   : PUNCH SENSING STATUS          HP210670
0046R CA10 0064R          73 *
                                74 START2     XHR     R0,R0          HP210680
004AR 4010 0046           75      STH     R0,X'44'          SET UP NEW PSW FOR IMMEDIATE INT.          HP210690
004ER CA20 0040R          76      LHI     R1,INT          HP210700
0052R 4A30 0082R          77      STH     R1,X'46'          HP210710
0056R DE30 0088R          78      LHI     R2,START2          R2 = START ADDRESS          HP210720
005AR 4A00 0080R          79      LH      DEV,DEVAOR          GET DEVICE ADDRESS          HP210730
005ER 9510                80      OC      DEV,SLEW          ENABLE INT., SLEW MODE          HP210740
0060R 4300 0040R          81 RSLEW     LH      R0,PSW2          R08= X'C000'          HP210750
                                82      EPSR     R1,R0          HALT PROCESSOR TILL INTERRUPTED          HP210760
                                83      B        START2          HP210770
                                84 *
                                85 * READER INTERRUPT RECEIVED          HP210780
                                86 *
0064R 9F05                87 INT       AIP     R0,STAT          ACKNOWLEDGE INTERRUPT          HP210790
0066P 0503                88      CLHR    R0,DEV          HP210800
0068R 4230 005AR          89      RME     RSLEW          IGNORE IF OTHER DEVICE INTERRUPTS          HP210810
006CR C450 0081           90      NHI     STAT,X'81'          OV, DU SHOULD BE RESET          HP210820
0070R 4230 0034R          91      STOP    STOP          STOP @ END OF TAPE          HP210830
0074R 9B34                92      RDR     DEV,CHAR          READ A CHARACTER          HP210840
                                93 *
0076R 41F0 0024R          94      BAL     LINK,PUNCH12          HP210850
007AR 4300 0056R          95      B        RSLEW-4          READ/PUNCH TILL END OF TAPE          HP210860
                                96 *
                                97 *
007ER 0000                98 PSW1      OC      0          DISABLE INT @ PROCESSOR LEVEL          HP210870
0080R C000                99 PSW2      OC      X'C000'          ENABLE INT AND HALT          HP210880
0082P 0013                100 DEVAOR   OC      X'13'          HSPTR/P DEVICE ADDRESS          HP210890
0084R 99                  101 INCR     DR      X'99'          DIS, RUN, INCR, RD          HP210900
0085R 59                  102 ENINCR   DR      X'59'          EN, RUN, INCR, RD          HP210910
0086R C2                  103 WRITE    DR      X'C2'          DISARM, WRT          HP210920
0087P 42                  104 WRITE2   DR      X'42'          EN,WRT          HP210930
0088R 55                  105 SLEW     DR      X'55'          EN, RUN, SLEW, RD          HP210940
0089R A5                  106 STOPSLEW DR      X'A5'          DIS, STOP, SLEW, RD          HP210950
                                107 *
                                108 *
0090R 0000                109 * READER   : INCREMENT MODE, READ UNDER INTERRUPTS          HP210960
0091R 0000                110 * PUNCH   : PUNCH UNDER INTERRUPTS          HP210970

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APPENDIX 2 (Continued)

		111	*	FOLLOWING EXAMPLE SHOWS SEQUENCE FOR READING THE TAPE IN		HP211110
		112	*			HP211120
		113	*	INCREMENT MODE AND PUNCHING THE TAPE. ONE CHARACTER IS		HP211130
		114	*	PROCESSED AT A TIME. BOTH READER & PUNCH OPERATIONS		HP211140
		115	*	ALTERNATE, THUS GENERATING THE CHANGE OF MODE INTERRUPT.		HP211150
		116	*	THIS EXAMPLE IGNORES LEADER PORTION OF TAPE		HP211160
		117	*	AND HALTS WHEN ZERO CHARACTER IS ENCOUNTERED.		HP211170
		118	*			HP211180
		119	*			HP211190
00AAR	0700	120	START3	XHR R0,R0		HP211200
00ACR	4000 0044	121		STH R0,X'44'	SET UP NEW PSW FOR IMMEDIATE INT.	HP211210
0090R	C820 008AR	122		LHI R2,START3		HP211220
0094R	4830 0082R	123		LH DEV,DEVADR	GET DEVICE ADDRESS	HP211230
0098R	0766	124		XHR LEADER,LEADER		HP211240
009AR	C810 0080R	125	READ	LHI R1,INT1		HP211250
009ER	4010 0046	126		STH R1,X'46'		HP211260
00A2R	DE30 0085R	127		OC DEV,ENINCR	INCR MODE	HP211270
		128	*		THIS COMMAND GENERATES FIRST INT.	HP211280
00A6R	4800 0080R	129	RINCR	LH R0,PSW2	R0 = X'C000'	HP211290
00AAR	9510	130		FPSR R1,R0	HALT PROCESSOR TILL INTERRUPTED	HP211300
00ACR	4300 008AR	131		R START3		HP211310
		132	*			HP211320
		133	*	READER HAS INTERRUPTED		HP211330
		134	*			HP211340
		135	*			HP211350
00R0R	9F05	136	INT1	AIP R0,STAT	ACKNOWLEDGE INTERRUPT	HP211360
00R2R	0503	137		CLHR R0,DEV		HP211370
00R4R	4230 00A6R	138		RNE RINCR	IGNORE IF OTHER DEVICE INTERRUPTS	HP211380
00R8R	0855	139		LHR STAT,STAT		HP211390
00RAR	4230 0038R	140		RN7 HALT	NON-ZERO STATUS INDICATES PROBLEM	HP211400
		141	*		HALT @ END OF TAPE; DU = 1	HP211410
00RER	9B34	142		RDP DEV,CHAR	READ A CHARACTER	HP211420
00C0R	0866	143		LHR LEADER,LEADER		HP211430
00C2R	4230 00CER	144		RN2 PUNCH		HP211440
00C6R	0844	145		LHR CHAR,CHAR		HP211450
00C8R	4330 00A6R	146		R7 RINCR	IGNORE LEADER	HP211460
00CCR	2461	147		LIS LEADER.1	SET 'LEADER READ' FLAG	HP211470
		148	*			HP211480
		149	*			HP211490
00CER	C810 00E4R	150	PUNCH	LHI R1,INT2		HP211500
00D2R	4010 0046	151		STH R1,X'46'	SET UP INT RETURN ADDRESS	HP211510
00D6R	DE30 0087R	152		OC DEV,WRITE2	ENABLE PUNCH	HP211520
00DAR	4800 0080R	153	P3	LH R0,PSW2		HP211530
00DER	9510	154		FPSR R1,R0	HALT PROCESSOR TILL INTERRUPTED	HP211540
00FOR	4300 008AR	155		R START3		HP211550
		156	*			HP211560
		157	*	PUNCH INTERRUPT RECEIVED		HP211570
		158	*			HP211580
00F4R	9F05	159	INT2	AIP R0,STAT		HP211590
00F6R	0503	160		CLHR R0,DEV		HP211600
00F8R	4230 00DAR	161		RNE P3	IGNORE IF OTHER DEVICE INTERRUPTS	HP211610
00FCR	0855	162		LHR STAT,STAT		HP211620
00FER	4230 0038R	163		RN2 HALT	STATUS SHOULD BE ZERO. HALT IF DU	HP211630
00F2R	9A34	164		WDR DEV,CHAR	PUNCH THE CHARACTER	HP211640
00F4R	0844	165		LHR CHAR,CHAR		HP211650
00F6R	4230 009AR	166		RN2 READ	READ CHARACTERS TILL TRAILER	HP211660

APPENDIX 2 (Continued)

00FAR 4300 0038R 167 R HALT
00FER 168 END

HP211670
HP211680

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APPENDIX 2 (Continued)

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

ARSTOP	0000																	
ADC	0002																	
BSY	0008	52	60															
CHAR	0004	53	61	92	142	145	145	164	165	165								
DEV	0003	47	48	49	53	57	58	61	64	79	80	88	92	123				
DEVADR	0082R	127	137	142	152	160	164											
DUI	0001	47	79	123														
ENTNCR	0085R	50	59															
EX	0004	127																
HALT	0038R	50																
IMPTOP	00FER	50	59	140	163	167												
INCR	0084R	48																
INT	0064R	76																
INT1	00B0R	125																
INT2	00E4R	150																
LANC	0001																	
LEADER	0006	124	124	143	143	147												
LINK	000F	54	62	94														
P3	00DAR	161																
PSW1	007ER	44																
PSW2	0080R	81	129	153														
PUNCH	00CER	144																
PUNCH12	0024R	54	94															
PURETOP	0000R																	
R0	0000	44	45	65	66	74	74	75	81	82	87	88	120	120				
R1	0001	121	129	130	136	137	153	154	159	160								
R2	0002	45	66	76	77	82	125	126	130	150	151	154						
READ	0C9AR	46	67	78	122													
READ1	000ER	166																
RINCR	00A6R	55																
RSLEW	005AR	138	146															
SLEW	0088R	89	95															
START1	0000R	80																
START2	0040R	46																
START3	008AR	78	83															
STAT	0005	122	131	155														
STOP	0034R	49	58	87	90	136	139	139	159	162	162							
STOPSLEW	0089R	91																
WRITE	0086R	64																
WRITE2	0087R	57																
		152																

APPENDIX 2 (Continued)

APPENDIX 3
PROGRAMMING EXAMPLES AND FLOW CHARTS FOR 32-BIT PROCESSORS

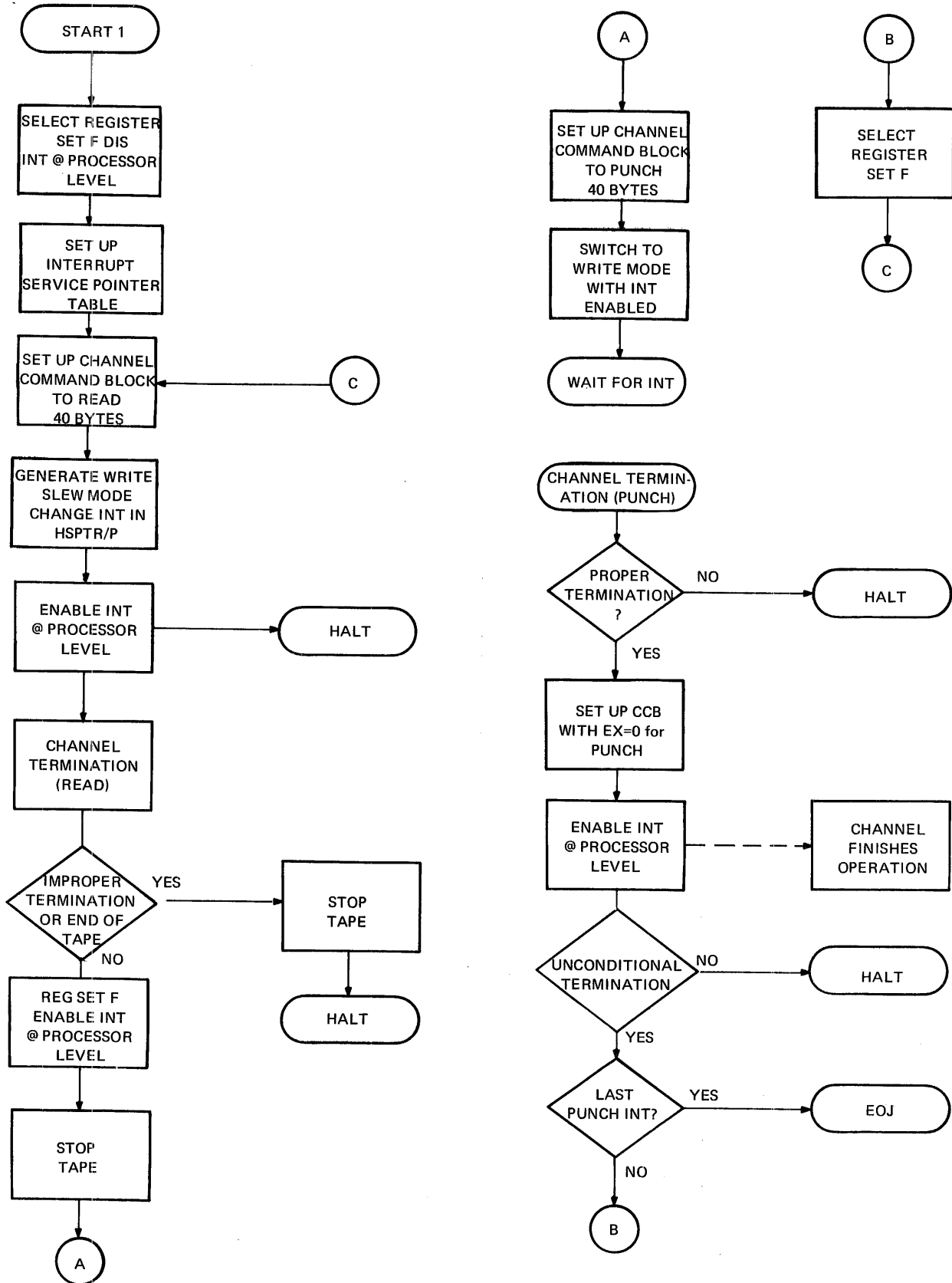


Figure A3-1. Auto-Driver Channel

APPENDIX 3 (Continued)

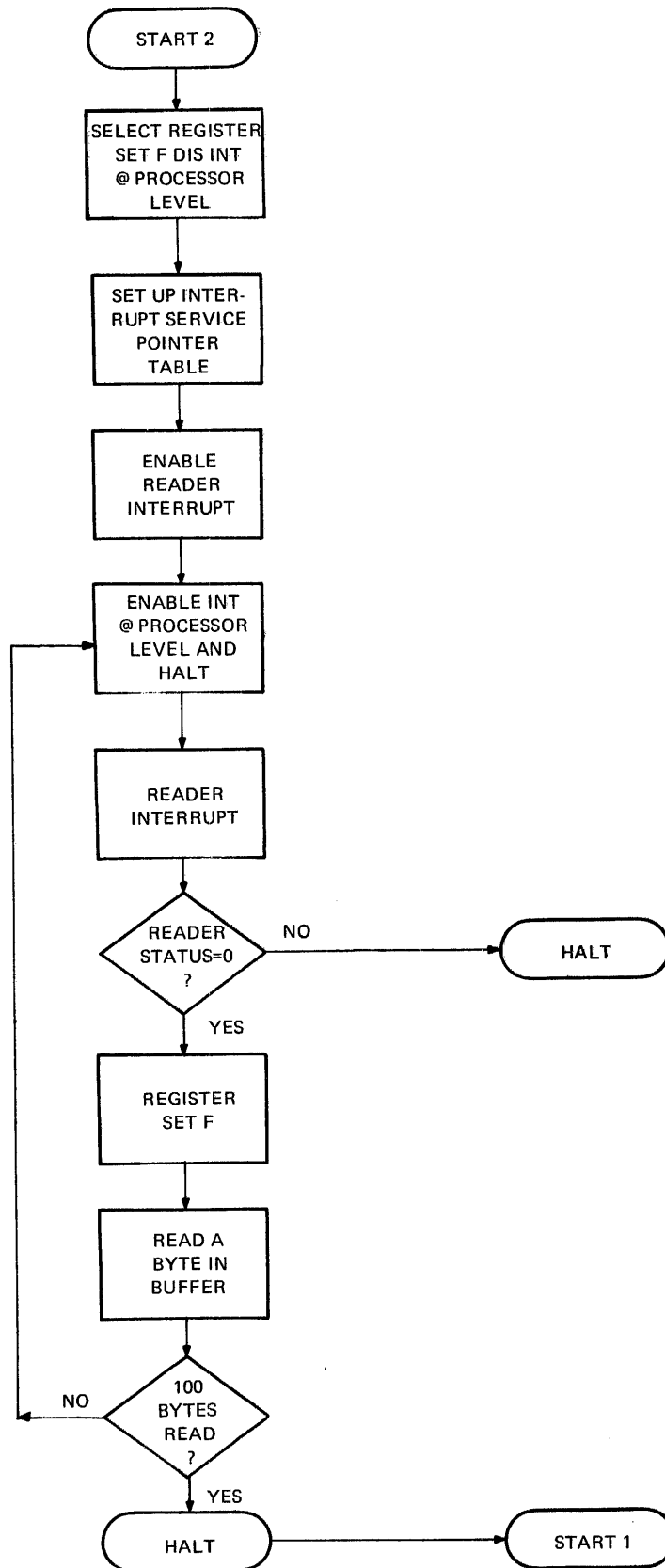


Figure A3-2. Read Tape Under Interrupt Control

PROG= *NONE* ASSEMBLED BY CAL 03-066R04-01 (32-BIT)

A3-3

```

1          SCRAT
2          CROSS
3          WIDTH 120
4          TARGET 32
5          NORX3
6          *
7          * THE FOLLOWING PROGRAM READS 40 BYTES FROM READER USING
8          * AUTO DRIVER CHANNEL & THEN PUNCHES THAT DATA USING THE
9          * AUTO DRIVER CHANNEL. THE PROGRAM HALTS PROCESSOR IF
10         * OV, NMTN, FX OR DU BIT(S) SETS IR READER STATUS; OR IF
11         * RSY OR DU BIT SETS IN PUNCH STATUS, CONDITION CODE AFTER
12         * THE ADC TRANSFER IS TESTED FOR PROPER TERMINATION, THE
13         * ROUTINE LOOPS TILL END OF TAPE IS DETECTED BY READER.
14         *
15         * THIS PROGRAM RUNS ON 32-BIT PROCESSOR
16         *
17         * REGISTER ASSIGNMENT
18         *
19         R0          FQU      0          WORK REGISTER
20         R1          FQU      1          WORK REGISTER
21         DFV         FQU      2          HOLDS HSPTR/P ADDRESS
22         R3          FQU      3          HOLDS HSPTR/P STATUS
23         COUNT      FQU      4          HOLDS BYTE COUNT
24         R15        FQU      15         EXAMPLE START ADDRESS
25         *
26         C          FQU      8          C = 1
27         V          FQU      4          V = 1
28         G          EQU      2          G = 1
29         L          FQU      1          L = 1
30         *
31         *
32         *
33         * READER : SLEW MODE; READ THRU AUTO DRIVER CHANNEL
34         * PUNCH  : PUNCH USING ADC.
35         *
36         START1    LI        R0,Y*F0*
37                 FPCR     R1,R0          REG SET F
38                 LHI     R0,HALT        SFT UP INTERRUPT SFRVICF POINTER TAB
39                 LHI     R1,X*00*
40         ISP1      STH     R0,0(R1)
41                 AIS     R1,2
42                 CLHI   R1,X*200*
43                 RLS     ISP1
44                 LH     DFV,DEVADR
45                 LP     R1,DEV
46                 AR     R1,R1
47                 LHI     R0,CCW+1
48                 STH     R0,X*00*(R1)   SFT UP INTERRUPT TABLE ENTRY
49                 LHI     R15,START1
50         *
51         NFXT40    LI        R0,Y*F781FFD9* SET UP CCB
52                 ST     R0,CCW          TO READ 40 BYTES IN FAST MODE
53                 LHI     R0,READ
54                 STH     R0,CCSUB       SUBROUTINE AFTER READ OPFRATION

```

APPENDIX 3 (Continued)

HP310010
HP310020
HP310030
HP310040
HP310050
HP310060
HP310070
HP310080
HP310090
HP310100
HP310110
HP310120
HP310130
HP310140
HP310150
HP310160
HP310170
HP310180
HP310190
HP310200
HP310210
HP310220
HP310230
HP310240
HP310250
HP310260
HP310270
HP310280
HP310290
HP310300
HP310310
HP310320
HP310330
HP310340
HP310350
HP310360
HP310370
HP310380
HP310390
HP310400
HP310410
HP310420
HP310430
HP310440
HP310450
HP310460
HP310470
HP310480
HP310490
HP310500
HP310510
HP310520
HP310530
HP310540

```

000000I F800 0000 00F0
000006I 9510
000008AI C800 00BAI
00000CI C810 00D0
000010I 4001 0000
000014I 2612
000016I C510 02D0
00001AI 2085
00001CI 4820 811F
000020I 0012
000022I 0A11
000024I CA00 0129I
000028I 4001 00D0
00002CI CAF0 0000I

000030I F800 F781 FFD9
000036I 5000 80EF
00003AI C800 0052I
00003EI 4000 80FA

```

A34

000042I	DE20 80FB	55	OC	DEV,ENSLEW	WRITE/READ MODE CHANGE INTERRUPT	HP310550
000046I	F810 0000 C0F0	56	LI	R1,Y'00F0'	R1 = '0000C0F0'	HP310560
00004CI	9501	57	FPSR	R0,R1	HALT PROCESSOR TILL INTERRUPTED	HP310570
00004EI	4300 FFFC	58	RFC	0,*	HANG	HP310580
		59	*			HP310590
		60	*	CHANNEL COMMAND INPUT IS TERMINATED		HP310600
		61	*			HP310610
000052I	42D0 8060	62	READ	RTC C+V+L,STOP	C,V,L FLAGS SHOULD BE RESET NORMALLY	HP310620
		63	*		STOP WHEN END OF TAPE IS DETECTED	HP310630
		64	*		L = 1 WHEN DU = 1.	HP310640
		65		RFC G,STOP	G FLAG SETS FOR PROPER TERMINATION	HP310650
000056I	4320 805C	66	LI	R1,Y'40F0'		HP310660
00005AI	F810 0000 40F0	67	FPSR	R0,R1	ENABLE INT @ PROCESSOR LEVEL	HP310670
000060I	9501	68	OC	DEV,STOPSLEW	STOP TAPE MOTION	HP310680
000062I	DE20 80DD	69	LI	R0,Y'F785FFD9'		HP310690
000066I	F800 F785 FFD9	70	ST	R0,CCW	TO PUNCH 40 BYTES IN FAST MODE	HP310700
00006CI	5000 80B8	71	LHI	R0,PUNCHED		HP310710
000070I	C800 0080I	72	STH	R0,CCBSUB	SUBROUTINE AFTER PUNCH OPERATION	HP310720
000074I	4000 80C4	73	*			HP310730
		74	OC	DEV,ENWRITE	READ/PUNCH MODE CHANGE INTERRUPT	HP310740
000078I	DE20 80C8	75	R	*	HANG	HP310750
00007CI	4300 FFFC	76	*			HP310760
		77	*	CHANNEL PUNCH OPERATION IS TERMINATED		HP310770
		78	*			HP310780
0000A0I	42D0 8036	79	PUNCHED	RTC C+V+L,HALT	C,V,L FLAGS SHOULD BE RESET	HP310790
0000A4I	4320 8032	80	RFC	G,HALT	G FLAG SETS FOR CORRECT TERMINATION	HP310800
		81	*			HP310810
0000A8I	F800 F705 FFD9	82	LI	R0,Y'F705FFD9'		HP310820
0000AEI	5000 8096	83	ST	R0,CCW	EXECUTE BIT IS RESET FOR	HP310830
000092I	C800 00A6I	84	LHI	R0,LASTINT	UNCONDITIONAL ADC TRANSFER TO	HP310840
000096I	4000 80A2	85	STH	R0,CCBSUB	'LASTINT' AFTER LAST PUNCH INT	HP310850
		86	*		IS CLEARED.	HP310860
00009AI	F810 0000 40F0	87	LI	R1,Y'40F0'		HP310870
0000A0I	9501	88	FPSR	R0,R1	ENABLE INT @ PROCESSOR LEVEL	HP310880
0000A2I	4300 FFFC	89	R	*	HANG	HP310890
		90	*			HP310900
0000A6I	42D0 8010	91	LASTINT	RTC C+V+L,HALT	C,V,G,L FLAGS SHOULD BE RESET	HP310910
0000AAI	F810 0000 00F0	92	LI	R1,Y'F0'		HP310920
0000A0I	9501	93	FPSR	R0,R1	REGISTER SET F	HP310930
0000A2I	4300 FF7A	94	R	NEXT40	TO READ & PUNCH NEXT 40 BYTES	HP310940
		95	*			HP310950
0000A6I	DE20 8089	96	STOP	OC DEV,STOPSLEW	STOP TAPE MOTION	HP310960
0000AAI	C810 080F	97	HALT	LHI R1,X'080F'		HP310970
0000AEI	1114	98	SELLS	R1,4	R1 = '000080F0'	HP310980
0000C0I	9501	99	FPSR	R0,R1	HALT PROCESSOR	HP310990
0000C2I	030F	100	RR	R15	START OVER	HP311000
		101	*			HP311010
		102	*			HP311020
		103	*	READER : INCREMENT MODE		HP311030
		104	*	NO PUNCH		HP311040
		105	*			HP311050
		106	*	TO READ DATA UNDER INTERRUPT CONTROL		HP311060
		107	*			HP311070
0000C4I	F810 0000 00F0	108	START2	LI R1,Y'F0'		HP311080
0000CAI	9501	109	FPSR	R0,R1	SELECT FULL WORD MODE, REG SET 15	HP311090
0000CCI	C8F0 00C4I	110	LHI	R15,START2		HP311100

APPENDIX 3 (Continued)

000000I	0744		111	XR	COUNT,COUNT		HP311110	
000002I	C800	00BAI	112	IHI	RO,HALT	SET UP INTERRUPT SERVICE POINTER TAB	HP311120	
000006I	C810	00D0	113	IHI	R1,X'D0'		HP311130	
00000AI	4001	0000	114	ISP2	STH	RO,0(R1)	HP311140	
00000EI	2612		115	ATS	R1,2		HP311150	
0000F0I	C510	02D0	116	CLHI	R1,X'2D0'		HP311160	
0000F4I	2085		117	PLS	ISP2		HP311170	
0000F6I	4810	8054	118	IH	R1,DEVADR		HP311180	
0000FAI	1111		119	SLUS	R1,1		HP311190	
0000FCI	C800	0108I	120	IHI	RO,INT		HP311200	
0000F0I	4001	00D0	121	STH	RO,X'D0'(R1)	SET UP X'D0' + 2(DEV ADR) LOCATION	HP311210	
			122	*			HP311220	
0000F4I	4820	8046	123	LH	DEV,DEVADR	GET DEVICE ADDRESS	HP311230	
0000F8I	DE20	8046	124	OC	DEV,ENINCR	ENABLE, INCR MODE	HP311240	
			125	*		THIS COMMAND GENERATES FIRST INT.	HP311250	
0000FCI	F810	0000 C0F0	126	LOOP	IT	R1,Y'0000C0F0'	HP311260	
000102I	9501		127	FPSR	RO,R1	HALT TILL INTERRUPTED	HP311270	
000104I	4300	FFFC	128	R	*	HANG	HP311280	
			129	*			HP311290	
000108I	0833		130	INT	LHR	R3,R3	REG SET 0	HP311300
00010AI	4230	FFAC	131	RM7	HALT	HALT WHEN NON-ZERO STATUS	HP311310	
00010EI	F810	0000 00F0	132	LT	R1,Y'F0'		HP311320	
000114I	9501		133	FPSR	RO,R1	REG SET 15	HP311330	
000116I	DB24	802B	134	RD	DEV,BUFFER0(COUNT)		HP311340	
00011AI	2641		135	ATS	COUNT,1		HP311350	
00011CI	C540	0064	136	CLHT	COUNT,100		HP311360	
000120I	4280	FFD8	137	RL	LOOP	LOOP TILL 100 BYTES ARE READ.	HP311370	
000124I	4300	FF92	138	R	HALT		HP311380	
			139	*			HP311390	
			140	*			HP311400	
			141	*	DATA CONSTANTS & STORAGE USED IN ABOVE EXAMPLES		HP311410	
			142	*			HP311420	
			143	*			HP311430	
000128I	0000	0000	144	CCW	OCY	0	CHANNEL COMMAND BLOCK	HP311440
00012CI	0000	016CI	145		OC	BUFFER0+39		HP311450
000130I	0000	0000	146		OCY	0,0,0		HP311460
000134I	0000	0000						
000138I	0000	0000						
00013CI	0052I		147	CCBSUB	OC	Z(READ)	SUBROUTINE ADDRESS	HP311470
			148	*				HP311480
00013EI	0013		149	DEVADR	OCX	13	HSPTR/P ADDRESS	HP311490
000140I	C2		150	DWRITE	OR	X'C2'	DISARM, PUNCH	HP311500
000141I	55		151	ENSLEW	OR	X'55'	EN, RUN, SLEW, RD	HP311510
000142I	59		152	ENINCR	OR	X'59'	EN, RUN, INCR, RD	HP311520
000143I	E5		153	STOPSLEW	OR	X'E5'	DISARM, STOP, SLEW, RD	HP311530
000144I	42		154	ENWRITE	OR	X'42'	EN, PUNCH	HP311540
			155	*				HP311550
000145I			156	BUFFER0	OS	100	DATA BUFFER FOR EXAMPLE 2	HP311560
			157	*				HP311570
00014AI			158		FND			HP311580

APPENDIX 3 (Continued)

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

A3-6

ABSTOP	0000 0000																			
ADC	0000 0004																			
BUFFER0	0000 0145I	134	145																	
C	0000 0008	62	79	91																
CCRSUB	0000 013CI	54	72	85																
CCW	0000 0128I	47	52	70	83															
COUNT	0000 0004	111	111	134	135	136														
DEV	0000 0002	44	45	55	68	74	96	123	124	134										
DFVADR	0000 013EI	44	118	123																
DWRITE	0000 0140I																			
ENTNCR	0000 0142I	124																		
ENSLEW	0000 0141I	55																		
ENWRITE	0000 0144I	74																		
G	0000 0002	65	80																	
HALT	0000 008AI	38	79	80	91	112	131	138												
IMPTOP	0000 01AAI																			
INT	0000 0108I	120																		
ISP1	0000 0010I	43																		
ISP2	0000 00DAI	117																		
I	0000 0001	62	79	91																
LADC	0000 0002																			
LASTINT	0000 00A6I	84																		
LOOP	0000 00FCI	137																		
NEXT40	0000 0030I	94																		
PUNCHED	0000 0080I	71																		
PURETOP	0000 0000P																			
R0	0000 0000	36	37	38	40	47	48	51	52	53	54	57	67	69						
		70	71	72	82	83	84	85	88	93	99	109	112	114						
		120	121	127	133															
R1	0000 0001	37	39	40	41	42	45	46	46	48	56	57	66	67						
		87	88	92	93	97	98	99	108	109	113	114	115	116						
		118	119	121	126	127	132	133												
R15	0000 000F	49	100	110																
R3	0000 0003	130	130																	
READ	0000 0052I	53	147																	
START1	0000 0000I	49																		
START2	0000 00C4I	110																		
STOP	0000 00B6I	62	65																	
STOPSLEW	0000 0143I	68	96																	
V	0000 0004	62	79	91																

APPENDIX 3 (Continued)

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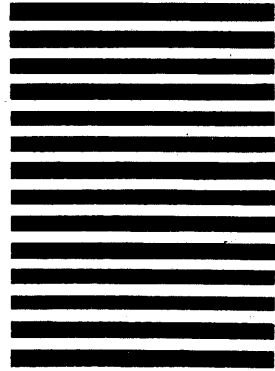
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