CONNCURRENT
COMPUTER CORPORATION
3205
PROCESSOR

STUDENT GUIDE

SECTION 1 INTRODUCTION TO THE 3205 PROCESSOR

TOPICS:

1.1 Features

1.2 General Physical Description

1.3 General Functional Description

OBJECTIVES:

Upon successful completion of this section, the student will:

1. Be familiar with the basic Features of the 3205 processor.

2. Be able to physically identify a 3205 system environment.

3. Be familiar with the basic Function of the 3205 processor.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 Processor

ADDITIONAL READING MATERIALS:

None

1.1 FEATURES

* 3205 Standard Features

  - Single Board Processor

  - 32 Bit Processor (32 Bit Internal Buses and Microwords)

  - .5MB To 1MB Memory Capability on the CPU Board
    You can go up to 4MB By changing PALS
    & SIPS.

  - Hardware Memory Manager (MAT) Integral to the Processor

  - Memory Error Correction and Logging

  - 16 Bit External I/O Bus

  - Direct Memory Access I/O Bus

  - I/O Support for 1023 External devices

Single In Line Package

1.1 FEATURES (cont.)

* 3205 Standard Features (Cont.)

  - Single and Double Precision Floating Point Instructions

  - Selector Channel Interface, Integral to the Processor

* 3205 Optional Feature

  - 1MB To 3MB Memory Capability on the Memory Expansion Board

  - Battery Backup

1.2 GENERAL PHYSICAL DESCRIPTION

* 3205 Processor

  - CPU

  - Memory System

  - Power Subsystem

  - I/O Subsystem (Muxed and DMA)

1.3 GENERAL FUNCTIONAL DESCRIPTION

* 3205 Processor

- CPU
Control Unit

Processing Unit

Instruction Register

Memory

Input/Output (I/O) Interface

Consolette Interface

Power Up/Down

- Memory System
Address Registers

MAT

ECC

Error Logger

Memory Refreash

- I/O Subsystem (Muxed and DMA)
MUX 1023 Devices

PMUX Up to 5 DMA Controllers

SECTION 2 3205 CPU ANALYSIS

TOPICS:

2.1 3205 CPU Block Diagram Analysis

2.2 User Programming Analysis

2.3 Memory System Block Diagram Analysis

2.4 Power Subsystem Analysis

OBJECTIVES:

Upon successful completion of this section the student will:

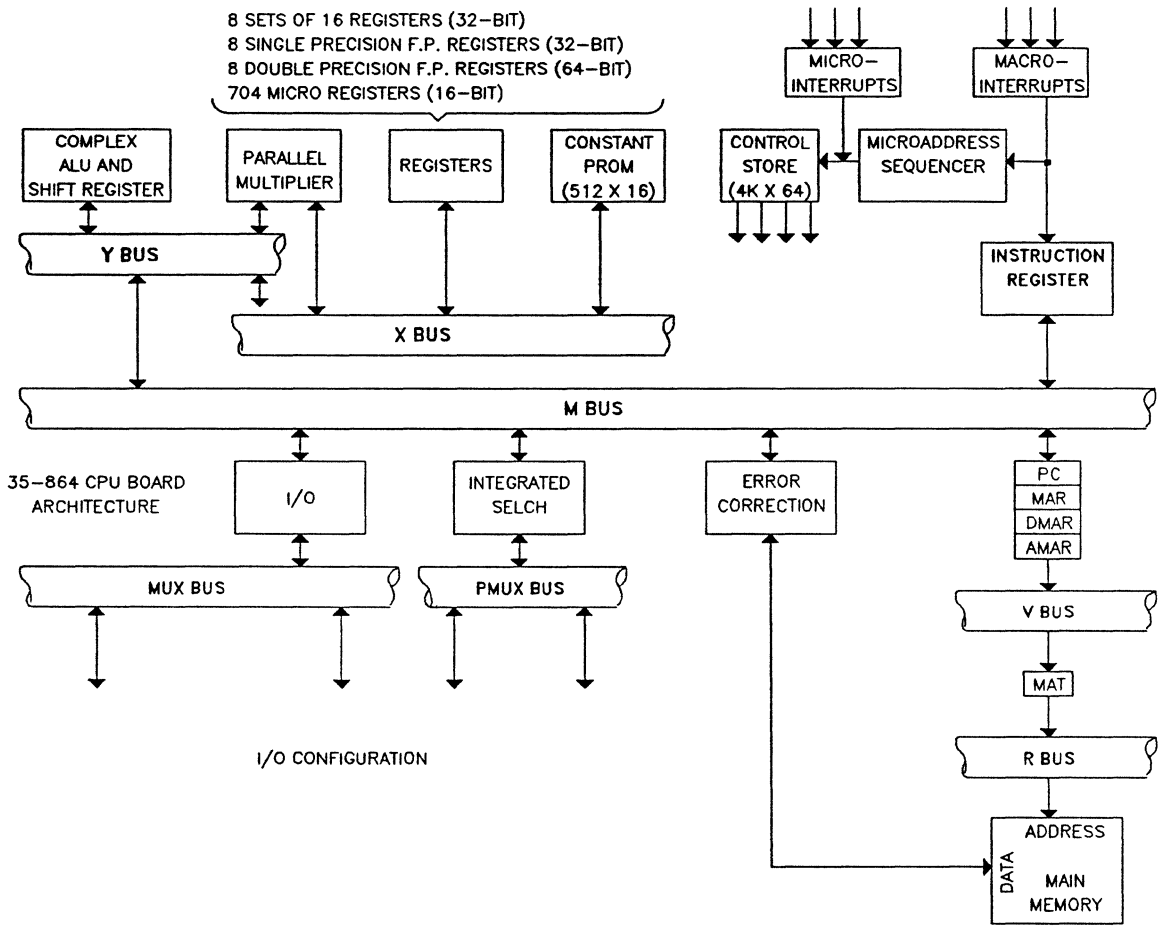
1. Be able to describe the function of each component in the system to include the CPU, Memory, and Power Subsystem.

2. Be able to analyze the control and flow of data within the processor, it's I/O, and Memory for various different Processor operations.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 Processor with an Operating System
35-864 CPU/Memory Board Theory of Operation Manual
3200 Programmer Pocket Guide
3205 System Instruction Set Reference Manual

2.1 3205 CPU Block Diagram Analysis



CPU/MEMORY BOARD BLOCK DIAGRAM

2.1 3205 CPU Block Diagram Analysis (cont.)

* CPU Block Diagram Overview

- Control Unit
Control Store (CS)
Control Register (CR)
Microaddress Sequencer
N Register (NR)
Condition Code Multiplexor (CCMUX)
Instruction Registers
Macrointerrupt Circuitry
Microinterrupt Circuitry

- Execution Unit
Arithmetic Logic Unit (ALU)
Multiplier
External Registers (Constant PROM)
Register External (REX)
P Register (PR)
Shift Registers

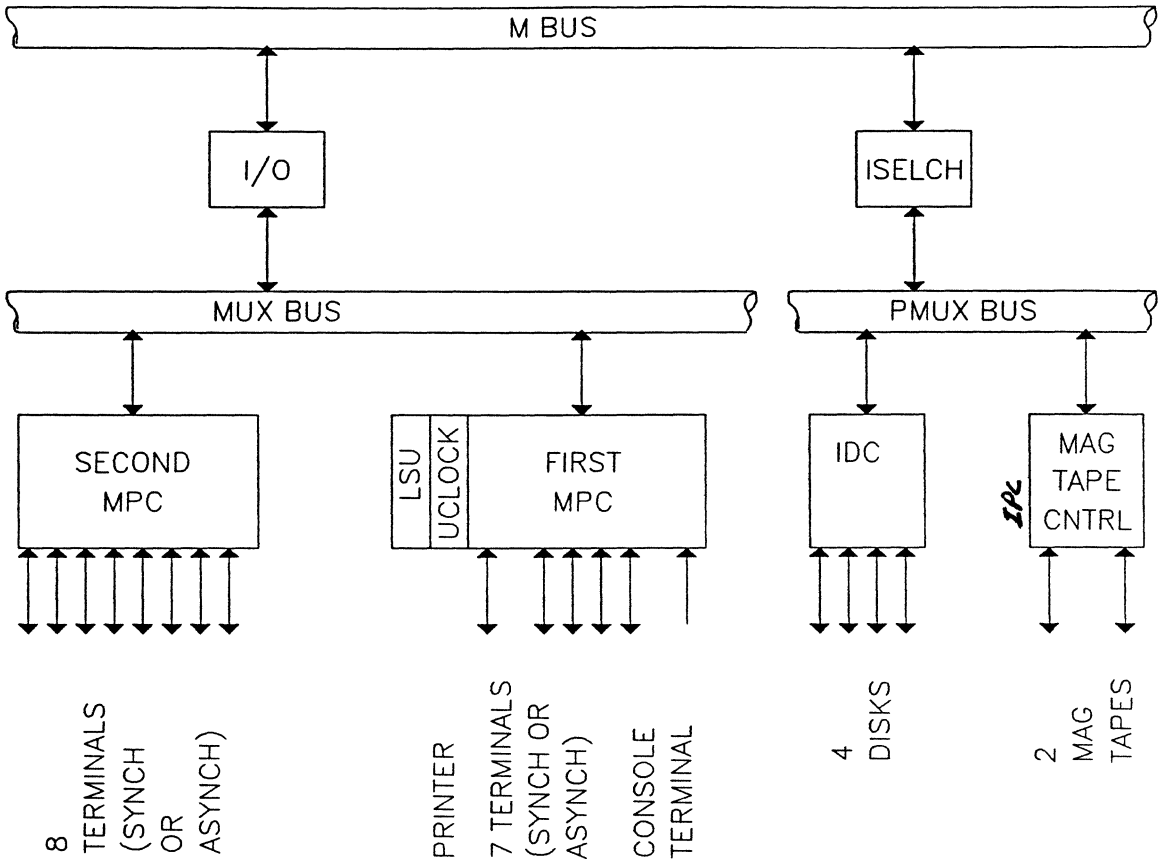
- Memory
Address Regieters
Memory Address Translator (MAT)
Error Check & Correction (ECC)
Error Logger
Direct Memory Access (DMA)
Word Counter
Memory Refresh

- Input/Output (I/O) Interface
MUX Bus
PMUX Bus

- Consolette Interface

- Power Up/Down

2.1 3205 CPU Block Diagram Analysis (cont.)



I/O UNIT BLOCK DIAGRAM

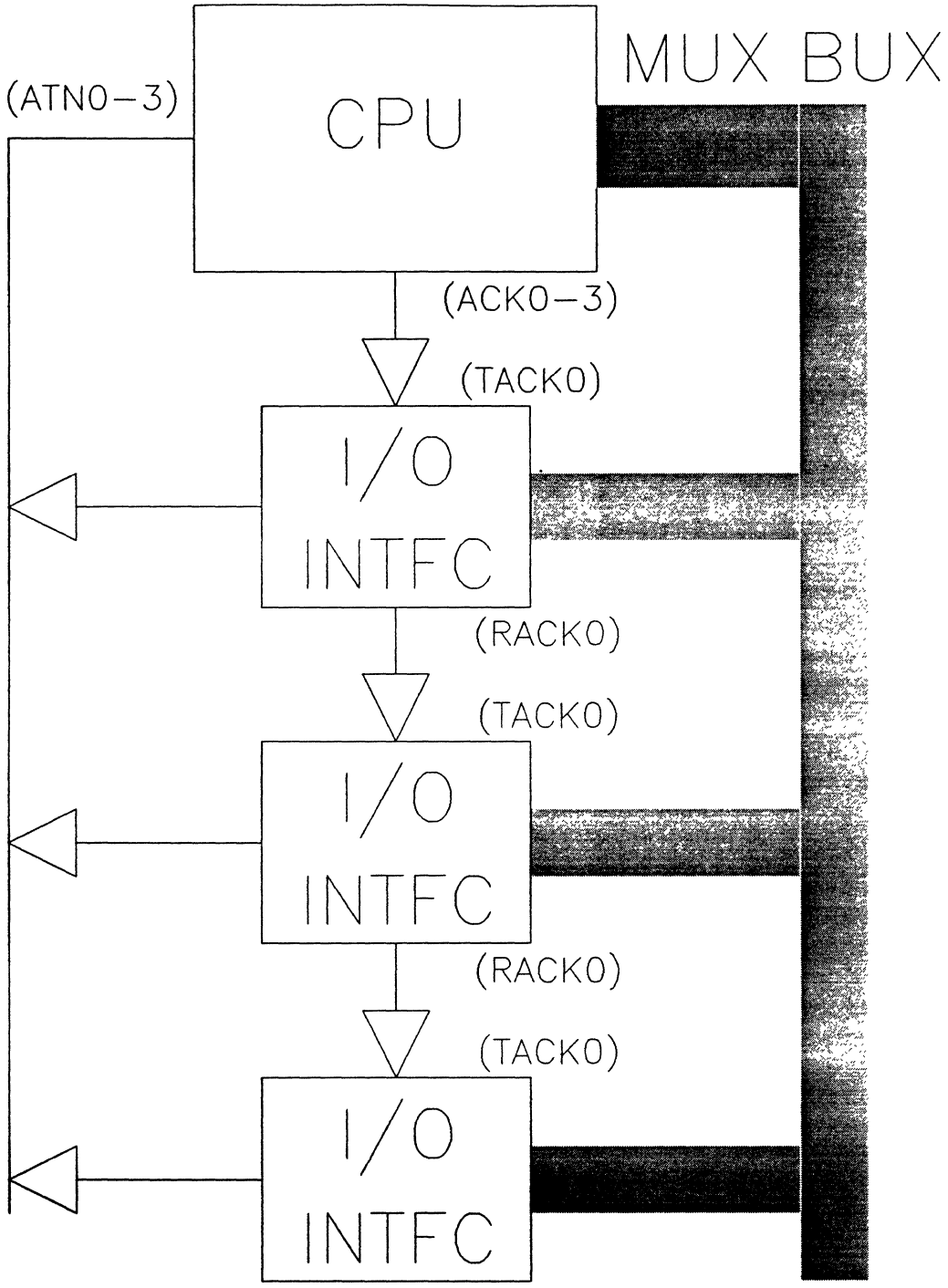
* Input/Output Concepts

  - Types of I/O

    MUXED

    DMA

2.1 3205 CPU Block Diagram Analysis (cont.)



- Types of I/O Control

STATUS DRIVEN

2.1 3205 CPU Block Diagram Analysis (cont.)

INTERRUPT DRIVEN

2.2 USER PROGRAMMING ANALYSIS

* PSW

* Processor Interrupts

* Reserved Memory Locations

* Data Alignment

* Instruction Alignment

2.2 USER PROGRAMMING ANALYSIS (cont.)

* User Instruction Formats

  - Purpose

  - Register to Register (RR)

  - Short Format (SF)

  - Register and Indexed Storage1 (RX1)

  - Register and Indexed Storage2 (RX2)

  - Register and Indexed Storage3 (RX3)

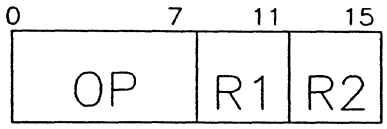
  - Register and Immediate Storage1 (RI1)

  - Register and Immediate Storage2 (RI2)

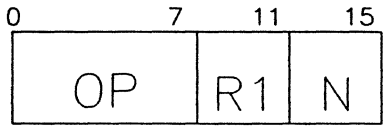
  - RXRX

2.2 USER PROGRAMMING ANALYSIS (cont.)

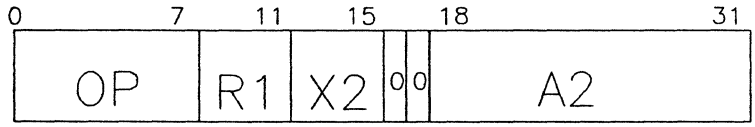
Register–To–Register (RR)



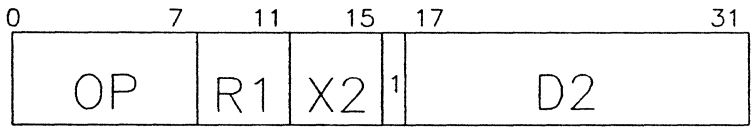
Short Format (SF)



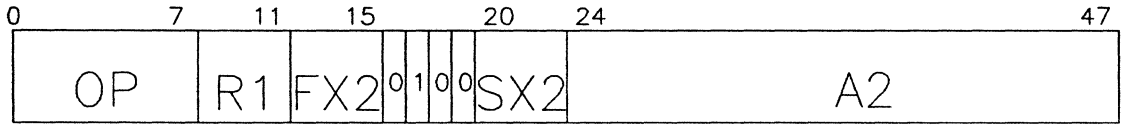
Register & Indexed Storage (RX1)



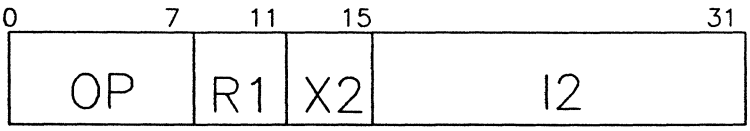
Register & Indexed Storage (RX2)



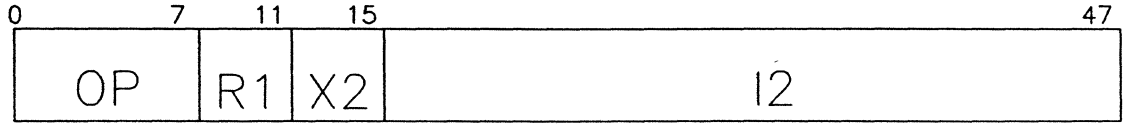
Register & Indexed Storage (RX3)



Register & Immediate Storage 1 (RI1)



Register & Immediate Storage 2 (RI2)



2.2 USER PROGRAMMING ANALYSIS (cont.)

* User Instruction Format Fields

- OP

- R1

- R2

- N

- X2

- D2

- FX2

- SX2

- A2

- I2

2.2 USER PROGRAMMING ANALYSIS (cont.)

* User Instruction Format Fields (cont.)

  - L1

  - L2

  - OPMOD

  - ADD1

  - ADD2

2.3 MEMORY SYSTEM ANALYSIS

* Local Bank Controller included on CPU

- Purpose

- Memory Support (3205) up to 4MB

- Memory Support (3203)

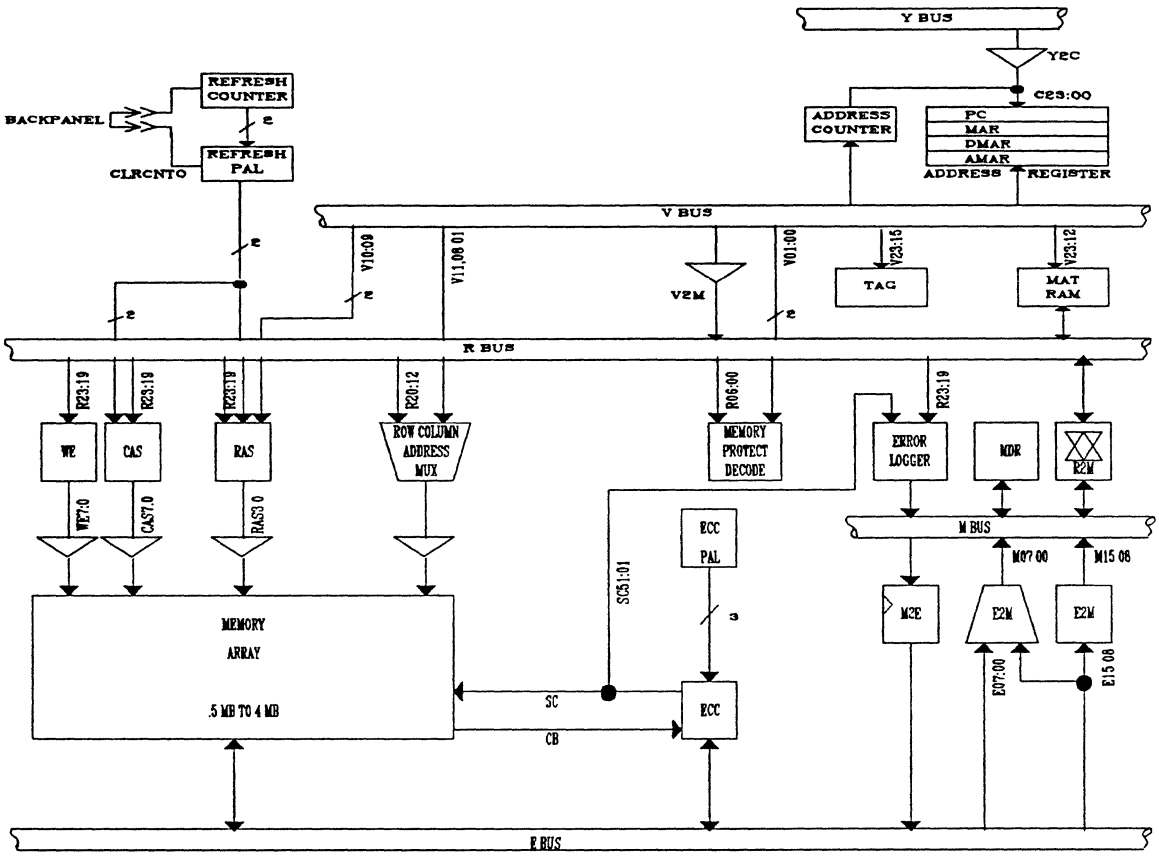
- Error Logger
LOG THE LAST LOCATION only.
This is on a ECC CHIP - 16 BIT

2.3 MEMORY SYSTEM ANALYSIS (cont.)

* Bus structure
* Memory address registers (MAR, PMAR, PC and AMAR)
* Memory register (MR)
* Memory data register (MDR)
* Memory address translator (MAT)
* Error check and correction (ECC)
* Error logger
* Memory array
* Memory refresh

2.3 MEMORY SYSTEM ANALYSIS (cont.)

* Memory Bus Structure



MEMORY UNIT BLOCK DIAGRAM

V-bus

R-bus

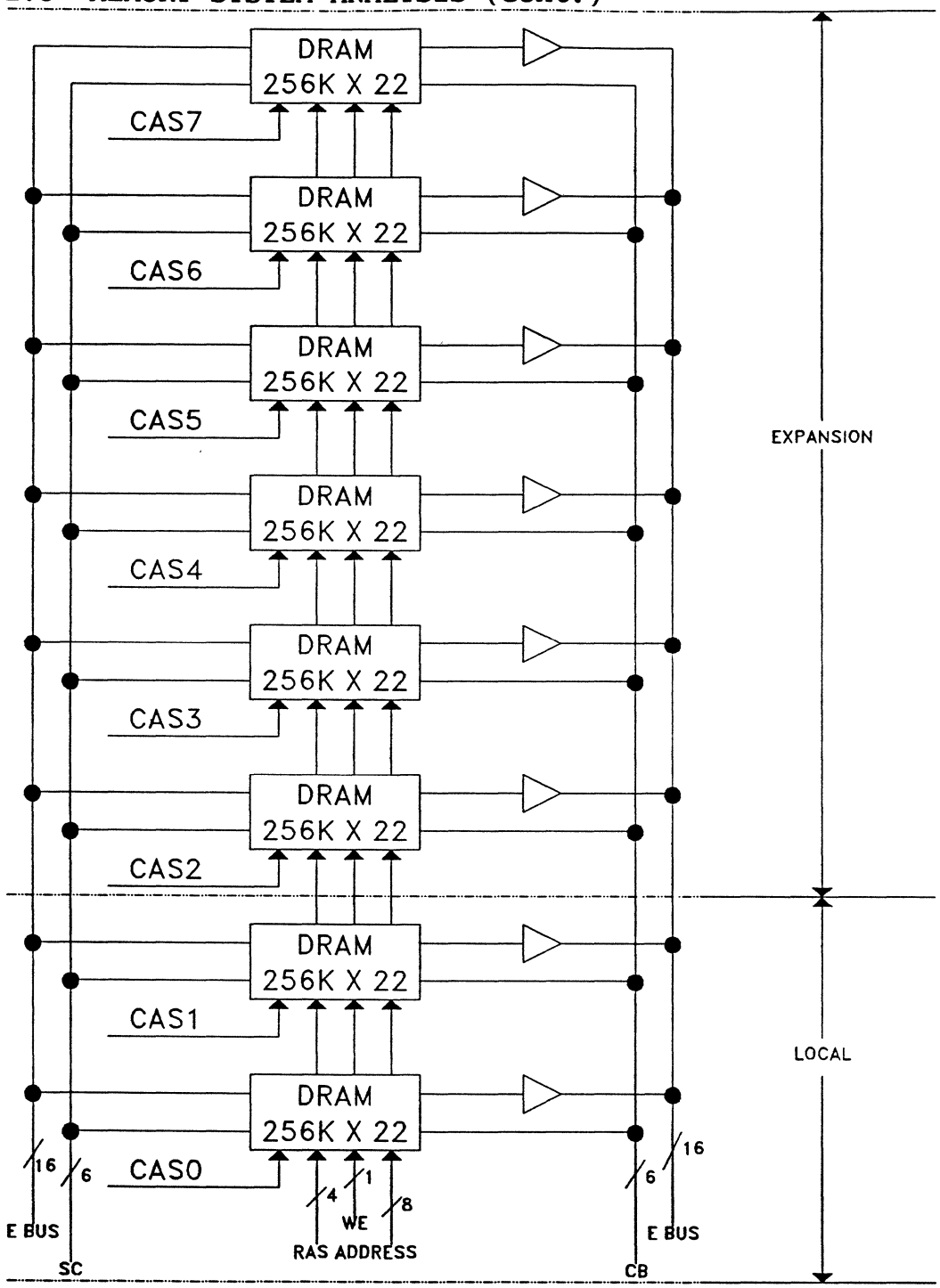
A-bus

C-bus

M-bus

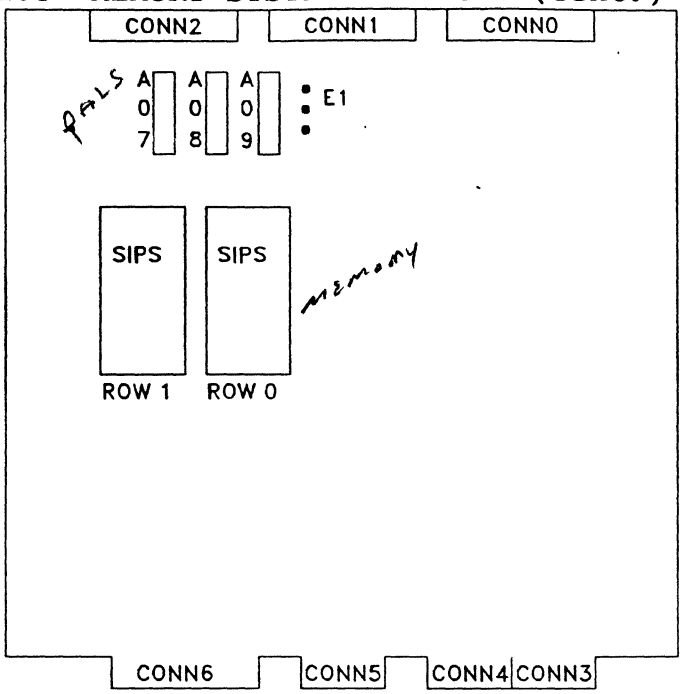
Y-bus

2.3 MEMORY SYSTEM ANALYSIS (cont.)

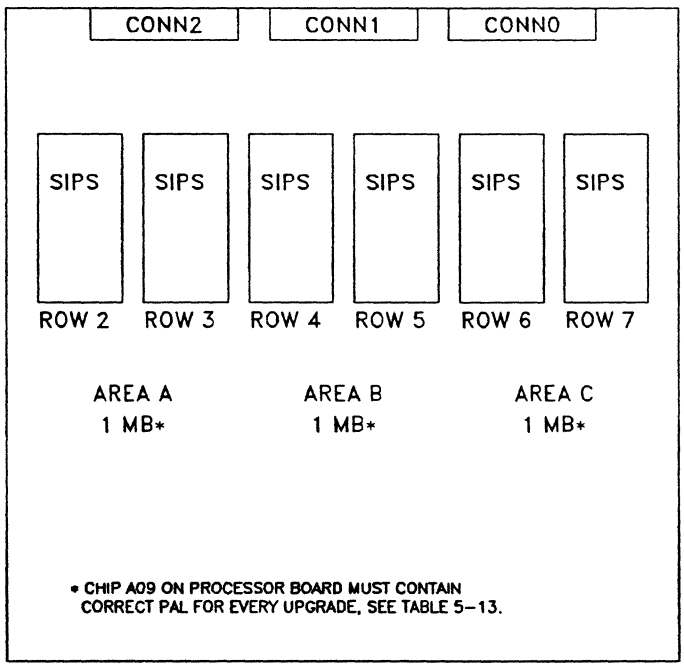


MEMORY ARRAY (with expansion board)

2.3 MEMORY SYSTEM ANALYSIS (cont.)



CPU/MEMORY BOARD



MEMORY EXPANSION BOARD

2.3 MEMORY SYSTEM ANALYSIS (cont.)

MEMORY SIZE	PROCESSOR BOARD	EXPANSION BOARD REQUIRED	CAS PAL REQUIRED LOC A07	WE PAL REQUIRED LOC A08	RAS PAL REQUIRED LOC A09	LOC E1 STRAP	MEMORY SIP REQUIRED
1/2MB	35-864 F00	NOT REQUIRED	19-339 F06	19-339 F07	19-339 F01	1-2	19-326
1MB	35-864 F01	NOT REQUIRED	19-339 F06	19-339 F07	19-339 F02	1-2	19-326
2MB	35-864 F02	35-865 F02	19-339 F06	19-339 F07	19-339 F03	1-2	19-326
3MB	35-864 F03	35-865 F03	19-339 F06	19-339 F07	19-339 F04	1-2	19-326
4MB	35-864 F04	35-865 F04	19-339 F06	19-339 F07	19-339 F05	1-2	19-326
2MB	35-864 F05	NOT REQUIRED	19-339 F09	19-339 F10	19-339 F03	1-2	19-517
4MB	35-864 F06	NOT REQUIRED	19-339 F09	19-339 F10	19-339 F05	1-3	19-517

MEMORY EXPANSION CONFIGURATION

2.4 Power Subsystem Analysis

* 3205

- Description

- Location

- CPU Power (P5 Master/Slave)

- Memory Power (P5U)

- DC Power Distribution

- Battery Backup

- AC Power Distribution

SECTION 3 3205 SYSTEM IDENTIFICATION AND CONTROL

TOPICS:

3.1 Detailed Physical Description

3.2 Operating System Description

3.3 System Control

OBJECTIVES:

Upon successful completion of this section the student will:

1. Be able to physically identify each major component in the 3205 processor system.

2. Be able to physically identify various different I/O devices and associated interfaces on the processor.

3. Be familiar with the basic structures of the Concurrent OS32MT Operating System.

4. Be able to excercise control of the processor outside of the O/S environment.

5. Be familiar with the hardware necessary to and be able to initiate an Operating System on the processor.

6. Be able to excercise control of the system through the use of various O/S commands and Utilities.

7. Be able to create and utilize a "Bootable" O/S tape for emergency use.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 System Installation and Configuration Manual
OS32MT Operators Reference Manual
OS32MT System Utilities Manual
3205 Processor

ADDITIONAL READING MATERIALS:

4.1 DETAILED PHYSICAL DESCRIPTION

* CPU Switches and Indicators

  - 3205

4.1 DETAILED PHYSICAL DESCRIPTION (cont.)

* Chassis and Backplane Identification

  - 3205

4.1 DETAILED PHYSICAL DESCRIPTION (cont.)

* CPU Module Identification

- 3205

4.1 DETAILED PHYSICAL DESCRIPTION (cont.)

* Power Subsystem Identification

- 3205

4.1 DETAILED PHYSICAL DESCRIPTION (cont.)

* Typical I/O Device Familiarization

- System Console

- System Printer

- System Disks

- System Tapes

- Communication Devices

4.2 OPERATING SYSTEM DESCRIPTION

* O/S Structures

- Memory Organization

OPERATING SYSTEM SPACE

TASK SPACE

DYNAMIC SYSTEM SPACE

- I/O Structures

O/S DRIVER

INTERRUPT SERVICE POINTER TABLE

DEVICE CONTROL BLOCK

CHANNEL COMMAND BLOCK

4.3 SYSTEM CONTROL

* Operating Instructions

- Consollette

- Console

- Power Subsystem

4.3 SYSTEM CONTROL (cont.)

* System Console Commands

  - Console Service Routine

* Initiate Program Load (IPL or Boot)

  - Memory Initialization

  - LSU Menu Selection

  - Expected IPL Results

4.3 SYSTEM CONTROL (cont.)

* Operating System Control

- Basic Initial Commands

SET TIME

DISPLAY MAP

DISPLAY DEVICES

INITIATING DEVICES (MARK)

LOAD

4.3 SYSTEM CONTROL (cont.)

* O/S Utilities

- FASTCHEK

- BACKUP

- COPY32

4.3 SYSTEM CONTROL (cont.)

* Initiating a System

- Building BOOT/TASK Tapes

- Loading Tasks from Tape

SECTION 4 SUPPORT/MAINTENANCE/TROUBLESHOOTING - 3205

TOPICS:

4.1 Recognizing Failures

4.2 RECOGNIZING FAILURES - MEMORY SYSTEM

4.3 RECOGNIZING FAILURES - POWER SYSTEM

OBJECTIVES:

Upon successful completion of this section the student will:

1. Be able to identify various different types of failures related to the 3205 Processor.

2. Be able to recognize and interpret various processor hardware Indications in determining CPU failures.

3. Be able to recognize and interpret various processor memory system hardware indicators in determining CPU memory failures.

4. Be able to identify various different types of failures related to the 3205 Processor Power Subsystem.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
35-864 CPU/MEMORY Board Theory of Operation Manual
3205 System Installation and Configuration Manual
3210 Power Subsystem Installation and Maintenance Manual
3205 Processor

ADDITIONAL READING MATERIALS:

4.1 Recognizing Failures - CPU

* O/S Error Indications

  - Error Messages

  - System Crashes

4.1 Recognizing Failures - CPU (cont.)

* Hardware Indications

- 3205

4.2 RECOGNIZING FAILURES - MEMORY SYSTEM

* Hardware Indications

  - 3205

4.3 RECOGNIZING FAILURES - POWER SUBSYSTEM

* Hardware Indications

  - 3205

SECTION 5 SYSTEM TROUBLESHOOTING

TOPICS:

5.1 Troubleshooting Approach

5.2 Understanding/Utilizing Available Tools

5.3 System Crash Troubleshooting

OBJECTIVES:

Upon successful completion of this section the student will:

1. Be able to logically approach processor and system failures for troubleshooting.

2. Be familiar with and be able to effectively troubleshoot processor failures utilizing various troubleshooting tools and aids to include On-line and Off-line diagnostics, Hardware test aids, Programming Handloops, as well as other tools.

3. Be familiar with the system's means for handling and be able to effectively troubleshoot various System Crashes.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 System Installation and Configuration Manual
35-864 CPU/Memory Board Theory of Operation Manual
3205 System Instruction Set Reference Manual
C3MMD Diagnostic Tape and Manuals
C3 On-Line Diagnostic Programs
3200 Programmer Pocket Guide
OS32MT Operators Reference Manual
OS32MT Operating System Map
3205 Processor
Data Line Monitor/Breakout Box
Logic Analyzer

ADDITIONAL READING MATERIALS

5.1 TROUBLESHOOTING APPROACH

*System Failures

- In Preparation

  MAINTAIN PROPER DOCUMENTATION (Manuals,Config,etc.)

  KEEP NOTES (Passed Failures, Setups, etc.)

  ENSURE PROPER TOOLS/AIDS ARE READILY AVAILABLE

  DEVELOP PROPER UNDERSTANDING OF SYSTEM

- Review All Symptoms

  QUERY USER

  EXAMINE PROBLEM

  ATTEMPT TO REPRODUCE PROBLEM

  AVOID HASTY DECISIONS

  AVOID MAKING ASSUMPTIONS

- Keep it Simple

  PHYSICALLY ELIMINATE UNNECESSARY POSSIBILITIES

  KEEP GOOD NOTES

  AVOID BACKTRACKING

  USE TOOLS WISELY (Manuals,Scopes,Meters,etc)

- Tips

  PROBLEM OFTEN PERIPHERALS (Electro/Mechanical)

  CABLES RARELY A PROBLEM (Once working)

  DON'T BECOME OVERWHELM BY PROBLEM (It can be fixed)

  RELY ON SUPPORT BUT ONLY AFTER EXHAUSTING EFFORTS

5.2 UNDERSTANDING/UTILIZING AVAILABLE TOOLS

* Hardware Test Aids

  - System Indicators

  - Meters, Scopes, Etc.

  - Data Monitors, BreakOut Boxes, etc.

  - Logic Analyzers

5.2 UNDERSTANDING/UTILIZING AVAILABLE TOOLS (cont.)

* Support Test Programs

- Diagnostics

ONLINE

OFFLINE

- Programming Handloops

5.3 SYSTEM CRASH TROUBLESHOOTING

* Crash Definition

* Crash Types

* Causes
  - Software
  - Hardware

* Panic Dump
  - Purpose
  - Procedures

5.3 SYSTEM CRASH TROUBLESHOOTING (cont.)

* System O/S Map

  - EREGS

* Using Panic Dump

* Crash tracking without Panic Dump

SECTION 6 INSTALLATION AND CONFIGURATION

TOPICS:

6.1 Site Considerations

6.2 Power Requirements

6.3 Cabling Requirements

6.4 Termination Requirements

OBJECTIVES:

Upon successful completion of this section the student will:

1. Be familiar with various considerations and requirements for the Configuration and Installation of a 3205 system including proper Site, Power, Cabling, and Termination.

2. Be able to effectively Configure and Install a 3205 system.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 System Installation and Configuration Manual
3205 System

ADDITIONAL READING MATERIALS:

34-038 Power SubSystem Installation and Maintenance Manual

6.1 SITE CONSIDERATIONS

* Size

* Environment

  - Cooling

  - Ventilation

6.2 POWER REQUIREMENTS

* CPU

* Peripherals

* Power Protection
  - Ground

  - Insulation

  - Current Requirements

6.3 CABLING REQUIREMENTS

* System Cabling

* Peripheral Cabling

6.4 TERMINATION REQUIREMENTS

* Purpose

* System Termination

* Peripheral Termination

SECTION 7 DOCUMENTATION

TOPICS:

7.1 C3 Documentation

7.2 Vendor Documentation

OBJECTIVES:

Upon successful completion of this section the student will:

1. Be familiar with the C3 as well as the Vendor documentation associated with the 3205 processor and various key peripherals and their interfaces.

TRAINING MATERIALS:

3205 Processor Hardware Course Student Guide
3205 System Installation and Configuration Manual
3205 System Instruction Set Reference Manual
35-864 CPU/Memory Board Theory of Operation Manual
34-038 Power Subsystem Installation and Maintenance Manual
C3 Maintenance Guide Manual
C3 Field Alerts
Concurrent Two Line Communications Multiplexer Manual

ADDITIONAL READING MATERIALS

7.1 C3 DOCUMENTATION

* C3 Maintenance Guides

* C3 Field Alerts

* Product Manuals

7.2 VENDOR DOCUMENTATION

* Concurrent
  - Processor Manuals
  - Memory System Manuals
  - Power Subsystem Manuals
  - Diagnostic Manuals

* Other Vendors
  - Product Manuals
  - Diagnostic Manuals

The Model 3205 is a low-cost, physically small 32-bit Processor. The Model 3205 is packaged in an eight-slot, seven-inch high chassis for mounting in a 19" EIA cabinet or enclosure. The Model 3205 processor is implemented as a single board with features such as floating point, Selector Channel and up to 1MB of memory integral to the design. A second board, the Multi-Peripheral Controller (MPC), contains the most commonly used peripheral items such as clocks, a boot loader, eight asynchronous or synchronous communications lines,and a parallel line printer interface. A third board is optional for expansion of memory up to a maximum of four megabytes.

32-bit Architecture -- The Model 3205 supports the full line of features characteristic of the Series 3200.

User Available Registers -- The Model 3205 incorporates eight sets of sixteen 32-bit general-purpose registers.

Comprehensive Instruction Set -- The Series 3200 instruction set includes a comprehensive array of instructions for general-purpose processing.

Memory Management -- Integral too the processor is a Memory Manager which provides memory segmentation, relocation and protection under operating system control.

Dual Bus Architecture -- The Model 3205 supports two communications buses: a man/machine path referred to as the Multiplexor Bus, and a high-speed machine/machine path, referred to as the Selector Channel Bus.

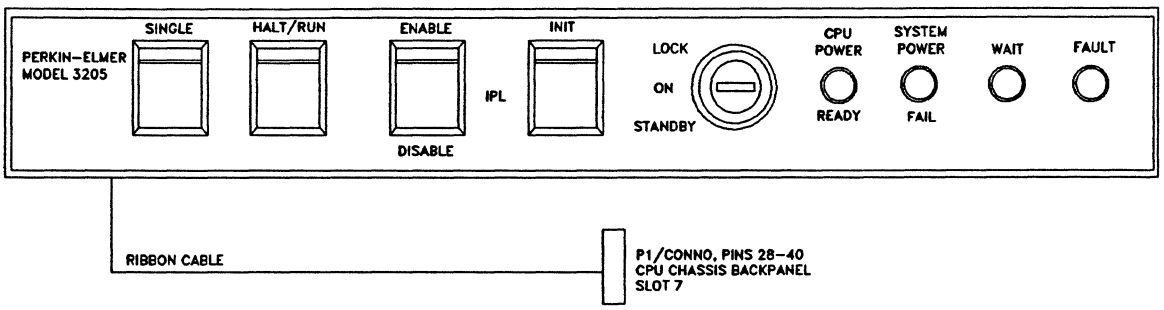
MEMORY STSTEM

The Model 3205 supports up to 4 MB of directly addressable main memory using 64K RAM technology. This enables the processor to support up to 1MB on the CPU board with an additional 3 MB on a memory expansion board. Memory is expandable in increments of 1, 2, or 3 megabytes.

Error Correcting Code -- Error detection and correction is a standard feature of the Model 3205 memory system. All single-bit errores are detected and corrected. all double-bit errors and some multi-bit errors are detected.

Error Logger -- The Error Logger records datd that allows the identification of error trends.

Battery Backup -- The model 3205 options include a battery power retention system. It provides memory power for up to 8 minutes.



CONSOLETTE CABLING

FUNCTION SWITCHES

1. KEY-OPERATED..... SECURITY LOCK

This is a 3-position (STANDBY/ON/LOCK) key-operated locking switch that controls the primary power to the system. The key lock performs the following functions:

STANDBY - Processor 5 volts is OFF. 5 volts STANDBY (P5U) is ON.

ON - Primary power is ON.

LOCK - Primary power is ON, and the INITIALIZE HALT/EXE and SINGLE switches on the system control panel are disabled.

2. INITIALIZE (INIT)... SWITCH (MOMENTARY SWITCH)

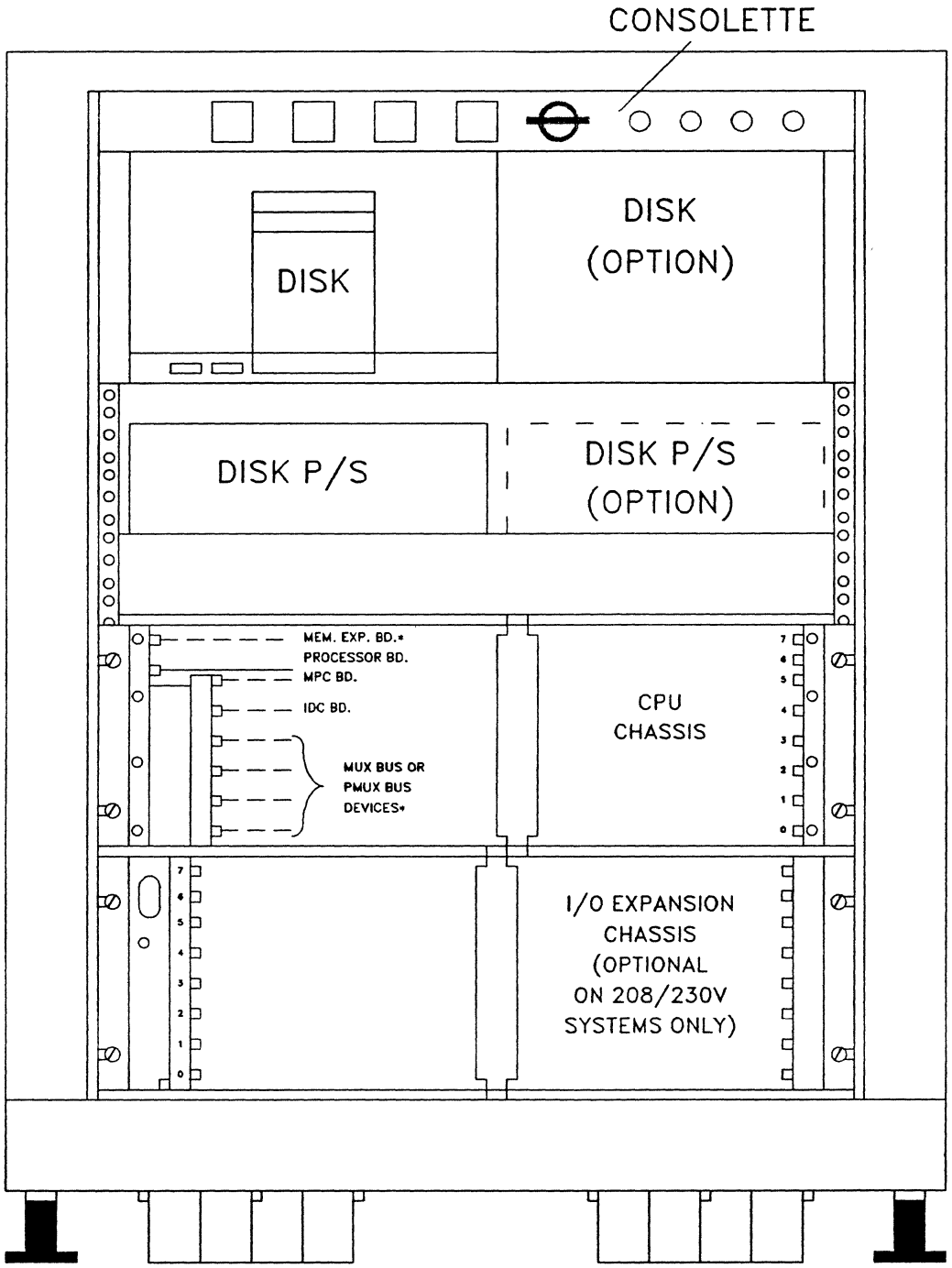
This switch causes the system to be initialized. After the initialized operation, all device controllers on the system multiplexor bus are cleared and certain functions in the processor are reset. This switch is disabled when the key is in the LOCK position.

3. IPL ENABLE/DISABLE SWITCH	When the IPL ENABLE/DISABLE switch is in the ENABLE position and AC power is restored, if the security lock switch is placed in the ON position from the STANDBY position, or if the INIT switch is depressed, the system is reloaded from the loader storage unit (LSU).
4. HALT/RUN SWITCH	When depressed, this single action switch causes a running system to halt and enter the processor console service state, or it forces a halted system in the processor console service state to enter the run mode.
5. SINGLE SWITCH	This switch, when placed in ON position, puts the processor in the single instruction cycle mode and takes a running program to the processor console service mode. When in the single instruction cycle mode, the processor is returned to the processor console service mode after execution of each user Instruction. The location counter displays the address of the next instruction to be executed. The status portion of the PSW reflects the execution of the previous instruction.

INDICATORS

1. CENTRAL PROCESSING UNIT (CPU) POWER	This indicates that CPU system power (P5) is ON.
2. MEMORY POWER	This indicates that memory system power (P5U) is ON.
3. WAIT	The running program can place the processor into the WAIT state by setting the WAIT bit of the current program status word (PSW). The WAIT indicator is lit to inform the operator of this condition. The indicator is also lit when the processor is in the console service mode.
4. FAULT	This indicator is lit during system initialization and remains lit until microcode power-up test is successfully completed. The indicator remains on if the processor 7elf-test fails.

CABINET CONFIGURATION



* OPTIONAL

MODEL 3205 SYSTEM CABINET

50Mb Cartridge Disk Drive (CDD50)

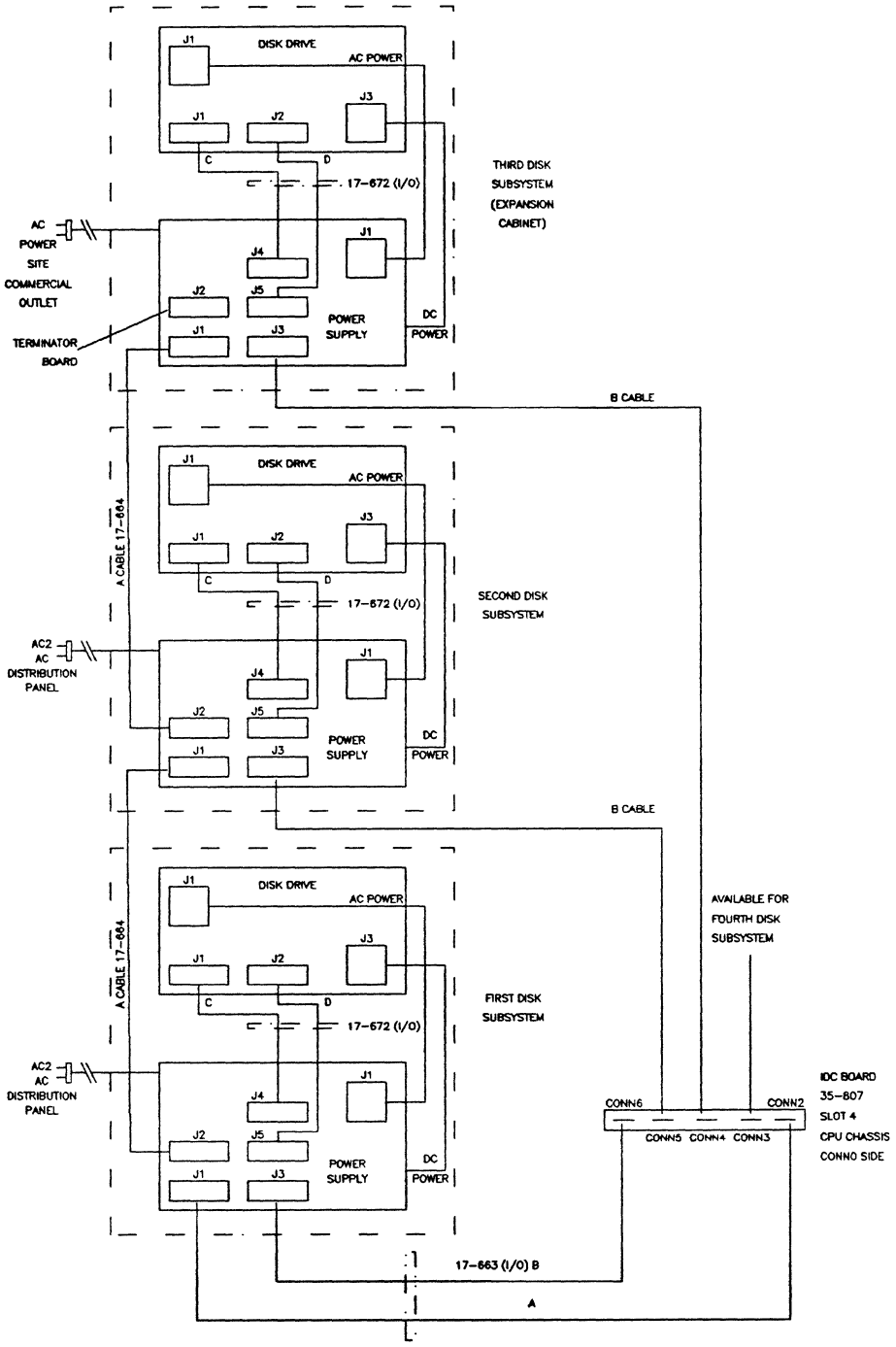
The disk chassis is mounted directly below the consolette to the front uprights. The disk power supply and power supply chassis are mounted below the disk drive chassis to the rear uprights. The 11-333 fan panel is mounted behind the disk drive chassis.

The disk drive is installed in the chassis by engaging the disk-mounting plates inthe guides of the chassis. The disk mounting plate is secured tothe disk chassis in the rear by one screw and is secured to the cabinet by two plastic fasteners located directly below the front of the disk. When installing the expansion disk drive in the cabinet, the disk stop mechanism must be mounted to the disk chassis by two screws.

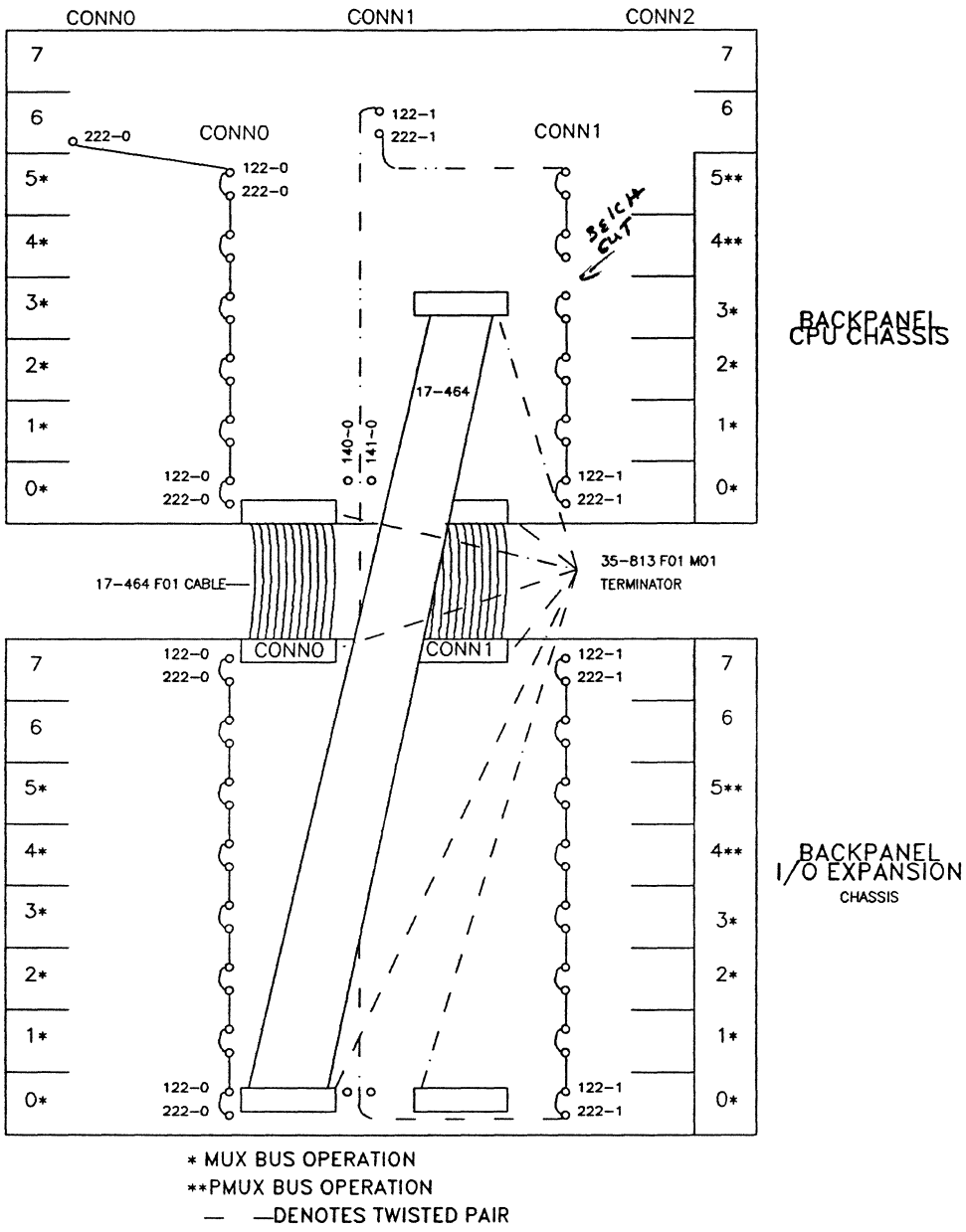
The disk drive is supported when extended from the cabinet to expose the locking pin located on the top surface of the disk drive. The carriage locking pin must be in the unlocked position for proper operation of the disk and in the locked position when the disk drive is removed from the cabinet.

CAUTION
DO NOT REMOVE THE CARRIAGE LOCKING PIN AT ANY TIME. THE AIR SYSTEM SEAL INTEGRITY OF THE DISK REQUIRES THAT THIS SCREW REMAIN IN THE TOP COVER AT ALL TIMES.

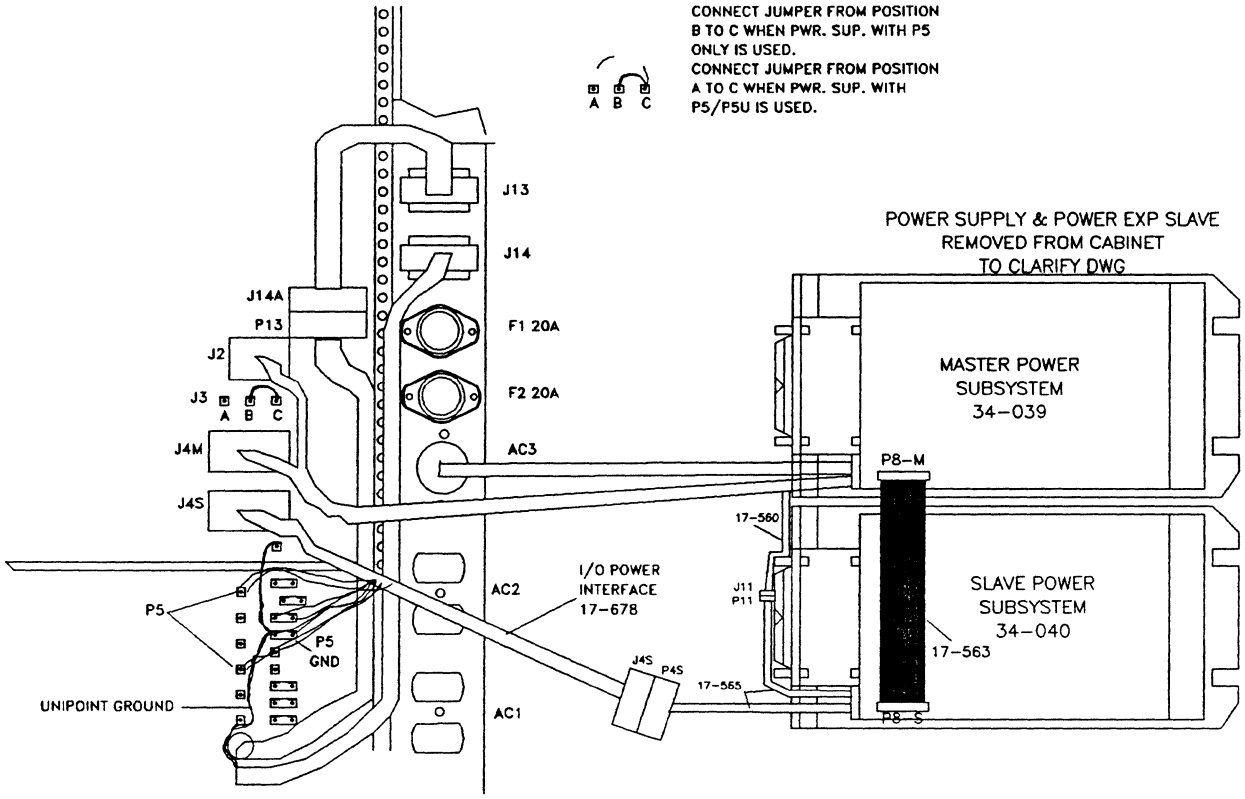
To remove the disk drive from the cabinet, it is necessary to override the stop mechanism located at the bottom surface of the disk chassis.



DISK DRIVE CABLING



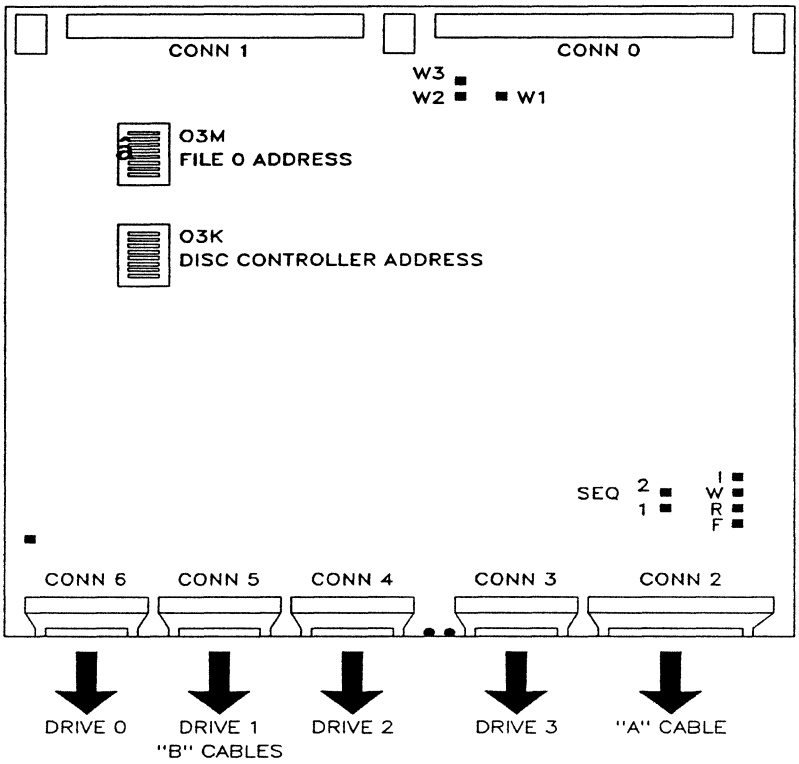
INTERRUPT PRIORITY WIRING



POWER SUPPLY AND SLAVE POWER SUBSYSTEM CABLING

IDC STRAPPING

The following are the strap options for the Concurrent Intelligent Disc Controllor, IDC.



IDC

CONTROLLER ADDRESS. Open=1, Closed=0. Example: All open except switch 6 - x'FB.
FILE ADDRESS. Switch positions 1 through 6 = six MSB of address. Example: 1 through 6 open = x'FC. Only the first file address needs to be set the rest are derived from this.
PROTOCOL. Switch 7 of O3M. Open=High Speed Protocol, Closed=Normal Protocol.
Format Enable. Switch 8 of O3M. Open=Format Enable, Closed=Format Disable.
W1,W2,W3. Strap W1-W3 when under Concurrent Bus Switch, W1-W2 all othe applications.
SEQUENCE. No strap=drives are powered up sequentially.