PROGRAMMING LANGUAGE

The basic language is of the symbolic assembly level, although both symbolic and octal changes will be provided for. If an acronym is desired, a memorable one would be IPL, for "IRAM Programming Language". The vocabulary and format of the language have been adopted wherever possible from the standard machine language coding of a major computer manufacturer. Numbers with a leading zero are taken as octal, otherwise as decimal.

1	2 6	7	8 10	11 12 15	16	
	LOCATION FIELD		OPER. CODE FIELD	Normally Unused	VARIABLE FIELD	COMMENTS

Coding Sheet Format

Location Field

This may contain a (location) symbol, required only if the word being coded is referred to elsewhere in the program. A symbol consists of from one to six alphanumeric characters, the first of which must be alphabetic, and none of which may be the special characters + (plus) - (minus) * (asterisk) / (slash) , (comma) $ (dollar). A pure number in the location field will set the core memory location to that value. Certain symbols have predefined numerical equivalences and/or meanings, hence can not safely be used except as intended: Register storage (A, B, C, Q, D0 through D9, E0 through E9, EA, EB) and all input-output signal designations, particularly analog outputs, which are allocated to "sacred cells" 1984 through 2022 (see IDC #2915.01/26 for equivalent instruction addresses).

Operation Code Field

For all machine instructions, a 3-letter mnemonic op code goes in columns 8-10. These are given below, in the information pertaining to each individual instruction. All assembler pseudo-operations, such as for constant definition, may also have 3-letter codes. These will be defined in a later document, and if longer, will extend into columns 11-15. If an instruction is to be indexed, an "*" is coded in column 11.

Variable Field

This may have as many as three subfields, separated by commas, each containing a "symbolic expression". A symbolic expression consists of one or more integers and/or symbols, separated by the integer arithmetic operators +, -, *, and /, signifying addition, subtraction, multiplication and division, respectively. The last two are performed on elements of an

expression, from left to right, before the first two are performed. For example, A-A/B*B is evaluated as A-[A/B]B, where [A/B] is "the greatest integer in A divided by B", and so the expression produces A modulo B. In any case, the first character must be in column 16, and there may be no imbedded blanks, for the first blank detected terminates the variable field. All other characters to the right on a card will be taken as comments. Columns 73-80 may be specialized to an identification number.

The special character $ in the variable field has the significance of "present location", or "here". It may be used within a symbolic expression as if it were a symbol. The combination $$, by itself, may be coded to indicate "to be initialized".

INSTRUCTION INFORMATION

The detailed information given below for each HCM-204 instruction is presented in the following format:

Octal Code Short Name Coding Usage Timing

Description of Operation of Instruction

The octal code is of the form UV or UV-W. U represents bits 18-16, V represents bits 15-13 (assuming a zero in bit 13), and W represents, where needed, the extended operation modifier in bits 10 and 11.

The short name is reasonably descriptive of the basic action of the instruction.

"Coding Usage" typifies the instruction as it is to appear on coding sheets. The 3-letter mnemonic operation code is on the left. An appended asterisk (*) indicates that the instruction is indexable, and will be indexed if the asterisk is so coded. Spaced to the right is a representation of the variable field (if any) to be coded for the instruction. Subfields, if any, are shown in their required sequence. Nothing in the following is to be construed as prohibiting any field or subfield from being coded as any legitimate symbolic expression, including an integer. Letters have been used in the variable field representations according to the following conventions:

- Y - RAM location
- N - Shift count
- B - Binary code
- D - Input-output signal designation (e.g., A54A, D120, G83)
- K - Block number
- C - Channel

Timing is given in terms of CT (clock time). For worst case drum slippage a clock time is currently about 2.71 μ s.

In the descriptions, any bits or contents of registers not specifically mentioned are not affected by execution of the pertinent instruction. Primed letters signify effective addresses after indexing, if selected, throughout. Thus Y′ is an effective location, and N′ is an indexed shift count.

DATA TRANSMISSION INSTRUCTIONS

04 Clear and Add — CLA* Y — 4 CT

The contents of RAM location Y' are loaded into the accumulator. Y' is unchanged.

16 Clear and Add Logical — CAL* Y — 4 CT

The positive magnitude of the contents of RAM location Y' is loaded into the accumulator. Y' is unchanged.

12 Clear and Subtract — CLS* Y — 4 CT

The two's complement of the contents of RAM location Y' is loaded into the accumulator. Y' is unchanged.

64 Store — STO* Y — 4 CT

The contents of the accumulator are stored in RAM location Y'. The accumulator is unchanged.

52 Store Address — STA* Y — 4 CT

The contents of the accumulator address field (ACC_{11-1}) are stored in the address field of RAM location Y′ (Y'_{11-1}). The accumulator and Y'_{18-12} are unchanged.

14 Load Q Register — LDQ* Y — 4 CT

The contents of RAM location Y' are loaded into the Q register. Y' is unchanged.

22 Store Q Register — STQ* Y — 5 CT

The contents of the Q register are stored in RAM location Y'. The Q register is unchanged.

ARITHMETIC INSTRUCTIONS

06 Add — ADD* Y — 4 CT

The contents of RAM location Y' are added to the contents of the accumulator. Y' is unchanged. The indicator is set if overflow occurs.

10 Subtract — SUB* Y — 4 CT

The contents of RAM location Y' are subtracted from the contents of the accumulator. Y' is unchanged. The indicator is set if overflow occurs.

40 Multiply — MPY* Y — 22 CT

The most significant portion of the product of the contents of the accumulator and RAM location Y' replaces the contents of the accumulator. The least significant portion replaces the contents of the Q register. Y' is unchanged.

42 Divide — DVP* Y — 22 CT

The quotient of the contents of the accumulator divided by the contents of RAM location Y' replaces the contents of the Q register. The contents of the accumulator are replaced by a remainder exactly as would have been computed by the Model VI Digitair, although one bit longer. Y' is unchanged. The indicator is set by a divide check and the quotient is appropriately set to positive or negative full scale.

LOGICAL INSTRUCTION

02 AND to Accumulator — ANA* Y — 4 CT

The logical AND of the contents of the accumulator and the RAM location Y' replaces the contents of the accumulator. Y' is unchanged.

SHIFT INSTRUCTIONS

24-0 Accumulator Left Shift ALS* N (N'+4) CT

The entire contents of the accumulator (ACC_{18-1}) are shifted left N' bit positions. Least significant bit positions vacated are filled with zeroes. Bits shifted beyond the sign bit (ACC_{18}) are lost. Note that this instruction is a logical left shift, as well as an algebraic left shift for two's complement numbers.

24-3 Algebraic Right Shift ARS* N (N'+4) CT

The entire contents of the accumulator (ACC_{18-1}) are shifted right N' bit positions. As the sign bit (ACC_{18}) is vacated at each step, it is replaced by itself, thus effecting a propagation of the sign bit into the N most significant magnitude bits, and preserving the sign of a two's complement number being shifted. Bits shifted beyond the least significant bit (ACC_1) are lost.

24-2 Logical Right LGR* N (N'+4) CT

The entire contents of the accumulator (ACC_{18-1}) are shifted right N' bit positions. As the sign bit (ACC_{18}) is vacated at each step, it is filled by a zero. Bits shifted beyond the least significant bit (ACC_1) are lost.

DISPLAY INSTRUCTIONS

56 Display RAM Location DRL* Y 4 CT

The contents of RAM location Y' are loaded into the display register. Y' is unchanged.

60-0 Display Accumulator DAC 4 CT

The contents of the accumulator are loaded into the display register. The accumulator is unchanged.

60-1 Display Index Register DXR 4 CT

The contents of the index register are loaded into the five least significant bit positions of the display register. The 13 most significant bits of the display register are set to zeroes. The index register is unchanged.

CONTROL INSTRUCTIONS

30 **Transfer** TRA* Y 4 CT

Control is unconditionally transferred to RAM location Y'.

32 **Transfer on Non-Zero** TNZ* Y 4 CT

Control is transferred to RAM location Y' if the contents of the accumulator are not zero. Otherwise, control goes to the next instruction in normal sequence.

34 **Transfer on Minus** TMI* Y 4 CT

Control is transferred to RAM location Y' if the sign of the accumulator contents is negative. Otherwise, control goes to the next instruction in normal sequence.

36 **Transfer if Indicator On** TIN* Y 4 CT

Control is transferred to RAM location Y' if the indicator is set. Otherwise, control goes to the next instruction in normal sequence. The indicator is reset only at the beginning of execution of an addition, subtraction or division instruction. It is set only if such execution results in overflow or the divide check condition.

46 **Halt, then Proceed** HPR* Y 4 CT

If halt is enabled, the computer stops. If the start button is then depressed, control goes to the next instruction in normal sequence. If halt is disabled, the following standard emergency procedure is initiated: The contents of channel 0 of the drum are read into blocks 0, 1, and 2 of the RAM. Then control is transferred to RAM location zero.

70-1 **Set "Not Lost"** SNL 4 CT

The "Not Lost" indicator is set. This prevents the standard emergency procedure from being initiated when the real time counter next overflows. The "Not Lost" indicator is reset at the time of each overflow. The program then has 5.12 seconds within which to set it by means of this instruction.

00 **No Operation** NOP 4 CT

Control goes to the next instruction in normal sequence, after a delay of four clock times.

50 Transfer and Set Return TSR* Y 5 CT

The program counter is stored in the address field on RAM location Y' (Y'_{11-1}). Control is then unconditionally transferred to RAM location Y'+1.

INDEX REGISTER INSTRUCTIONS

54 Transfer on Index TIX Y 4 CT

The contents of the index register are tested. If not zero, control is transferred to RAM location Y. Otherwise, control goes to the next instruction in normal sequence. In either case, the contents of the index register are decremented by one after the test.

44 Transfer on Index Bit TXB Y,B 4 CT

Control is transferred to RAM location Y if the specified index register bit is a one. Specification is by means of the binary code B, which goes in bits 12 and 13 of the instruction. The index register bit position selected is one greater than the value of B, e.g., B=2 corresponds to bit 3. The most significant bit of the index register cannot be tested. If the selected bit is a zero, control goes to the next instruction in normal sequence. In any case, the index register is unchanged.

60-3 Place Accumulator in Index PAX 4 CT

The three most significant magnitude bits of the accumulator are placed into the three least significant bit positions of the index register. The two most significant bits of the index register are set to zero. The accumulator is unchanged.

66 Load Index from Address LXA Y 4 CT

The five least significant bits of the address field of RAM location Y replace the contents of the index register. Y is unchanged.

20 Store Index in Address SXA Y 5 CT

The contents of the index register replace the five least significant bits of the address field of RAM location Y. The index register and the 13 most significant bits in Y are unchanged.

INPUT-OUTPUT INSTRUCTIONS

72-2 Read Analog Input RAI* D 108-225 CT

The AC or DC voltage in 10-bit digital form specified by signal designation D' is read into bits 1-10 of the accumulator (ACC_{10-1}). Other bits of the accumulator are set to zero. set to zero.

72-3 Read Digitizer RDG* D 108-225 CT

The 13-bit input from the air data computer digitizer specified by signal designation D' is read into bits 2-14 of the accumulator (ACC_{14-2}). Other bits of the accumulator are set to zero. set to zero

72-1 Load Index from Input LXI D 4 CT

The 4-bit digital input group containing the signal of designation D is loaded into the least significant bits of the index register. The most significant bit is set to zero. D may also be a group designation.

72-0 Read Digital Input RDI* D 4 CT

The 4-bit digital input group containing the signal of designation D' is loaded into the least significant bits of the accumulator (ACC_{4-1}). All other accumulator bits are set to zero. D may also be a group designation.

72-0 Real-Time Counter RTC 4 CT

The current contents of the 10 most significant bits of the real-time counter are read into bits 4-13 of the accumulator. The counter is unchanged. Remaining bits of the accumulator are set to zero. The bits read have a resolution of 5 ms, and therefore, the clock overflows at 5.12 sec. If at least once between overflows the SNL instruction is not executed, the standard emergency procedure is instituted when overflow occurs.

24-1 Read Data Link RDL N (2N+4) CT

The next N bits from the current data link message are right-shifted into the N most significant magnitude bits of the accumulator, entering through bit 17. The accumulator sign bit must be in the zero condition for successful execution of this instruction.

In practice, N will have the values 5, 16, 16 and 2, in a cycle to access the complete 39 bits of a data link message. Each reading will be followed by a logical right shift sufficient to right-justify the message portion to accumulator bit 2, so that the former accumulator contents are entirely lost, except that bit 17 has been moved to bit 1. The last three portions are then stored, based on the address in the first. The data link message-storing routine is entered as the result of a program interrupt made when a new message becomes available: The hardware simulates a transfer and set return instruction, storing the current program counter in RAM location zero and transferring control to location one.

70-0 Write Digital Output WDO* D 4 CT

The digital output(s) containing the signal of designation D' is(are) sent from the accumulator to the input-output section of the computer. The accumulator is unchanged. The actual address assembled for the HCM 204 word will differentiate between 1-, 2- and 4-bit outputs, from accumulator bits 18, 17-16 and 17-14, respectively. D may also be a group designation.

64 Store Analog Output SAO* D 4 CT

The contents of the accumulator are stored in the RAM "sacred cell" Y' allocated to signal D'. Within 15 milliseconds the 10 most significant magnitude bits of Y' (Y'_{17-8}) are converted to a DC voltage.

DRUM INSTRUCTION

76 Read Drum Block(s) RDB K,B,C (1538 X No.Blocks)+ 150 CT minimum

The blocks (specified by the 3-bit code B) of channel C of the drum are read into the RAM starting at the first word of block number K, with location zero following location 2047. The code B is of the form UVW, where U,V and/or W are zero or one according as to whether the first, second, and/or third blocks are to be read in (Mnemonic device: zero is a hole through which the desired block can fall into core). Consecutive blocks must be selected, so that codes 111 and 010 must not be used. After the instruction is given, drum reading will start only after a point on the drum has been passed which is 150 CT before the beginning of the first block to be read.

DR - 138

HUGHES AIRCRAFT COMPANY

INTERDEPARTMENTAL CORRESPONDENCE

TO: D. B. Robinson
ORG. 29-23-01

CC: See Distribution

DATE: 18 May 1965
REF. 2923.10/358

SUBJECT: Programmers' Description of HCM-204

FROM: D. W. Giedt
ORG. 29-23-01

BLDG. 6 MAIL STA. E 107
EXT. 6377

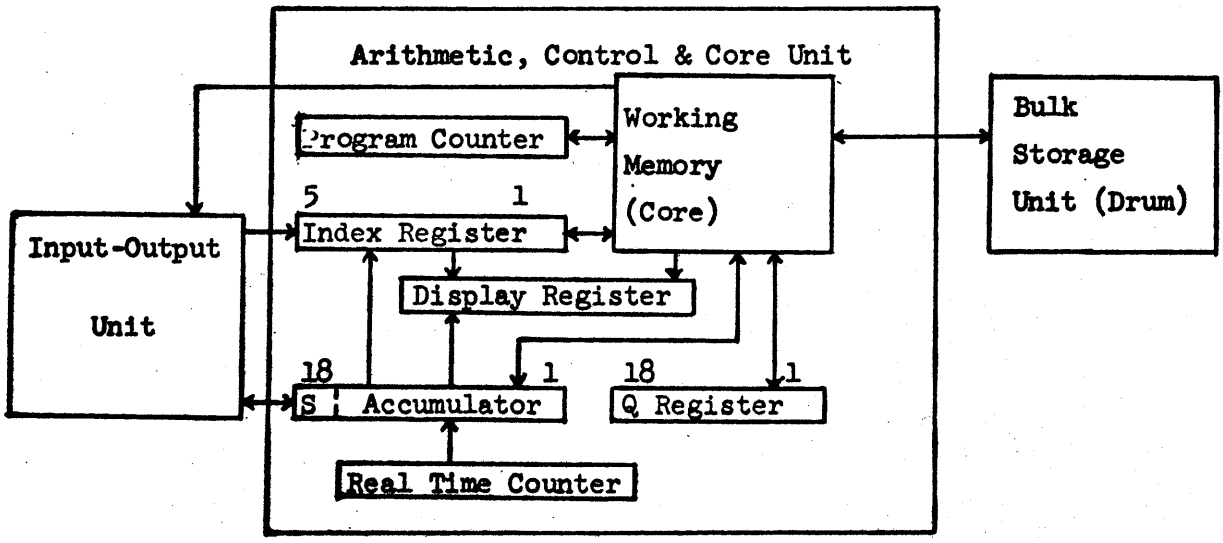
NOTE: This IDC supersedes IDC 2923.10/340.

The purpose of this document is to provide an understanding of the HCM-204 from the programming viewpoint, both for those who are directly concerned with HCM-204 programs, and for those who will write IBM 7094 programs concerning the HCM-204.

The HCM-204 is a general purpose, parallel, digital computer being applied as the direct replacement of the Model VI Digitair computer in the MA-1 Navigation and Fire Control System of the F-106 interceptor. The following general description is thought to be accurate as of publication, but is certainly subject to change.

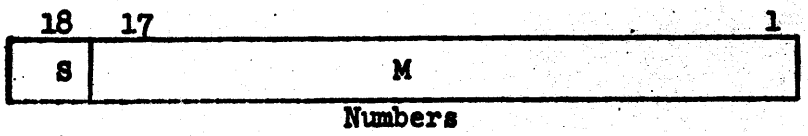
Arithmetic system is two's complement, with the binary point effectively between the sign and most significant magnitude bits of a word.

Word length is 18 bits throughout, including sign of number. Instructions have single-address structure, the address field normally being the least significant 11 bits. Operation codes are found in the most significant five bits, occasionally having a 2-bit modifier.



Machine Organization, Showing Effective Data Paths

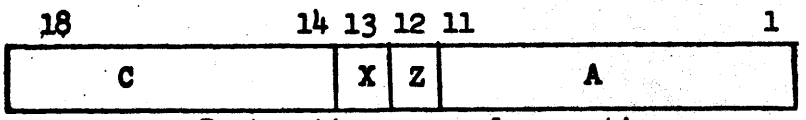
Word formats are given following. Bit positions are numbered as at top of diagrams. Fields are designated by letters inside, and described below.



Numbers

Field S - Sign

Field M - Magnitude



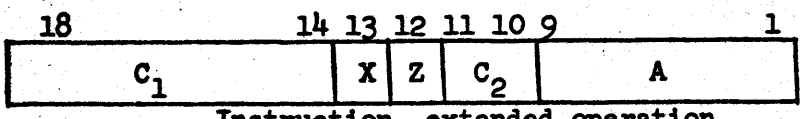
Instruction, normal operation

Field C - Operation Code

Field X - Index register selection

Field Z - Unused in all but two instructions

Field A - RAM address, except for special usage in three instructions concerning drum.



Instruction, extended operation

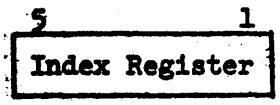
Field C_1 - Basic operation code

Field X - Index register selection

Field Z - Unused

Field C_2 - Modifier, to extend operation code

Field A - Specialized address, sometimes unused



Indexing, where available and selected by a one in bit 13, is effected by adding the contents of the 5-bit index register to the instruction. This results in an "effective address", A'. Indexing which will make the address field overflow should be avoided, since carries beyond the address field are not inhibited, so that under particular circumstances even the operation code can become altered.

Working memory is a 2048-word random access core memory (RAM). It is considered to consist of eight 256-word blocks, numbered 0 through 7.

Bulk storage is provided by a non-executable drum having 44 channels of 768 words each, for a total of 33,792 words. A channel is divided into three 256-word blocks. Any one, two or three consecutive blocks from a channel may be transferred by one instruction into any one, two or three consecutive core blocks, with block 0 following block 7.

Programmable registers consist of the accumulator, Q register and the display register, all 18 bits in length; the program counter, 11 bits; the real-time counter, 10 bits with a resolution of five milliseconds, and the 5-bit index register. Action of these registers is defined in a separate programming manual, IDC 2923.10/345.

Instruction timing is in terms of clock times (CT). A clock time is currently 2.71 microseconds, definitely subject to change.

Analog outputs are taken from the RAM on a time-shared basis, one each 117 CT, or as soon as the instruction execution in progress is completed. All other inputs and outputs involve the accumulator directly (except 4-bit digital inputs, which enter the index register), and "hang up" the computer until completed. The data link input is made in four parts, on demand, as shown below.

Table of Inputs and Outputs

TYPE	SIZE	NUMBER	ACCUMULATOR BITS
Inputs			
Analog	10-bit	49	10-1
Analog	13-bit	2	14-2
Digital	4-bit	19	4-1 (Index Register)
Real-time clock	10-bit	1	13-4
Data link	39-bit	1	17-13, 17-2, 17-2, 17-16
Outputs			
Analog	10-bit	39	17-8 (RAM word)
Digital	1-bit	29	18
Digital	2-bit	4	17-16
Digital	4-bit	5	17-14

Definitive documents on input-output are IDC's 2115.5/1300 and 2915.01/26.

D. W. Giedt

DWG:nd