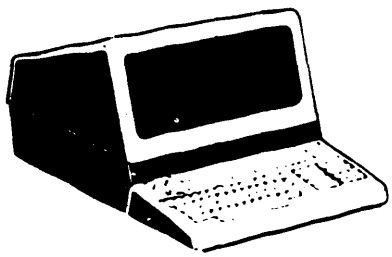
DATA TERMINAL
TECHNICAL INFORMATION



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HP 13255

COMPOSITE VIDEO INTERFACE MODULE

Manual Part No. 13255-91119

REVISED

APR-14-78

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The Composite Video Interface Module allows the 264XX line of data terminals to be connected to compatible large screen video monitors and video hard copy units.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Composite Video Interface Module is contained in tables 1.0 through 5.3.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60119	Composite Video I/F PCA	12.9 x 4.0 x 0.5	0.38
Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	0.258 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 100 mA	@ mA	@ 10 mA	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: MHz

NOT APPLICABLE

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
S1		
Jumper A	Processor Continues to RUN During Copy	Allows Printer $\overline{\text{BUSY}}$ Line to Stop Terminal Processor
A9	Module $\overline{\text{ADDR9}}$ = 0	Module $\overline{\text{ADDR9}}$ = 1
A10	Module $\overline{\text{ADDR10}}$ = 0	Module $\overline{\text{ADDR10}}$ = 1
A11	Module $\overline{\text{ADDR11}}$ = 0	Module $\overline{\text{ADDR11}}$ = 1
A4	Module $\overline{\text{ADDR4}}$ = 0	Module $\overline{\text{ADDR4}}$ = 1
ADD DISAB	Disables Bus Interface	Enable Bus Interface

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3		Not Used
-4	-12V	-12 Volt Power Supply
-5		Not Used
-6		
-7		
-8		
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10		Not Used
-11		
-12		
-13		
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		Not Used
-18		
-19		
-20		
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		}
-C		} Not used
-D		}
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H		}
-J		}
-K		} Not Used
-L		}
-M		}
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		}
-S		} Not Used
-1	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		}
-W		} Not Used
-X	RUN	Allow Processor to Access Bus
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1		
-2		Not Used
-3		
-4	WRITE	Output Character
Pin -5 through Pin -9		Not Used
-10	RETURN	Logic Signal Return
-11	$\overline{\text{BUSY}}$	Negative True, Copy Unit Busy Input
-12	$\overline{\text{REMOTE COPY}}$	Negative True, Copy Unit Copy Command Output
-13		Not Used
-14	COMP VID OUT	Composite Video Output
-15	VIDEO RETURN	Composite Video Return
P2, Pin A through Pin -S		Not Used

5.2 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P4, Pin 1	VIDEO	Video
-2	$\overline{\text{BUF HLF BRT}}$	Negative True, Buffered Half-Bright
-3	GND	Ground
-4	VDR	Vertical Drive
-5	HDR	Horizontal Drive
-6	GND	Ground

5.3 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P5, Pin 1	VIDEO	Video
-2	$\overline{\text{BUF HLF BRT}}$	Negative True, Buffered Half-Bright
-3	GND	Ground
-4	VDR	Vertical Drive
-5	HDR	Horizontal Drive
-6	GND	Ground

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts lists (02640-60119) located in the appendix.

The Composite Video Module performs two independent functions. The first is to provide a 75-ohm composite video output available from P2 (the rear connector) of the PCA. This output can be used to power any video monitor which is capable of tracking the 22.5 kHz line rate of the terminal. The second function of the Composite Video Interface PCA is to provide bus decoding, which allows the user to generate a copy either from the terminal keyboard, or remotely from a computer. The Composite Video Interface Module functional blocks are sync timing, video level generator, bus decoder logic, and copy command timing.

3.1 SYNC TIMING.

3.1.1 The sync timing block accepts the Vertical (VDR) and Horizontal (HDR) Drive signals from the Display Timing PCA and converts them to a composite vertical and horizontal sync signal which meets the overall composite video timing specification.

3.1.2 The sync timing block is comprised of three one-shots and two gates. The HDR and VDR signals are each applied directly to one-shots. The vertical one-shot Q output (U2, Pin 13) is used to produce a pulse width of 100 microseconds which becomes the Vertical Sync pulse at U2, Pin 13. The horizontal one-shot produces a pulse width of 0.95 microseconds. The Q output (U3, Pin 13) is used to trigger a third one-shot which generates the Horizontal Sync pulse of 3.5 microseconds at U3, Pin 12 and the $\overline{Q}$ output (U3, Pin 4) is gated with the Vertical Sync pulse to "serrate" it. These serations keep the horizontal oscillator in the monitor synchronized during the vertical sync interval. The output timing to the sync timing block is shown as the time dimensions on the composite video portion of the timing diagram figure 3.

3.2 VIDEO LEVEL GENERATOR.

3.2.1 The video level generator takes the TTL inputs from the sync timing block and the VIDEO and $\overline{\text{BUF HLF BRT}}$ signals from the Display Timing PCA and converts them to a single Composite Video (COM VID OUT) signal of 1.4 volts peak-to-peak capable of driving a 75-ohm cable.

3.2.2 Three open-collector AND gates (U7) are used as a simple D/A converter. Transistor Q2 clamps the full-bright level, R6 and R11 form a voltage divider which sets the half-bright level. Resistor R6 with R11 and R12 in parallel, set the blanking (black level) and the saturation drop of U7 sets the sync tip level. The node at which these components are joined is buffered by emitter follower Q1 and connected to connector P2 by a 75-ohm resistor (R10). Resistor R10 serves both to give an output impedance of 75 ohms, and to protect Q1 from being destroyed if the output becomes shorted to ground or +5 volts.

3.3 BUS DECODER LOGIC.

3.3.1 The bus decoder logic allows a copy to be generated either from the terminal keyboard or from a computer.

3.3.2 Module address of the Composite Video Interface PCA is set by four switches which connect to U1. They cause the outputs of U1 which are connected together to go high with an input of either high or low logic level depending on the switch position. During a print cycle, the terminal processor will first access the bus decoder and request a status byte. Bus bits $\overline{\text{BUS0}}$ and $\overline{\text{BUS7}}$ are then gated out onto the bus to indicate that the bus decoder is not disabled and is operational. $\overline{\text{BUS1}}$ will go low if the copy unit is available (not busy). Once the processor has determined that the copy unit is available, it outputs a $\overline{\text{WRITE}}$ along with a character on the bus bits. The bus decoder then generates a WRITE signal at U6, Pin 8, but ignores the character as the hard copy unit gets its information from the composite video waveform and requires no logic inputs other than the $\overline{\text{REMOTE COPY}}$ command. Once the hard copy unit receives the $\overline{\text{REMOTE COPY}}$ command, it drops $\overline{\text{BUSY}}$ which stops the terminal processor by pulling down RUN through gate U4, freezing the display and preventing the screen from being changed either from the keyboard or from a remote source. Switch S1-A is included to disable this line should the operator not wish the terminal processor to be stopped during a copy.

3.4 COPY COMMAND TIMING.

3.4.1 The copy command timing block generates the 500-microsecond $\overline{\text{REMOTE COPY}}$ pulse which is required to start the hard copy unit, and also prevents multiple copies from being made each time the print command is issued from the terminal.

3.4.2 The terminal can dump more than one character when a print command is issued. The hard copy unit ignores the character stream output from memory and only copies the data which actually appears on the CRT display. Each character, however, causes a WRITE signal to be generated by the bus decoder, and the copy command timing block must reject all of the WRITE pulses except the first. This is done by one-shot U9 which is a retriggerable one-shot with a timing interval of 0.7 seconds. The first WRITE pulse is allowed to trigger the Copy Command one-shot (U2), because U9 has not been triggered. AS the $\overline{\text{BUSY}}$ line goes low and stops the terminal processor before U2 times out, no further WRITE pulses will be generated until the copier is finished.

When $\overline{\text{BUSY}}$ goes high it triggers U9 which disables U2. The WRITE pulses will continue to retrigger U9 until there is a 0.7 second pause which will allow U9 to time out and re-enable U2.

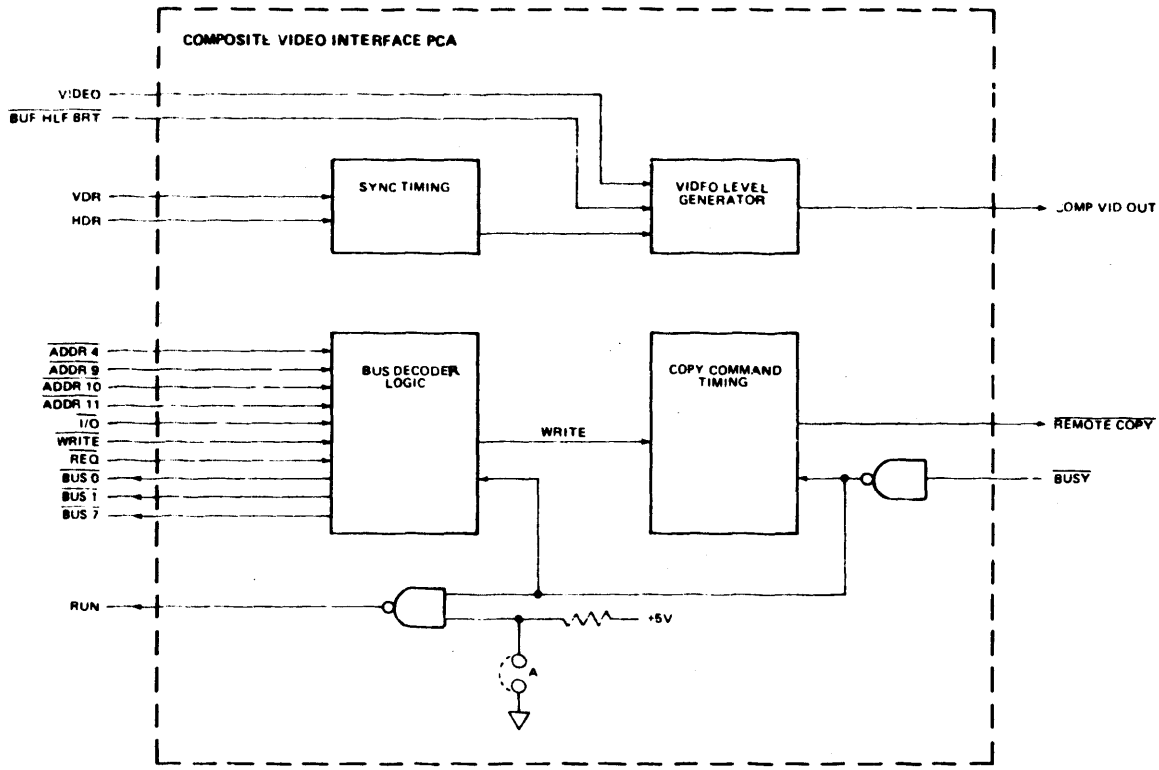

Figure 1
Composite Video Interface Block Diagram
APR-14-78 13255-91119

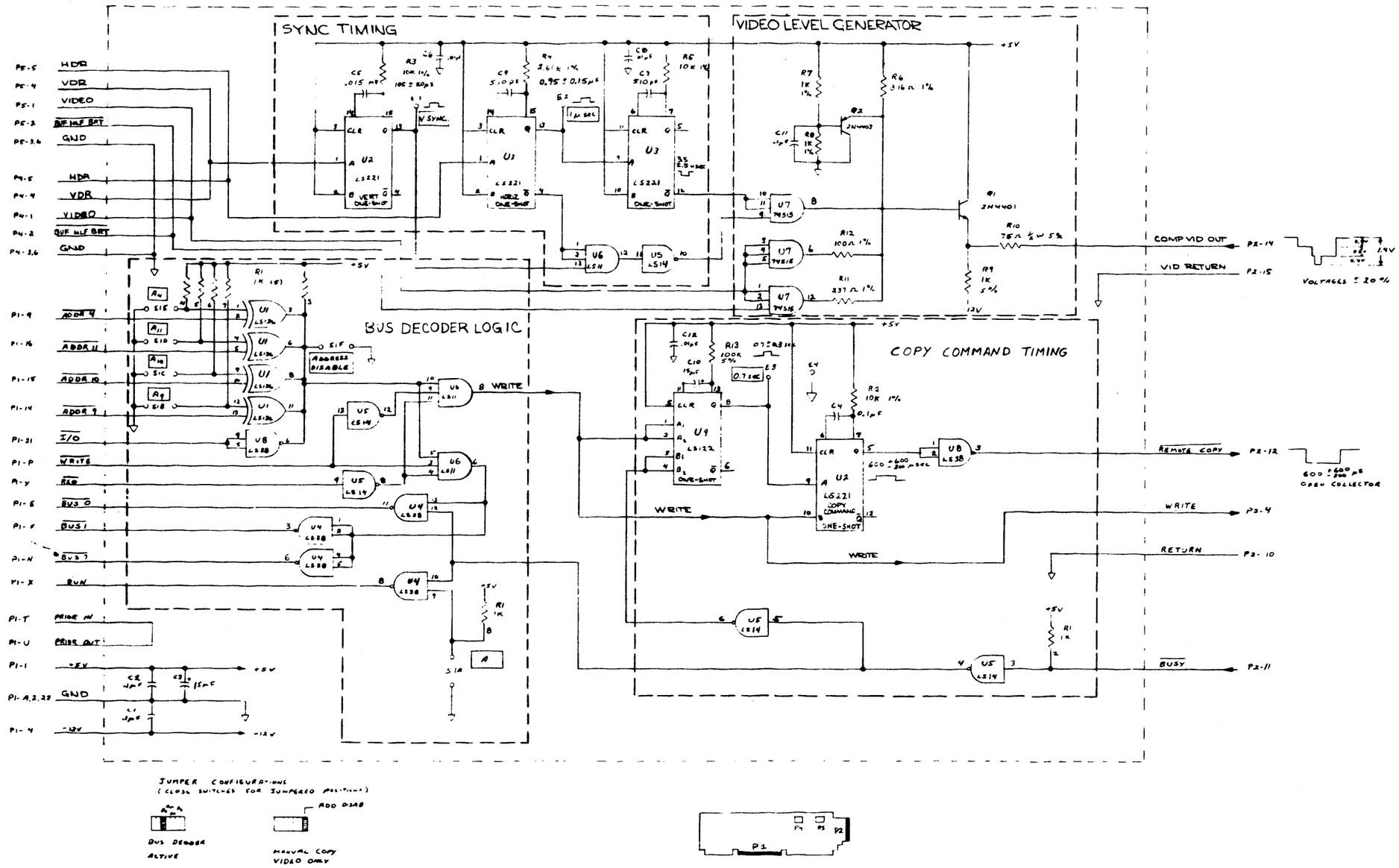

Figure 2
Composite Video Interface PCA Schematic Diagram
APR-14-78 13255-91119

SIGNAL NAME	CONNECTOR AND PIN NO
COMP VID OUT (HORIZONTAL RATE)	P2, Pin 14
COMP VID OUT (VERTICAL RETRACE)	P2, Pin 14
REMOTE COPY	P2, Pin 12
BUSY	P2, Pin 11

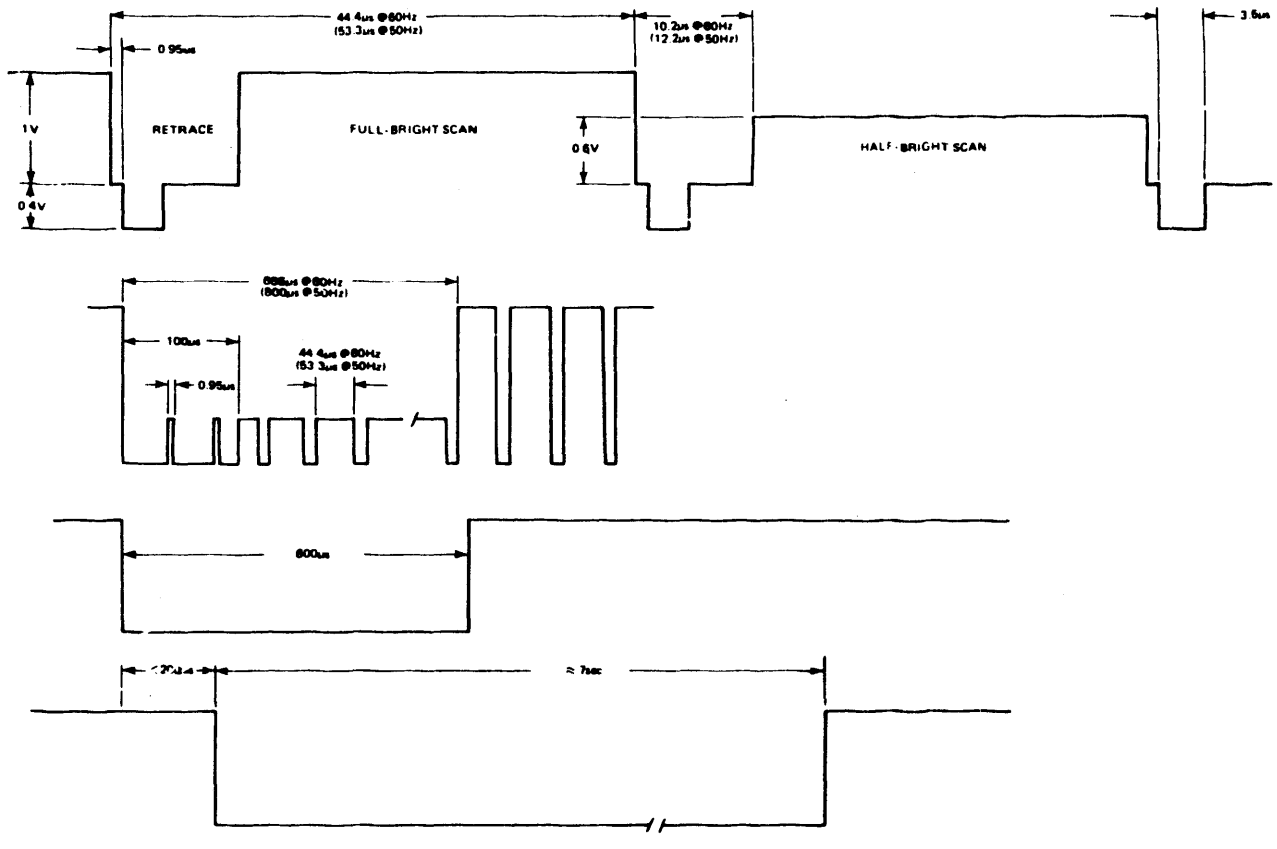

Figure 3
Composite Video Interface Timing Diagram
APR-14-78 13255-91119

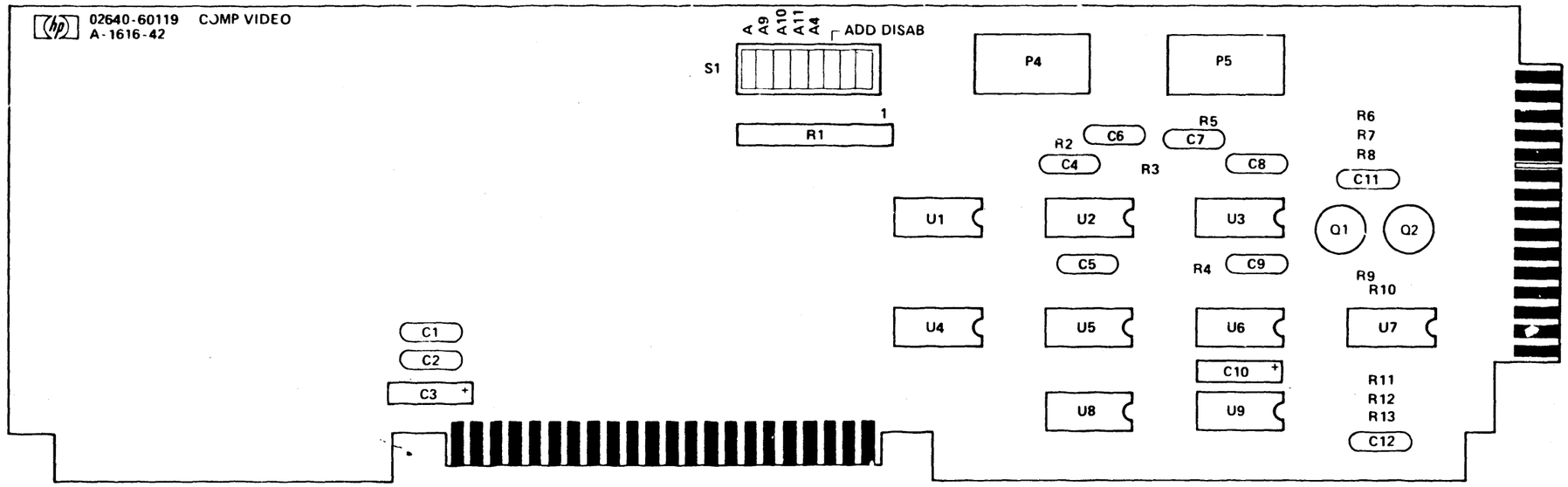

Figure 4
Composite Video Interface Component Location Diagram
APR-14-78 13255-91119

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60119	1	COMPOSITE VIDEO INTERFACE ASSEMBLY DATE CODE: A-1616-42 REVISION DATE: 09- -76	28480	02640-60119
C1	0150-0121	4	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C2	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C3	0180-1746	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C4	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C5	0160-0194	1	CAPACITOR-FXD .015UF +-10% 200WVDC POLYE	56289	292P15392
C6	0160-2055	3	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-3534	2	CAPACITOR-FXD 510PF +-5% 100WVDC MICA	28480	0160-3534
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-3534		CAPACITOR-FXD 510PF +-5% 100WVDC MICA	28480	0160-3534
C10	0180-1746		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C11	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	4	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
P4	1251-3766	2	CONNECTOR 6-PIN M POST TYPE	27264	09-88-2061
P5	1251-3766		CONNECTOR 6-PIN M POST TYPE	27264	09-88-2061
Q1	1854-0467	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q2	1853-0271	1	TRANSISTOR PNP 2N4403 SI TO-92 PD=310MW	04713	2N4403
R1	1810-0030	1	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	0757-0442	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R3	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R4	0698-0085	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
R5	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
R6	0698-3444	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-TO-316R-F
R7	0757-0280	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
R8	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
R9	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0686-7505	1	RESISTOR 75 5% .5W CC TC=0+412	01121	EB7505
R11	0698-3442	1	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-TO-237R-F
R12	0757-0401	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
R13	0757-0465	1	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1003-F
S1	3101-2094	1	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392	1	COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
U1	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U2	1820-1457	2	IC-DIGITAL SN74LS221N TTL LS DUAL	01295	SN74LS221N
U3	1820-1457		IC-DIGITAL SN74LS221N TTL LS DUAL	01295	SN74LS221N
U4	1820-1209	2	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U5	1820-1416	1	IC-DIGITAL SN74LS14N TTL LS HEX 1 INV	01295	SN74LS14N
U6	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U7	1820-0687	1	IC-DIGITAL SN74S15N TTL S TPL 3 AND	01295	SN74S15N
U8	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U9	1820-1422	1	IC-DIGITAL SN74LS122N TTL LS	01295	SN74LS122N