

HP 13255

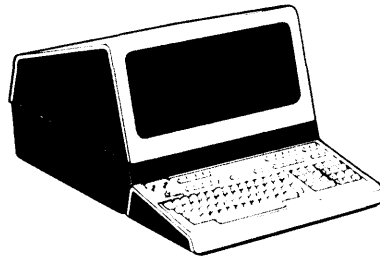
4K UV PROM MODULE

Manual Part No. 13255-91007

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The 4K UV PROM Module provides 4K bytes of nonvolatile program storage organized in two blocks of 2K bytes that are separately addressable. The board utilizes ultra-violet PROMs to provide flexibility in firm-ware development.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the 4K UV PROM Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60007	4K UV PROM PCA	12.5 x 4.0 x 0.5	0.63
02640-60149	Same as 02640-60007		

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B	() Other:
Restrictions:	Type tested at product level	
Failure Rate:	0.556 (percent per 1000 hours)	

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply @ 300 mA	+12 Volt Supply @ mA NOT APPLICABLE	-12 Volt Supply @ 500 mA	-42 Volt Supply @ mA NOT APPLICABLE
115 volts ac @ A NOT APPLICABLE		220 volts ac @ A NOT APPLICABLE	
Clock Frequency: 4.915 MHz			

Table 4.0 Jumper (Switch) Definitions

PCA Designation	Function	
	In (Closed)	Out (Open)
BLOCK A: 32K	Add 0 to block start addr.	Add 32K to block start addr.
16K	Add 0 to block start addr.	Add 16K to block start addr.
8K	Add 0 to block start addr.	Add 8K to block start addr.
4K	Add 0 to block start addr.	Add 4K to block start addr.
2K	Add 0 to block start addr.	Add 2K to block start addr.
DISABLE	Inhibit reading data from block A.	Allow reading data from block A.
BLOCK B: All jumpers	Same function as block A jumper with the same label.	Same function as block A jumper with the same label.

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	ADDR0	Negative True, Address Bit 0
-6	ADDR1	Negative True, Address Bit 1
-7	ADDR2	Negative True, Address Bit 2
-8	ADDR3	Negative True, Address Bit 3
-9	ADDR4	Negative True, Address Bit 4
-10	ADDR5	Negative True, Address Bit 5
-11	ADDR6	Negative True, Address Bit 6
-12	ADDR7	Negative True, Address Bit 7
-13	ADDR8	Negative True, Address Bit 8
-14	ADDR9	Negative True, Address Bit 9
-15	ADDR10	Negative True, Address Bit 10
-16	ADDR11	Negative True, Address Bit 11
-17	ADDR12	Negative True, Address Bit 12
-18	ADDR13	Negative True, Address Bit 13
-19	ADDR14	Negative True, Address Bit 14
-20	ADDR15	Negative True, Address Bit 15
-21	I/O	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	POLL	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	BUS0	Negative True, Data Bus Bit 0
-F	BUS1	Negative True, Data Bus Bit 1
-H	BUS2	Negative True, Data Bus Bit 2
-J	BUS3	Negative True, Data Bus Bit 3
-K	BUS4	Negative True, Data Bus Bit 4
-L	BUS5	Negative True, Data Bus Bit 5
-M	BUS6	Negative True, Data Bus Bit 6
-N	BUS7	Negative True, Data Bus Bit 7
-P	WRITE	Negative True, Write/Read Type Cycle
-R	ATN2	Negative True, CTU and Polled Interrupt Request
-S	WAIT	Negative True, wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	PROC ACTIVE	Negative True, Processor Active (Controlling Bus)
-W	BUSY	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	REQ	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts list (02640-60007) located in the appendix.

This PCA provides 4K bytes of memory contained in UV erasable PROMs. The PCA is divided into 2 blocks of 2K bytes each. The PROMs are Intel 1702A, organized as 256 x 8 bits, with an access time of 1.2 microseconds.

3.1 BLOCK A.

3.1.1 This block consists of eight 1702A PROMs.

3.1.2 A particular PROM is selected by the chip select (CS) signals from the access control block. The byte of interest within the selected PROM is determined by the signals ADDR0-7. The 8 bits of data are sent to the data path to be output onto the terminal bus.

3.2 BLOCK B.

3.2.1 See 3.1.1.

3.2.2 See 3.1.2.

3.3 BLOCK STARTING ADDRESS.

3.3.1 This block allows each 2K byte block of PROMs to be selectively enabled or disabled independently of the other block. The starting address of each 2K byte block may be independently set to any 2K byte boundary within a 64K byte address space.

3.3.2 The 74LS136 gates act as comparators between the jumpers and the

address signals ADDR11-15. If the address line is low and the corresponding jumper is out, the output of the exclusive-or gate is high (note that the address lines are negative true); this is also the case if the address line is high and the jumper is in (grounding the input of the exclusive-or). Otherwise, the output of the exclusive-or is low. The outputs of the exclusive-or gates are wire-anded for each block to determine whether the address corresponds to that selected by the jumpers--if any output is low, then the signals BLOCK A and BLOCK B will be low. An additional jumper is provided to connect the signals BLOCK A or BLOCK B directly to ground, inhibiting the PROM block from being selected, irrespective of the state of the address lines.

3.4 ACCESS CONTROL.

3.4.1 This block selects the specific PROM to be accessed, enables the appropriate portion of the data path and determines when the processor reads the data from the terminal bus.

3.4.2 When $\overline{\text{WRITE}}$ and $\overline{\text{I/O}}$ are high, i.e. a read from memory is desired, and $\overline{\text{REQ}}$ is low, then U210, pin 8 is high. If BLOCK A is high, then U17, pin 11 is low and ENABLE A is high; similarly, if BLOCK B is high, then U17, pin 3 is low and ENABLE B is high. The signal ENABLE A enables decoder U15 and ENABLE B enables decoder U11. ADDR8-10 are decoded to determine the appropriate chip select as shown below:

ADDR10	ADDR9	ADDR8	PROM ENABLED
0	0	0	A1, B1
0	0	1	A2, B2
0	1	0	A3, B3
0	1	1	A4, B4
1	0	0	A5, B5
1	0	1	A6, B6
1	1	0	A7, B7
1	1	1	A8, B8

If either ENABLE A or ENABLE B is high, then the signal PROM SELECT is high also.

3.5 DATA PATH.

3.5.1 This block allows data from the PROMs to be routed onto the terminal bus.

3.5.2 If ENABLE A is high, then U25 and U35 are enabled, allowing data from A1-A8 to appear on the terminal bus in ground true form. If ENABLE B is high, then U211 and U311 are enabled, allowing data from B1-B8 to appear on the terminal bus in ground true form.

3.6 TIMING.

3.6.1 This block determines the time at which the processor is allowed to read the data on the terminal bus.

3.6.2 The heart of this circuit is the 93L10 counter. When PROM SELECT is low, the counter is reset so that Q0=Q1=Q2=Q3=0, and the differing inputs on U310 will cause the outputs of the two exclusive-or gates

to be high. Two gates are used for the output to the signal $\overline{\text{WAIT}}$ to provide the current sinking capabilities required for bus signals (note that a 74LS38 would normally be used in this situation).

When PROM SELECT goes high, indicating that data from one of the PROMs is to be read, the following sequence takes place:

Q3	Q2	Q1	Q0	CEP	CET	$\overline{\text{PE}}$	$\overline{\text{WAIT}}$
0	0	0	0	1	1	1	0
0	0	0	1	1	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	1	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	0
1	0	0	0	1	0	1	1

The time during which $\overline{\text{WAIT}}$ is low corresponds to 6 clock cycles = 1.2 microseconds. when the last state is reached the counter will remain in this state, since CET is low, until PROM SELECT goes low, resetting the counter to the initial state.

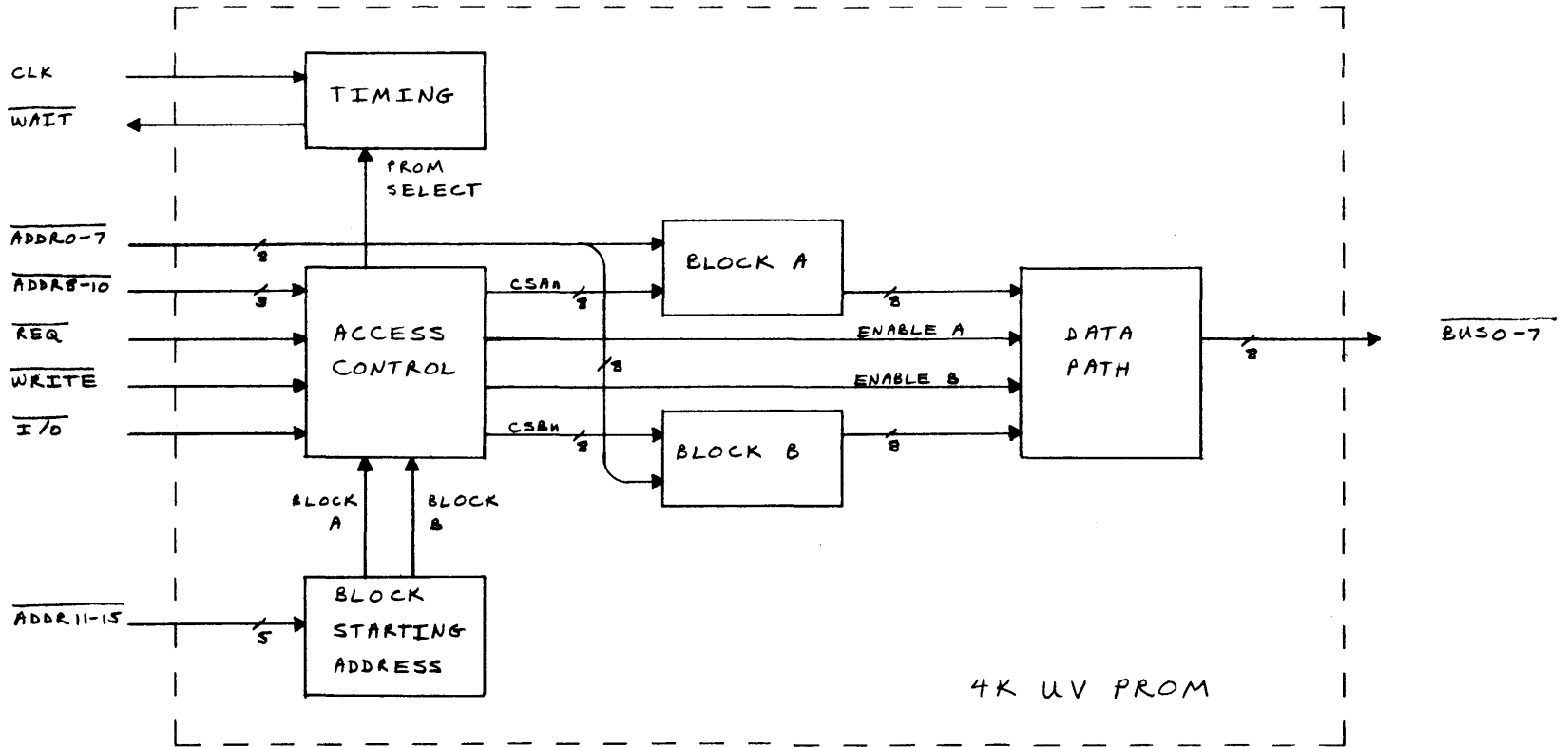


Figure 1
 4K UV PROM PCA Block Diagram
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PI-T
PI-U

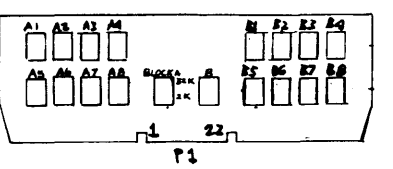
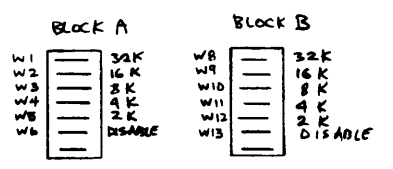
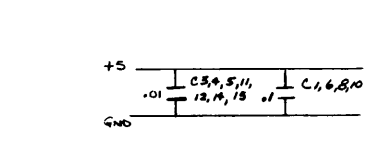
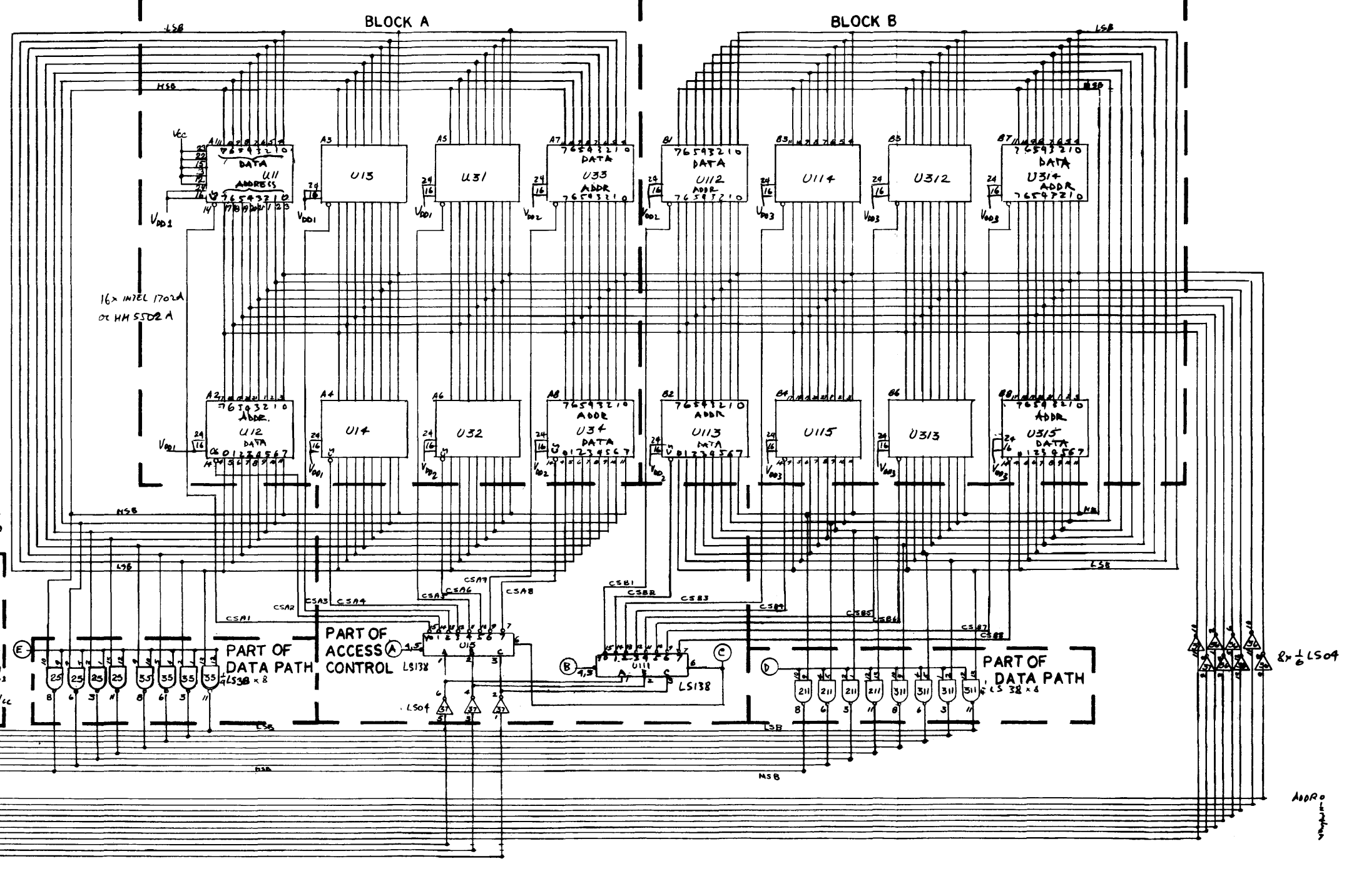
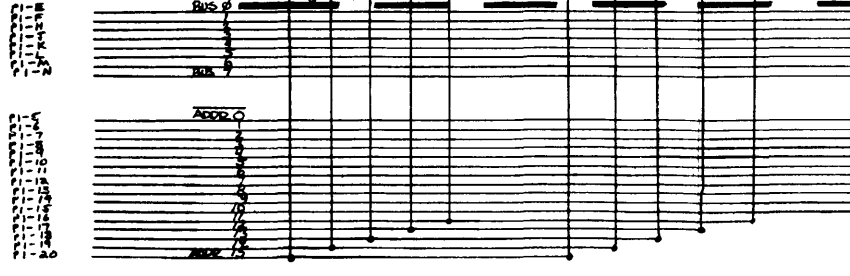
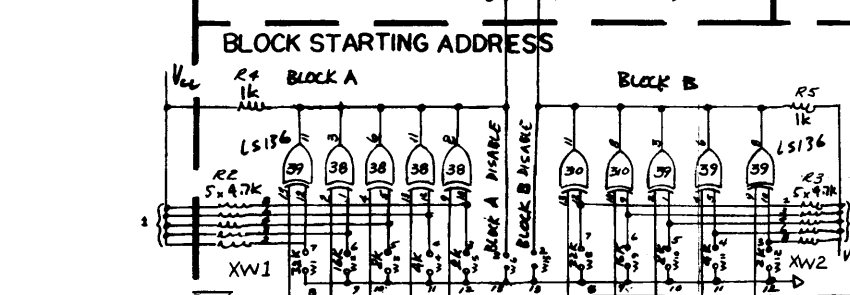
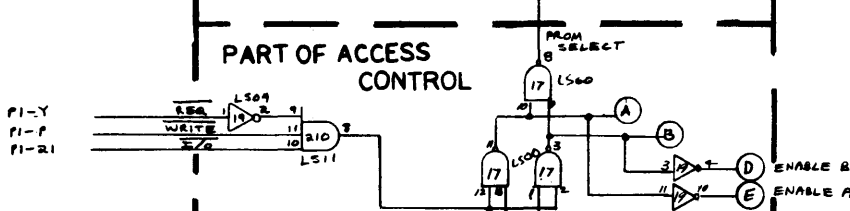
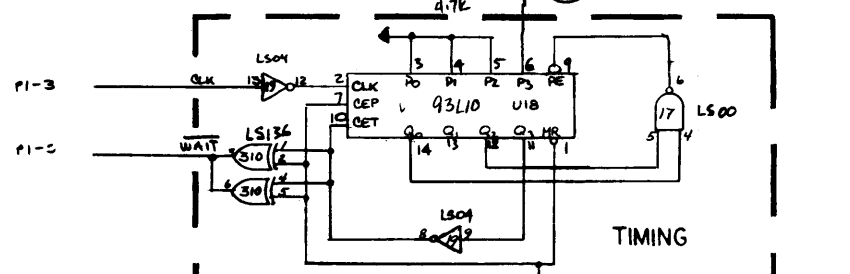
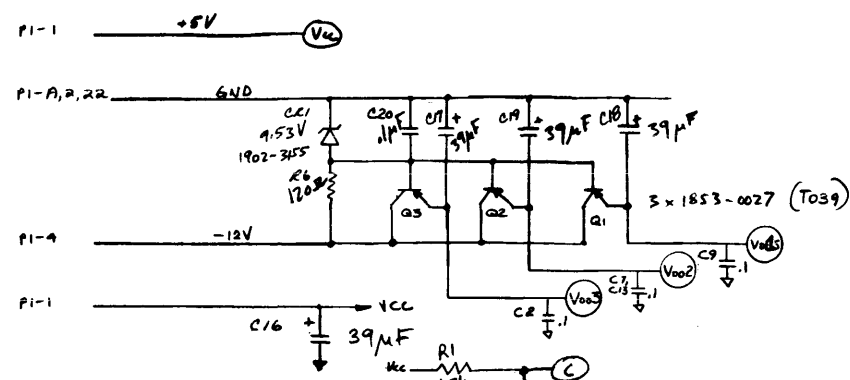


Figure 2
4K UV PROM PCA Schematic Diagram
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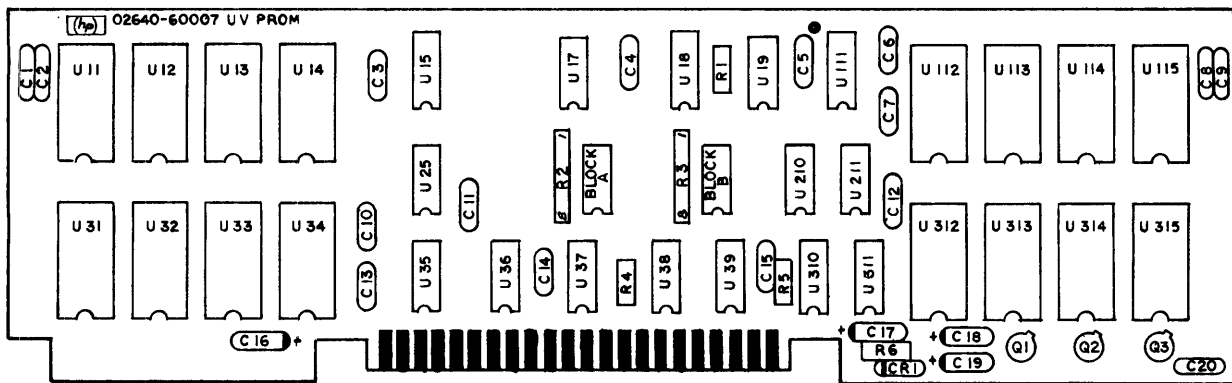


Figure 3
 4K UV PROM PCA Component Location Diagram
 AUG-01-76 13255-91007

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60007	1	ASSEMBLY-4K PROM REVISION DATE: 12-11-76		02640-60007
C1	0150-0121	9	CAPACITOR-FXD 0.1UF		0150-0121
C2	0150-0121		CAPACITOR-FXD 0.1UF		0150-0121
C3	0160-2055	7	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0150-0121	9	CAPACITOR-FXD 0.1UF		0150-0121
C7	0150-0121		CAPACITOR-FXD 0.1UF		0150-0121
C8	0150-0121		CAPACITOR-FXD 0.1UF		0150-0121
C9	0150-0121		CAPACITOR-FXD 0.1UF		0150-0121
C10	0150-0121		CAPACITOR-FXD 0.1UF		0150-0121
C11	0160-2055	7	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0150-0121	9	CAPACITOR-FXD 0.1UF		0150-0121
C14	0160-2055	7	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0180-0393	4	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C17	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C18	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C19	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C20	0150-0121	9	CAPACITOR-FXD 0.1UF		0150-0121
CR1	1902-3155	1	DIODE 9.53 V		1902-3155
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
Q1	1853-0027	3	XSTR PNP SI T05		1853-0027
Q2	1853-0027		XSTR PNP SI T05		1853-0027
Q3	1853-0027		XSTR PNP SI T05		1853-0027
R1	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R2	1810-0125	2	RESISTOR NET 7X4.7K		1810-0125
R3	1810-0125		RESISTOR NET 7X4.7K		1810-0125
R4	0683-1025	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-1215	1	RESISTOR 120 5% .25		0683-1215
U15	1820-1216	2	IC-DIGITAL SN74LS138N		SN74LS138N
U17	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U18	1820-0669	1	IC-DIGITAL 93L10DC		93L10DC
U19	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U25	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U35	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U36	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U37	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U38	1820-1215	3	IC-DIGITAL SN74LS136N		SN74LS136N
U39	1820-1215		IC-DIGITAL SN74LS136N		SN74LS136N
U111	1820-1216	2	IC-DIGITAL SN74LS138N		SN74LS138N
U210	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U211	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U310	1820-1215	3	IC-DIGITAL SN74LS136N		SN74LS136N
U311	1820-1209	2	IC-DIGITAL SN74LS38N		SN74LS38N