HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	AS ISSUED	8-15-79	TK

Model No. | Stock No. 1MB5-9010

Title: ELECTRICAL SPECIFICATION

Description: TRANSLATOR CHIP | Date: 8-15-79

By | Sheet No. 1 of 10

Drawing No. A-1MB5-9010-1

ELECTRICAL SPECIFICATIONS

I. Absolute maximum ratings (all voltages referenced to the most negative supply).

1. Supply voltages	0V to 20V
2. Input voltage	0V to 20V
3. Input voltage protection	1000V (Note 1)
4. Operating free-air temperature, T_A	0 to 60 °C
5. Storage temperature	-40 to 75°C
6. Operating junction temperature	0 to 75°C

Note 1: 100pF discharged through 1.1K

II. Operating Parameters (all voltages referenced to V_{SS}, $0° < T_A < 60°C$).

Parameter	Symbol	MIN	TYP	MAX	UNITS	Comments
Power Supplies	V_{BB}	-5.25	-5.0	-4.75	V	
	V_{SS}		0.0		V	
	V_{CC}	4.75	5.0	5.25	V	
	V_{DD}	5.7	6.0	6.3	V	
	V_{GG}	11.4	12.0	12.6	V	
Supply Current	I_{BB}			100	uA	
	I_{CC}		6	12	mA	
	I_{GG}		2	4	mA	
	I_{DD}		1	2	mA	
Input Current	I_{IH}			10	uA	$V_{IN} = V_{GG}$
Total Power Dissipation	P_T			130	mW	
Clocks (2 phase)						see fig. 1
Rise time	t_{CR}			40	ns	
Fall time	t_{CF}			40	ns	
Frequency	F_C		613		kHz	+-.02%
Pulse width	t_{CPW}		204		ns	+-.02%
Pulse spacing	t_{CPS}		816		ns	+-.02%
Input high	V_{CIH}	9.6		V_{GG}	V	
Input low	V_{CIL}			0.8	V	
Input load	C_C			20	pF	

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				ELECTRICAL SPEC. - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
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LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG. NO A-1MB5-9010-1
		REVISIONS			

Parameter	Symbol	MIN	TYP	MAX	UNITS	Comments
PWO						See Fig. 2
Input high	V_{PIH}	3.6		V_{DD}	V	
Input low	V_{PIL}			0.8	V	
Input load	C_P			5	pF	
Rise delay	t_{PR}	1.0			ms	From time power supplies and clocks are within specification.
Delay to 1st $\overline{LMA}$	t_{PD}	3.2			us	
$\overline{LMA}$, $\overline{RD}$, $\overline{WR}$ Output						See Fig. 3
Output high	V_{NOH}	4.0		V_{DD}	V	Load = 150 pF
Output low	--					Never occurs.
Output valid high	t_{NHLO}			300	ns	Load = 150 pF
Hold time	t_{NHO}	40		150	ns	"
$\overline{LMA}$, $\overline{RD}$, $\overline{WR}$ Input						
Input high	V_{NIH}	3.6		V_{DD}	V	
Input low	V_{NIL}			0.8	V	
Input valid high	t_{NLH}	0			ns	
Input valid low	t_{NHL}			400	ns	
Hold time	t_{NH}	40		150	ns	
Input load	C_L			10	pF	
B0 - B7						See Fig. 4
Output valid	t_{BR2}			400	ns	Load = 150 pF
Input valid	t_{BF1}	0			ns	
Hold time	t_{BH1}	40		150	ns	
Output high	V_{BOH}	4.0			V	
Output low	V_{BOL}			0.4	V	
Input high	V_{BIH}	3.6			V	
Input low	V_{BIL}			0.8	V	
Float voltage	V_{BF}	3.6		V_{DD}	V	This voltage must be supplied by another chip in the system. (i.e. 1MA8)
Input Load	B_{IL}			10	pF	

Parameter	Symbol	MIN	TYP	MAX	UNITS	Comments
$\overline{RC}$						See Fig. 5
Fall time	t_{IF2}			380	ns	Open drain output
Output low	V_{IOL}			0.4	V	Load = 80 pF I_{sink}= 4 mA
Hold time	t_{RCH}			200	ns	
SC0, SC1, SC2						
Input low	V_L			0.8	V	
Low level input current				-1	mA	at V_L
$\overline{IRL}$, $\overline{HALT}$						See Fig. 6
Fall time	t_{IF3}			500	ns	Open drain output
Output low	V_{IOL}			0.4	V	Load = 80 pF I_{sink}=4mA
$\overline{PRIH}$, $\overline{PRIL}$						See Fig. 7
$\overline{PRIH}$ set up time	t_{su}	0			ns	
$\overline{PRIL}$ fall time	t_{F1}			450	ns	
Propagation delay	t_{PPD}			100	ns	Load = 80 pF
$\overline{PRIH}$ input high	V_{PIH}	3.6		V_{DD}	V	
$\overline{PRIH}$ input low	V_{PIL}			0.8	V	
$\overline{PRIL}$ output high	V_{PIH}	4.0			V	
$\overline{PRIL}$ output low	V_{PIL}			0.4	V	
$\overline{PRIH}$ input load	C_I			5	pF	
$\overline{ALE}$						See Fig. 8
Pulse width	t_{ILL}	150			ns	With 11 MHz crystal
Address set up time	t_{IAL}	70			ns	
Address hold time	t_{ILA}	50			ns	
Rise time	t_{IR}		30		ns	
Fall time	t_{IF}		30		ns	
$\overline{IWR}$						See Fig. 8
Pulse width	t_{ICC}	300			ns	
Data set up time	t_{IDW}	250			ns	
Data hold time	t_{IWD}	40			ns	Load = 20 pF
Address set up to WR	t_{IAW}	200			ns	
$\overline{IRD}$						See Fig. 8
Pulse width	t_{ICC}	300			ns	
$\overline{IRD}$ to data valid	t_{IRD}			200	ns	
Address set up to RD	t_{IAD}			400	ns	
Data hold time	t_{IDR}	0		100	ns	

Parameter	Symbol	MIN	TYP	MAX	UNITS	Comments
D0 - D7 , ALE, $\overline{IRD}$, $\overline{IWR}$						See Fig. 8
Output low voltage	V_{IOL}			0.4	V	Load = 50 pF I_{sink}=1.6mA
Output high	V_{IOH}	2.4		V_{CC}	V	
Input high	V_{IIH}	2.4			V	
Input low	V_{IIL}			0.8	V	
ADR2, $\overline{ADR3}$, $\overline{RESET}$, $\overline{INT}$						
ADRx valid	t_{IAR}			200	ns	Load = 30 pF(I_{sink}=1.6mA
Output high	V_{OH}	4.0			V	$\overline{RESET}$ and $\overline{INT}$)
Output Low	V_{OL}			0.4	V	

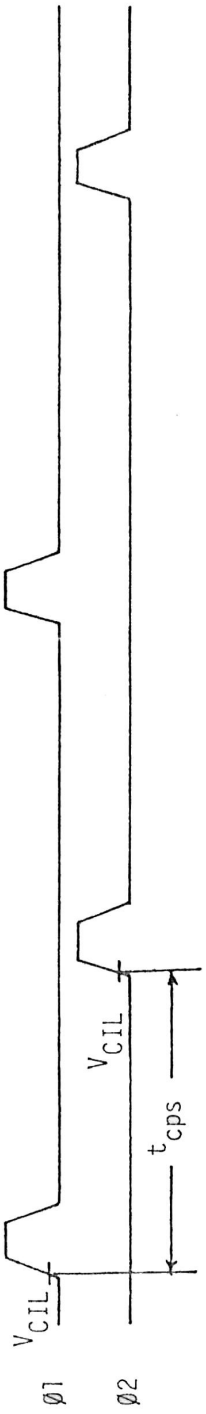
LTR	P.C. NO	APPROVED	DATE
	SEE	SHEET 1	

MODEL | STK NO 1MB5-9010

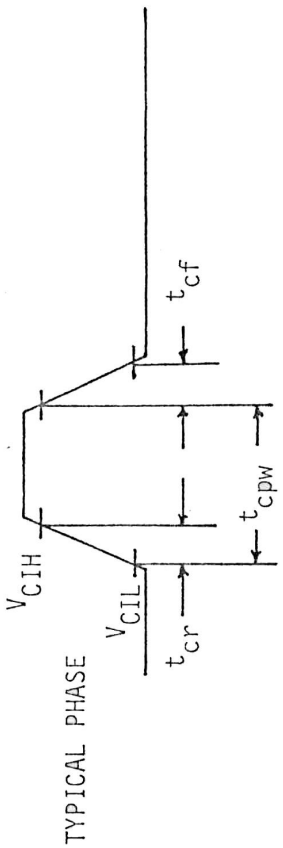
ELECTRICAL SPEC. - TRANSLATOR CHIP

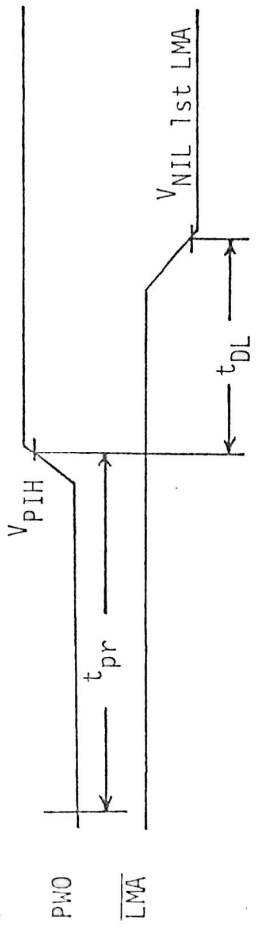
BY T. KRAEMER | DATE 8-15-79

APPD | SHEET NO 5 OF 10



CLOCK TIMING
FIG. 1





POWER-ON TIMING
FIGURE 2

	SEE	SHEET 1		MODEL	STK NO. 1MB5-2010
				ELECTRICAL SPEC. - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
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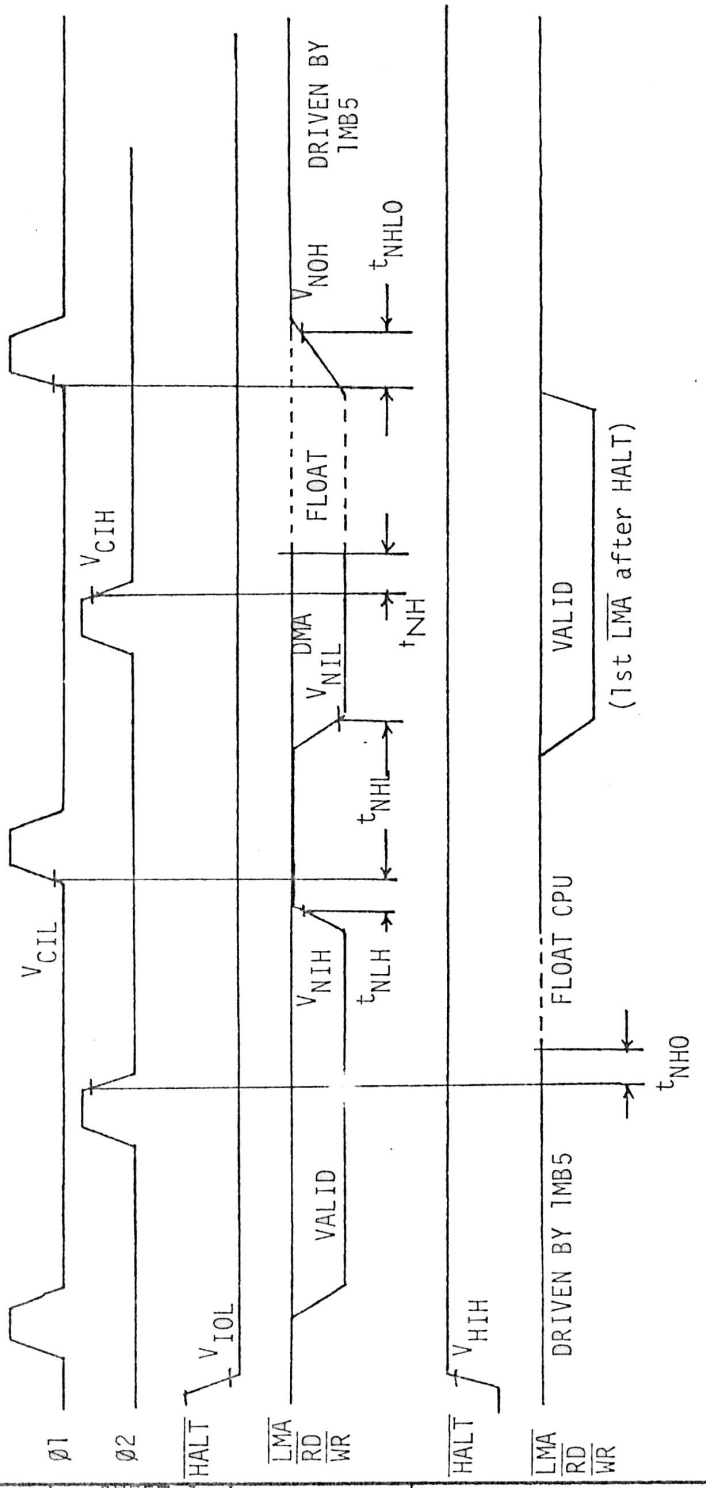

CONTROL TIMING

FIGURE 3

	SEE	SHEET 1		MODEL	STK. NO 1MB5-9010
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				BY T. KRAEMER	DATE 8-15-79
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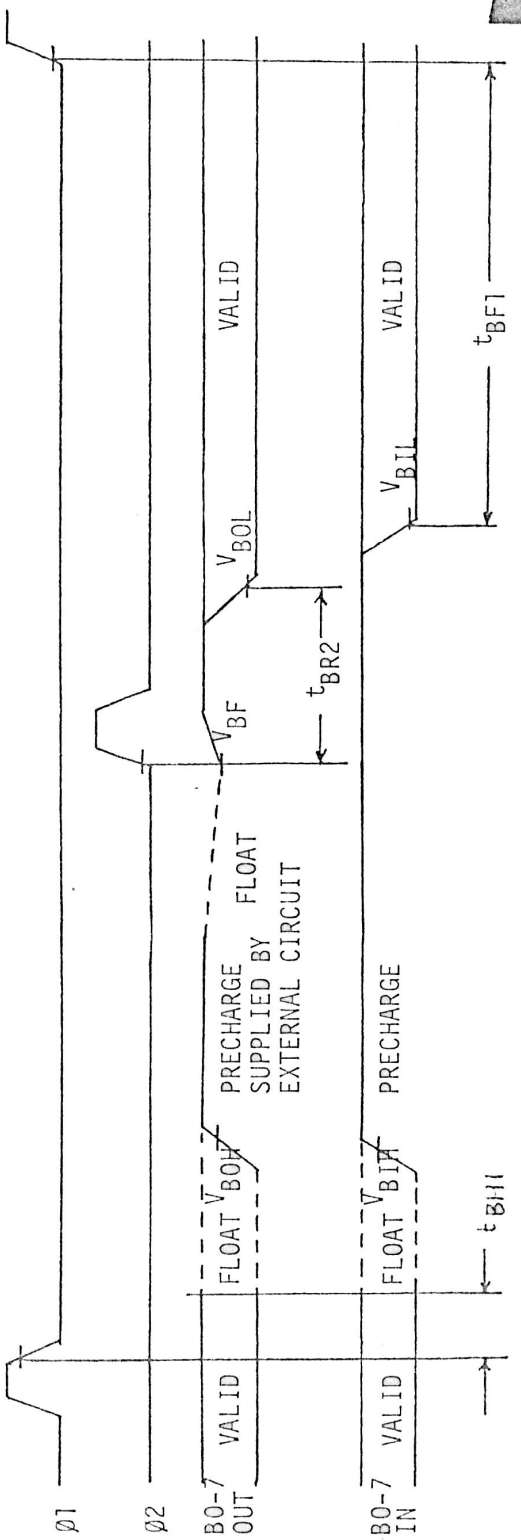

BUS TIMING

FIGURE 4.

	SEE	SHEET 1		MODEL	STK NO. 1MB5 - 9010
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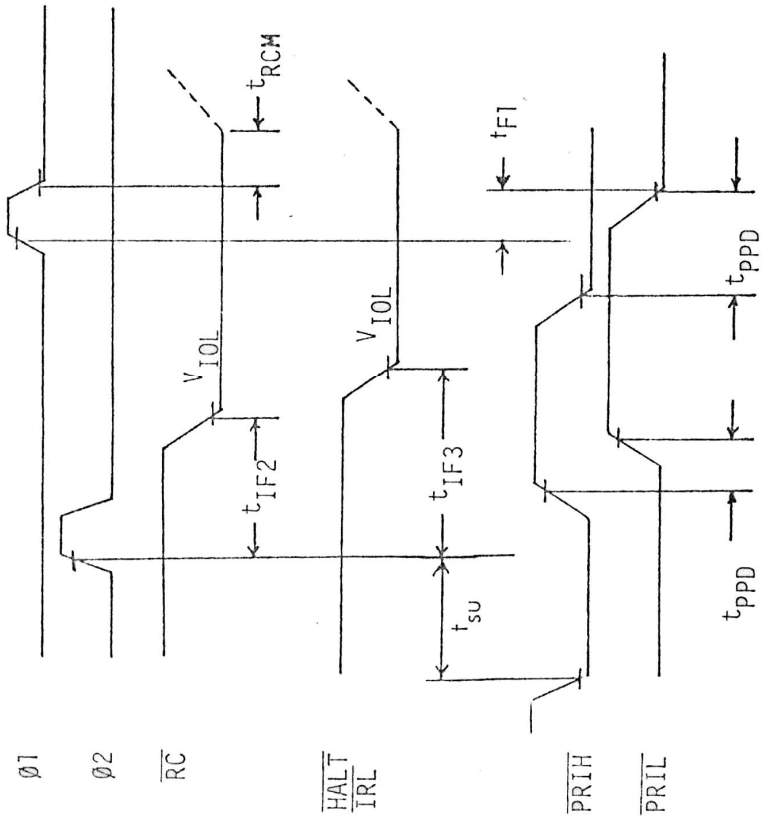
$\overline{RC}$ TIMING
FIG. 5

$\overline{IRL}$, $\overline{HALT}$ TIMING
FIG. 6

$\overline{PRIH}$, $\overline{PRIL}$ PROPAGATION DELAY
FIG. 7



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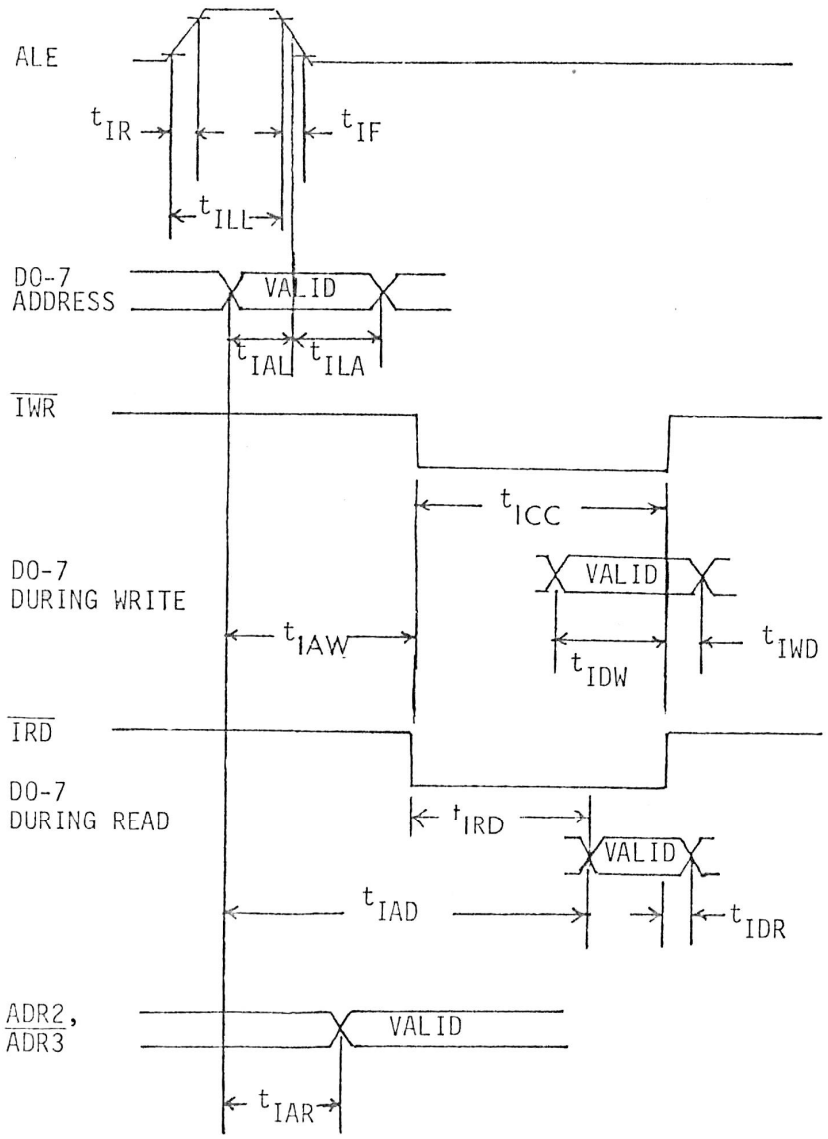

8049 TIMING

FIG. 8

	SEE	SHEET 1		MODEL	STK NO 1MB5- 9010
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