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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

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A	as issued	10·9·85	JQ𝒲

Model No.	98561A	Stock No.	

Title   Model 310 Processor BD, 14 Aug. 1985

Description		Date 8-15-85
By Martin Speer		Sheet No. 1 of 22
Supersedes		Drawing No. A-98561-66512-9

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SERIES 300 MODEL 310 MC68010 PROCESSOR BOARD
THEORY OF OPERATION

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INTRODUCTION:

BOBCAT is the code name of a project with the goal of creating a family of components(Series 300) which give our customers the ability to trade off cost, performance, and features for themselves. This document will deal with one of the many components that comprise Series 300, the 98561-26512(P/N of unloaded PC board) processor board. This board's contribution to the BOBCAT project is that it makes possible a low cost minimum component system which is capable of running UNIX*. A disc drive, keyboard, and video monitor is all that is necessary to have a useful system using the 98561-66512 based SPU box. In the low cost system, the SPU box would only contain a power supply and the 98561-66512 CPU board(The 98561-66511 CPU board is less expensive but only has 1/2 Mega-byte of RAM and hence will not be capable of running UNIX* as it is currently implemented).

System RAM and Display components will optionally be loaded on 98561-26512 resulting in three supported loading options and hence three different processor boards. 98561-66511 will have all Display components and one half the RAM(1/2 Mega-Byte) loaded. 98561-66512 will be fully loaded, while 98561-66513 will have all the RAM(One Mega-Byte) but none of the Display components loaded. These three boards allow our customers still more flexibility in trading off cost, performance, and features.

The Model 310 processor boards(98561-66511,2,3) feature a 10 MHz MC68010 microprocessor, up to One Mega-byte of on board RAM, 98561-66519(Model 320) style MMU, 98644A style RS-232, TOPCAT based display subsystem, HP-HIL keyboard electronics with battery backed up real time clock, HP-IB interface, and miscellaneous other system components needed by our software(UNIX, Pascal, BASIC). A block diagram is available as D-98561-66512-6. Each of these systems will be briefly discussed with an emphasis on compatibility with current software. A detailed discussion will then follow for all systems except the MMU. The MMU is documented in the MCA2800ALS Gate Array Theory of Operation/ERS which is listed below. Additional information on the MMU, the DIO bus, or the MC68010 micro processor can be found in the following documents:

- MCA2800ALS Gate Array ERS; Nick Mati and Dan Swanson
- MC68010 Users Manual; Motorola
- WOPR ERS and Theory of Operation; Jon Rubinstein
- UMM ERS and Theory of Operation; Mike Schubert
- DIO BUS SPECIFICATION; 5955-7669

* UNIX is a trademark of Bell Laboratories.

SERIES 310 FEATURES AND SOFTWARE COMPATIBILITY:

A) PROCESSOR AND PROCESSOR SUPPORT

Model 310 processor boards use a 10 MHz MC68010 microprocessor packaged in a 64 pin DIP plastic package. Model 310 is not the first product to use a MC68010, however, it is the first product to operate at 10 MHz(The 09826-66517 currently uses a 12.5 MHz MC68000 and may soon change over to either a 10 MHz or a 12.5 MHz MC68010). The only board currently using a MC68010 microprocessor is the 09817-66511 board, and this board operates at 8.0 MHz.

Model 310 processor boards do not have the same MMU as do 09826-66517 and 09817-66511 processor boards. Model 310 uses the MMU architecture developed for Model 320 processor board (The MC68020 based processor board, 98561-66519). See the 'INTRODUCTION' for a list of documents which contain additional information on the MMU.

Other system components which have been on previous Series 200 processor boards are BOOTROMs, MC6840 system timer, CPU board test LEDs, software security hardware, and a CPU configuration register. The following paragraphs describe which of these components are supported by the Model 310 processor boards and to what extent.

BOOTROMs and MC6840 programmable timer module(PTM) are present on Model 310 processor boards and look the same to software as do BOOTROMs and PTM on all previous CPU boards. One exception to the above generalization is the speed of access to these components. BOOTROM access time for Model 310 processor boards is approximately 1.5 times as long as it is for all other processor boards. PTM access time is only slightly longer.

CPU test LEDs are also present on Model 310 processor boards and operate in the same way as they do for previous CPU board designs. Location and orientation of these LED's will be the same for both the Model 310 and Model 320 processor boards. This location is at the front of the board in a place which is visible through the front panel slots.

Software security hardware, however, is completely different. In the past, a PROM at physical memory locations $5F0000 thru $5F3FFF(lower bytes only) was used. This 'ID PROM' contains the computer's serial, model number, and other miscellaneous information. Series 300 hardware will not have this 'ID PROM'. Software security will be handled using either the unique number stored in the ITF keyboard or by using the 'SOFTWARE' security module which is currently being developed. In either case, software security will be handled via a HP-HIL device.

Accessing the ID PROM's memory locations on all Series 300 processor boards will result in a 'BUS ERROR' being generated.

This is the same response software would get when run on older
CPU boards which do not have an 'ID PROM'. 'BUS ERROR' is also
the response software would get when run on a 9816 computer.
9816 CPU boards which had an 'ID PROM' did not have their 'ID
PROM' located at physical addresses $5F0000 thru $5F3FFF. These
CPU boards had their 'ID PROM' tied to the keyboard processor
and software accessed the 'ID PROM' through commands given to
the keyboard processor.

The Processor Configuration Register, which is multiple mapped
in the upper bytes of the 'ID PROM' address space, is also
missing. Reading or writing this register will cause a 'BUS
ERROR' to be generated, the same response as reading or writing
to the 'ID PROM'('ID PROM' data is returned in the lower bytes
when an 'ID PROM' is present).

B) SYSTEM RAM

Up to one mega-byte of RAM is supported by the Model 310
processor boards. This RAM has optional parity and is
auto-locating to one mega-byte boundaries when one mega-byte is
loaded, and is auto-locating to 1/2 mega-byte boundaries when
1/2 megabyte of RAM is loaded. Two jumpers on the board
configure the RAM array for 0, 1/2, or 1 megabyte operation.
Parity is allowed or dis-allowed by loading or not loading the
parity RAM(No parity currently is not a supported option). When
the parity RAM is loaded, the control of parity and the
reporting of parity errors is handled exactly the same way as it
is on the 98257A RAM card. One definition change was made
within the MCA2800ALS RAM controller logic which system test
code writers need to be aware of. When parity RAM is not
loaded, writing to physical memory location $5BXXX1(98257A
parity control register) will not generate a 'BUS ERROR'. Hence,
the ability to write to the parity control register should not
be construed as an indication that some of the RAM in the system
checks parity.

RAM control is performed by the MCA2800ALS gate array which also
serves as the MMU. With the exception of I/O cells, the
MCA2800ALS uses ECL as the logic technology. The speed provided
by ECL allows the Model 310 processor boards to run 4 cycle RAM
accesses at 10 MHz to on board RAM. This RAM access time is
also the same for both mapped and un-mapped RAM access cycles.

Due to timing constraints of the DIO bus, RAM located on the DIO
bus will run approximately 50% slower than RAM located on Series
310 processor boards. RAM located on the DIO bus has a minimum
access time of approximately 620 nano-seconds compared to the
400 nano-second access time for on board RAM. Model 310
processor boards will also be slightly faster than other
processor boards when running DIO bus cycles to RAM or any other
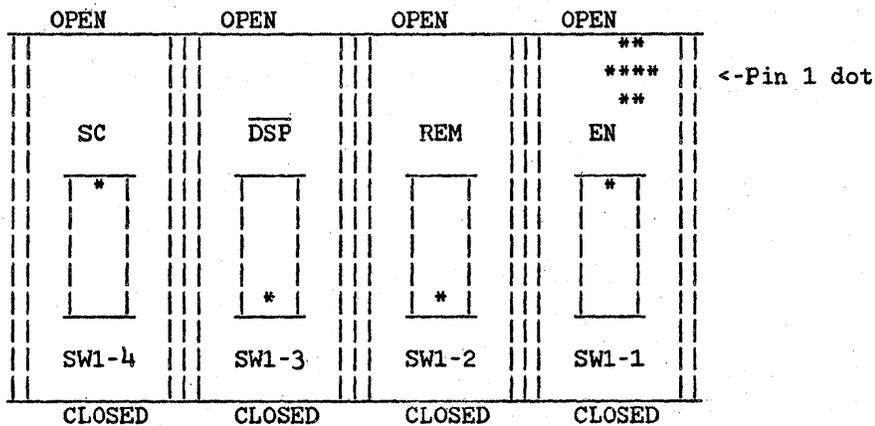DIO device. This speed improvement is less than 1%, however.

C) RS-232

Model 310 processor boards implement one RS-232 port which looks very similar to the 98644A DIO card. The Model 310 implementation of the 98644A card differs in three ways:

1) The Model 310 processor board implementation allows interrupts to occur at level 5 only. There are no switches to change the interrupt level as there are on the 98644A card.

2) The Model 310 processor board implementation permanently sets the select code to 9. The 98644A card has switches which allow this address to be changed.

3) The Model 310 processor board implementation does not allow the user to change the 'ID' of the RS-232 interface in order to emulate a 98626A card. The 98644A card has a switch to do this.

The third item mentioned may cause some trouble until all user applications add 98644A card support.

Two switches on the Model 310 processor board are associated with RS-232,SW1-1 and SW1-2(See Figure 1). SW1-2 controls the local/remote bit in the ID register. SW1-1 sets the handshake input lines to their default condition, all ones. More information on Model 310's RS-232 implementation can be found in the 'RS-232 THEORY OF OPERATION' section of this document.

```
     OPEN          OPEN          OPEN          OPEN
 ||         ||  ||        ||  ||        ||  ||    **   ||
 ||         ||  ||        ||  ||        ||  ||   **** ||  <-Pin 1 dot
 ||         ||  ||        ||  ||        ||  ||    **   ||
 ||   SC    ||  ||  DSP   ||  ||  REM   ||  ||   EN    ||
 ||         ||  ||        ||  ||        ||  ||         ||
 ||  | * |  ||  ||  |   | ||  ||  |   | ||  ||  | * |  ||
 ||  |   |  ||  ||  |   | ||  ||  |   | ||  ||  |   |  ||
 ||  |   |  ||  ||  |   | ||  ||  |   | ||  ||  |   |  ||
 ||  |   |  ||  ||  | * | ||  ||  | * | ||  ||  |   |  ||
 ||  SW1-4  ||  ||  SW1-3 ||  ||  SW1-2 ||  ||  SW1-1  ||
     CLOSED        CLOSED        CLOSED        CLOSED
```

* indicates switch set in this direction.

FIGURE 1
DEFAULT PROCESSOR BOARD SWITCH SETTINGS

D) DISPLAY

All the electronics for a TOPCAT based single plane bit-mapped
display can be optionally loaded on the Model 310 processor
board. 98561-66513 is the only Model 310 processor board at
present which does not have the bit-mapped electronics loaded.
The electronics consist of eight 16K by 4 RAMs which make up the
frame buffer, a TOPCAT controller IC, an 8 kilo-byte display ID
ROM, a video shift-register, a pixel clock, and miscellaneous
resistors, capacitors, jumpers, inductors, and transistors.
When these components are loaded and a customer wishes to
upgrade to some other bit-mapped display board, SW1-3(see
Figure 1) must be opened in order to disable decoding and
'DTACK' generation for the on-board display. A missing
jumper(JP15) on the 98561-66513 board inhibits the function
of SW1-3 and permanently disables the remaining bit-mapped
support logic.

The resolution that is being supported by the Model 310
processor boards with bit-mapped display components loaded is
1024 pixels by 400 lines. Other resolutions may be possible in
the future as long as that resolution is supported by TOPCAT's
low-resolution pixel port. The components which will need to be
changed in order to move to a different resolution are the
Display ID ROM and the pixel clock oscillator. More information
on the display subsystem can be found in the DISPLAY THEORY OF
OPERATION section of this document. Additional information on
TOPCAT can be found in the following documents:

    (1)   TOPCAT ERS; DWG # A-1FH2-2001-007

    (2)   Graphics Subsystems Application Note;
           DWG # A-5958-4374-1

E) HP-IB

Model 310 processor boards implement HP-IB similar to and
software compatible with 'INTERNAL' HP-IB implementations of all
past Series 200 computers. This design is based on the Texas
Instruments TMS9914 HP-IB controller which allows data transfer
rates up to 450 kilo-bytes/second. The TMS9914 is a memory
mapped I/O device which is multiple mapped within a 64 kilo-byte
internal I/O device slot. The physical address of this internal
I/O device slot is $47XXXXX.

In past 'INTERNAL' HP-IB implementations, two additional
registers external to the TMS9914 were added. Model 310
processor boards implement these registers plus two new ones.
The two new registers control hardware which can generate an
interrupt in response to a HP-IB device responding to a parallel
poll. This feature was added to improve the speed and

efficiency of multi-tasking software. More information can be found in the HP-IB THEORY OF OPERATION section of this document.

F) KEYBOARD ELECTRONICS

One new feature has been added to the keyboard interface electronics on Model 310 processor boards, a battery backed up real time clock. Software gains access to this new resource through the use of previously unused instructions to the 8042 keyboard processor. This keeps the keyboard interface software compatible with the 9817(MARBOX) and was the least expensive way to add this new feature.

Other functions of the 8042 keyboard interface are beeper control, HP-HIL interface/control, and miscellaneous other timer/time-keeping functions. More information on the keyboard interface can be found in the KEYBOARD INTERFACE AND OTHER RELATED SUBSYSTEMS section of this document. Additional information on the 8042 keyboard controller's firmware can be found in HP Drawing A-1820-4379-2.

SERIES 310 PROCESSOR BOARD THEORY OF OPERATION

A) INTRODUCTION

Model 310 processor boards can be partitioned into two separate systems, the CPU/MMU/RAM/DIO bus interface subsystem and the I/O subsystem. Page one of the schematic(HP Drawing E-98561-66512-4) and page one of the block diagram(HP Drawing D-98561-66512-6) show the CPU/MMU/RAM/DIO bus interface subsystem. Page 2 of both documents show the I/O subsystem.

U29, the Motorola MC2800ALS gate array, has three primary functions which are MMU, DRAM controller, and DIO bus controller. This part is the heart of the CPU/MMU/RAM/DIO bus interface subsystem. U29 sits between the MC68010 and the DIO bus and runs DIO bus cycles when the MC68010 is bus master. DIO bus cycles from U29 meet the timing requirements as specified in the 'DIO BUS SPECIFICATION', HP Drawing 5955-7669.

MC68010 RAM access cycles to on board RAM should not be considered a DIO bus cycle, even though address and control signals are driven out on the DIO bus. On board RAM access cycles originated by the MC68010 happen faster than allowed by the DIO bus specification since the on board RAM sits directly on the MC68010 data bus and is accessed synchronously. Data from these accesses is not driven out on the DIO bus. On board RAM timing for alternate bus masters(i.e. the DMA card) does meet DIO bus timing specifications and is driven out on the DIO bus during RAM read cycles. More information covering the on board RAM can be found in the next section of this document.

A watchdog timer also exists within U29 which will assert 'BERR*' should 'BAS*' remain low longer than 5.6 uS. Another function of U29 is to provide a 20 MHz clock which is used by the I/O subsystem. The MMU which consists of U29 and RAMs U57, U58, and U59 will not be covered in this document. Refer to the 'INTRODUCTION' on page 3 for a list of documents which contain information on the MMU among other things.

U65 and U66 contain almost all control circuits necessary to support the I/O subsystem on Model 310 boards. U65 sits on the I/O buffered address bus(IBA) and detects accesses to the system timer(U97,MC6840), RS-232, HP-IB, BOOTROMS, test LEDs, bit mapped display, display ID ROM, and 8042 peripheral processor(keyboard control, beeper control, timers, and RTC). Chip select information is then passed to U66 which handles the DIO bus cycle as well as guaranteeing the timing specs are met for each I/O device(address setup and hold time, etc.). U66 also contains support registers for all the I/O devices which need support as well as special control signals needed by HP-IB to support DMA. Both U65 and U66 contain new circuitry which allows an interrupt to be generated as the result of a device on HP-IB responding during a parallel poll. More information on the specific support provided to each I/O device can be found

defined bit in Registers 3 and 5 for both read and writes.

```
READ STATUS        7     6     5     4     3     2     1     0
$470003
REGISTER 3
                 |  1  | INT |  X  |  X  |  X  |  0  |  X  | DE  |


WRITE CONTROL      7     6     5     4     3     2     1     0
$470003
REGISTER 3
                 |  X  |  X  |  X  |  X  |  X  |  X  |  X  | DE  |


READ EXT. STATUS   7     6     5     4     3     2     1     0
$470005
REGISTER 5*                                    | KBD |
                 | SYS |  AC |  X  |  X  |  X  | NMI |  X  |  1  |
```

INT = HP-IB interrupt bit
DE = DMA enable on Channel 0
SYS = System Controller line on HP-IB
AC = Controller in Charge(Pin 30 on TMS9914A,U96)
KBD NMI = Keyboard interrupt on level 7
X = Floating data when read,no effect when written

* No bits in Register 5 can be written.

FIGURE 4
STATUS/CONTROL REGISTERS FOR HP-IB

There are only two active bits in Register 3,'INT' and 'DE'.
'INT' is a read only bit which, when set, means there is an
un-serviced level 3 interrupt form the TMS9914A HP-IB
controller. 'DE', on the other hand, is a read/write bit. This
bit, when set, enables the HP-IB interface for DMA transfers on
channel 0. Refer to the 'DIO Bus Specification' for more
detailed information on how DMA works.

Register 5 is a read only register with 3 active bits. The
'SYS' bit is connected to a switch and to pin 1 of a
SN75162(U71) HP-IB BUS Transceiver. This bit, when set, allows
the HP-IB interface to be System Controller. The 'AC' bit is
connected to pin 30 of the TMS9914A and allows software to
determine if the TMS9914A(U96) is currently the Controller in
Charge. When 'AC' is low, the TMS9914A is the Controller in
Charge. 'KBD NMI', the final active bit in Register 4, allows
software to test the keyboard controller and determine if it is
responsible for an interrupt on level 7(More on the keyboard
controller in the next chapter).

Bits in Registers 3 and 5 which return a '0' or '1' as shown in
Figure 4 have special meanings when set to their opposite
values. These bits are only used in some Series 200 computers
and should never be used in Series 300. The definition of these
three bits will not be covered in this document since current
Series 300 computers set these bits to their inactive values.

Registers 7 and 9 are new registers which have been added to
the HP-IB interface. These new registers add the capability
of generating an interrupt from a parallel poll response to
the HP-IB interface. Figure 5 shows the name and location of
each defined bit in Registers 7 and 9.

READ PARALLEL
POLL STATUS
$470007
REGISTER 7

7	6	5	4	3	2	1	0
IE	IR	0	0	0	0	0	0

WRITE PARALLEL
POLL STATUS
$470007
REGISTER 7

7	6	5	4	3	2	1	0
IE	IR	X	X	X	X	X	X

READ PARALLEL
POLL INTERRUPT
MASK
$470009
REGISTER 9

7	6	5	4	3	2	1	0
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

WRITE PARALLEL
POLL INTERRUPT
MASK
$470009
REGISTER 9

7	6	5	4	3	2	1	0
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

IE = INTERRUPT ENABLE BIT (1=ENABLE)
IR = INTERRUPT REQUEST BIT (1=INTERRUPT PENDING)
HDn = HP-IB DATA BUS BIN n
X = Floating data when read,no effect when written

FIGURE 5
HP-IB PARALLEL POLL REGISTERS

Register 7 allows software to enable/disable parallel poll
interrupts and to report the status or clear interrupt
requests. Setting 'IE' high enables interrupts while setting
'IE' low disables them. The 'IR' bit is set high when an
interrupt condition exists within the parallel poll circuits.

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Writing a '0' to this bit acknowledges the interrupt and clears the 'IR' bit.

Register 9 is the interrupt mask register which allows software to ignore parallel poll responses on selected HP-IB data lines. More specifically, wherever a '0' exists in the interrupt mask register, the corresponding HP-IB data line is ignored when looking for a parallel poll response. In Figure 5, 'HD7' corresponds to 'DIO8' on the HP-IB data bus, 'HD6' corresponds to 'DIO7', and so forth. A parallel poll response in the case of the Model 310 implementation is a '1' being returned on the of the HP-IB data lines when the HP-IB is in the parallel poll state. The IEEE-488 standard also allows for the opposite polarity to be set up as a valid response, however, hardware limitations in the Model 310 design did not allow a 'logic sense' register to be implemented.

The HP-IB parallel poll state machine has most of its logic located in U66, however, terms form this circuitry are fed into the chip select equations of U65. When parallel poll is enabled, the parallel poll state machine looks for a processor bus cycle that is not to the I/O subsystem of the Model 310 processor board. When such a cycle is detected, the parallel poll logic then takes over the local data bus(preparing for a read from register 6 within the TMS9914A), drives the TMS9914A register 6 address out on the RS0 thru RS2 address lines, waits for valid data to be returned from the TMS9914A, then starts looking for a parallel poll response. Should the processor request access from one of the I/O subsystem's devices, the parallel poll state machine will hold off this access from 800 to 900 nS while it frees up the local data and address bus. After the processor has finished with this I/O cycle, the parallel poll logic starts looking for another bus cycle which is not to the I/O subsystem of the Model 310 processor board. Once in the parallel poll mode and a parallel poll response is detected, interrupt level 3 is asserted. At approximately the same time, the parallel poll state machine begins the cycle to give up the I/O subsystem's data and address bus(RS0, RS1, and RS2). The parallel poll state machine will not return into the parallel poll sampling state until the parallel poll interrupt is cleared. One word of caution to programmers writing code which uses the parallel poll mechanism, you can not have DMA enabled for the on board HP-IB at the same time the parallel poll circuit is also enabled. A bus conflict may result which could cause corrupt data. More detailed information on U65 and U66 can be found in the "ERS for Bobcat Standard Cell Components(1820-4153 and 1820-4154)", HP Drawing A-5958-4363-1.

H) KEYBOARD INTERFACE AND OTHER RELATED SUBSYSTEMS

An Intel 8042 Universal Peripheral Interface 8-Bit Microcomputer(U67) is used as the interface to the keyboard. Because of the flexibility and power of this part, it has taken

on more than just keyboard tasks. The 8042 also serves as the
interface to a Texas Instruments SN76494(U63) digital complex
sound generator, provides several 10 milli-second resolution
timers, does key-code conversions for the ITF keyboard, manages
the HP-HIL interface(thru U62), and has a battery backed up
real time clock(U73) tied to its peripheral data path.

There are no external registers associated with the 8042. Two
registers within the 8042 are multiple mapped throughout a 64
kilo-byte memory block beginning at $420000 and ending at
$42FFFF. The 'DATA' register's primary address is $420001 and
the 'COMMAND' register's primary address is $420003. Once
again, due to the way the keyboard interface was designed for
past products, current software does not use the primary
addresses to talk to the 8042. In some past implementations,
the actual address was used to determine the 'DTACK' speed. This
is not true for the Model 310 processor board's implementation.
Since the 8042's registers are mapped every 4 bytes, current
software need not be changed.

For more information on the 8042 keyboard controller, refer to
HP drawing A-1820-4379-2.

in the following chapters on that specific I/O device. Memory
map(multiple map information), chip select bus definition, and
other information specific to U65 and U66 can be found in the
"ERS for Bobcat Standard Cell Components(1820-4153 and
1820-4154)", HP Drawing A-5958-4363-1.

B) ON BOARD RAM

Two jumpers(JP3 and JP4) on the Model 310 Processor Boards
configure the RAM controller(located within the MOTOROLA
MCA2800ALS gate array,U29) for 0, 1/2, or 1 Megabyte operation.
A table showing the jumper settings can be found on Page 1 of
the schematic, HP Drawing E-98561-66512-4. Parity for the
on-board RAM is also an option which is allowed/disallowed by
loading/not loading the parity RAM. Within the RAM controller,
parity RAM is assumed to not be present until a 0 is seen on the
low parity line($\overline{PL}$ on U29 pin E14) during a read from on-board
RAM. Once parity RAM is detected by the RAM controller, the RAM
array behaves like a 98257A card with one exception. The access
time for the on-board RAM is 400 nano-seconds compared to 620
nano-seconds for the 98257A RAM card.

Parity is always generated for writes. Writing a '1' to memory
location $5BXXXX enables detection of parity errors for reads
from all memory in the system which has parity. Writing a '0'
disables parity detection for all system memory. When a parity
error is detected, NMI(interrupt level 7) is asserted and
remains asserted until either the system is RESET or a '0' is
written to $5BXXXX. Software can determine if a parity error is
responsible for the NMI by reading location $5BXXXX. Reading
memory location $5BXXXX will result in a 'BUS ERROR' if no
parity errors are pending. If a parity error is pending, the
read to location $5BXXXX will occur successfully however, the
data read back has no meaning and should be ignored.

A test feature has been incorporated into all RAM controllers
which support parity. Writing a '2' to memory location $5BXXXX
enables the RAM controller to generate 'ODD' parity. Since the
RAM controller always detects 'EVEN' parity, this feature
allows software to force parity errors at specific memory
locations.

If parity RAM is not loaded, there exists one potential
problem. Writing to memory location $5BXXXX(RAM control
register) can occur without a 'BUS ERROR'. In past systems, a
successful write to the RAM control register implied that
parity was in the system. Now, however, a parity error will
have to be forced in order for software to be certain that
parity detection is occurring. This should only affect test
code, not any of the operating systems or languages currently
supported on Series 300.

MMU/DRAM controller(U29) signals MA1 thru MA9 serve multiple
purposes. These lines transfer DIO addresses BA1 thru BA9 from

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the MMU(U29) to the DIO address bus interface system(U89, U94, U106, and U107), from the DIO address bus interface system to the MMU when an alternate bus master is active, as well as providing row and column addresses to the on board RAM. The MMU/DRAM controller also controls the DIO address bus interface system as well as generating the row addresses, column addresses, and control signals($\overline{RAS},\overline{CAS},\overline{WE}$) for the RAM array.

RAM address and control signals are buffered by U80, U82, and U83. A hardware test feature is present which allows test equipment to tri-state these buffers by taking U77 pin 13 low. The ability to tri-state the RAM address/control buffers allows test equipment to drive its own signals on these lines thus increasing the testability of the board. Taking U77 pin 13 low also disables the clock generator(U33) for the bit-mapped display.

JP13 and JP14 are present to allow future revisions of the MMU/DRAM controller(U29) to correct an oversight. When an alternate bus master is active(i.e. DMA) and addressing on board RAM, MA9 presently does not drive BA18 information to the RAM during the RAM's $\overline{CAS}$ cycle. U88 currently serves as both a buffer for driving BA9 information on the MA9 line when appropriate as well as a mechanism for getting BA18 information driven on the MA9 line for RAM $\overline{CAS}$ cycles when an alternate bus master is active and addressing on board RAM. By moving both JP13 and JP14 from their 2-4 positions to their 1-3 positions, U89 is only allowed to drive BA9 information on the MA9 bus when it is enabled to do so. There should then be a MMU/DRAM controller loaded in the board that has the ability to drive the correct information on MA9 when an alternate bus master is active. **CAUTION!** Future turns of the MMU/DRAM controller may *not* fix the oversight mentioned above. More information on the RAM controller can be found in the MCA2800ALS Gate Array ERS written by Nick Mati and Dan Swanson.

C) MC6840 SYSTEM TIMER

With the variety of Series 200 microprocessor boards and the difference in instruction execution speeds between many of these boards, Series 200 software required hardware support for its time dependent operations. The MOTOROLA MC6840 timer is the device chosen for past processor boards and is the device which Model 310 will also use.

There are no external registers implemented to supplement the registers which already exist within the MC6840. Registers within the MC6840 are multiple mapped within a physical 16 kilo-byte memory region beginning at $5F8000 and ending at $5FBFFF. The function of registers within the MC6840 will not be covered in this document. For information as to the function of the registers within the MC6840, the reader is referred to

the MC6840 Programmable Timer Module(PTM) data sheet which can
be found in the MOTOROLA MICROPROCESSORS DATA MANUAL. Table 1
shows the primary physical memory locations where each register
within the MC6840 can be accessed.

DIO ADDRESS	REGISTER NUMBER	RS2	RS1	RS0
$5F8001	0	0	0	0
$5F8003	1	0	0	1
$5F8005	2	0	1	0
$5F8007	3	0	1	1
$5F8009	4	1	0	0
$5F800B	5	1	0	1
$5F800D	6	1	1	0
$5F800F	7	1	1	1

TABLE 1
MC6840 MEMORY MAP

There are three 16 bit binary counters located within the
MC6840(U97) which can be clocked from two sources, the Enable
clock('E') and an external clock. It is recommended that none
of the counters be enabled to use 'E' as the clock source. The
frequency of this clock will vary from processor board to
processor board. All Series 200 and Series 300 processor boards
which have a MC6840 PTM will have the following in common. The
external clock pins(U97 P28,P7) for counters 1 and 3 have a 250
kilo-hertz clock connected to them. Counter 2 has its external
clock source connected to the output pin of counter 3. Gate
inputs for counters 1, 2, and 3(U97 P26,P2,P5) are all tied low
which permanently enables all counters. The interrupt output
pin(U97 P9) is also tied directly to 'IR6*' thru an open
collector buffer. Interrupt enable/disable is controlled
through registers within the MC6840.

In order to reduce capacitive loading on the RAM/MMU/68010 data
bus, the MC6840 was placed on the IBD data bus. By doing this,
special interface logic was required. The MC6840 interface
logic was designed to allow the use of the less expensive slower
access speed parts. This logic is part of U66, one of the two
TI standard cell ICs. U66 generates a high true chip select(U66
P48) which is synchronized to 'E'. 'E' is also generated by
U66(P2). The timing on these two signals meet the timing
requirements of the MC6840, which can be found in the MC6840
data sheet mentioned above. In order to guarantee valid data to
the 68010 during reads from the MC6840(U97), U66 latches the
data from the MC6840 and holds it on the IBD bus until 'BAS*'
goes inactive. 'DTACK*' for the MC6840 is also generated by U66.

U65, the other TI standard cell IC, decodes the address for the
MC6840 and feeds this information to U66 via the encoded chip
select bus(CS0 thru CS3 and CSEN). Additionally, U65 divides
the 20 MHz clock from U29(Motorola MC2800ALS gate array) and
generates the 250 KHz clock for the MC6840's counters.

D) BOOTROMs and TEST LEDs

Model 310 processor boards support up to four ROM packages and
a maximum of 128 kilo-bytes of ROM memory starting at DIO
address $000000 through $01FFFF. Jumpers on Model 310
processor boards allow the use of JEDEC ROMs, Mostek ROMs, or
JEDEC EPROMs from the 128 kilo-bit size up to the 512 kilo-bit
size. Only two 512 kilo-bit ROM/EPROMs should be loaded since
only the first 128 kilo-bytes will be decoded by U65(custom TI
IC). JP11 and JP 12 select the type of ROM which is to be used
while JP10 adjusts the size of the address space represented by
the two output enable signals, OEL and OEH. With this
architecture, 128K bit ROM/EPROMs will be multiple mapped within
the 128K byte address space for which 'DTACK' is always
generated(U66 contains 'DTACK' logic, U65 contains decoding
logic). 256K bit ROM/EPROMs will not be multiple mapped while
two 512K bit ROM/EPROMs will completely use up the 128K byte
address space. Detailed information on how to set the jumpers
can be found on page 2 of the schematic, HP drawing
E-98561-66511-4.

Test LEDs have been on all recent CPU boards and help service
personnel in trouble shooting. There are 8 test LEDs tied to
data lines D0 thru D7 which software can set or clear by writing
to BOOTROM memory locations $010001 through $01FFFF(lower
bytes). Writing to the upper bytes(D8 thru D15) in this address
range will clock whatever is on the lower data bus(D0 thru D7)
into the test LED register(U105), however, this feature should
not be counted on for other products. Writing '1's to the test
LEDs turn them off while writing '0's turn them on.

Model 310 and Model 320 processor boards put their test LEDs
in the same location and orientation. Viewing the board from the
front of the product, the LEDs read from left to right with the
left most LED being the one tied to D7(MSB).

At power on, the test LEDs are turned on by 'hard reset'.
BOOTROM software will turn off all test LEDs should no hardware
problem be found. Before the BOOTROM turns off the test LEDs
it will flash many different patterns on them as various BOOTROM
system tests are started. If a hardware problem is detected,
the test LEDs display a code which identifies the problem. A
list of error codes displayed on the test LEDs by the BOOTROM
and more information on the BOOTROM can be found in "THE
BRIARPATCH TECHNICAL REFERENCE SPECIFICATION" by Anny Randel, HP
document number A-5958-4350-2.

E) RS-232

One RS-232 port is supported on Model 310 processor boards.
This port is based on National Semiconductor's INS8250 UART and
has an implementation almost identical to the 98644A RS-232
Serial Interface card. The differences between the 98644A card

and the Model 310 implementation is mentioned in the 'RS-232'
section of the chapter titled 'SERIES 310 FEATURES AND SOFTWARE
COMPATIBILITY' found earlier in this document.

In addition to the registers built into the INS8250 UART, two
external registers have also been implemented. Table 2 is a
memory map showing the primary address of both external and
internal registers. Both sets of registers are multiple mapped
within the 64 kilo-byte region of memory associated with I/O
select code 9(DIO Address space $690000 thru $69FFFF).
For information on the operation of the INS8250 and its
registers, refer to the 'INS8250A Asynchronous Communications
Element' data sheet from National Semiconductor.

DIO ADDRESS	REGISTER
	EXTERNAL REGISTERS
$690001	ID/RESET(REGISTER 1)
$690003	STATUS/CONTROL(REGISTER 3)
	INS8250A REGISTERS
$690011	Tx/Rx and DIVISOR LATCH(LSB)
$690013	INT. EN. and DIVISOR LATCH(MSB)
$690015	INTERRUPT IDENTIFICATION(READ)
$690017	LINE CONTROL
$690019	MODEM CONTROL
$69001B	LINE STATUS
$69001D	MODEM STATUS
$69001F	SCRATCH PAD MEMORY

TABLE 2
RS-232 SERIAL INTERFACE MEMORY MAP

U65 and U66(the two TI custom ICs) perform all address decoding,
control signal generation, and external register support for the
Model 310 RS-232 implementation. U65 decodes the address and
sends this information to U75 and U66 via the chip select
bus(CSEN, CS0, CS1, CS2, and CS3). U75 detects CPU accesses to
the INS8250's(U64) registers and generates/drives a chip select
to U64 pin 14. U66 detects all CPU accesses to RS-232 registers
and starts I/O cycles which consists of either IOR or IOW going
low(IOR for read cycles, IOW for write cycles) and DTACK being
generated at the appropriate time.

U65 also generates the basic frequency needed by U64's integral
baud rate generator, 2.4576MHz. The actual frequency is not
2.4576MHz, but 2.4614MHz which is generated within U65 by first
dividing 20MHz by 8 seven times then dividing by 9 once. The
resulting clock will have jitter if viewed on an oscilloscope.
Since this jitter occurs once every eight clock pulses and the
INS8250A(U64) uses a 16X clock to sample data, this jitter
should cause no or very little error. The slightly higher
frequency will result, however, in a 0.16% error in the baud

Sub Fig. 1 for RevM

rate for both input sampling and output signal generation. This error will not be noticeable if the RS-232 cables are within specification and the equipment at the other end does not have any gross errors in its baud rate clock.

External Register 1(Shown in Figure 2) is the ID/RESET register common to all DIO cards which reside within the DIO address space $600000 through $7FFFFF. When this register is read $42(or $C2 if the RS-232's REMOTE bit is set) is returned which is the 98644A card ID. Writing this register(data is ignored) resets the serial interface. More information on setting or clearing the REMOTE bit and on the RS-232 interface in general can be found in the 'RS-232' chapter located within the 'SERIES 310 FEATURES AND SOFTWARE COMPATIBILITY' section of this document.

External Register 3 is the STATUS/CONTROL register. Figure 2 shows the name and location of each bit for both read and write operations. 'IE' is the interrupt enable bit and can be set or cleared by software. 'IR' is the interrupt request bit which allows software to read the status of U64 pin 30.

READ ID
$690001

7	6	5	4	3	2	1	0
REMOTE /LOCAL BIT	1	0	0	0	0	1	0

WRITE RESET
$690001

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

READ STATUS
$690003

7	6	5	4	3	2	1	0
		INTERRUPT LEVEL					
IE	IR	1	0	0	0	0	0

WRITE CONTROL
$690003

7	6	5	4	3	2	1	0
IE	X	X	X	X	X	X	X

FIGURE 2
STATUS/CONTROL REGISTER

Figure 3 shows the pin definitions for the DB25S connector.

See Pg. 1 for Revi.

Also shown in this figure is the INS8250 signal and pin tied
indirectly to the DB25S connector. Signal OUT2 on the INS8250
is not connected to anything in both the Model 310 RS-232
implementation nor in the 98644A RS-232 card implementation.
This signal was called OCD2(DRS) on the 98626A RS-232 card.

DB25S PIN #	SIGNAL NAME/DESCRIPTION	INS8250 SIGNAL NAME	INS8250 PIN NUMBER
1	SAFETY GROUND [PROTECTIVE GROUND]	-----	--
2	TRANSMIT DATA [SDu]	SOUT	11
3	RECEIVE DATA [RD(A)]	SIN	10
4	REQUEST TO SEND [RS(u)]	RTS*	32
5	CLEAR TO SEND [CS(A)]	CTS*	36
6	DATA SET READY [DM(A)]	DSR*	37
7	SIGNAL GROUND [SG]	-----	--
8	CARRIER DETECT [RR(A)]	DCD*	38
20	DATA TERMINAL READY [TR(u)]	DTR*	33
22	RING INDICATE [OCR1]	RI*	39
23	DATA RATE SELECT [OCD1]	OUT1*	34

* Indicates negative true signal names.

All pins not shown for the DB25S connector are no connects.

FIGURE 3

SW1-1(See figure 1) is tied to the input of four open collector
buffers, U32 pins 5, 9, 11, and 13. When this switch is in the
open position, the output transistors in the open collector
buffers are turned off and hence have no effect on the buffered
versions of CTS, CD, DSR, and RI. However, if SW1-1 is closed,
the output transistors in the open collector buffers turn on and
force '0' on the INS8250A's input lines to which the buffered
versions of CTS, CE, DSR, and RI are tied. Since the INS8250A
has inverting inputs, closing SW1-1 forces ones for the four
signals mentioned above thus disabling these modem handshake
lines.

F) BIT MAPPED DISPLAY(98561-66511 and 98561-66512 Boards Only)

Two Model 310 processor boards(98561-66511 and 98561-66512) have
a single plane byte per pixel bit mapped display included on
them. This bit mapped display has 1024 horizontal by 400
vertical dot resolution, however, due to the geometry of the
raster on the monitor, 1024 by 400 results in
non-square(rectangular) pixels. Due to this, graphics software
treats this display as if it had 512 by 400 dot resolution by

always turning on two adjacent pixels instead of one. The
benefit of having 1024 by 400 is that the character fonts are
much more readable than they would have been if the display were
truly 512 by 400.

The frame buffer for the Model 310 boards is memory mapped at
DIO addresses $200000 thru $2FFFFF. When the frame buffer is
read, invalid data will be returned for the unused planes. The
fact that invalid data is returned when the frame buffer is
read, that the pixels are non-square, plus other information is
all encoded within the DISPLAY ID ROM(U98) which is memory
mapped at odd DIO addresses $560001 thru $563FFF. The Display
ROM's definition can be found in HP drawing A-_____-_____-2 by
Steve Wolf.

The heart of the bit mapped display is TOPCAT, U35. TOPCAT
control registers are memory mapped at DIO addresses $564000
thru $564FFF. Additional information on TOPCAT can be found in
the following documents:

   (1) TOPCAT ERS; DWG # A-1FH2-2001-007

   (2) Graphics Subsystems Application Note;
        DWG # A-5958-4374-1

Model 310 processor boards have TOPCAT connected such that it
can be only used in 'low resolution' applications. The range of
'low resolutions' available with TOPCAT can be found in the ERS
listed above. Changing resolutions on Model 310 processor
boards(for future products) will involve changing the frequency
of Y1 and redefining the Display ID ROM(U98).

U33(74F195) and Y1(35.904 MHz oscillator) form the TOPCAT clock
generator/video shift register circuit. When using the 'V1BUS1'
and V1BUS2' video outputs from TOPCAT for 'low resolution'
applications, the clock input must be 1/2 the dot rate
frequency. The first two registers of U33(74F195 4-BIT
parallel-access shift register, outputs QA and QB) form the
clock divider and the load/shift signal circuit. QB(U33 pin 14)
outputs the clock signal(17.952 MHz) to TOPCAT(U35 pin E13).
QA(U33 pin 15) is the shift/load signal which if fed back into
pin 9 of U33. The shift/load signal not only determines when to
sample video data from TOPCAT, this signal is an integral part
of the ring counter which divides the dot rate frequency in
half. The last two stages of the 74F195 shift register sample
the video data from TOPCAT(V1BUS1 and V1BUS2) and convert it to
a serial bit stream. This TTL video signal then goes to the
circuits which add the TTL video and TTL sync signals together
to be driven out to one of the supported 'low resolution'
monitors. This composite video signal meets the voltage and
timing specifications of the JACKPOT 12" monochrome monitor. See
HP Drawing A-35731-90004-1 written by Carl R. Haynie(RTD) for
more information on the JACKPOT monitor(35731 A/B).

G) HP-IB

HP-IB's implementation is based upon the Texas Instruments
TMS9914A General Purpose Interface Bus(GPIB) Controller(U96).
The architecture of this implementation is based upon the
internal HP-IB design used in all Series 200 computers. One new
feature has been added to this interface, the ability to
generate an interrupt from a parallel poll response. For this
feature, two new registers external to the TMS9914 have been
added. These two new registers are in addition to the two
external registers that exist for other Series 200 computers.

All registers associated with the HP-IB are multiple mapped
within a 64 kilo-byte block of memory beginning at $470000 and
ending at $47FFFF. Table 3 shows all HP-IB registers and their
primary memory address. Due to the limitations of past
implementations, current software does not access the primary
HP-IB address but one of the secondary(multiple mapped)
addresses. In some past implementations, part of the address
was used to determine the access time(time taken to drive
'DTACK'). This is not true for the Model 310 processor board's
implementation. To preserve software compatibility, however,
Model 310 multiple maps its HP-IB registers every 32 bytes
within the HP-IB address space.

DIO ADDRESS	REGISTER	
	EXTERNAL REGISTERS	
	READ / WRITE	
$470003	STATUS/CONTROL(REGISTER 3)	
$470005	AUX. STATUS/CONTROL(REGISTER 5)	
$470007	P.POLL STAT./CONTROL(REGISTER 7)	
$470009	PARALLEL POLL MASK (REGISTER 9)	
	TMS9914A REGISTERS	
$470011	INT. STATUS 0 / INT. MASK 0	
$470013	INT. STATUS 1 / INT. MASK 1	
$470015	ADDRESS STATUS /	
$470017	BUS STATUS / AUXILIARY CMD.	
$470019	/ ADDRESS	
$47001B	/ SERIAL POLL	
$47001D	CMD PASS THRU / PARALLEL POLL	
$47001F	DATA OUT / DATA IN	

TABLE 3
HP-IB INTERFACE MEMORY MAP

Information on the TMS9914A and its registers can be found in
the 'TMS9914A General Purpose Interface Bus(GPIB) Controller'
Data Manual from Texas Instruments. The four external registers
associated with HP-IB are documented in the following
paragraphs.

Registers 3 and 5 existed in past Series 200 internal HP-IB
implementations. Figure 4 shows the name and location of each