64000

HP64000 Logic Development System

Model 64340A Software Analyzer

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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Your cooperation in completing and returning this form will be greatly appreciated. Thank you.

READER COMMENT SHEET

Service Manual
Model 64340A, Software Analyzer
64340-90901, December 1984

Your comments are important to us. Please answer this questionaire and return it to us. Circle the number that best describes your answer in questions 1 through 7. Thank you.

1. The information in this book is complete:

Doesn't cover enough (what more do you need?)	1 2 3 4 5	Covers everything

2. The information in this book is accurate:

Too many errors	1 2 3 4 5	Exactly right

3. The information in this book is easy to find:

I can't find things I need	1 2 3 4 5	I can find info quickly

4. The Index and Table of Contents are useful:

Helpful	1 2 3 4 5	Missing or inadequate

5. What about the "how-to" procedures and examples:

No help	1 2 3 4 5	Very helpful
Too many now	1 2 3 4 5	I'd like more

6. What about the writing style:

Confusing	1 2 3 4 5	Clear

7. What about organization of the book:

Poor order	1 2 3 4 5	Good order

8. What about the size of the book:

too big/small	1 2 3 4 5	Right size

Comments: _____

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Name (optional): _____
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Particular pages with errors?

_____

Name (optional): _____
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Company: _____
Address: _____

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used on Equipment or in Manuals.

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).

 **OR** 

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.

 **OR** 

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE:

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

HEWLETT PACKARD

SERVICE MANUAL

MODEL 64340A
SOFTWARE ANALYZER

REPAIR NUMBERS

This manual applies to **HP 64340A Software Analyzer** with a repair number prefix of 2426A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Chapter 1.

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LOGIC SYSTEMS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

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Manual Part No. 64340-90901

PRINTED: December 1984
UPDATED: May 1985

Printing History

Each new edition of this manual incorporates all material updated since the previous edition. Manual change sheets are issued between editions, allowing you to correct or insert information in the current edition.

The part number changes only when each new edition is published. Minor corrections or additions may be made as the manual is reprinted between editions. Vertical bars in a page margin indicate the location of reprint corrections.

First Edition . . . . . **December 1984 64340-90901**
Update 1 . . . . . **May 1985**

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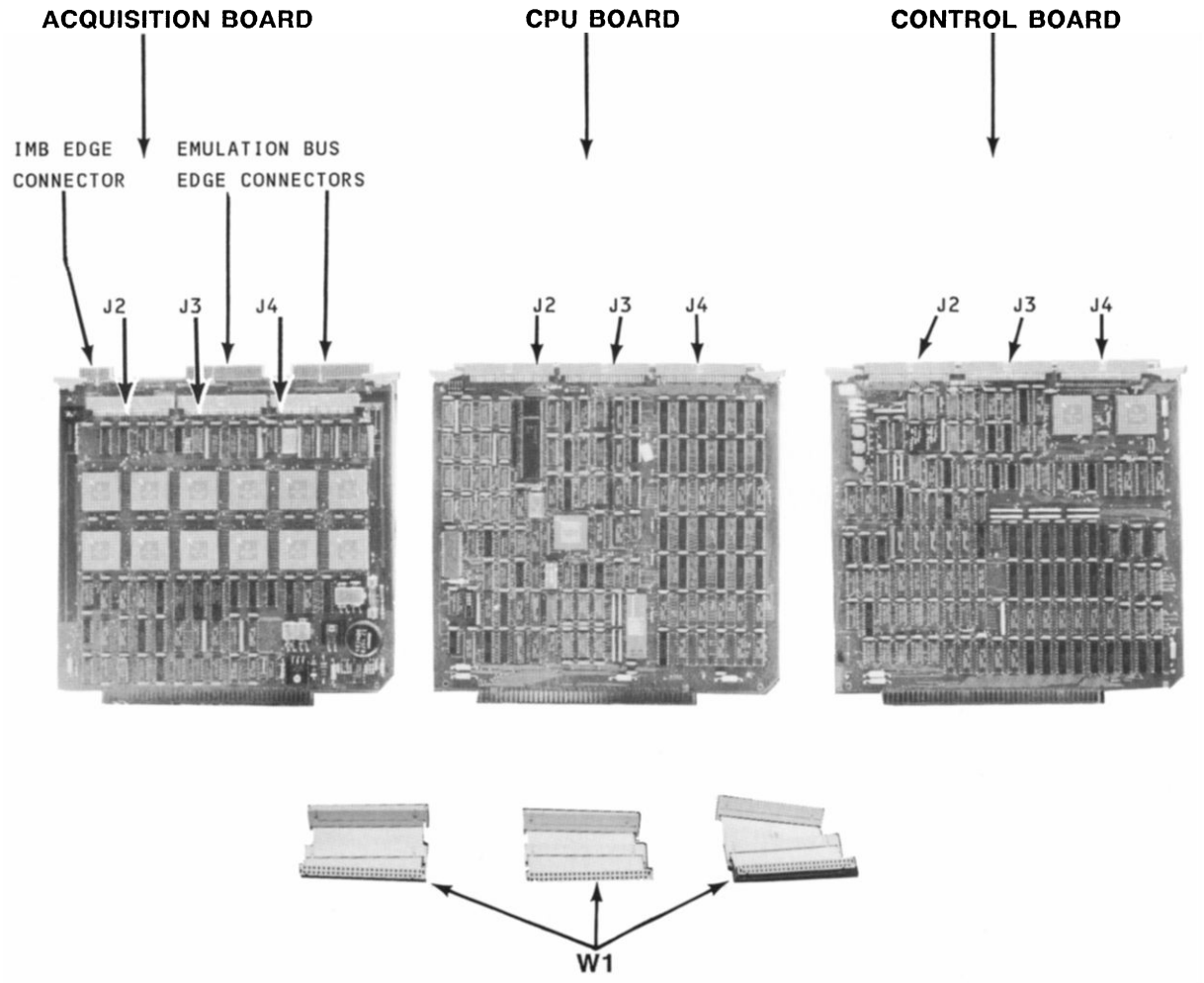


Figure 1-1. Model 64340A Software Analyzer

Chapter 1
GENERAL INFORMATION

INTRODUCTION

This manual contains information concerning the installation, maintenance and troubleshooting of the Model 64340A Software Analyzer to the "Bluestripe" board level. In the event a board does fail, it can be shipped back to the factory and replaced with a replacement board at a lesser cost than buying a new board. Refer to the nearest Hewlett-Packard Sales/Service Office for more information on the Bluestripe program.

MANUAL ORGANIZATION

This is a Bluestripe service manual and is organized in six chapters. These are:

Chapter 1 contains general information on the Model 64340A, including electrical specifications and equipment requirements.

Chapter 2 explains how to install the Model 64340A in the HP 64100A Logic Development Station, and also includes information on environmental limits of operation and packing instructions.

Chapter 3 contains performance verification procedures for verifying operation of the HP 64340A Software Analyzer. This chapter also contains block level theory and troubleshooting procedures.

Chapter 4 contains information on adjustments the the Model 64340A Software Analyzer requires periodically.

Chapter 5 lists all parts of the Model 64340A that may be directly replaceable.

Chapter 6 contains information on the product serial prefix number(s) this manual applies to, and how to adapt this manual to instruments which the contents do not directly apply.

INSTRUMENTS COVERED BY THIS MANUAL

Printed on the printed circuit board is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed on the title page.

An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Change supplement.

For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

ELECTRICAL SPECIFICATIONS

Table 1-1. HP 64340A Software Analyzer Power Consumption

CPU POWER	TYPICAL	TYPICAL +20%
+5V POWER	24.38 W	29.26 W
-5.2V POWER	1.26 W	1.51 W
-3.25V POWER	1.33 W	1.55 W
TOTAL POWER	26.97 W	32.32 W

CNTL POWER	TYPICAL	TYPICAL +20%
+5V POWER	17.52 W	21.02 W
-5.2V POWER	4.25 W	5.10 W
TOTAL POWER	21.77 W	26.12 W

ACQ POWER	TYPICAL	TYPICAL +20%
+5V POWER	22.05 W	26.46 W
-5.2V POWER	.36 W	.43 W
TOTAL POWER	22.41 W	26.89 W

TOTAL POWER CONSUMPTION OF ALL THREE BOARDS	TYPICAL	TYPICAL +20%
		85.33 W
+5V POWER	61.95 W	76.74 W
-5.2V POWER	5.87 W	7.64 W
TOTAL POWER	71.15 W	85.33 W

SOFTWARE ANALYZER DESCRIPTION

The HP 64340A Software Analyzer is an automated software measurement system designed to work with the HP 64100A Logic Development System to improve the productivity of the software engineer in the areas of debugging, testing, and designing. It is a three board set, and has the following capabilities:

Program/data flow measurements. Provide for overview of program control flow, data flow, program control flow/data flow interactions, and data modifications.

Program performance/testing measurements. Provide for real-time count and time metrics on program statement and module execution.

View and modify variables.

Measurement control. Commands for conditional execution of the measurements using comparisons between variables and values, or program execution and line numbers.

ACCESSORIES SUPPLIED

There are no accessories supplied with the basic HP 64340A Module (3 board set). When ordering other options to be used with the HP 64340A Module (such as State/Timing), special cable configurations will be required. Tables 2-1 (68000/10) and 2-2 (80186/88) list configurations, current usages, and cable options.

There are specific HP Software Part Numbers that are required to run the HP 64340A Module; these part numbers for the various supported emulators are as follows:

MODEL	EMULATOR	SOFTWARE PART NO.
64242A	68000	64341BA
64249A	68010	64341DA
64224A	80186	64341EA
64225A	80188	64341FA

NOTE

64224A 80186 Emulators must have a serial prefix of 25XXA or greater. If your emulator has a serial prefix number less than 25XXA (example : 24XXA), call your nearest Hewlett-Packard Sales/Service Office about purchasing an upgrade kit.

EQUIPMENT REQUIRED BUT NOT SUPPLIED

(for calibration).....1726A Oscilloscope (275 MHz)

(for calibration).....10017A Scope probe (Qty 2)

(for calibration.....64110-66503 Extender board (Qty 3)

(for calibration).....Adjustment Tool (insulated flathead type)

MANUALS SUPPORTING THIS PRODUCT

Service Manual for 64340A
Operating Manual - 64341BA/DA for 68000/10
Operating Manual - 64341EA/FA for 80186/88

Chapter 2

INSTALLATION

INTRODUCTION

This chapter contains information to install the HP 64340A Software Analyzer in the 64000 System. Information concerning initial inspection, damage claims, environmental considerations, storage and shipment is also included.

INITIAL INSPECTION

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents have been checked for completeness and the HP 64340A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the HP 64340A does not pass Performance Verification, notify the nearest Hewlett-Packard Office. If the shipping container or cushioning material is damaged, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP Office will arrange for repair or replacement at HP option without waiting for claim settlement.

INSTALLATION

All three boards of the HP 64340A Software Analyzer are installed into the 64100A Logic Development Station. They must be placed into the System cardcage a follows (from low to high card slot numbers): The CPU board must be first, the Control board second, and the Acquisition board third. See figure 2-3. The lowest numbered card slot is closest to the front of the development station.

Procedure To Install the HP 64340A Module:

a) Power down the development station.

b) Remove the four screws that secure the cardcage cover to the top of the HP 64100A Logic Development Station. See figure 2-1.

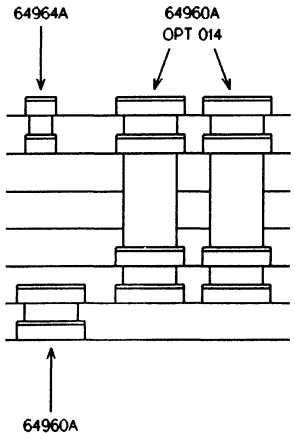
c) Install the three inter-connect cables (W1) onto J2, J3, and J4 of the Acquisition board (A3). See figure 2-2.

d) Install the CPU board in first. Note the position of the CPU board to the other options (State/Timing, Analysis). See tables 2-1 and 2-2.

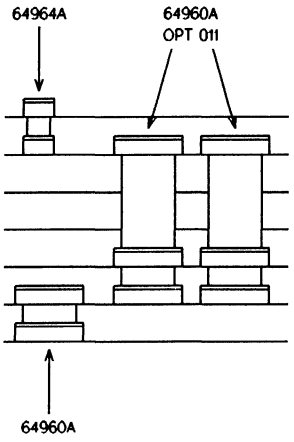
e) Install the other two boards into the development station cardcage. The position of the HP 64340A three board set in the cardcage should always be: CPU board first, the Control board second, and the Acquisition board third. See figure 2-3.

f) Connect the three inter-connect cables that were attached to the Acquisition board from "step c" to the HP 64340A Control and CPU boards. See figure 2-3.

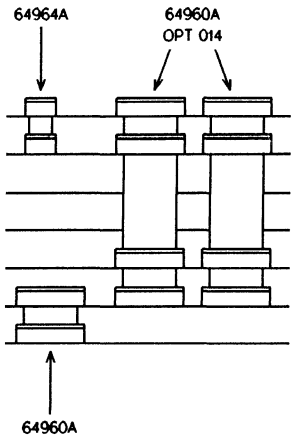
Table 2-1. HP 64340A (68000/10) Configurations, Current Usage, and Cable Options



		(+5 V)
SLOT 9	64302A ANL	3.70 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64242A/64249A EC	6.10 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	30.20 A



		(+5 V)
SLOT 9	64303A IMB	1.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64242A/64249A EC	6.10 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	28.30 A



		(+5 V)
SLOT 9	64310A ANL	5.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64242A/64249A EC	6.10 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	32.30 A

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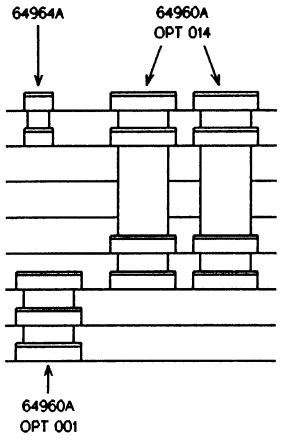
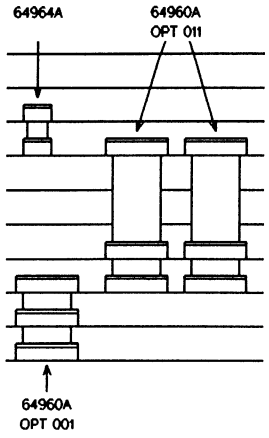
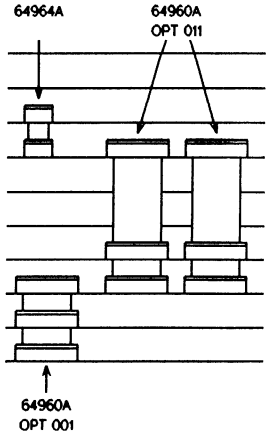


		(+5 V)
SLOT 9	64310A ANL	5.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64242A/64249A EC	6.10 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
2	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	33.90 A

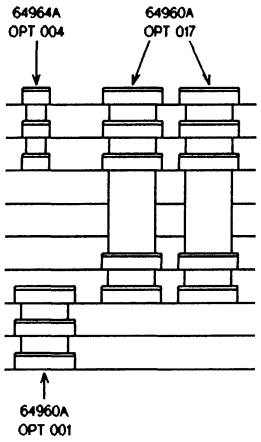


		(+5 V)
SLOT 9	OPT 011 20 CH ACQ	
8	OPT 011 40 CH ACQ	
7	64620S STATE CNTL	10.40 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64242A/64249A EC	6.10 A
2	64155A WIDE-ADDR MC	3.80 A
1	64161A 128K BYTE EM	1.60 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	38.50 A

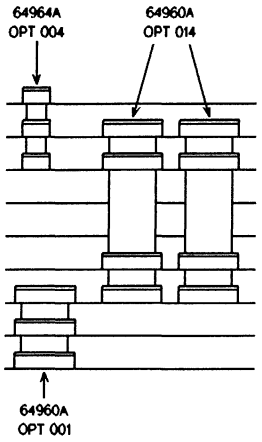


		(+5 V)
SLOT 9	OPT 012 40 CH ACQ	
8	OPT 012 40 CH ACQ	
7	64620S STATE CNTL	12.20 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64242A/64249A EC	6.10 A
2	64155A WIDE-ADDR MC	3.80 A
1	64161A 128K BYTE EM	1.60 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	40.30 A

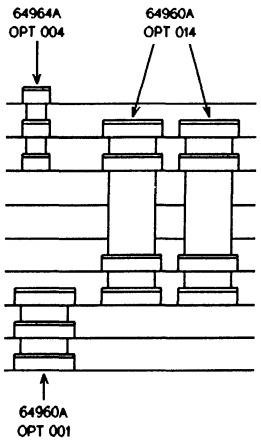
Table 2-1. HP 64340A (68000/10) Configurations, Current Usage, and Cable Options



			(+5 V)
SLOT 9	64302A	ANL	3.70 A
8	64310A	ANL	5.80 A
7	64340A	ACQ	5.00 A
6	64340A	CNTL	5.00 A
5	64340A	CPU	5.00 A
4	64242A/64249A	EC	6.10 A
3	64155A	WIDE-ADDR MC	3.80 A
2	64161A	128K BYTE EM	1.60 A
1	64161A	128K BYTE EM	1.60 A
	TOTAL CURRENT		37.60 A

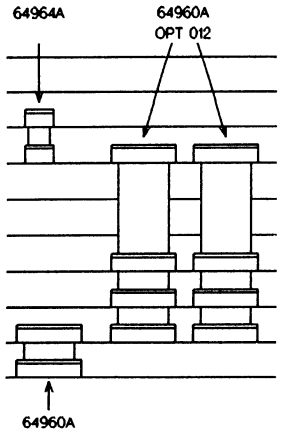


			(+5 V)
SLOT 9	64303A	IMB	1.80 A
8	64310A	ANL	5.80 A
7	64340A	ACQ	5.00 A
6	64340A	CNTL	5.00 A
5	64340A	CPU	5.00 A
4	64242A/64249A	EC	6.10 A
3	64155A	WIDE-ADDR MC	3.80 A
2	64161A	128K BYTE EM	1.60 A
1	64161A	128K BYTE EM	1.60 A
	TOTAL CURRENT		35.70 A

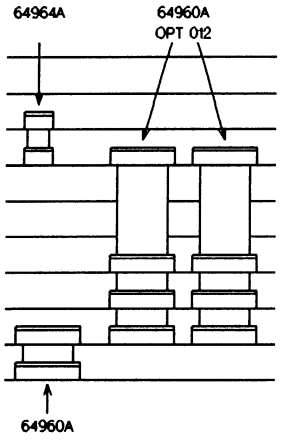


			(+5 V)
SLOT 9	64303A	IMB	1.80 A
8	64302A	ANL	3.70 A
7	64340A	ACQ	5.00 A
6	64340A	CNTL	5.00 A
5	64340A	CPU	5.00 A
4	64242A/64249A	EC	6.10 A
3	64155A	WIDE-ADDR MC	3.80 A
2	64161A	128K BYTE EM	1.60 A
1	64161A	128K BYTE EM	1.60 A
	TOTAL CURRENT		33.60 A

Table 2-1. HP 64340A (68000/10) Configurations, Current Usage, and Cable Options

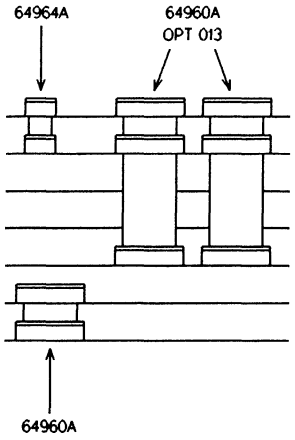


		(+5 V)	
SLOT 9	OPT 011 20 CH ACQ		
8	OPT 011 40 CH ACQ		
7	64620S STATE CNTL	10.40	A
6	64340A ACQ	5.00	A
5	64340A CNTL	5.00	A
4	64340A CPU	5.00	A
3	64304A EBPP	1.50	A
2	64242A/64249A EC	6.10	A
1	64155A WIDE-ADDR MC	3.80	A
0	64161A 128K BYTE EM	1.60	A
	TOTAL CURRENT	38.40	A

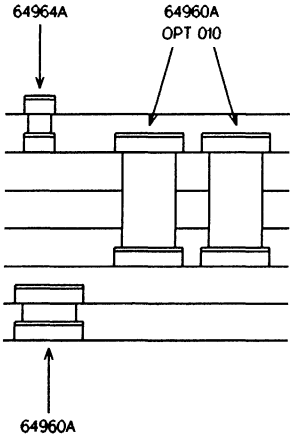


		(+5 V)	
SLOT 9	OPT 012 40 CH ACQ		
8	OPT 012 40 CH ACQ		
7	64620S STATE CNTL	12.20	A
6	64340A ACQ	5.00	A
5	64340A CNTL	5.00	A
4	64340A CPU	5.00	A
3	64304A EBPP	1.50	A
2	64242A/64249A EC	6.10	A
1	64155A WIDE-ADDR MC	3.80	A
0	64161A 128K BYTE EM	1.60	A
	TOTAL CURRENT	40.20	A

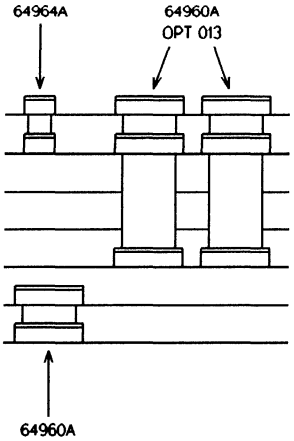
Table 2-2. HP 64340A (80186/88) Configurations, Current Usage, and Cable Options



		(+5 V)
SLOT 9	64302A ANL	3.70 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64224A/64225A EC	6.20 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	30.30 A

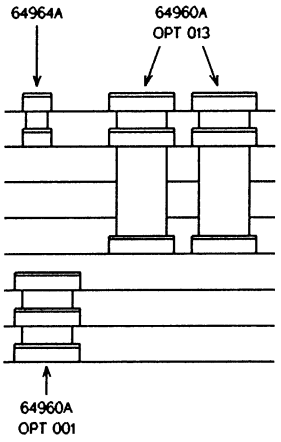


		(+5 V)
SLOT 9	64303A IMB	1.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64224A/64225A EC	6.20 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	28.40 A

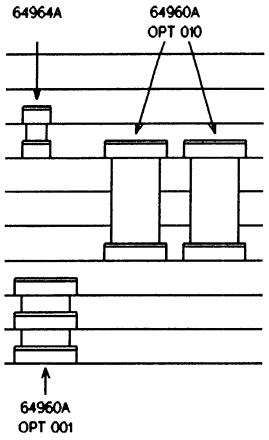


		(+5 V)
SLOT 9	64310A ANL	5.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64224A/64225A EC	6.20 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	32.40 A

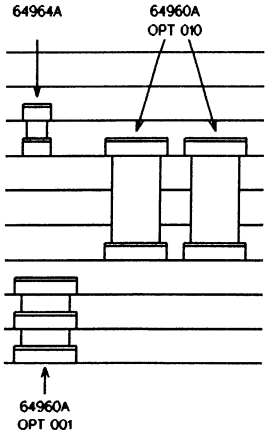
Table 2-2. HP 64340A (80186/88) Configurations, Current Usage, and Cable Options



		(+5 V)
SLOT 9	64310A ANL	5.80 A
8	64340A ACQ	5.00 A
7	64340A CNTL	5.00 A
6	64340A CPU	5.00 A
5	64224A/64225A EC	6.20 A
4	64155A WIDE-ADDR MC	3.80 A
3	64161A 128K BYTE EM	1.60 A
2	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	34.00 A

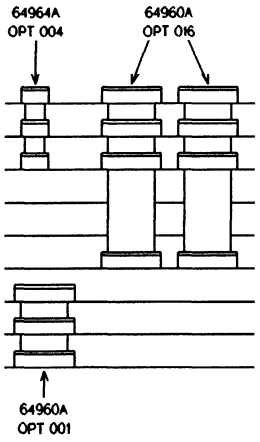


		(+5 V)
SLOT 9	OPT 011 20 CH ACQ	
8	OPT 011 40 CH ACQ	
7	64620S STATE CNTL	10.40 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64224A/64225A EC	6.20 A
2	64155A WIDE-ADDR MC	3.80 A
1	64161A 128K BYTE EM	1.60 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	38.60 A

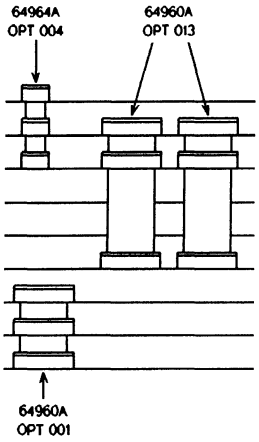


		(+5 V)
SLOT 9	OPT 012 40 CH ACQ	
8	OPT 012 40 CH ACQ	
7	64620S STATE CNTL	12.20 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64224A/64225A EC	6.20 A
2	64155A WIDE-ADDR MC	3.80 A
1	64161A 128K BYTE EM	1.60 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	40.40 A

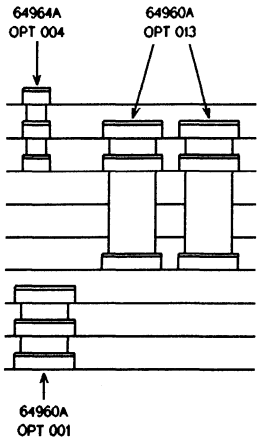
Table 2-2. HP 64340A (80186/88) Configurations, Current Usage, and Cable Options



		(+5 V)
SLOT 9	64302A ANL	3.70 A
8	64310A ANL	5.80 A
7	64340A ACQ	5.00 A
6	64340A CNTL	5.00 A
5	64340A CPU	5.00 A
4	64224A/64225A EC	6.20 A
3	64155A WIDE-ADDR MC	3.80 A
2	64161A 128K BYTE EM	1.60 A
1	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	37.70 A

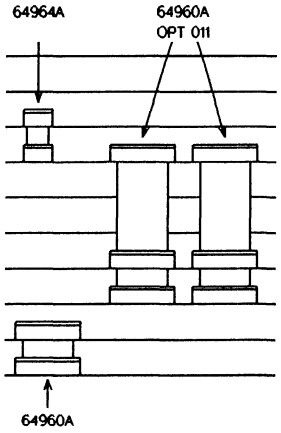


		(+5 V)
SLOT 9	64303A IMB	1.80 A
8	64310A ANL	5.80 A
7	64340A ACQ	5.00 A
6	64340A CNTL	5.00 A
5	64340A CPU	5.00 A
4	64224A/64225A EC	6.20 A
3	64155A WIDE-ADDR MC	3.80 A
2	64161A 128K BYTE EM	1.60 A
1	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	35.80 A

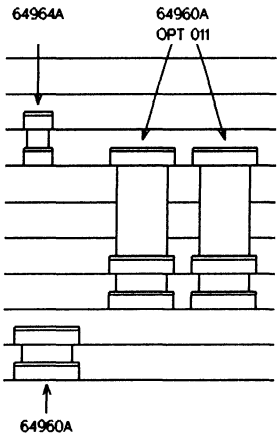


		(+5 V)
SLOT 9	64303A IMB	1.80 A
8	64302A ANL	3.70 A
7	64340A ACQ	5.00 A
6	64340A CNTL	5.00 A
5	64340A CPU	5.00 A
4	64224A/64225A EC	6.20 A
3	64155A WIDE-ADDR MC	3.80 A
2	64161A 128K BYTE EM	1.60 A
1	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	33.70 A

Table 2-2. HP 64340A (80186) Configurations, Current Usage, and Cable Options



		(+5 V)
SLOT 9	OPT 011 20 CH ACQ	
8	OPT 011 40 CH ACQ	
7	64620S STATE CNTL	10.40 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64304A EBPP	1.50 A
2	64224A/64225A EC	6.20 A
1	64155A WIDE-ADDR MC	3.80 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	38.50 A



		(+5 V)
SLOT 9	OPT 012 40 CH ACQ	
8	OPT 012 40 CH ACQ	
7	64620S STATE CNTL	12.20 A
6	64340A ACQ	5.00 A
5	64340A CNTL	5.00 A
4	64340A CPU	5.00 A
3	64304A EBPP	1.50 A
2	64224A/64225A EC	6.20 A
1	64155A WIDE-ADDR MC	3.80 A
0	64161A 128K BYTE EM	1.60 A
	TOTAL CURRENT	40.30 A

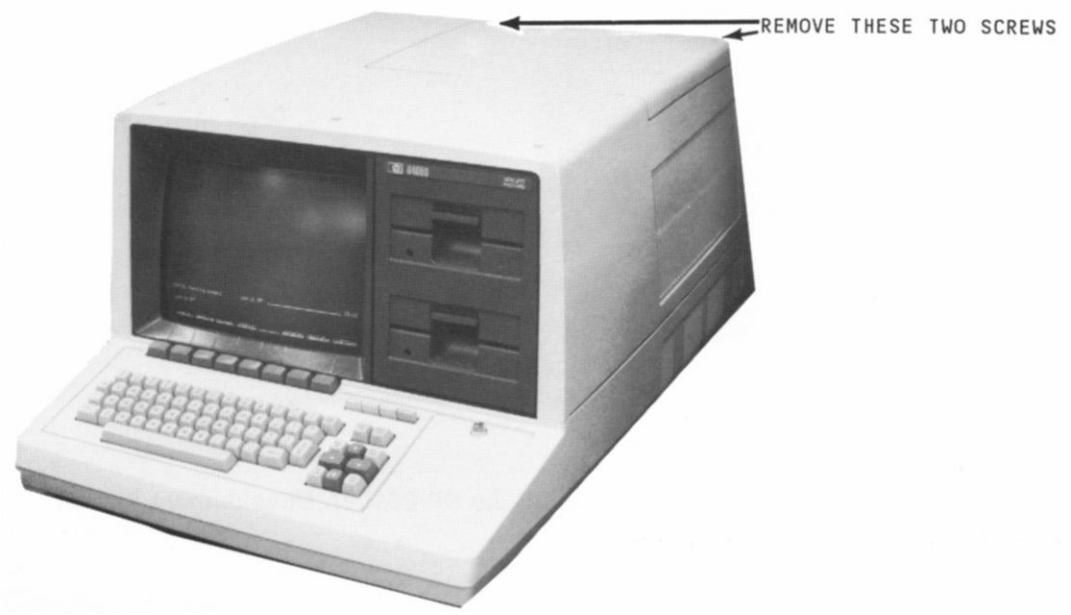


Figure 2-1. HP 64100A Cardcage Cover Removal

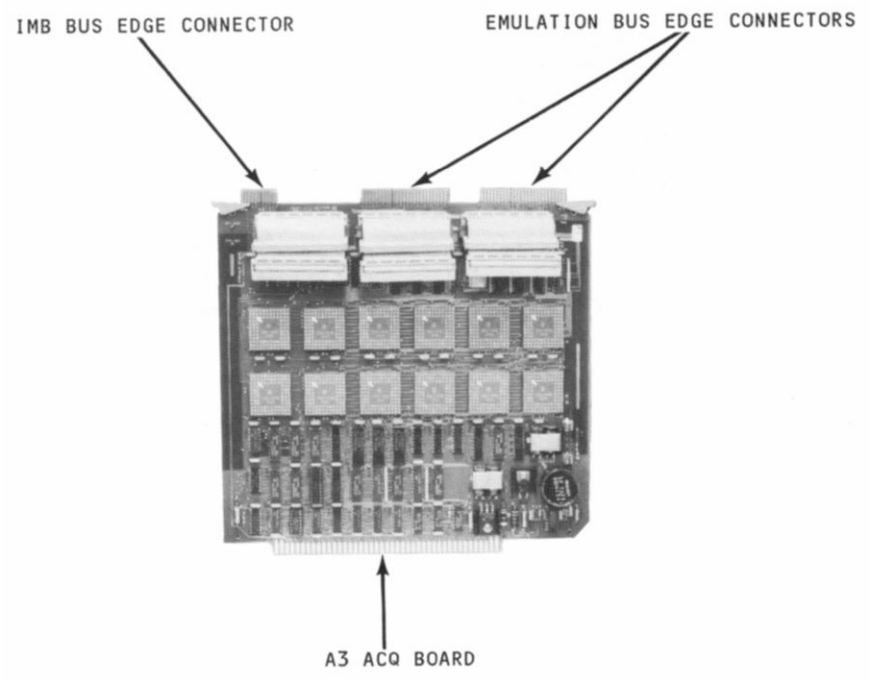


Figure 2-2. Installation of the Inter-connect Cables to the Acquisition board

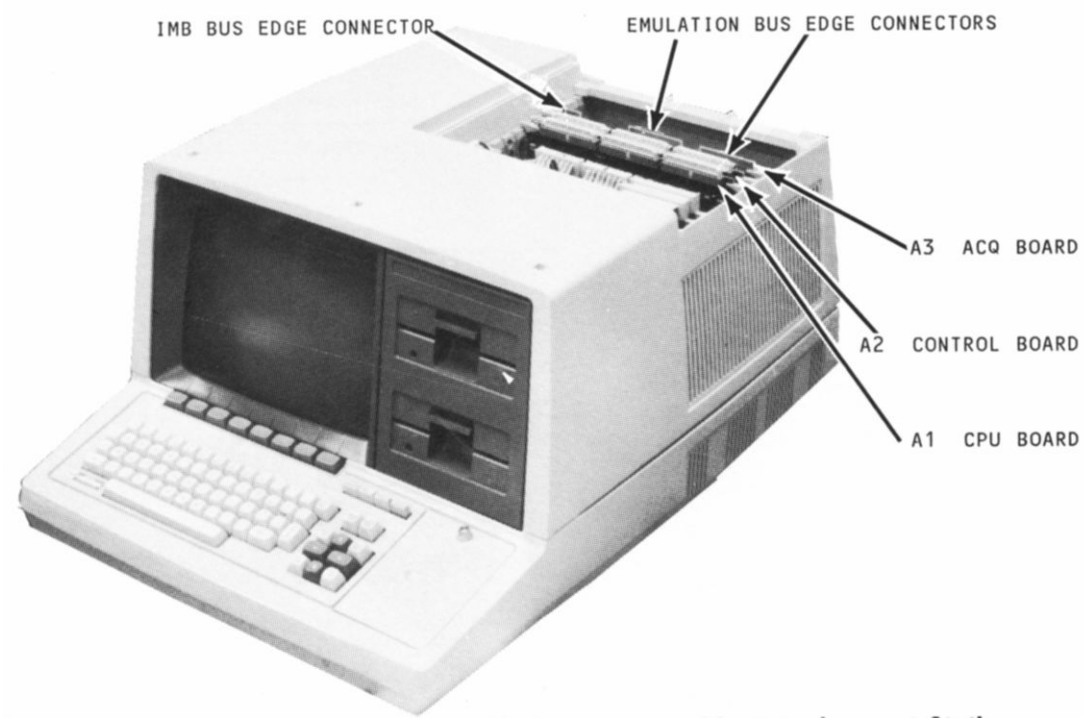


Figure 2-3. Installing the Model 64340A into the HP 64100A Development Station

OPERATING ENVIRONMENT

The Model 64340A may be operated in environments within the following limits:

```
Temperature ..... 0 to +40 C
Humidity ..... 5 to 80% relative humidity at +40 C
Altitude ..... 4 600 meters (15 000 ft)
```

The HP 64340A Software Analyzer should be protected from temperature extremes which cause condensation.

STORAGE AND SHIPMENT

Environment

The Model 64340A may be stored or shipped in environments within the following limits:

```
Temperature ..... -40 to +75 C
Humidity ..... 5 to 80% relative humidity
Altitude ..... 15 000 meters (50 000 ft)
```

Original Packaging

Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard Offices.

Other Packaging

The following general instructions should be used for re-packing with commercially available materials:

a. Wrap each of the HP 64340A Software Analyzer boards in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the HP 64340A Module to provide firm cushioning and prevent movement inside the container.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to insure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

CAUTION

The following precautions should be taken while using Hewlett-Packard Software Analyzer. Damage to the circuitry may result if these precautions are not observed.

POWER DOWN THE SYSTEM UNDER TEST

Turn off power to develoment station before installing the HP 64340A Module into the cardcage. This will avoid circuit damage that may result from voltage transients.

PROTECT AGAINST STATIC DISCHARGE

The three boards of the HP 64340A contain components which are susceptible to damage from static discharge. To avoid damage, take these precautions before handling the HP 64340A Module. Handle boards from the sides ONLY! Never touch the bottom of a HP 64340A board!

Chapter 3
PERFORMANCE VERIFICATION

INTRODUCTION

This chapter describes performance verification (PV) procedures for testing and troubleshooting the HP 64340A Software Analyzer. Performance Verification displays are included with each test description for convenience.

PERFORMANCE VERIFICATION

Performance verification for the HP 64340A Module is a subset of the system Option Test Performance Verification. The system level PV tests all option modules that are located in the development station cardcage.

Procedure To Run Main Test Performance Verification:

To verify that the HP 64340A passes performance verification, perform the following:

a) Press the [---ETC---] softkey until the [opt_test] softkey appears.

b) Press the [opt_test] softkey, followed by the RETURN key.

c) Select one of the three HP 64340A Software Analyzer boards, and type in its card slot position, followed by the RETURN key. NOTE: It makes no difference which board is selected, i.e., the same test will be executed no matter which of the three boards is selected.

d) If IMB stimulus is present in the cardcage, the screen will ask for the IMB stimulus slot number. Type in its slot position, followed by the RETURN key.

NOTE

By selecting the HP 64340A CPU board as the IMB stimulus, the IMB tests will be bypassed.

e) Press the [cycle] softkey to test all three HP 64340A Software Analyzer boards.

f) Press the [end] softkey to stop the test and return to the [opt_test] screen.

g) Press the [end] softkey again to leave performance verification.

If any of the three tests fail, refer to the Troubleshooting Flowchart, table 3-1 in this chapter.

STANDARD OPTION TEST

Option_test softkeys are used to command the execution of performance verification tests in a desired sequence. Pressing a particular softkey will produce the following results:

[end]	} stops the execution of any test and causes the exit of the present module PV testing. The result is a menu of card slot options awaiting a selection for Performance Verification testing.
[cycle]	} causes all tests on the screen to be executed in sequence. All subtests below a listed test are executed.
[next_test]	} causes the enhanced line to move to the next test displayed on the screen.
[start]	} causes the displayed test to be executed. The test will continue to execute until some other displayed softkey is pressed or the [start] softkey is pressed again.
[disp_test]	} will display a list of tests or a single test associated with the test highlighted by inverse video.
[exit_test]	} will stop a test and exit to the previous display.
[print]	} will print the current display to a printer attached to the 64000 station.

THEORY AND TROUBLESHOOTING

Read the Safety Summary at the front of this manual before attempting to service the HP 64340A Software Analyzer.

SOFTWARE ANALYZER SUBSYSTEM DESCRIPTION

The Software Analyzer Subsystem consists of a CPU board, Control board, and the Acquisition board. The system will not operate alone. It must be installed into a HP 64100A and connected to an Emulation Module, or a State/Timing Module.

THEORY OF OPERATION

The block theory will be broken up into four sections. These are:

1) Overall Block Theory
2) CPU Board Block Theory
3) Control Board Block Theory
4) Acquisition Board Block Theory

General Block Description of the HP 64340A Hardware

The HP 64340A hardware is comprised of three option boards; the "CPU board" which is the 64340-66501 board, the "Control board" which is 64340-66502 board, the "Acquisition board" which is the 64340-66503 board. These three boards are interconnected by three ribbon cables. The J2, J3, and J4 edge connectors on top of each of these three boards are connected together by their respective ribbon cable (i.e. J2 on the CPU board, J2 on the Control board, and J2 on the Acquisition board are connected together).

The ID generated from the CPU board is 0104 HEX. This ID is in the range of IDs that have Inter Modular Bus (IMB) capability. The IMB cable connector tab is located on top of the Acquisition board. The IMB drive and receive circuitry is on the Control board. The CPU board only appears to have IMB capability since it communicates with the host processor, the Control board does all the talking over the IMB.

The ID generated from the Control board is 1008 HEX, and the ID generated from the Acquisition board is 1009 HEX. The Control and Acquisition boards have no direct communication with the host processor except for ID generation and LPOP reception by the Control board. The Control and Acquisition boards are controlled by the HP 64340A CPU board.

The order in which the three HP 64340A boards are placed into the 64000 cardcage is important. The Acquisition board has the IMB edge connector located on the upper-left hand corner. It is connected by this IMB edge connector to other Analysis boards which may occupy higher card slot positions. See tables 2-1 and 2-2. The Acquisition board should be placed one card slot higher than the Control board. The Control board should be placed one card slot higher than the CPU board. So, from the least significant card slot number, the order of boards must be: 1) CPU board, 2) Control board, 3) Acquisition board. This does not mean that the HP 64340A CPU board has to be placed in card slot number one. It means it must be placed in the least significant card slot number available depending on which Emulation or other options boards are used. See tables 2-1 and 2-2.

General Block Description of the HP 64340A Hardware (Cont'd)

External Analyzer boards such as the 64300A, 64302A, and 64310A need to be positioned in a greater card slot position than the HP 64340A Software Analyzer subsystem.

Up to two Emulation Analyzers, in addition to the HP 64340A Software Analyzer can be connected to the emulation bus (because of loading restrictions).

The left most of the inter-board cables (connects to J2 on all three HP 64340A boards) transfers buffered versions of the 68000 address and data busses from the HP 64340A CPU board to the other two boards. The center inter-board cable (connects J3 on all three boards) connects five ECL signals. These signals come from IMB edge connector on the Acquisition board and go to the Control board where the IMB interface logic resides. This center inter-board cable also distributes clocks generated by the Control board to the other two boards along with dedicated function signals. The right most inter-board cable connects address and status busses between all three HP 64340A boards.

CPU Board Block Theory

The CPU used on the HP 64340A CPU board is a MC68000R8. This is a 8 Mhz 68000 microprocessor. The clock source is an 8 Mhz TTL oscillator. There are two possible interrupt sources: Delta time, and Host Processor Interrupt. The interrupts are driven by open collector drivers so that emulators can be plugged into the HP 64340A for code development.

The 68000 address bus which is connected to all three HP 64340A boards, is buffered to prevent drive and propagation delay problems. The address bus output enable is controlled by the bus arbitrator with the exception of the upper four bits. When the Host Processor is using the HP 64340A system bus, the address lines are pulled up on the inputs to the buffers forcing the Host Processor to access only the DRAM. The Host Processor is not allowed access to any other hardware at any time.

The 68000 Bus Arbitrator control unit is implemented with a finite state machine. All asynchronous signal inputs are synchronized by the state machine. State changes occur on the next rising edge after the signal has been internally synchronized and recognized.

The DRAM controller chip controls address multiplexing, refresh processing, and RAS/CAS generation. The DRAMs have a 9 bit multiplexed address bus and separate I/O. RAS and CAS are used to clock the row column address into the DRAMs. The DRAMs have a cycle time of 260 nano seconds and an access time of 150 nano seconds.

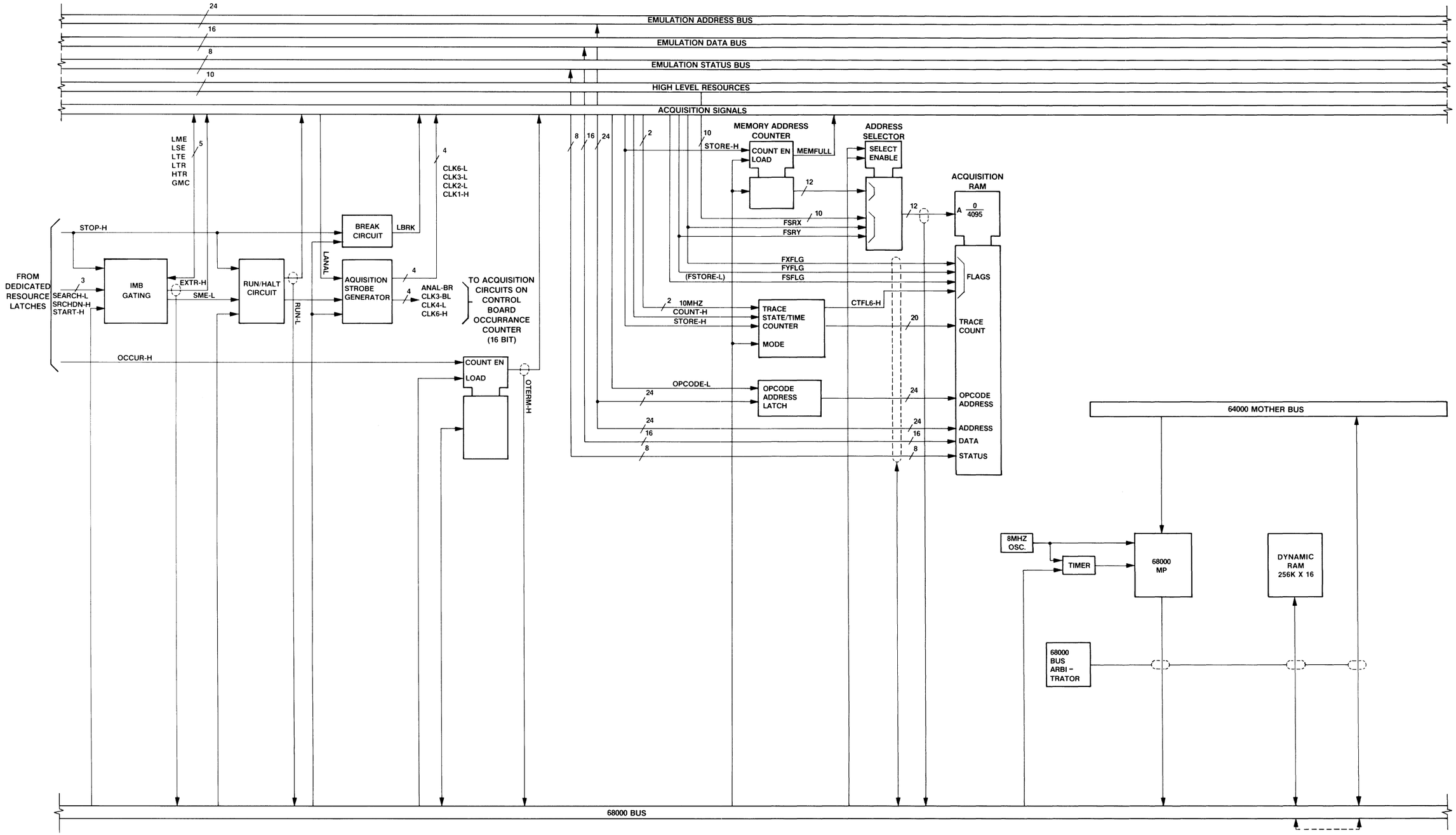


Figure 3-1.
CPU Board Block Diagram

Acquisition Board Block Theory

This section will address the Acquisition Block Theory by briefly describing the overall block diagram of the HP 64340A Acquisition board.

The AME chip compares binary patterns and checks the range it operates within in a 1, 0, X (don't care) fashion on 32 bits of input data. It also has two sets of outputs to provide the same range information on the upper and lower 16 bits of input data.

The Strobe Generator combines two signals to generate the strobes needed to load the address LLRs (Low Level Resources). These signals are buffered to drive the address LLRs and HLRs (High Level Resources).

The Mapper RAMs are used to determine which Counter RAM location to increment based on the address present on the emulation bus. The RUN mode forces the RAMs into a constant read enable state. The Load/Unload mode provides the address and data to the RAMs. The RAMs are mapped directly into the CPU's address space with the only restriction being that they are in the Load/Unload mode.

The Counter Circuitry is responsible for the following: First the counter pointer is latched into the counter pointer register. Then the contents of that RAM location are latched into the previous number latch. That value is then passed to the incrementer which adds 1 to it (except upon overflow). Then the output of the incrementer is loaded back into the RAM at the same location. When the measurement is done, the count values are unloaded by loading the counter pointer register and reading the values from the count data port. The counter RAMs are cleared by writing a zero to the previous number latch, disabling the incrementer, and manually clocking the outputs into all the RAM locations.

The ID generator takes a combination of signals which creates the ID of 1009 HEX for the Acquisition board.

The 10 Mhz Clock is generated from a 20 Mhz clock that is divided by two.

There are only three banks of Recognition Logic on the Acquisition board: 1) Low level data recognition (LLR), 2) Low level address recognition (LLR), 3) High level recognition (HLR). The sample emulation data bus is connected to all the data recognition chips in parallel. The sample emulation address and status bus are connected to all the address recognition chips with the status bus being connected to the most significant bits. This allows the ranging on address with a given status pattern. All of the used outputs of the LLRs, address and data LLRs, are connected to all of the inputs of the HLRs. Any HLR can be programmed to recognize any pattern of inputs corresponding to a desired pattern on the sample emulation bus coupled with a given occurrence count and IMB condition. The outputs of the HLRs are buffered into signals HLR0-9. These signals are used by both the Control board and Acquisition memory.

There are four latches for the address and status busses. The latches are clocked on the rising edge of the analysis clock.

There are three data bus latches. All byte transactions are steered to the lower bus so that they are in a known place to be used later. This prevents the latches from being tied up during other operations. The IMB signals are taken off the IMB tab and transferred directly to the Control board on J3. There is no IMB circuitry on the Acquisition board.

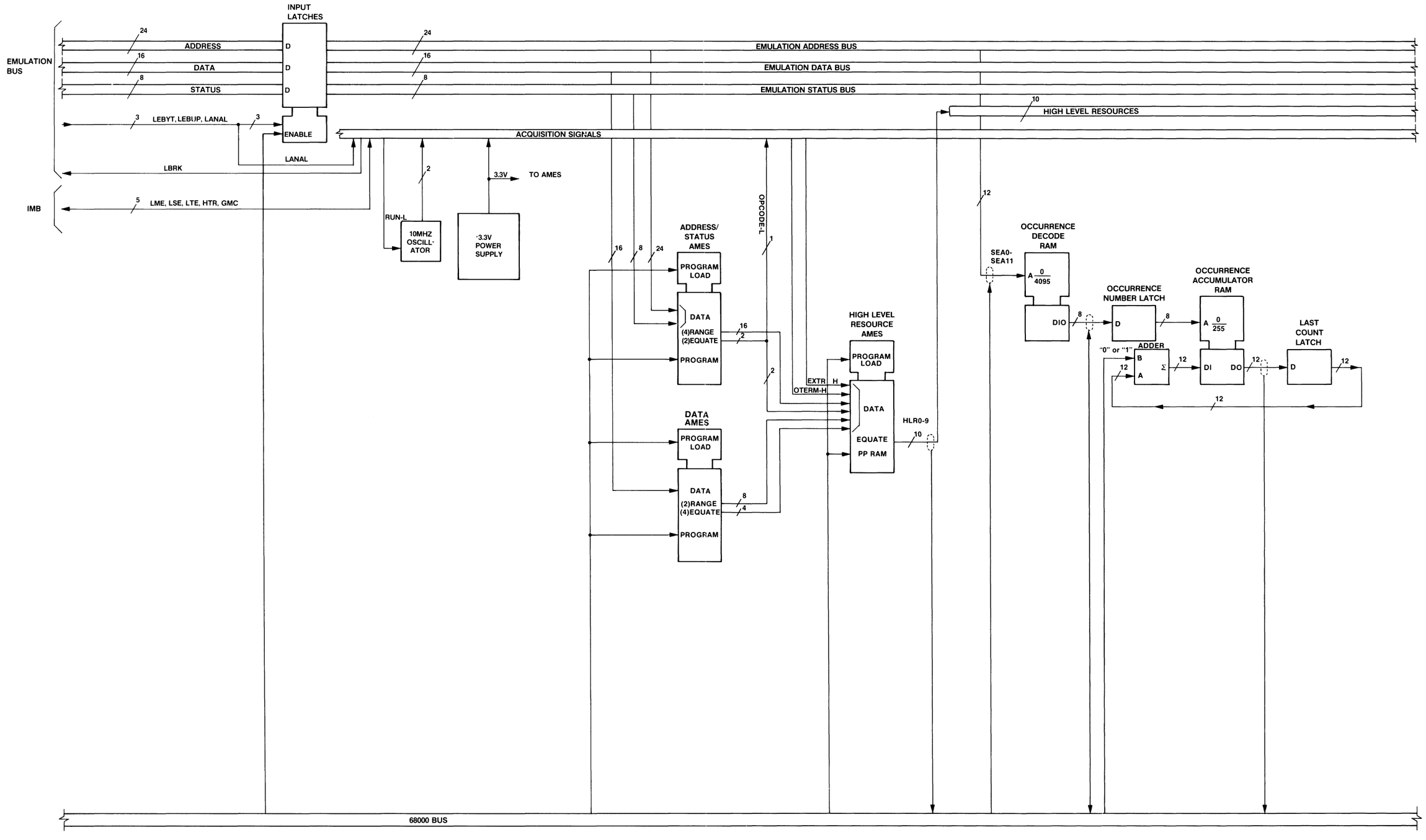


Figure 3-2.
Acquisition Board Block Diagram

Control Board Block Theory

The Timing Generator on the Control board generates the various clocks used by three HP 64340A boards. Five major timing signals are produced. These are: "Clock 1", "Clock 2", "Clock 3", "Clock 4", and "Clock 6". The "Low Analyzer" signal is routed from the Emulation bus connector on the Acquisition board to the Control board via the HP 64340A inter-board bus.

All other clocks generated by the timing generator are done using ECL logic. Signals going in and clocks coming out go thru level translators. There are three adjustable delay generators, each with an adjustable resistor.

TP3 is used as a reference for calibration. The HP 64340A has three "edges" that need to be calibrated with respect to the reference edge. "Clock 3" (TP2) needs both its rising and falling edges calibrated. "Clock 6" (TP1) needs its falling edge calibrated. Adjustable resistor R2 controls the delay between the rising edge on TP3 (the reference), and the falling edge on TP2. Adjustable resistor R3 controls the delay between the falling edge on TP2 and the rising edge on TP2. Adjustable resistor R1 controls the delay between the rising edge of "Clock 2" and the falling edge on TP1.

The "X" and "Y" Function Generators translate general purpose, high level resource from the Acquisition board into special purpose, dedicated functions. The dedicated functions produced are used to control specific parts of the HP 64340A Software Analyzer. For example, the "Store" function determines whether or not the current cycle will be stored in Acquisition memory.

The "X" and "Y" Function Generator has three major parts. These are: the X Generator, the Y Generator, and the Dedicated Functions Generator. Signals from the X and Y Generators are combined by the Dedicated Functions Generator to produce the nine following dedicated functions: Start, Timer Count, Timer Load, Occurrence, Count, Store, Search (and Search Done), and Sequence Start.

The X Generator is made up of a 4K deep by 20-bit mapper RAM, a 12-bit multiplexer which selects what goes on the RAM address bus, and a 4-bit latch in the feedback path. Bus transceivers are used to connect the RAM data bus to the common data bus on the Control board.

The Y Function Generator is similar to the X Function Generator. The differences are the following: the Y Generator RAM is 16 bits wide instead of 20 bits. The Y Generator RAM address multiplexer selects a different set of signals.

The Y Generator RAM takes twelve input signals and performs arbitrary, programmable functions on them producing sixteen output signals. Four of these outputs define the "next state" and the rest go to the Dedicated Functions Generator.

The Dedicated Function Generator combines the sixteen signals from the X Generator, the twelve signals from the Y Generator, and three special purpose signals into nine dedicated functions. Six control signals determine which dedicated function(s), if any, are qualified by the "Start" function. The "Search" function can not be qualified by "Start". The "Timer Count" and "Timer Load" functions share a single control signal for "Start" qualification.

Control Board Block Theory (Cont'd)

The Fast-Sequencer consists of a 4K by 48-bit RAM memory, a 5-bit state register, a 12-bit RAM address multiplexer, a 24-bit adder, a 24-bit operand multiplexer, a 24-bit accumulator register, two AME comparator chips, and a 7-bit hold latch.

The Fast-Sequencer takes the Sampled Emulation Address bus, the Sampled Emulation Status bus, and the "Sequence Start" dedicated function as input. It produces four principal outputs from these inputs. These are the following: "Fast-Sequencer Source X", "Fast-Sequencer Source Y", "Fast-Sequencer Store", and "Fast-Sequencer Stop". The "Fast-Sequencer Source X" goes to the X Generator, the "Fast-Sequencer Source Y" goes to the Y Generator, " Fast-Sequencer Store" and "Fast-Sequencer Stop" go to the Dedicated Function Generator.

The "Fast-Sequencer Source X", "Fast-Sequencer Source Y", and "Fast-Sequencer Store" signals also are sent to the Acquisition memory on the HP 64340A CPU board to be stored as flags.

The Fast-Sequencer RAM address bus is driven by a 12-bit multiplexer. This multiplexer selects between the buffered HP 64340A Address bus, used for loading the RAM, and twelve other signals which are used during measurement.

The AME chip is the "heart" of the Fast-Sequencer circuitry. The 24-bit sum from the adder circuit together with the 8-bit status pattern from the Fast-Sequencer RAM can be loaded into one or both of the AME chips on the Control board. The program port on each AME chip directs the 32-bit pattern to one of four registers within the AME chip.

The 32-bit data ports of both AME chips are connected to the 24-bit Sampled Emulation Status bus.

The AME chips require +3.3 volts to operate. This special supply voltage comes from the Acquisition board over six lines on the three inter-board cables.

The Time/State Timer is a flexible, 24-bit counter that can be programmed for a variety of uses. This Timer can count either a 10 Mhz time clock or a state clock.

The Timer is used in two ways. It can be initialized to 000000 HEX before the measurement, and then simply count an event until the end of the measurement. The second way the Timer is used involves active participation in the measurement. The Timer can alter a sequence, cause a state to be stored, or possibly stop the analyzer.

The Occurrence Counter is a multipurpose counter that does "occurrence" and "time interval" functions. The counter can count up to 65,536 and can interact with measurements. As with the Time/State Timer, the Occurrence Counter can be used to count state events during a measurement.

The HP 64340A can drive all five IMB signals and can receive four IMB signals. The one IMB signal that can not be received is the "GMC" signal (may also be referred to as "PDC").

The IMB comes into the HP 64340A board set on the Acquisition board (upper-left tab). The Acquisition board has no logic pertaining to IMB. It merely routes the IMB signals to the center inter-board connector. The Control board has all the driving and receiving circuitry for the IMB.

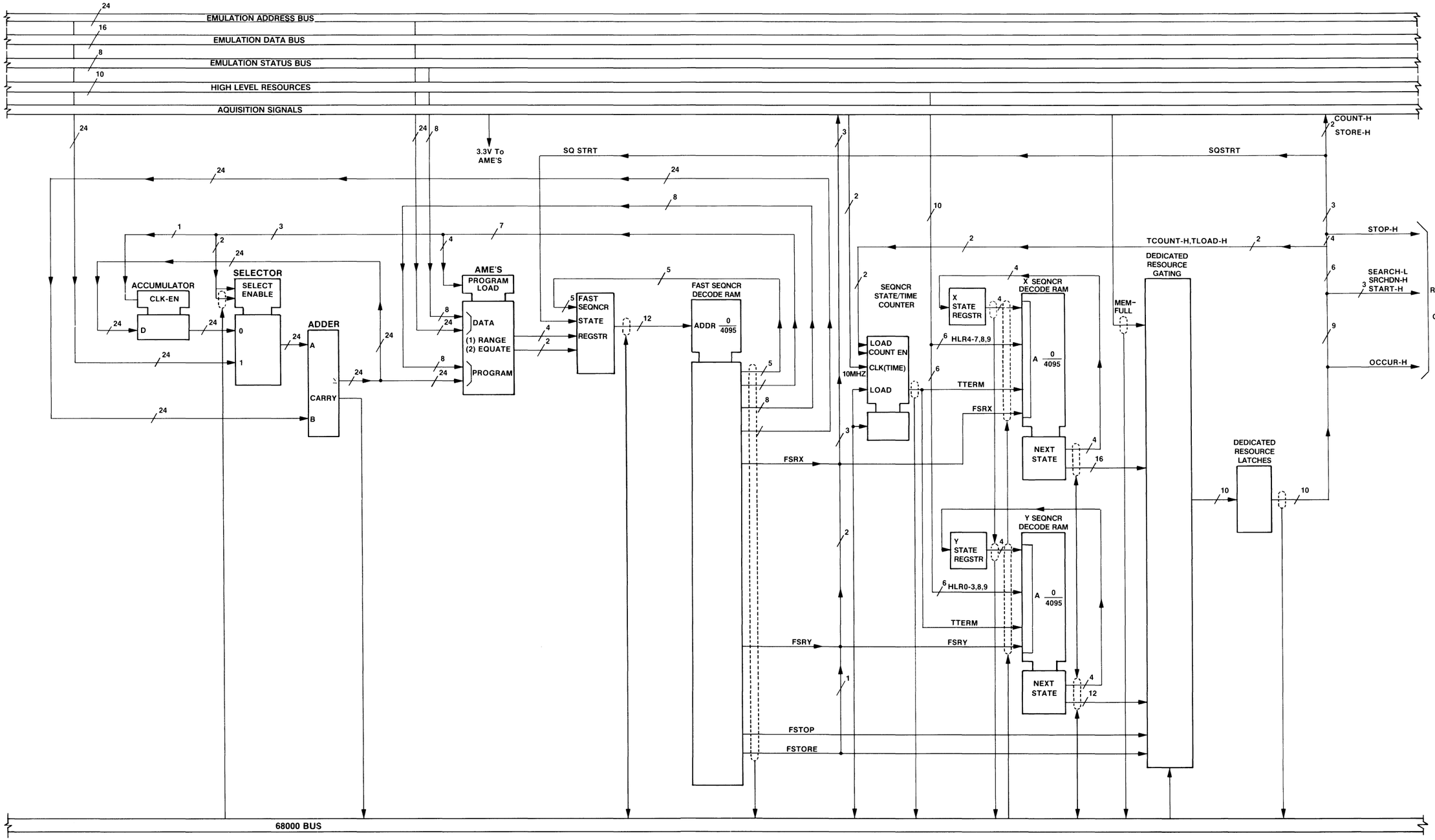


Figure 3-3. Control Board Block Diagram

TROUBLESHOOTING

If a HP 64340A failure is suspected, follow the procedures in the **Troubleshooting Flowchart, table 3-1.** The Troubleshooting Flowchart will aid in isolating the failure to board level. Most of the performance verification tests interact on all three boards. Some failures can not be narrowed down to one board. Always replace the board with highest percentage of failures that occur during performance verification. The following example will give a better understanding to this troubleshooting technique.

EXAMPLE:

The CPU board has 20 tests, the Control board has 19 tests, and the Acquisition board has 6 tests. See figure 3-4.

If the CPU board has 10 failures (out of 20 tests), then 10/20 = .5 x 100 = 50% of its tests failing. If the Control board has 5 failures (out of 19 tests), then 5/19 = .26 x 100 = 26% of its tests failing. If the Acquisition board has 5 failures (out of 6 test), then 5/6 = .83 x 100 = 83% of its tests failing.

In the above example the Acquisition board should be replaced first because 83% of its tests failed. If that does not fix the failure, replace the CPU board next since it had a 50% failure rate. See figure 3-4.

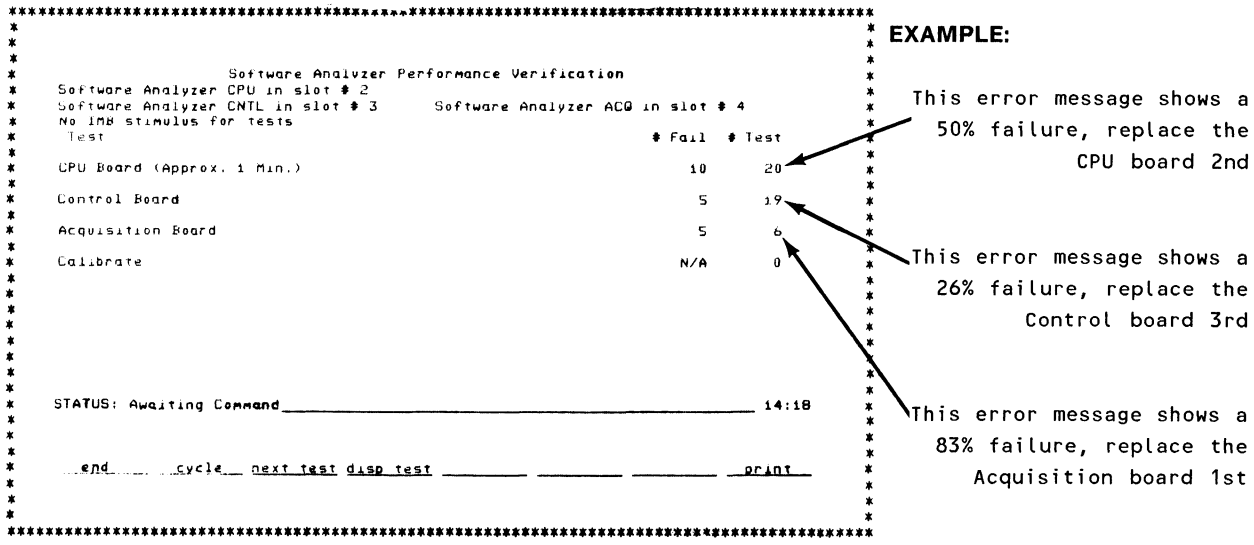


Figure 3-4. Software Analyzer Performance Verification (main test)

NOTE

Always suspect cable and board connections. Reseat all HP 64340A boards/cables before running performance verification.

TROUBLESHOOTING HINTS

a) Power the development station OFF. Reseat option cards to ensure proper contact to the Motherboard edge connectors. Power development station ON.

b) Make sure the inter-connect cables are firmly attached to J2, J3, and J4 of each of the three HP 64340A boards.

c) Power development station OFF. Move the HP 64340A three board set into different option slots to avoid slot-dependent-failures. Power development station ON.

Procedure to Run the HP 64340A Software Analyzer Performance Verification:

a) Press the [---ETC---] softkey until the [opt _test] softkey is displayed.

b) Press the [opt_test] softkey, then the RETURN key.

c) Type in the cardcage slot number where the Software Analyzer CPU, CNTL, or ACQ board resides, then press the RETURN key.

d) If there are any IMB stimulus boards in the cardcage, the screen will display the message "Select IMB stimulus for test:". Select and type in the IMB stimulus slot number where it resides in the cardcage, then press the RETURN key.

NOTE

By selecting the HP 64340A CPU board for the IMB stimulus, the IMB tests in performance verification will be bypassed.

e) Press the [cycle] softkey.

f) To stop the test, press the [cycle] softkey again.

g) If a failure occurs remove all option boards except for the HP 64340A Module from the development station cardcage.

h) To exit test, press the [end] softkey.

Procedure to Run the External IMB Performance Verification Test:

a) Press the [---ETC---] softkey until the [opt _test] softkey is displayed.

b) Press the [opt_test] softkey, then the RETURN key.

Procedure to Run the External IMB Performance Verification Test (Cont'd):

c) Type in the cardcage slot number where the Software Analyzer CPU, Acquisition, or the Control board resides, then press the RETURN key.

d) Type in the cardcage slot number where the IMB Stimulus resides, then press the RETURN key.

e) Press the [next_test] softkey once so that the "Control Board" test is highlighted.

f) Press the [disp_test] softkey.

g) Press the [next_test] softkey four times so that the "IMB Interface" test is highlighted.

h) Press the [disp_test] softkey.

i) Press the [next_test] softkey until the "External Stimulus" test is highlighted.

j) Press the [disp_test] softkey.

k) Press the [start] softkey to activate test.

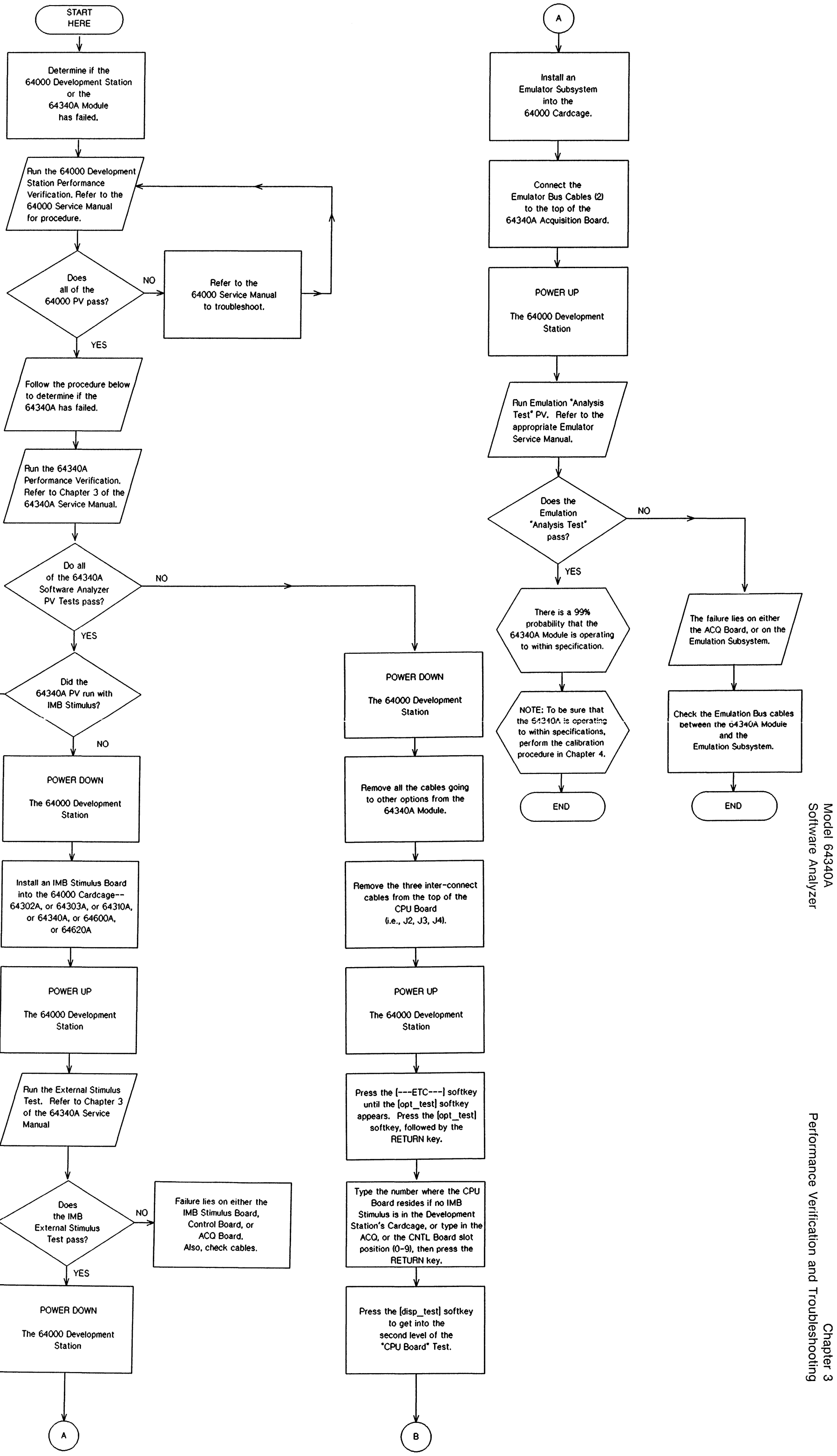


Table 3-1. Bluestripe Troubleshooting Flowchart

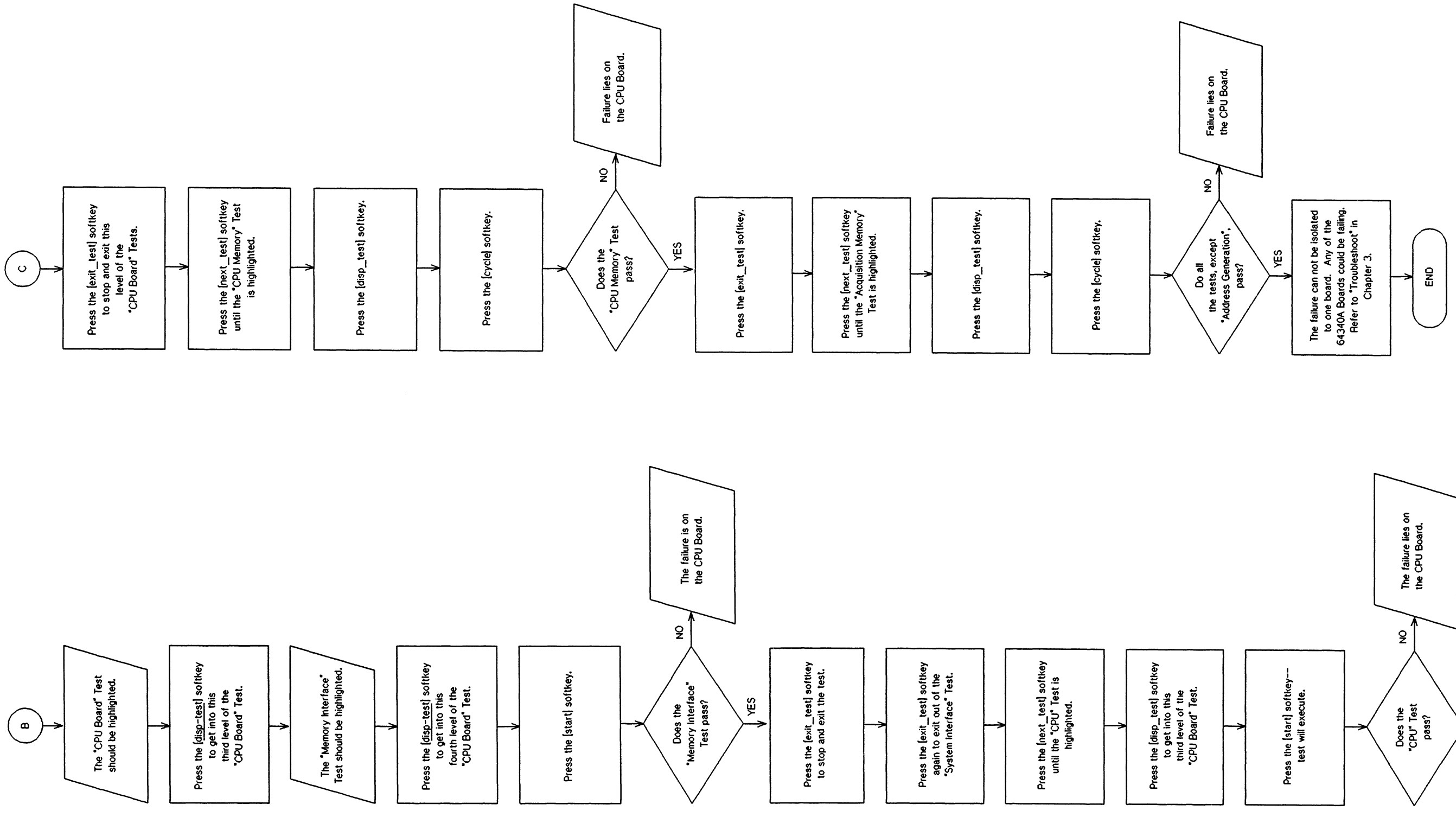


Table 3-1.
Bluestripe Troubleshooting Flowchart (Cont'd)

PERFORMANCE VERIFICATION TEST DISPLAYS

There are three choices to choose from to enter into the second level of HP 64340A Performance Verification. These are: the CPU Board test, the Control Board test, and the Acquisition Board test. Each of the first level tests will bring the system into the same second level of tests. Select one:

Some of the lower level tests will not be pictured in this manual because they are for factory use only. The performance verification test screens shown on the following pages track the **Troubleshooting Flowchart** procedures in **table 3-1.**

```
                    Software Analyzer Performance Verification
Software Analyzer CPU in slot # 3
Software Analyzer CNTL in slot # 4      Software Analyzer ACQ in slot # 5
No IMB stimulus for tests
 Test                                                    # Fail   # Test

CPU Board (Approx. 1 Min.)                                  0        0

Control Board                                               0        0

Acquisition Board                                           0        0

Calibrate                                                 N/A        0




STATUS: Awaiting Command_____________________________________________ 14:18


   end    cycle   next test disp test  ________  ________  ________   print
```

Figure 3-5. Software Analyzer Performance Verification (first level)

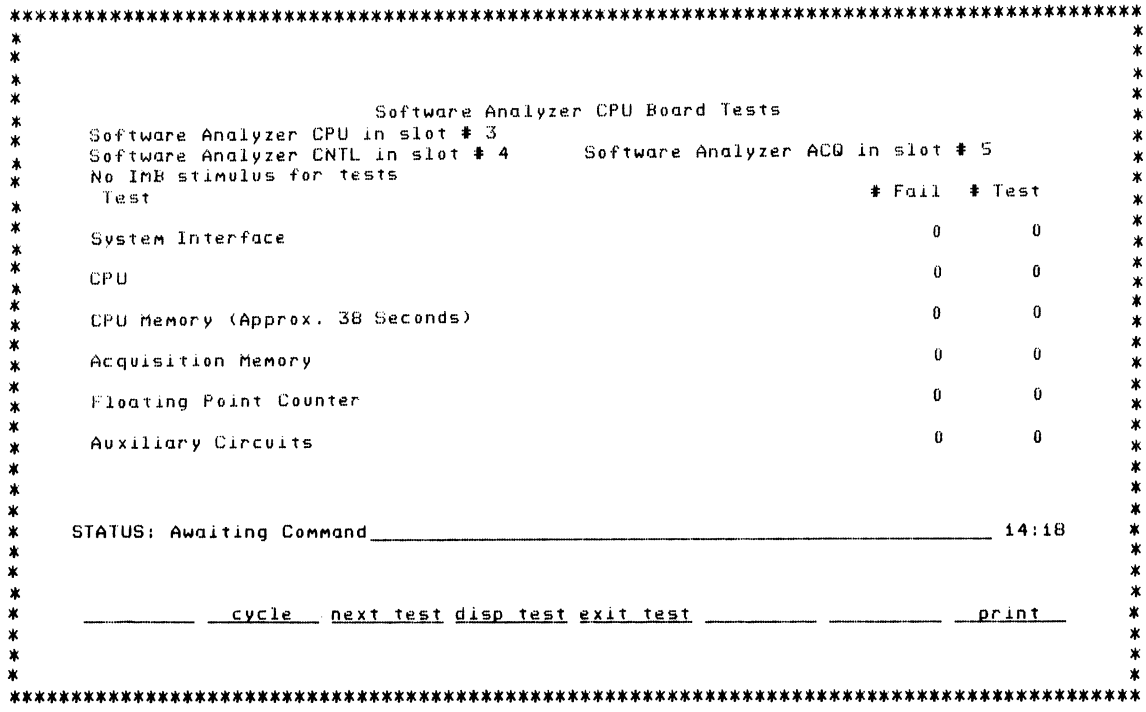


Figure 3-6. Software Analyzer CPU Board Tests (second level)

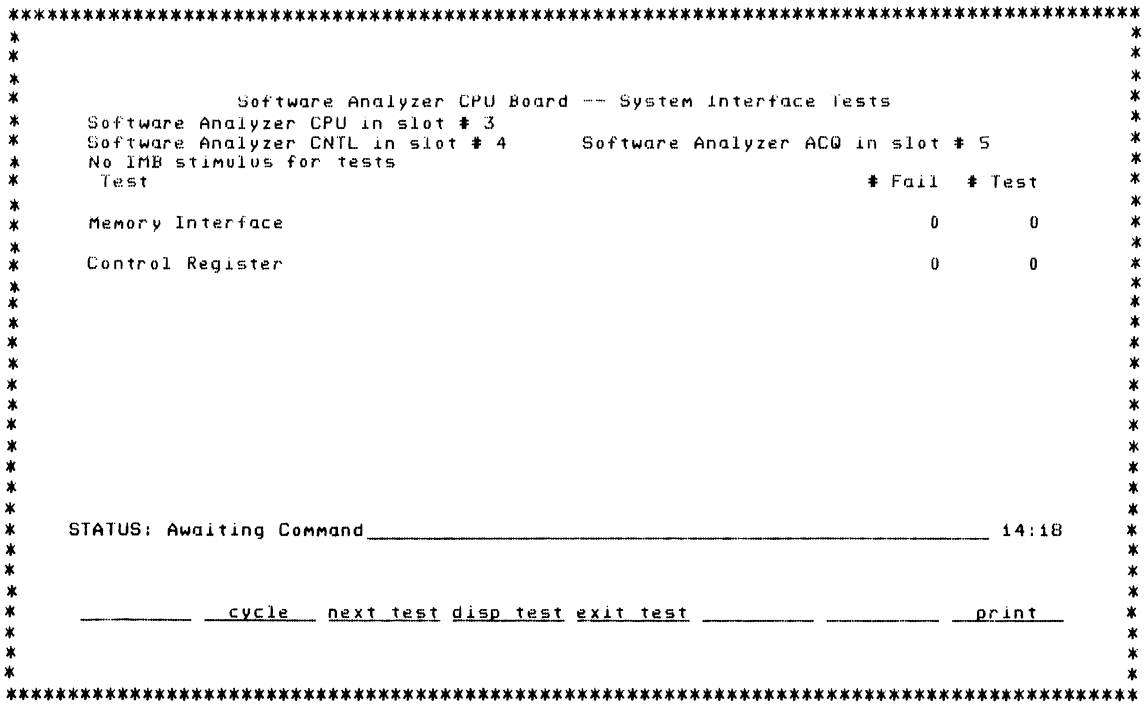


Figure 3-7. CPU Board - System Interface Tests (third level)

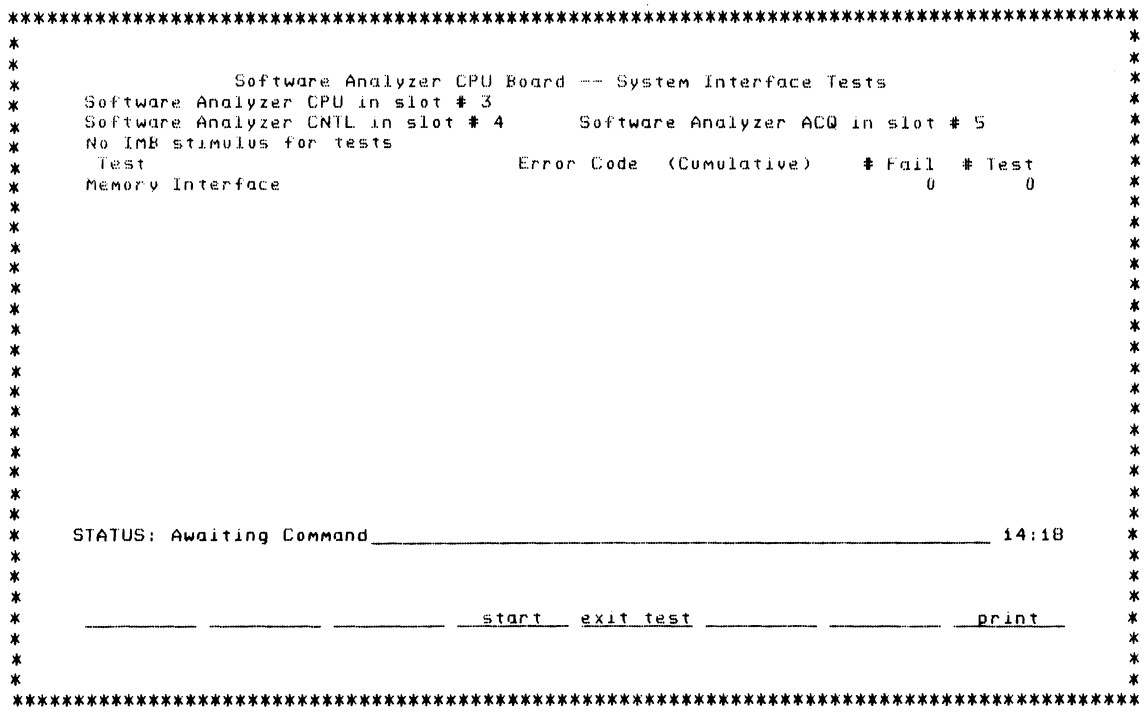


Figure 3-8. CPU Board - Memory Interface Tests (fourth level)

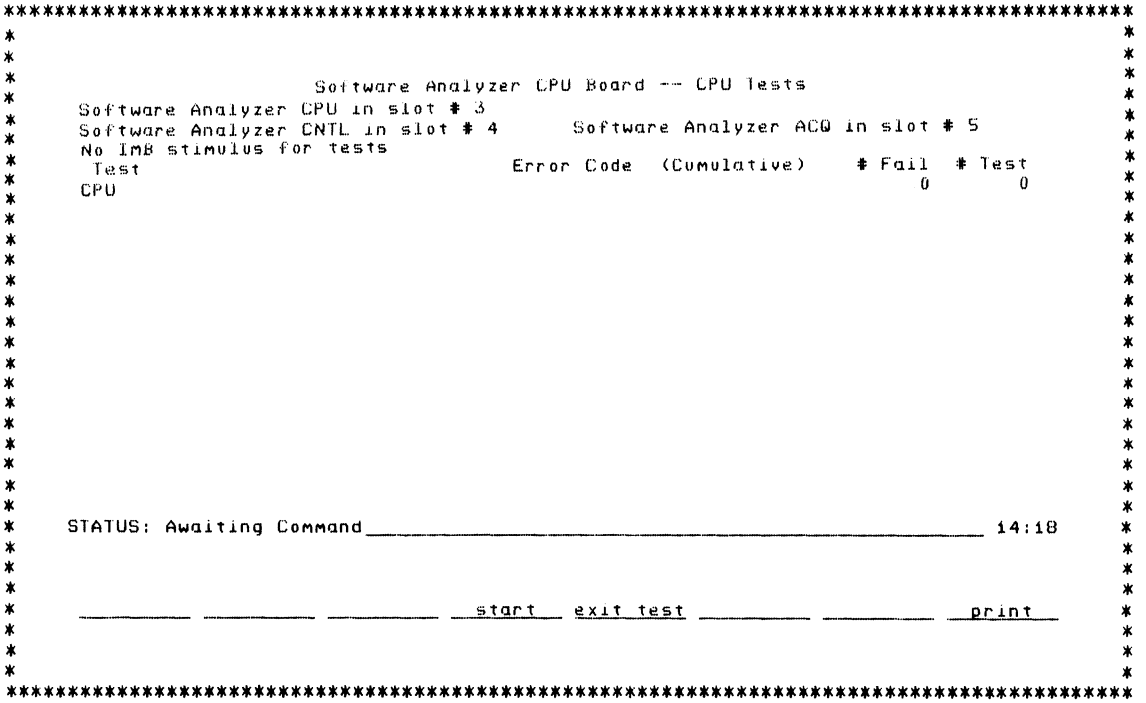


Figure 3-9. CPU Board - CPU Tests (third level)

```
Software Analyzer CPU Board -- CPU Memory Tests
Software Analyzer CPU in slot # 3
Software Analyzer CNTL in slot # 4      Software Analyzer ACQ in slot # 5
No IMB stimulus for tests
 Test                                Error Code  (Cumulative)    # Fail  # Test
CPU Memory

        [0 - 16k] (approx. 3 sec.)                                    0       0


        [16k - 256k] (approx. 35 sec.)                                0       0


STATUS: Awaiting Command                                                      14:18

 _________ __cycle__ next test __start__ exit test _________ _________ __print__
```

Figure 3-10. CPU Board - CPU Memory Tests (third level)

```
Software Analyzer CPU Board -- Acquisition Memory Tests
Software Analyzer CPU in slot # 3
Software Analyzer CNTL in slot # 4      Software Analyzer ACQ in slot # 5
No IMB stimulus for tests
 Test                                                        # Fail  # Test

Address Generation                                             0       0

Control                                                        0       0

Data RAM                                                       0       0
Address RAM                                                    0       0
Status/Address RAM                                             0       0

Opcode RAM                                                     0       0
Flag/Count/Opcode RAM                                          0       0
Count RAM                                                      0       0


STATUS: Awaiting Command                                                      14:18


 _________ __cycle__ next test disp test exit test _________ _________ __print__
```

Figure 3-11. CPU Board - Acquisition Memory Tests (third level)

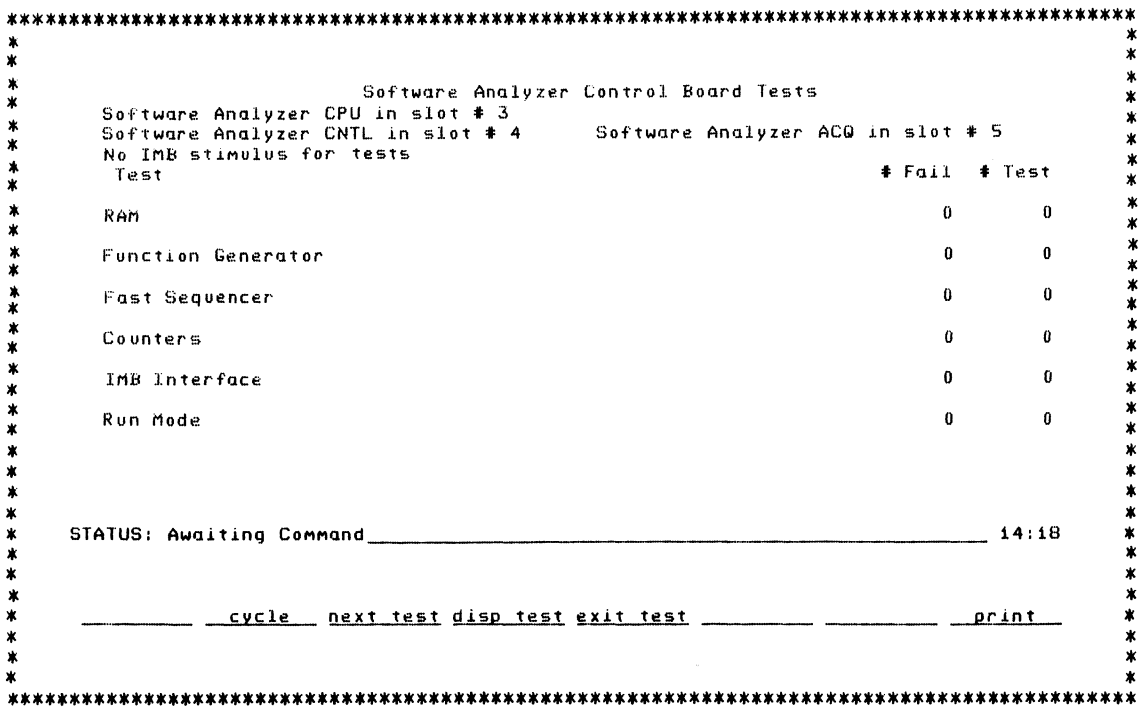


Figure 3-12. Control Board - Control Board Tests (second level)

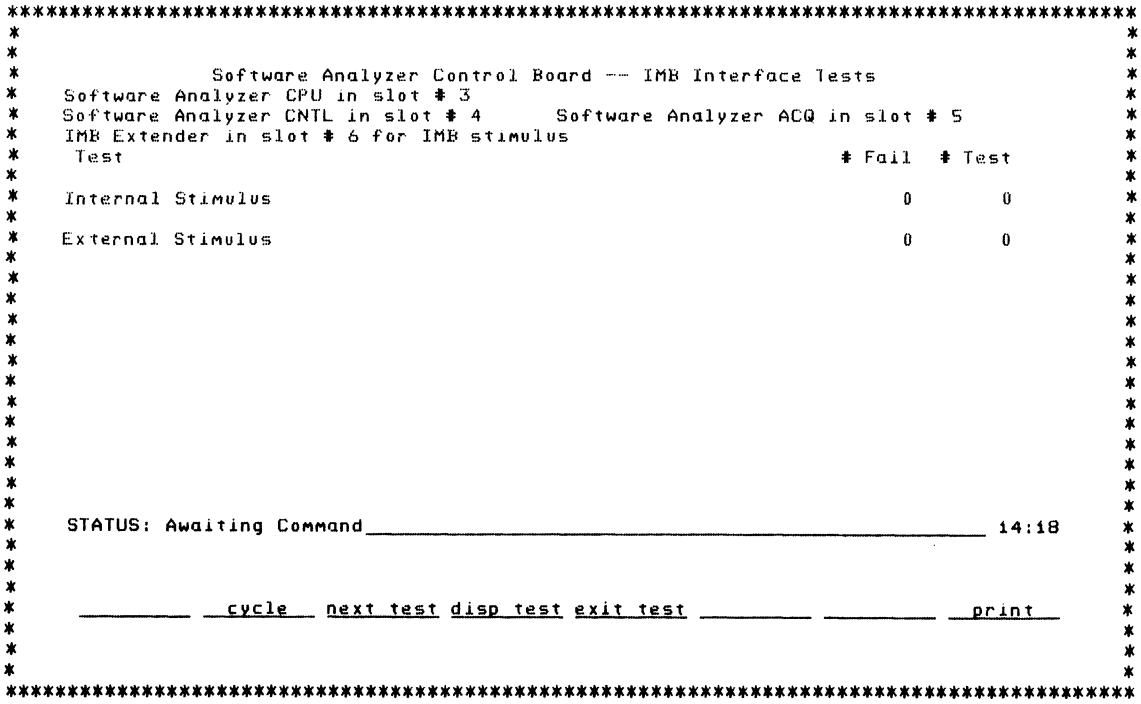


Figure 3-13. Control Board - IMB Interface Tests (third level)

```
Software Analyzer Control Board -- IMB Interface Tests
Software Analyzer CPU in slot # 3
Software Analyzer CNTL in slot # 4      Software Analyzer ACQ in slot # 5
Wide Emul. Analysis in slot # 6 for IMB stimulus
 Test                              Error Code  (Cumulative)     # Fail  # Test
External Stimulus                                                  0       0
        Drive Master Enable (LME)          0          (0)
        Drive Trigger Enable (LTE)         0          (0)
        Drive Storage Enable (LSE)      --UNABLE TO TEST--
        Drive Trigger (HTR)                0          (0)
        Drive Gated Master Clock (GMC)  --UNABLE TO TEST--

        Receive Master Enable (LME)        0          (0)
        Receive Trigger Enable (LTE)       0          (0)
        Receive Storage Enable (LSE)    --UNABLE TO TEST--
        Receive Trigger (HTR)              0          (0)

STATUS: Awaiting Command_____________________________________________ 14:18

 _________ _________ _________ __start__ _exit test_ _________ _________ __print__
```

Figure 3-14. Control Board - External Stimulus Test (fourth level)

```
Software Analyzer Performance Verification
No Software Analyzer CPU for tests
Software Analyzer CNTL in slot # 7      Software Analyzer ACQ in slot # 8
IMB Extender in slot # 9 for IMB stimulus


Unable to execute Performance Verification:

    Software Analyzer CPU card not present

STATUS: Awaiting Command_____________________________________________ 14:18

 ___end___ _________ _________ __start__ _________ _________ _________ __print__
```

Figure 3-15. CPU Board Missing Message

```
                    Software Analyzer Performance Verification
    Software Analyzer CPU in slot # 6
    No Software Analyzer CNTL for tests     No Software Analyzer ACQ for tests
    No IMB stimulus for tests
     Test                                                    # Fail   # Test

    CPU Board (Some Tests Not Cycled Thru)                        0        0

    Control Board                                                 0        0

    Acquisition Board                                             0        0

    Calibrate                                                   N/A      N/A

    STATUS: Awaiting Command                                                14:18

     _________ _________ _________ __start__ _exit test_ _________ _________ __print__
```

Figure 3-16. Incomplete Set of Cards Message

```
                    68000 Emulation System Performance Verification

  General Purpose Controller with 68000 pod in card slot # 8
     Test                                Error Code  (Cumulative)    # Fail   # Test
    Analysis Stimulus                                                    0        0

    STATUS: Awaiting Command                                                14:18

     _________ _________ _________ __start__ _exit test_ _________ _________ __print__
```

Figure 3-17. Emulation Analysis Screen - Test Can Be Executed

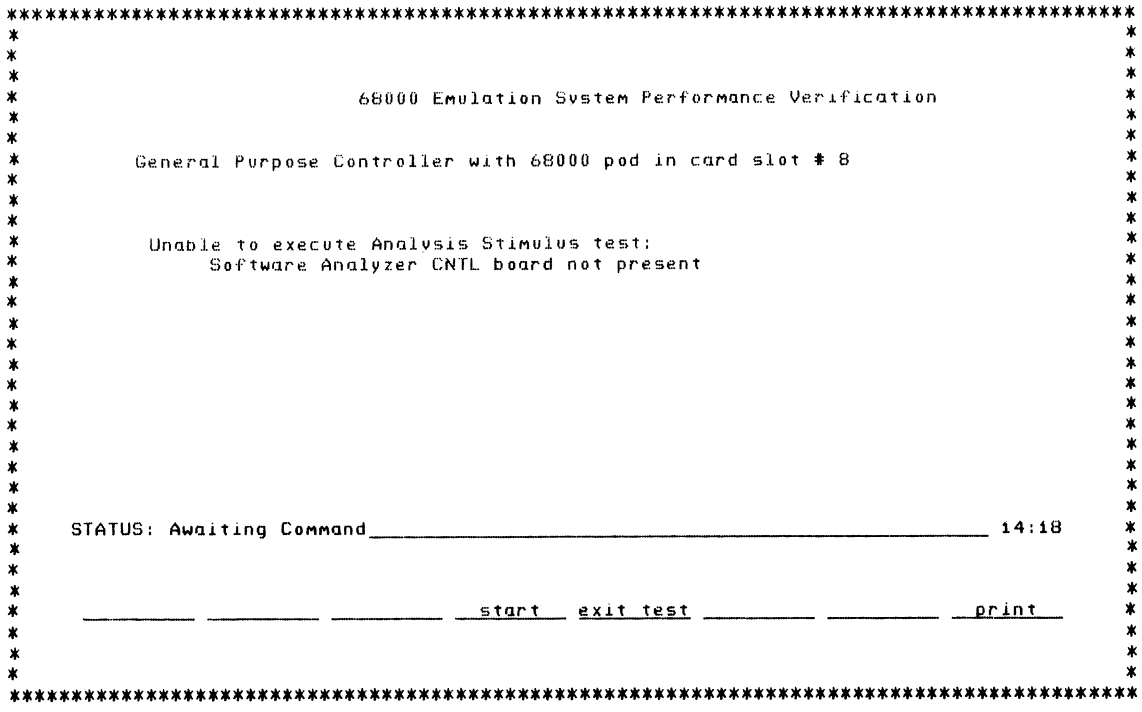


Figure 3-18. Emulation Analysis Screen - No Control Board

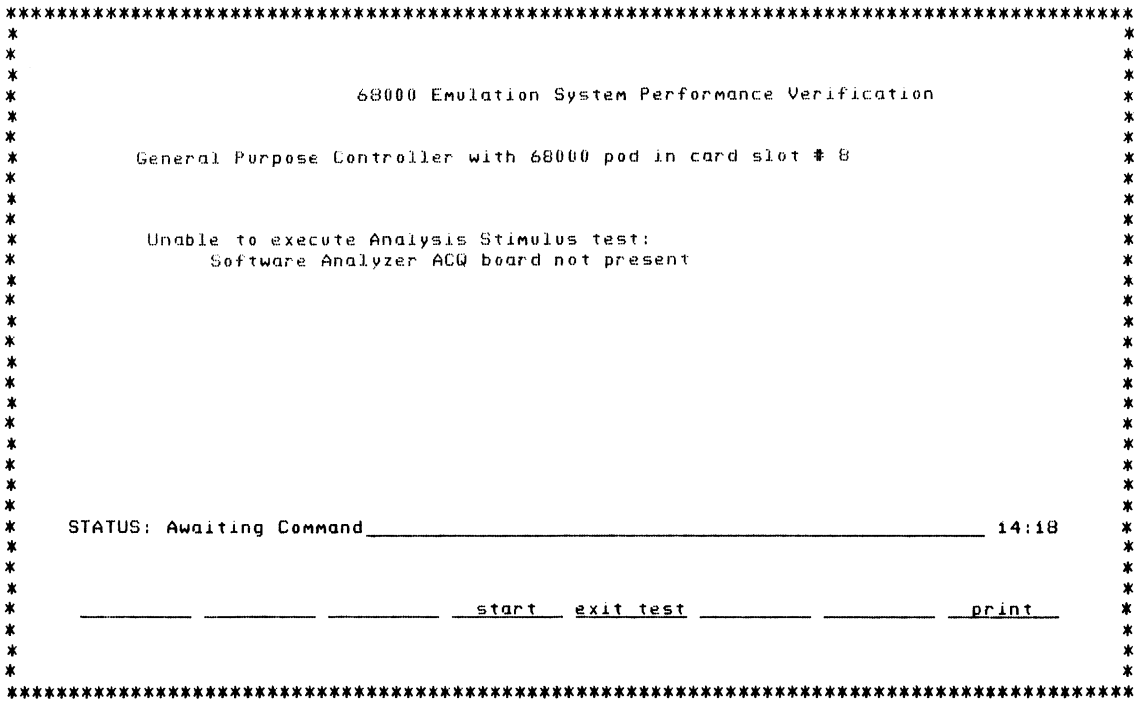


Figure 3-19. Emulation Analysis Screen - No ACQ Board

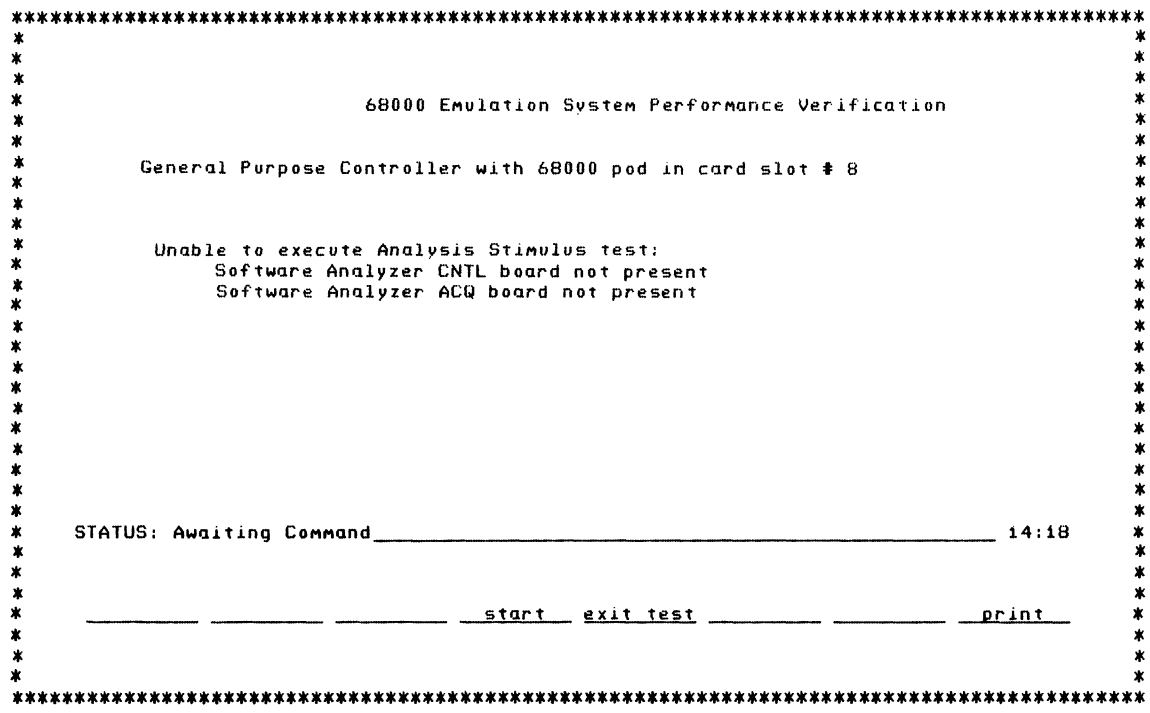


Figure 3-20. Emulation Analysis Screen - No Control and ACQ Boards

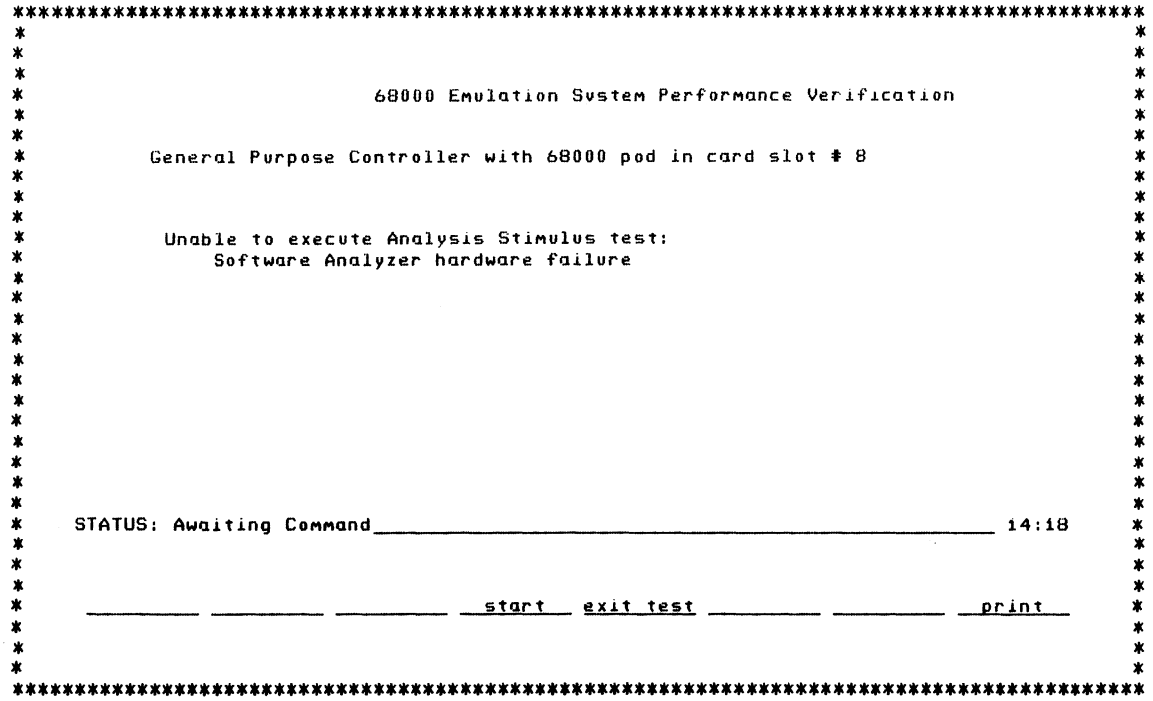


figure 3-21. CPU Fails Handshake

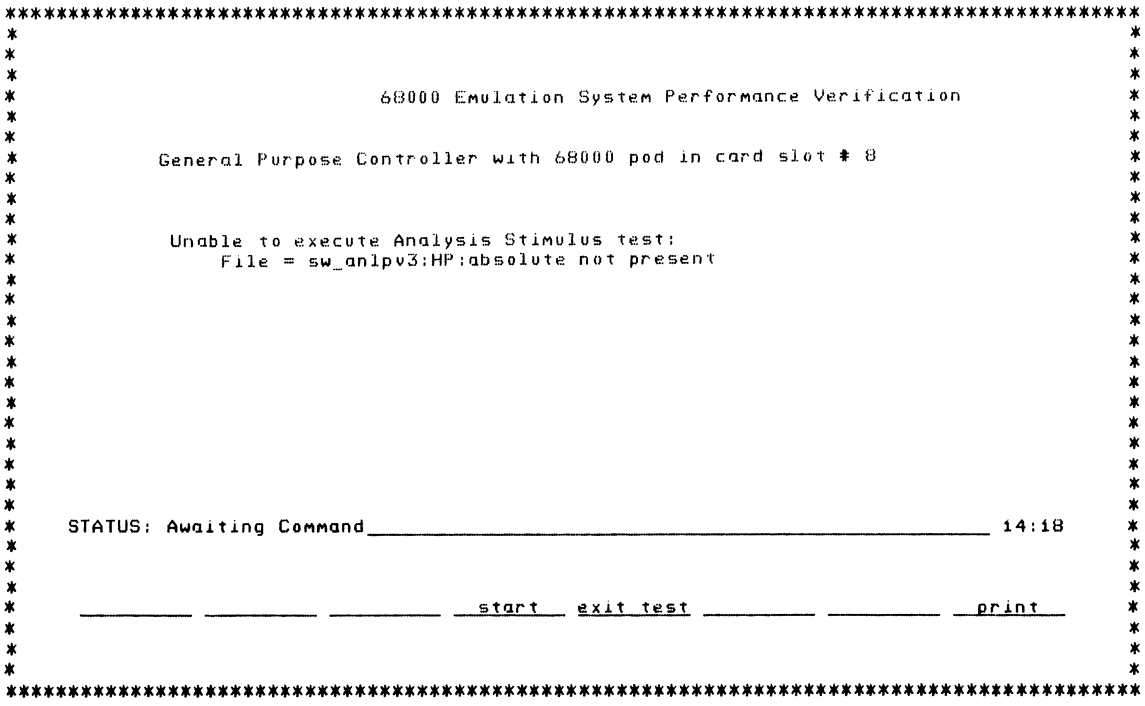


Figure 3-22. File Containing 68000 Stimulus Code Missing

NOTES

Chapter 4
ADJUSTMENTS

INTRODUCTION

This chapter describes the adjustment required to return the instrument to within operating specifications. Periodical maintenance is required on the 64340-66502 Control board after approximately one year of use. Follow the calibration procedures outlined in this section to make the adjustments necessary to bring the Control board clock signals to within specifications.

SAFETY REQUIREMENTS

Read the Safety Summary at the front of this manual before attempting any adjustments on the HP 64340A Software Analyzer. Failure to observe these safety procedures could result in personal injury or damage to the instrument. **Any adjustments required should be performed only by qualified personnel.**

EQUIPMENT REQUIRED

The following test equipment is required to perform the calibration procedure on the 64340-66502 Control board:

HP 64100A Logic Development Station
HP 64340A Software Analyzer (3 board set)
1726A Oscilloscope (275MHz)
10017A Scope probe (Qty 2)
64110-66503 Extender board (3)

CALIBRATION PROCEDURE

a) Install the HP 64340A boards into the 64000 Logic Development Station. All three boards must be installed on extender boards. The Control board (64340-66502) must placed in front of the other two boards to perform the procedure. The CPU board (64340-66501) should be placed in the middle, and the Acquisition board (64340-66503) should be placed in the rear of the cardcage. Power on the HP 64100A.

b) Turn ON HP 64100A Logic Development Station and allow HP 64340A Module to warm up for 5 minutes.

c) Press the [---ETC---] softkey until the [opt_test] softkey appears.

d) Press the [opt_test] softkey, then the RETURN key.

e) Type in the slot number where any one of the three HP 64340A boards resides in the cardcage, then press the RETURN key.

f) If IMB stimulus is present, type in an IMB stimulus slot number where the board resides in the cardcage.

NOTE

The HP 64340A CPU board can be selected as the IMB stimulus, but this will disable the IMB tests. During calibration the IMB tests are not used.

g) Press the [next_test] softkey until the "Calibrate" test is highlighted.

h) Press the [start] softkey to activate the test.

i) Connect the scope to the Control board as follows;

Channel A : TP3 .1V/div **Main sweep : .05 usec/div**

Channel B : TP2 .1V/div **Delayed sweep : .02 usec/div**

Vert Display : ALT

Trigger : Ch A

polarity : " - "

j) Set both channels to GND. Adjust the "position control" so that the traces are 1.3 divisions below the center line of the display on the oscilloscope.

NOTE

All procedures take place on the 64340-66502 Control board.

k) Adjust R2 for 135 +/- 0.5 ns delay between the rising edge of TP3 and the falling edge of TP2. Use the 1.3 volt crossing to make the measurement. See figure 4-1.

l) Adjust R3 for 180 +/- 0.5 ns delay between the rising edge of TP3 and the rising edge of TP2. Make the measurement at the 1.3 volt crossing of the waveform. See figure 4-1.

m) Connect the scope probe channel B to TP1.

n) Adjust R1 for 225 +/- 1 ns delay between the rising edge of TP3 and the falling edge of TP1. Make the measurement at the 1.3 volt crossing of the waveform. See figure 4-1.

NOTE

Recheck the above measurements to insure that all still meet the specifications since the R3 and R1 adjustments interact with the R2 adjustment.

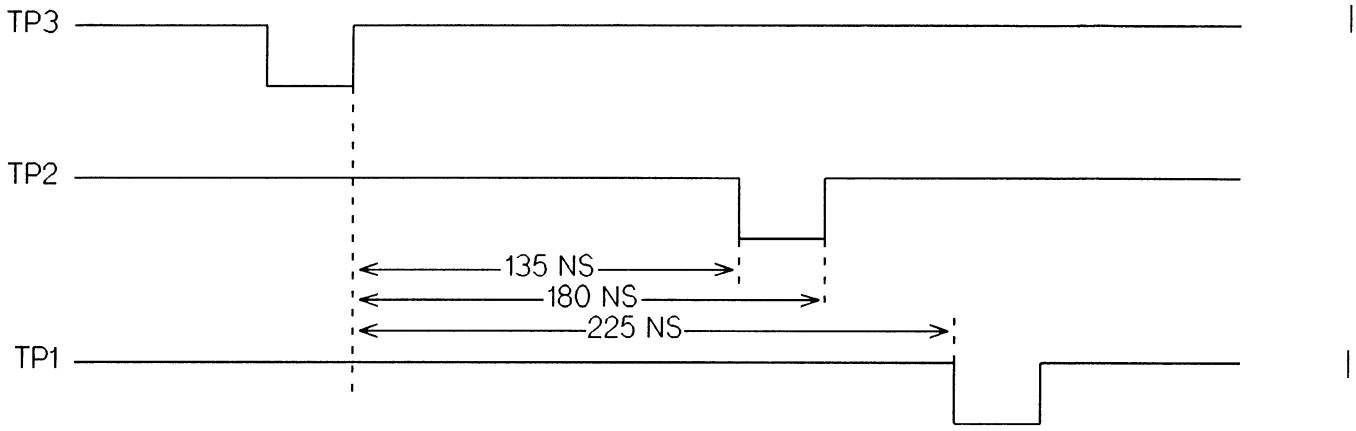


Figure 4-1. Calibration Timing Relationship

NOTES

Chapter 5
REPLACEABLE PARTS

INTRODUCTION

This section contains information for ordering parts for the Software Data Analyzer. Table 6-1 lists parts that may be ordered directly for the Model 64340A. Table 5-2 lists abbreviations that may be used throughout the manual.

REPLACEABLE PARTS

Table 5-1 shows part numbers for replaceable parts for the Model 64340A Software Analyzer.

Table 5-1. Replaceable Parts

Reference Designator	CD	Qty	Description	Part Number
A1	5	1	CPU BOARD ASSEMBLY	64340-69501
A2	6	1	CNTL BOARD ASSEMBLY	64340-69502
A3	7	1	ACQ BOARD ASSEMBLY	64340-69503
W1	6	3	INTER-CONNECT CABLE	64340-61601
H1	0	3	64340A PC EXTRACTOR	64340-85001
H2	1	1	CPU BD EXTRACTOR	64340-85002
H3	2	1	CNTL BD EXTRACTOR	64340-85003
H4	3	1	ACQ BD EXTRACTOR	64340-85004

ABBREVIATIONS

Table 5-2 lists abbreviations that may be used in this manual. The designators and abbreviations are presented in upper cased letters and their definitions are lower cased.

Table 5-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

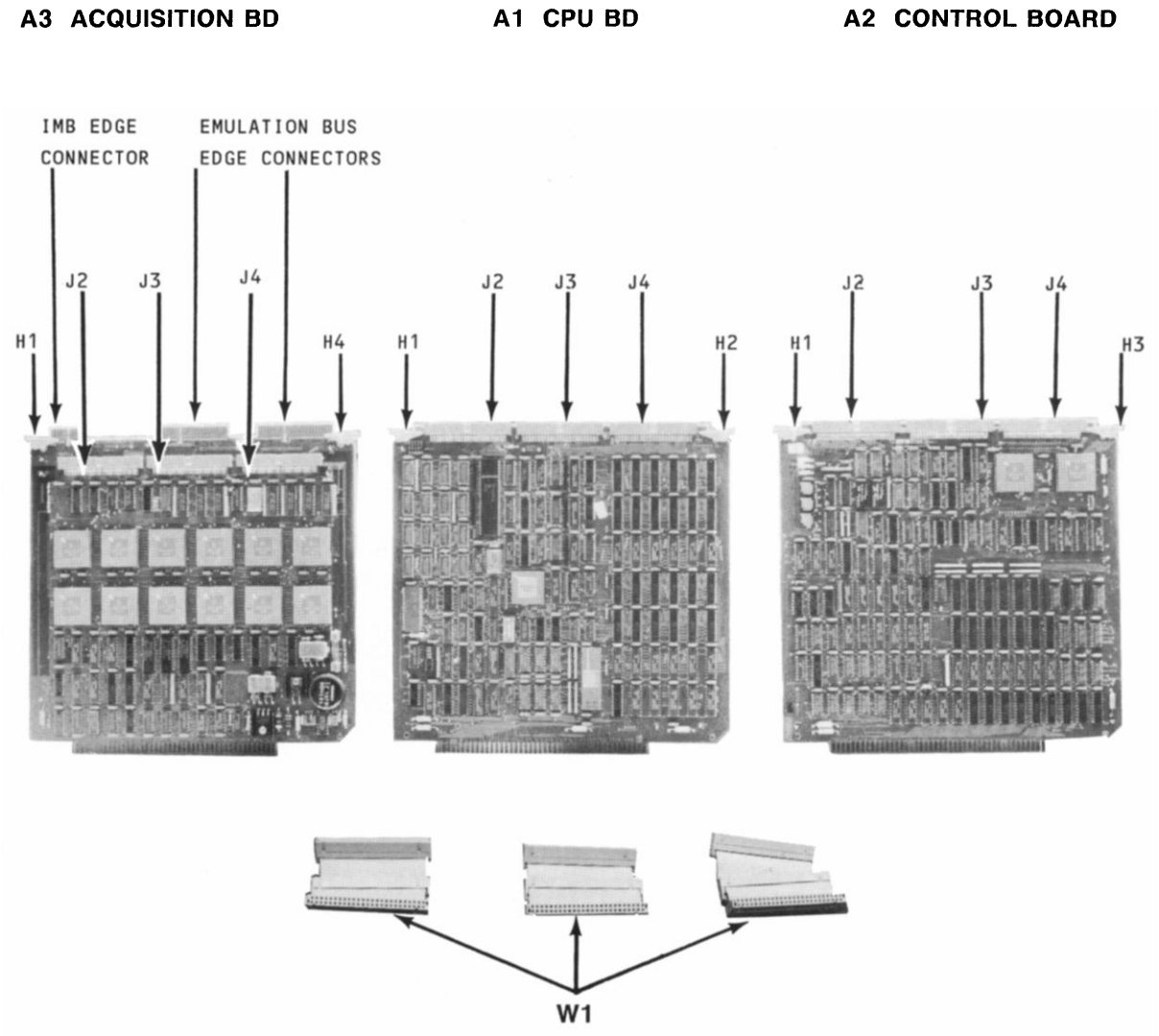


Figure 5-1. Reference Designator Breakdown

NOTES

Chapter 6
MANUAL CHANGES

INTRODUCTION

This chapter normally contains information required to backdate or update this manual for a specific instrument. Since the information in this manual applies directly to HP 64340A Software Analyzer with the serial prefixes listed on the title page, no change information is given.

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18th Floor, Great Eagle Centre
23 Harbour Road, Wanchai
HONG KONG
Tel: 5-8330222
Telex: 74766 SCHMC HX
A,M

ICELAND
Elding Trading Company Inc.
Hafnarnvoli-Tryggvagotu
P.O. Box 895
*IS-***REYKJAVIK**
Tel: 1-58-20, 1-63-03
M

INDIA
Computer products are sold through Blue Star Ltd.All computer repairs and maintenance service is done through Computer Maintenance Corp.

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24 Residency Rd.
BANGALORE *560 025*
Tel: 55660
Telex: 0845-430
Cable: BLUESTAR
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Blue Star Ltd.
Band Box House
Prabhadevi
BOMBAY *400 025*
Tel: 422-3101
Telex: 011-3751
Cable: BLUESTAR
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Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
BOMBAY *400 025*
Tel: 422-6155
Telex: 011-71193
Cable: FROSTBLUE
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Kalyan, 19 Vishwas Colony
Alkapuri, **BORODA,** *390 005*
Tel: 65235
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Blue Star Ltd.
7 Hare Street
***CALCUTTA** 700 001*
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Telex: 021-7655
Cable: BLUESTAR
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133 Kodambakkam High Road
MADRAS *600 034*
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
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Blue Star Ltd.
Bhandari House, 7th/8th Floors
91 Nehru Place
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Tel: 682547
Telex: 031-2463
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Blue Star Ltd.
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PUNE *411 011*
Tel: 22775
Cable: BLUE STAR
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Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
SECUNDERABAD *500 003*
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
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Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
TRIVANDRUM *695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation Ltd.
115, Sarojini Devi Road
SECUNDERABAD *500 003*
Tel: 310-184, 345-774
Telex: 031-2960
*CH***

INDONESIA
BERCA Indonesia P.T.
P.O.Box 496/Jkt.
Jl. Abdul Muis 62
JAKARTA
Tel: 21-373009
Telex: 46748 BERSAL IA
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P

BERCA Indonesia P.T.
P.O.Box 2497/Jkt
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JAKARTA-PUSAT
Tel: 21-344-181
Telex: BERSAL IA
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BERCA Indonesia P.T.
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Jl. Kutei No. 11
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Telex: 31146 BERSAL SB
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Telex: 212-455 HEPAIRAQ IK
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Cardiac Services Ltd.
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ISRAEL
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Computation and Measurement
Systems (CMS) Ltd.
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Telex: 038 410
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E

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Boite Postale 156
CASABLANCA
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Sema-Maroc
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CASABLANCA
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Telex: 21261 HEPAC NL
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NL 5612 LV **EINDHOVEN**
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Telex: 51484 hepae nl
A,CH**,E,M

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Arranged alphabetically by country

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Courtenay Place, **WELLINGTON 3**
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Cable: HEWPACK Wellington
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Northrop Instruments & Systems Ltd.
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P.O. Box 8602
AUCKLAND
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Telex: 60605
A,M

Northrop Instruments & Systems Ltd.
110 Mandeville St.
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CHRISTCHURCH
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Northrop Instruments & Systems Ltd.
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A,M

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N-5033 **FYLLINGSDALEN** (Bergen)
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Telex: 16621 hpnas n
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Hewlett-Packard Norge A/S
UCOsterndalen 16-18
P.O. Box 34
N-1345 **OCUSTERÅS**
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OMAN
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P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB
E

Imtac LLC
P.O. Box 8676
MUTRAH
Tel: 601695
Telex: 5741 Tawoos On
A,C,M

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Sector F-6/3
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Mushko & Company Ltd.
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Tel: 524131, 524132
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Cable: COOPERATOR Karachi
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ElectrOnico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
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PANAMA *5*
Tel: 63-6613, 63-6748
Telex: 3483 ELECTRON PG
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PERU
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Los Flamencos 145, San Isidro
Casilla 1030
LIMA *1*
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
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SAMS
Rio De La Plata 305
SAN ISIDRO
Tel: 419928
Telex: 394 20450 PELIBERTAD
P

PHILIPPINES
The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
Metro **MANILA**
Tel: 815-38-11 (up to 16)
Telex: 63274 Online PN
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Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
Cubao, **QUEZON CITY**
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MAC-KAY BOOTH
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Mundinter
Intercambio Mundial de ComAErcio S.A.R.L.
P.O. Box 2761
Av. Antonio Augusto de Aguiar 138
*P-***LISBON**
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
1298 **LISBOA** *Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
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Telex: 12598
CM,E

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QATAR
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M

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CM

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August 1984

HP distributors are printed in italics.

64340-90901,December 1984

UPDATED: MAY 1985
PRINTED IN U.S.A.