Series III

Preliminary ERS for the HP3000/35 CPU and I/O System

Project Number 3101

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1.0 Scope

This document describes an enhancement to the HP3000 Series II CPU and I/O system to allow the addressability of 1024K words (K=1024) of memory. For discussion purposes the computer system containing this enhancement will be designated the HP3000/35. Only details and changes directly pertaining to the enhancement are described here, all other aspects of the Series II CPU and I/O system not mentioned may be assumed to remain the same. The reader is assumed to be familiar with the detailed operation of the Series II CPU and I/O system. Necessary changes to the system maintenance panel and maintenance panel interface will also be discussed.

2.0 Related Documents and Standards

For information regarding the operation of the HP3000 Series II CPU and I/O system refer to the following:

Design Objective for HP3000/30 CPU-I/O
Project Number 2148
Don Jenkins
04 June 1973
Rev. A 27 June 1973

HP3000/30 ERS
Don Jenkins
10/73
Revised 3/4/74

30036A Multiplexer Channel ERS
Project No. 2148
Wally Chan
01/22/75

HP3000 Series II System Reference Manual
Part No. 30000-90020

Engineering Diagrams Set
HP3000 Series II Computer System
Part No. 30000-90076

Signal and Power Distribution Manual
HP3000 Series II Computer System
Part No. 30000-90021

HP3000 Series II Writeable Control Store ERS
ET-10907
Robert Horst
March 8,1977 (Revised November 29,1977)

For information relating to the HP3000/35 project refer to the following:

HP3000/35 Error Correction Memory ERS
Bill Berte
Lloyd Summers
Project No. 3123
4/20/78

30003-60022 Skip-Special Schematic
30003-60025 SBUS Schematic
30003-60028 IOP Schematic
30003-60030 Central Data Bus Terminator Schematic
30007-60005 Memory Control and Logging Schematic
30008-60003 128K Semiconductor Memory Array Schematic
30030-60020 Port Controller Schematic
30030-60021 Selector Channel Register Schematic
30036-60002 Multiplexer Channel Schematic
30354-60001 Maintenance Panel Schematic
30354-60003 Maintenance Panel Interface Schematic
HP3000/35 Microcode listing

3.0 Overview

The following overview will discuss the modifications made to the HP3000 Series II CPU and I/O system for the HP3000/35 project.

The modifications to the CPU and I/O system were confined to the following PCA's:

	Series II	replaced by HP3000/35
ROM PCA	30003-60001	30003-60021
Skip-special PCA	30003-60002	30003-60022
SBUS PCA	30003-60005	30003-60025
IOP PCA	30003-60008	30003-60028
CPU Backplane PCA	30003-60009	30003-60029
CTL Bus Terminator PCA	30001-60009	30003-60030
Port Controller PCA	30030-60016	30030-60020
Selector chan. reg. PCA	30030-60018	30030-60021
Multiplexer chan. PCA	30036-60001	30036-60002

The HP3000/35 has the capability of addressing 1024K words of memory. The extended address capability is achieved by expanding the bank registers in the CPU, Multiplexer Channel and Selector Channels from two to four bits and by expanding the MCU Data,I/O Data, and Port Controller Data busses from 16 to 18 bits to accomodate an 18 bit address. The two additional address bits are held "low" during data transfers. Memory appears to the CPU, I/O system, and software as 16 banks (maximum) of 64K words

each. In order to keep the existing modular organization of the system, and to minimize changes to the hardware, module numbers 0,1,2 and 3 are reserved for memory modules even though there can only be two memory modules (maximum). The first module will respond to both module numbers 0 and 1, and the second module will respond to both module numbers 2 and 3. Module number 4 is reserved for the Port Controller and module number 5 must be the CPU. The twenty bit address needed to uniquely access a given memory location is broken up into two bits for module selection (via the TO-1 and TO-2 lines) and an 18 bit address sent over the expanded MCU Data bus. The capabilty to interleave some memory configurations has been provided by including module mapping switches in the CPU and selector channel. The interleavable memory sizes are 256K, 512K, and 1024K words.

The logic that generates address parity for memory references in the CPU and I/O system has been modified to generate odd parity on an eighteen bit address. The logic that performs illegal address checking has been modified so that the configurable maximum memory sizes are 128K, 256K, 384K, 512K, 768K, and 1024K words.

Due to a limited availabilty of signal paths three compromises were made in system capability. A /35 cannot be configured to have two CPU's. The maximum number of selector channels is three (was four on Series II). The number of independent MCUCLK lines available for I/O card cages is six (was eight on Series II).

The microcode which performs the system memory dump has been modified to accomodate the larger memory capacity and to include the capability for recovering from tape errors. The error recovery philosophy is to do a "backspace-record" and "write-gap" followed by a retry whenever an error is detected. For non-recoverable errors, the system environment prior to the dump is restored (except for the contents of the current instruction register) so that the dump can be attempted again without the loss of any information. The /35 memory dump requires that 32 words (decimal) of bank zero starting at 001400 be reserved for storing the contents of CPU registers and for building SIO programs.

The microcode which initiates the cold-load sequence has also been modified since much of it is shared with the dump microcode.

The microcoded CPU register test has been modified to test the additional two bank bits of each CPU bank register. The memory address diagnostic has been modified slightly in the way tnat it handles errors. The N**2 memory diagnostic has been eliminated and a pattern test has been substituted.

Several other control panel inititated functions have been implemented in microcode. These include the ability to interrogate the memory fault logging subsystem, the ability to read and write memory, the ability to display most of the CPU

registers, and the expansion and/or addition of some I/O functions and tests.

Four new instructions have been implemented in microcode to allow a writeable control store PCA (ET-10907) to be used with any /35 system.

The system maintenance panel was modified to allow the two new bank bits to be set and displayed. This was accomplished using existing logic, switches, and LED's on the panel making field upgrades of existing panels possible.

4.0 Performance Specifications

The performance of the Series II CPU and I/O hardware has not been changed in any way. Overall system performance will improve due to the larger memory capacity (and possibly by interleaving the memory). A description of system performance is beyond the scope of this document.

5.0 Operational Characteristics

The implementation of the /35 will be discussed on a PCA-by-PCA, bus-by-bus basis. Changes to the system firmware will then be described.

5.05 ROM PCA 30003-60021

The modifications to the firmware required replacing 17 ROM's. No other changes were made to the ROM PCA.

5.1 CPU SSF (Skip-special) PCA 30003-60022

The four bank registers (ABS, PB, S, DB) were expanded from two to four bits. UBUS bits U12 and U13 were brought in from the backplane to allow setting the new bank bits from the UBUS. Two new backplane signals originating at the Maintenance Panel Interface, XSWi2 and XSWi3, were brought in allowing the new bank bits to be set from the maintenance panel. The new bank bits are brought out to the backplane and designated B12 and B13.

Six free pins were needed at the backplane connectors of the SSF PCA to accomodate the new signals. Only three were available. The clock signals -MCUCLK0, -MCUCL0R, -MCOCLK1, and -MCUCL1R were eliminated thus freeing up four pins. As a consequence the number of I/O card cages that can be attached to a /35 is limited to six because each needs its own independent MCUCLK

line.

5.2 CPU SBUS PCA 30003-60025

The illegal address comparator and memory size configuration switch (S3) were modified so that the configurable /35 memory sizes are:

S3 switch position	Memory size (words)
1	128K
2	256K
3	384K
4	512K
5	768K
6	1024K

Two lines of the MCU bus were redefined to accommodate the expanded address (see 5.9). These two lines become the most significant bits of an 18 bit address and are designated CB14 and CB15 on the MCU bus. They are held low during HSEL (data to memory). The address parity logic generates odd parity on the full 18 bit address.

Module mapping switches (S1 and S2) allow interleaving of 256K, 512K, or 1024k words. The switch settings and mappings for the various configurations are shown below:

	M A P P I N G			
MCU signal	Non-interleaved	1024K	512K	256K
TO-1	B12	A15	A15	A15
TO-2	B13	B13	B12=0	B13=0
CB14	B14	B14	B14	B13=0
CB15	B15	B15	B15	B15
MCUD0	A0	A0	A0	A0
MCUD1	A1	A1	A1	A1
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
MCUD15	A15	B12	B13	B14

To configure, "close" the following switches:

S1-	1,2,3,4	3,4,5,6	3,5	4,5
S2-	*6	*6	1,2,*6	3,4,*5

* - Applies to IOP PCA only, this same table will be refered to in the IOP and Selector Channel Register PCA discussions.

The bank compare logic was modified to compare all four bank bits (B12, B13, B14, B15) with the bank bits from the maintenance panel (XSW12, XSW13, XSW14, XSW15) so that

breakpoints can be set from the panel at all addresses in the expanded memory.

When memory is interleaved special consideration must be given when setting breakpoints because of the mapping taking place on the MCU bus. Set the breakpoint as if memory was not interleaved then make the changes indicated below to the breakpoint address for the various memory sizes:

1024K	512K	256K
A15 <= B12	A15 <= B13	A15 <= B14 B14 <= 0

Provisions were made to allow gating the two new bank bits onto the SBUS (for reading the bank registers).

5.3 CPU MCU (Module Control Unit) PCA 30003-60007

No changes were made to this PCA, however the CPU in the /35 must be configured to be CPU number 1 and module number 5. Also, the jumper that allows the CPU to pull down ENABLE 5 must not be installed since the ENABLE 5 line is used for one of the new address bits on the MCU bus (see 5.9). The following jumpers must be installed to correctly configure the MCU for a /35: W1, W6, W8, W10, and W13.

5.4 IOP (I/O Processor) PCA 30003-60028

The illegal address comparator and memory size configuration switch (S3) were modified so that the configurable /35 memory sizes are as listed for the SBUS in 5.2. Module mapping switches (S1 and S2) were added to allow interleaving as described for the SBUS in 5.2. Some additional switches and logic were neccessary to correct the parity on addresses sent from the multiplexer channel to the IOP before sending it on to memory. The multiplexer channel is totally ignorant of interleaving and always generates address parity as if the memory was not interleaved. The setting of the additional switches for the various memory configurations is also shown in 5.2.

Two new I/O bank bits (-IOX12, -IOX13) are brought in from two redefined lines (see 5.11) of the IOP bus and latched into an additional register. The two old I/O bank bits (-IOX14, -IOX15) become part of an 18 bit address sent to memory.

The -XERR signal (called -IODPE elsewhere) was moved from the IOP bus over to the IOP/POWER bus to make room for one of the new address bits (-IOX13). See Appendices B and D.

The SIOMAP register contents has been redefined as follows:

BIT	Contents
0	IOTO2
1	IOTO1
2	ILGADDR
3	SYSPE
4	APE
5	B15
6	B14
7	B13
8	B12
9	P (PARITY)
10	ALWAYS 0
11	B15IN
12	B14IN
13	B13IN
14	B12IN
15	PIN (PARITY IN)

5.5 CPU Backpane PCA 30003-60029

Several additional connections were made on the CPU backplane.

SIGNAL	1A1	1A2	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
B12	P1-21		P1*24			P1-30				
B13	P1-22		P1*23			P1-12				
CB14						P2*12		P2:30	P2*1	P2-31
CB15						P2*32		P2:25	P2*73	P2-45
U12			P2-9	P2*19	P2:19	P2:19	P2:19		P2:19	
U13			P2-42	P2*21	P2:21	P2:21	P2:21	P1:57	P2:21	
XSW12	P1*26		P1-26			P1-13				
XSW13	P1*28		P1-25			P1-23				
-IOX12									P2:66	P3:45
-IOX13									P2:10	P3: 2
-XERR									P1:38	P1:14

* => NEW CONNECTION (SOURCE)
\- => NEW CONNECTION
: => OLD CONNECTION SHOWN FOR COMPLETENESS

5.6 I/O Multiplexer Channel PCA 30036-60002

The auxiliary RAM was expanded to accomodate the additional two bank bits. The bank register was also expanded by two bits. The two new bank bits are gated out to two redefined IOP bus lines, -IOX12 and -IOX13. They are only gated out with the address for a RD/WR transfer. They are held low otherwise. Odd parity is generated on the 18 bit address.

In order to get a free signal path for one of the new bank bits (-IOX13) on the IOP bus, the -IODPE signal was moved over to the

IOP/POWER bus (see appendices B and D).

5.7 Selector Channel Port Controller PCA 30030-60020

The two new address bits (PB14, PB15) can be gated from the Port Controller Bus onto the MCU bus and vice-versa.

In order to make room for the two additional bits (PB14 and PB15) on the Port Controller Bus two signal paths had to be freed. The TO2-1 and TO2-2 signals were eliminated. As a consequence, the maximum number of selector channels that can be connected to a /35 is three (#2 has been eliminated leaving #1,#3, and #4). To configure in #3 or #4 requires that a ribbon cable be installed connecting J3 of the Port Controller to J3 of the SC register PCA.

5.8 Selector Channel Register PCA 30030-60021

The bank register was expanded to four bits. The additional two address bits are gated out onto the two redefined port controller bus lines (PB14,PB15) to become part of an 18 bit address. These lines are held low during data transfers. The illegal address comparator and memory size configuration switch (S3) were modified to allow the configurations as listed for the SBUS in 5.2. Mapping switches (S1 and S2) to allow interleaving some memory configurations were added as described for the SBUS in 5.2. Odd parity is generated on 18 bits for all addresses.

The Port Controller Bus data parity checking logic was modified to not check bus parity on addresses sent from the register PCA. Previously it was checking bus parity on all transmissions 'from' the PCA (as a self-test) which would have caused a problem for address transmissions since the parity is generated on 18 bits and only checked on 16 bits.

5.9 Central Data Bus

To obtain the signal paths for the two new address bits (CB14 and CB15) it was decided to use the Ready 6 line and the Enable 5 line. This is made possible by configuring the CPU to be module number 5 and by not installing the MCU PCA jumper that lets the MCU pull-down ENABLE 5. See appendix A.

5.10 Central Data Bus Terminator PCA 30003-30030

The Central Data Bus Terminator was modified so that the termination of the CB14 line (was READY 6) is similar to the termination of the MCU data lines. The CB15 line (was ENABLE 5) was already terminated properly.

5.11 IOP BUS

The two additional signal paths necessary to accomodate the new address bits (-IOX12 and -IOX13) were obtained by using the one available spare line and by moving the -IODPE signal over to the IOP/POWER Bus. See appendices B and D.

5.12 IOP/POWER Bus

See 5.11 and Appendix D.

5.13 Port Controller Bus

The two additional signal paths for PB14 and PB15 were obtained by using the lines previously occupied by TO2-1 and TO2-2. This makes it impossible to connect selector channel #2 to a /35 system. See 5.7 and Appendix C.

5.14 Cold load and system dump firmware

It was necessary to modify the cold-load and system dump firmware. The new microcode makes use of a 32 word (decimal) reserved area of memory beginning at location 001400 in bank 0. When a cold-load or dump is initiated from the control panel the firmware begins by initializing the reserved area of memory as follows:

(For cold-loads to device numbers greater than 3 all of memory is first initialized with HALT 10 = 030370 instructions).

```
1400  MACHINE ID = 1 FOR HP3000/35
1401  OLD CONTENTS OF DEV#*4
1402  SM
1403  SP1
1404  SP2
1405  DB
1406  (0:4)=DB BANK; (4:4)=PB-BANK; (12:4)=S-BANK
1407  Z
1410  DL
1411  X
1412  Q
1413  CIR
1414  PB
1415  PL
1416  P
1417  CPX1
1420  STATUS
1421  (0:8)=CPX2(8:15);  (8:8)=# BANKS
1422  SIO CONTROL
1423  BACK SPACE RECORD/WRITE EOF COMMAND
1424  SIO CONTROL
```

```
1425  WRITE GAP/REWIND-OFFLINE
1426  SIO JUMP
1427  JUMP ADDRESS= 001436
1430  SIO SET BANK
1431  BANK
1432  SIO CONTROL
1433  COMMAND FROM SWITCH REGISTER BITS (0:7)
1434  WRITE 4K IF DUMP/READ 16 IF COLD LOAD
1435  ADDRESS (INITIALLY 0 FOR DUMP,  001400 IF COLD LOAD)
1436  SIO END WITH INTERRUPT IF DUMP/SIO JUMP IF COLD LOAD
1437  JUMP ADDRESS= 001400 IF COLD LOAD
```

The firmware then modifies the SIO program pointer for the device whose DRT number is in switch register bits (9:7) to point to the SIO program starting at 1430. It then sends an SIO command to the device and proceeds as follows.

Cold-load:

A 16 word continuation of the SIO program is read into memory beginning at 1400. The SIO program continues to run until an "END WITH INTERRUPT" order is executed. The CPU enters a firmware wait loop until the device interrupts. Any other interrupting devices are sent RIL's (reset interrupt) and the CPU continues to wait for the device specified in the switch register. When the interrupt is received, the CPU sends a RIL to the device and then treats "cold-load" as an internal interrupt executing on the ICS.

System dump:

The SIO program starting at 1430 dumps 4K word blocks of memory to the tape unit whose device number is preconfigured into the system control panel (usually 6). The bank and address of the 4K block to be dumped (at 1431 and 1435) are continually updated by the firmware. The program is restarted until all of memory has been dumped.

If an error occurs, the SIO program pointer is modified to point to the error recovery SIO program starting at 1422 and an SIO command is issued to the device. This program does a "backspace-record" and "write-gap" on the tape unit. If the error recovery SIO program completes successfully another attempt is made to write the record that got the error. The error recovery procedure can be repeated indefinitely as long as it completes successfully. If it fails, the machine environment prior to the dump is restored and the system halts. The dump can be tried again without the loss of information (except for the contents of CIR). During a dump the CIR displays the sum of the bank and beginning address of the 4K block being dumped.

If the tape unit is not on-line or no write-ring has been installed when the dump is initiated the machine will halt immediately with CIR displaying 000000. No system information

is lost except for the contents of CIR. The dump may be attempted again after the problem is corrected.

When a successful dump completes an end-of-file will be written and the the tape will rewind off-line. The system environment prior to the dump is restored (except for CIR) so that another dump will produce the same results.

5.15 Instruction Set Changes

The only standard Series II instruction that was modified was the PCN (push CPU number - opcode:%020362). This instruction is now used for the purpose of determining CPU type (Series II or /35) rather than CPU number since multiple CPU configurations are not possible on the /35. The firmware for the instruction was modified so that the number returned to the TOS is a 2 for the /35 (was 1 on Series II). IMPORTANT: In order for this instruction to operate correctly on either a Series II or /35 system the MCU PCA must be configured for CPU #1.

The instructions LOCK (opcode: %020361) and UNLK (opcode: %020363) will not be supported on the /35 since the new memory does not have "read/write-ones" capabilty.

The function of the CMD instruction will be slightly modified if executed on a /35 configured for interleaving. This is due to the address mapping that takes place. The effect will be that the least significant bit of the parameter being passed to the destination module may be inverted. This should not be a problem on the /35 since this instruction is used only by diagnostics.

From a functional standpoint any instruction that referenced a bank register in any way on Series II will now reference a four bit register on the /35.

5.151 Writeable Control Store Instructions

Four instructions were added to the standard firmware to allow a writeable control store (ET-10907) to be used with any HP3000/35 system. All four instructions are privileged. All have opcode %020562. They are distinguished from each other by the value on the TOS when the instructions are entered. All of these instructions currently will cause an unimplemented instruction trap if executed on a Series II.

Writeable Control Store Status (WCSS) Opcode: %020562, TOS=0

WCSS returns CCE if a WCS PCA is installed in the system, otherwise it returns CCL. The word (0) on TOS is <u>not</u> popped!

Load Control Store (LCS) Opcode: 020562, TOS=1

LCS loads from 0 to the entire 8K double words of control store. Interrupts are checked during the instruction since loading all 8K requires approximately 33 msec. The instruction is entered with:

```
TOS-3  =  WCS address to begin loading (0- 17777)
TOS-2  =  DB relative address of first data word
TOS-1  =  Positive word count (=1/2 #WCS double words)
TOS    =  1   (LCS instruction identifier)
```

When the instruction completes all four words are popped off of the stack and CCE is set. This instruction will cause an unimplemented instruction trap if executed on an HP3000/35 without a WCS installed.

Verify Control Store (VCS) Opcode: 020562, TOS=2

VCS compares data from a DB-relative array with the contents of the control store. It is entered with:

```
TOS-3 = WCS address to begin verify (0- 17777)
TOS-2 = DB-relative address of first data word
TOS-1 = Positive word count (=1/2 #WCS double words)
TOS   = 2   (VCS instruction identifier)
```

If the verify is successful, CCE is set and all four words are popped. If an error occurs, the instruction immediately terminates leaving three words on the TOS as follow:

```
TOS-2 = WCS address of the error
TOS-1 = DB-relative addr of the data word in error
TOS   = number of words not verified
```

If the error occured while verifying the most significant 16 bits CCL will be returned. If the error occured while verifying the least significant 16 bits CCG will be returned.

The VCS instruction is interruptable since it takes 29 msec to verify the entire 8k of WCS. This instruction will cause an unimplemented instruction trap if executed on an HP3000/35 without a WCS installed.

Map Control Store (MCS) Opcode: 020562, TOS=3

This instruction loads the least significant 8 bits of the word at TOS-1 into the WCS map registers. Bits (12:4) are loaded into map register 1 and bits (8:4) are loaded into map register 2. The map word and the instruction identifier are popped at the end of the instruction. CCE is set by the instruction. This instruction will cause an unimplemented instruction trap if executed on an HP3000/35 without a WCS installed.

5.16 Control panel initiated functions and tests

Several functons and tests that can be invoked from the system control panel have been either modified or added to the standard firmware. The functions or tests are invoked by entering an option number in the switch register and then "cold-loading".

5.161 CPU Register Test

This test is invoked by cold-loading with 000001 in the switch register. This test is the same as for Series II with the exception that upon detection of an error the test will pause in run mode with the CIR displaying "bad-bits" until the run/halt switch is depressed. Then the test will system-halt with CIR displaying a code for the failing register (same as for Series II).

5.162 Memory Pattern Test

This test is invoked by cold-loading with 100000 in the switch register. It writes then immediately reads back any pattern entered in the switch register throughout all of memory. The initial pattern is 100000. The current pattern is displayed in the CIR. The test will halt if the run/halt switch is depressed until the end of a pass. Any error will halt the test with CIR displaying the error type as shown below:

```
CIR   =0  => Data compare error
CIR(4)=1  => System parity error
CIR(5)=1  => Address parity error
CIR(6)=1  => Multiple-bit error
```

Subsequent depressions of the run/halt switch will display bank, address, and (expected data XOR actual data).

5.163 Memory Address Test

This test is invoked by cold-loading with 000000 in the switch register. This test is the same as for Series II except in the way that errors are handled. Upon detection of an error the test halts with CIR displaying the error type as shown below:

```
CIR   =0  => Data compare error
CIR(4)=1  => System parity error
CIR(5)=1  => Address/data bus parity error
CIR(6)=1  => Multiple-bit error
```

Subsequent depressions of the run/halt switch will display bank, address, actual data, and expected data in the CIR.

5.164 I/O Test (TIO)

This test is invoked by cold-loading with 000002 in the switch register. It will send a TIO to device numbers 2 through 177. It pauses with CIR equal to the TIO status of each responding device. Depress the run/halt switch to advance to the next device. The test will complete by system-halting with CIR= 000200.

5.165 I/O Test (SIO)

This test is invoked by cold-loading with 100002 in the switch register. It executes an SIO program consisting of only an END-ORDER (without interrupt) for all devices that have the SIO OK bit set in the TIO status word. The test pauses with CIR displaying the END-ORDER status for each SIO device. Depressing the run/halt switch will advance the test to the next device. The test will "hang" if the SIO program should fail.

5.166 Display Memory Logging Errors Function

This function transfers the contents of the error logging array on the memory control and logging PCA(s) to the I/O logging array on the fault logging interface PCA (FLI). It then interrogates the FLI and displays the RIO status word in CIR for each error logged. The RIO status word contains the information needed to find the failing RAM(s).

RIO STATUS WORD DISPLAYED IN CIR

```
**************************************************
* 0 * 1  2  3* 4  5  6* 7  8  9*10 11 12*13 14 15*
**************************************************
  E   R     R  D  L  ********10 BIT ADDRESS******
  R   /     E  I  /  ***** ******* **CHECK BITS**
  R   W     A  S  U     S       R     1  2  3  4  5
  O         D  W        M       O
  R   O        E  M     A       W
      K     S  C  C
            C     L     #       #
            A
            N
```

This function is invoked by cold-loading with 001000 in the switch regster. The test first pauses in halt mode with CIR= 001000. For each subsequent depression of the run/halt switch the RIO status word for each error logged will be displayed in CIR. The function will system-halt upon completion with CIR= 000000 if no errors were found. A halt with CIR= 030370 will occur if the FLI (device #2) does not respond. See the HP3000/35 Error Correcting Memory ERS for information about decoding error information.

5.167 Panel Read/Write Memory Function

This function allows memory to be written or read from the system control panel on a word-by-word basis. The function has four options as indicated below:

Write,increment:	Cold-load with	002000 in the switch register
Write,decrement:	Cold-load with	102000 in the switch register
Read,increment:	Cold-load with	003000 in the switch register
Read,decrement:	Cold-load with	103000 in the switch register

After cold-loading the function initially pauses with CIR displaying the option number in the switch register. Enter the desired bank in switch register bits (12:4) and press run. The function pauses with CIR=bank. Then enter the address in the switch register and press run. The function will pause with CIR=address.

For read: Each depression of the run/halt switch will cause the function to pause with CIR displaying the contents of the next address (beginning with the address entered in the switch register).

For write: Enter data to be stored in the switch register and depress the run/halt switch. The data will be stored and the function will pause with CIR=data. Repeat to store at the next address.

The address will be incremented if switch register bit 0 is set to 0 when cold-loading, otherwise it will be decremented. Addresses do not cross bank boundaries (i.e. they wrap around within bank). A system-halt will occur if an attempt is made to read or write non-existent memory.

5.168 Display Register Function

This function displays the contents of most of the CPU registers and also the contents of the top-of-stack in memory. The function is invoked by cold-loading with 004000 in the switch register. The function will first pause with CIR displaying 004000. Each depression of the run/halt switch will cause CIR to display the contents of the following registers in the order shown below:

00-STATUS	10-DB bank
01-SP1	11-DB
02-SP2	12-S bank
03-TOS=MEM(SM)	13-DL
04-PB bank	14-Q
05-PB	15-SM
06-P	16-Z
07-PL	17-X

The function will system-halt when the index regiser (X) is displayed.

5.169 Start I/O Function

This function issues a start I/O command to a device then waits for an interrupt from that device (a RIL is sent to any other interrupting devices). After receiving the interrupt the function will system-halt with CIR displaying the TIO status from the device if the command was successful or 030370 if the SIO command failed.

The function is invoked by cold-loading with 005000 in the switch register. It will pause with CIR displaying 005000. Then enter the device number in switch register bits (9:7). Depressing the run/halt switch will issue the SIO command to the device.

This function assumes that an SIO program is already in memory and that the DRT pointer at dev#*4 has been initialized.

5.1691 Mag-tape Subsystem Test

This test writes one 4K word record to tape from each memory bank. It corrects for tape errors by issuing a backspace-record followed by a write-gap then retrying. After writing, the tape is rewound and each 4K word record is read into another area of its source memory bank. The data read is compared with the data written and the test will halt if an error is detected. The test will run continuously if no errors are found. The CIR displays the current bank in bits (0:4) and the mag-tape command in bits (12:4). If the SIO command to the tape unit fails the test will halt with CIR displaying 030370.

The test is invoked by cold-loading with CIR= 006000. It will first pause with CIR= 006000. Enter the device number of the tape unit to be tested in switch register bits (9:7). To start the test depress the run/halt switch. Depressing the run/halt switch until a pass has completed will halt the test. If an error is detected the test will halt. Subsequent depressions of the run/halt switch will display the contents of the registers shown below:

```
STATUS   =  14001  (PRIV-MODE, ENB INT, CST#1)
SP1      = DATA WORD WRITTEN
SP2      = DATA WORD READ
TOS      = NOT USED
PB-BNK   = CURRENT I/O BANK ADDRESS
PB       = SP1 XOR SP2   (FAILING BIT)
P        = WRITE BUFFER ADDRESS
PL       = READ BUFFER OFFSET
DB-BNK   = NOT USED
DB       = DEVICE NUMBER BEING TESTED
S-BNK    = ALWAYS ZERO
DL       = CCPX PARAMETER WORD
Q        = DEVICE NUMBER * 4 (DRT)
SM       = USED FOR ADDRESS POINTER TO BUILD SIO PROGRAM
```

Z = I/O BANK IN BITS(0:3)
INDEX(X) = INTERRUPTING DEVICE NUMBER

5.1692 Asynchronous Terminal Controller and Terminal Test

This test is invoked by cold-loading with 007000 in the switch register. It will first pause with CIR= 007000. Enter the ATC device number in switch register bits (9:7) and the channel number in bits (3:4). Depress the run/halt switch. The test will pause with CIR equal to the switch register. Enter the character size parameter in switch register bits (5:3) and the baud rate parameter in bits (8:8). Depress the run/halt switch. The test will pause with CIR equal to the switch register. All characters typed on the selected terminal will be echoed. The ASCII code for each character will be displayed in CIR bits (9:7). A non-responding device will cause the test to system-halt with CIR= 030370.

The character size parameter is the least significant three bits of the sum of the number of start, parity, data, and stop bits in a transmitted character minus one. The baud rate parameter is computed by the following equation:

baud rate parameter = [14,400 / device bit rate] - 1
(where [] means round to the nearest integer)

Some examples of character size and baud rate parameters are shown below:

DEVICE	CHAR PARM	BAUD PARM	OVERALL( )
TTY ASR 33	2	202	1202
IBM 2741 SELECTRIC	0	157	157
30 CPS TERMINAL (10-BIT)	1	057	457
60 CPS TERMINAL	1	027	427
120 CPS TERMINAL	1	013	413
240 CPS TERMINAL	1	005	405
150 BAUD BAUDOT TERM	7	137	3537

5.17 Maintenance Panel PCA 30354-60001

The 30354A Maintenance Panel was modified to allow setting and displaying the two new bank bits B12 and B13, and to display the two new MCU data bus signals CB14 and CB15. These modifications use existing logic, switches, and LED's so that field upgrades of existing panels will be possible.

The switches previously used for the two most significant bits of the VBUS jump register are now used to set the new bank bits B12 and B13. The LED's previously used to display the two most

significant VBUS bits are now used to display B12 and B13. Since the new MCU data bus signals CB14 and CB15 were actually created by redefining the READY6 and ENABLE5 lines they are displayed in the positions previously occupied by these without any modifications.

5.18 Maintenance Panel Interface PCA 30354-60003

The changes to the Maintenance Panel interface involve installing four jumpers to allow the two new bank bits B12 and B13 to be set and displayed by the panel.

Appendix A - HP3000/35 Central Data Bus

PIN	SIGNAL	PIN	SIGNAL
1	GND	26	FROM 1
2	MCUD0	27	FROM 2
3	MCUD1	28	MOP0
4	MCUD2	29	MOP1
5	MCUD3	30	GND
6	MCUD4	31	CB14 (WAS READY 6)
7	MCUD5	32	SYSPRTY
8	GND	33	READY 0
9	MCUD6	34	READY 1
10	MCUD7	35	READY 2
11	MCUD8	36	READY 3
12	MCUD9	37	READY 4
13	MCUD10	38	READY 5
14	GND	39	GND
15	MCUD11	40	ENABLE 0
16	MCUD12	41	ENABLE 1
17	MCUD13	42	ENABLE 2
18	MCUD14	43	ENABLE 3
19	MCUD15	44	ENABLE 4
20	MCUDPRTY	45	CB15 (WAS ENABLE 5)
21	GND	46	GND
22	TO 0	47	-APE
23	TO 1	48	-SYSPE
24	TO 2	49	-MCURST
25	FROM 0	50	GND

Appendix B - HP3000/35 IOP Bus

PIN	SIGNAL	PIN	SIGNAL
1	-IODPRTY	26	IOD 4
2	-IOX13 (WAS -IODPE)	27	IOD 5
3	GND	28	GND
4	-IOCMD 00	29	IOD 6
5	-IOCMD 02	30	IOD 7
6	-IOCMD 01	31	GND
7	GND	32	IOD 8
8	DEVNO 0	33	IOD 9
9	DEVNO 1	34	GND
10	GND	35	IOD 10
11	DEVNO 2	36	IOD 11
12	DEVNO 3	37	GND
13	GND	38	IOD 12
14	DEVNO 4	39	IOD 13
15	DEVNO 5	40	GND
16	GND	41	IOD 14
17	DEVNO 6	42	IOD 15
18	DEVNO 7	43	GND
19	GND	44	-INTREQ
20	IOD 0	45	-IOX12 (WAS SPARE)
21	IOD 1	46	GND
22	GND	47	-IOX14
23	IOD 2	48	-IOX15
24	IOD 3	49	GND
25	GND	50	-INTACK

Appendix C - HP3000/35 Port Controller Bus

PIN	SIGNAL	PIN	SIGNAL
1	-ERR1	26	PCD 0
2	LSEL1	27	PCD 1
3	GND	28	GND
4	HSEL1	29	PCD 2
5	STRB1	30	PCD 3
6	-CWREQ1	31	GND
7	GND	32	PCD 4
8	-RRREQ1	33	PCD 5
9	TO1-1	34	GND
10	GND	35	PCD 6
11	TO1-2	36	PCD 7
12	-ERR2	37	GND
13	GND	38	PCD 8
14	LSEL2	39	PCD 9
15	HSEL2	40	GND
16	GND	41	PCD 10
17	-STRB2	42	PCD 11
18	-CWREQ2	43	GND
19	GND	44	PCD 12
20	-RRREQ2	45	PCD 13
21	PB14 (WAS TO2-1)	46	GND
22	GND	47	PCD 14
23	PB15 (WAS TO2-2)	48	PCD 15
24	NOT USED	49	GND
25	GND	50	PCDPRTY

Appendix D - HP3000/35 IOP/POWER Bus

PIN NO. 56-PIN	PIN NO. 20-PIN	SIGNAL	PIN NO. 56-PIN	PIN NO. 20-PIN	SIGNAL
1		+5	30		GND
2		+5	31		-5B
3		+5	32		-5B
4		+5	33		-3B
5	2	-PF WARN	34		-3B
6	1	ENTIMER	35		+5B
7	4	SPARE	36		+5B
8	3	SPARE	37		+12B
9	6	PWR ON	38		+12B
10	5	PWR ON GND	39		+12.7B
11	8	IORESET	40		+12.7B
12	7	IORESET GND	41	12	-HSREQ
13	10	-MCUCLKS	42	11	-HSREQ GND
14	9	-MCUCLKS GND	43		SEE NOTE
15		GND	44		SEE NOTE
16		GND	45	14	-IODPE (WAS SPARE)
17		-5	46	13	-IODPE GND
18		-5	47		SEE NOTE
19		GND	48		SEE NOTE
20		GND	49	16	-SI
21		+15	50	15	-SI GND
22		+15	51		SEE NOTE
23		+15	52		SEE NOTE
24		+15	53	18	-SO
25		-15	54	17	-SO GND
26		-15	55		SEE NOTE
27		-15	56		SEE NOTE
28		-15		20	SPARE
29		GND		19	GND

NOTE: Reserved for interrupt and data poll.