HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12559A

9-TRACK MAGNETIC TAPE UNIT INTERFACE KIT

(FOR 2115 AND 2116 COMPUTERS)

Card Assemblies
02116-6159, Rev. 752
02116-6160, Rev. 913

Note

This manual should be retained with Volume Three of the HP Computer System Documentation.

12559-9001

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GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The Hewlett-Packard 12559A 9-Track Magnetic Tape Interface Kit (figure 1-1) provides an interface between a HP 2115 or 2116 Computer and a HP H01-D3030G 9-Track Magnetic Tape Unit. The kit contains two interface cards (magnetic tape 1 and magnetic tape 2, hereafter called mag tape 1 and mag tape 2) which permit input, output, or combined input/output operations between the computer and the magnetic tape unit. Sections II through V of this manual provide installation and programming, theory of operation, maintenance, and replaceable parts information for the interface kit.

1-3. DESCRIPTION.

1-4. The mag tape 1 and 2 interface cards enable an HP computer to record on and read from 1/2-inch, 9-channel, NRZI (non-return to zero with a flux reversal for every "1"), IBM-compatible magnetic tape with the HP H01-D3030G 9-Track Magnetic Tape Unit (hereafter referred to as the magnetic tape unit). Coupled with the interface kit, the magnetic tape unit reads and records at 800 bits per inch density. Tape speed is 75 inches per second which provides a data transfer rate of 60,000 eight-bit characters per second. Data formats and data transfers are accomplished under program control or through the direct memory access (DMA) option. The mag tape 1 and 2 interface cards plug into any two adjacent slots of the computer with the mag tape 1 interface card assigned the higher priority.

1-5. Data is written in records on the magnetic tape with each record having a minimum of 12 characters. A nominal 0.6-inch interrecord gap must be provided on the magnetic tape in order to allow the tape to stop and/or start between records.

1-6. A character is recorded on tracks (channels) across the width of the magnetic tape, with each track containing one bit of the character. There are nine tracks, of which

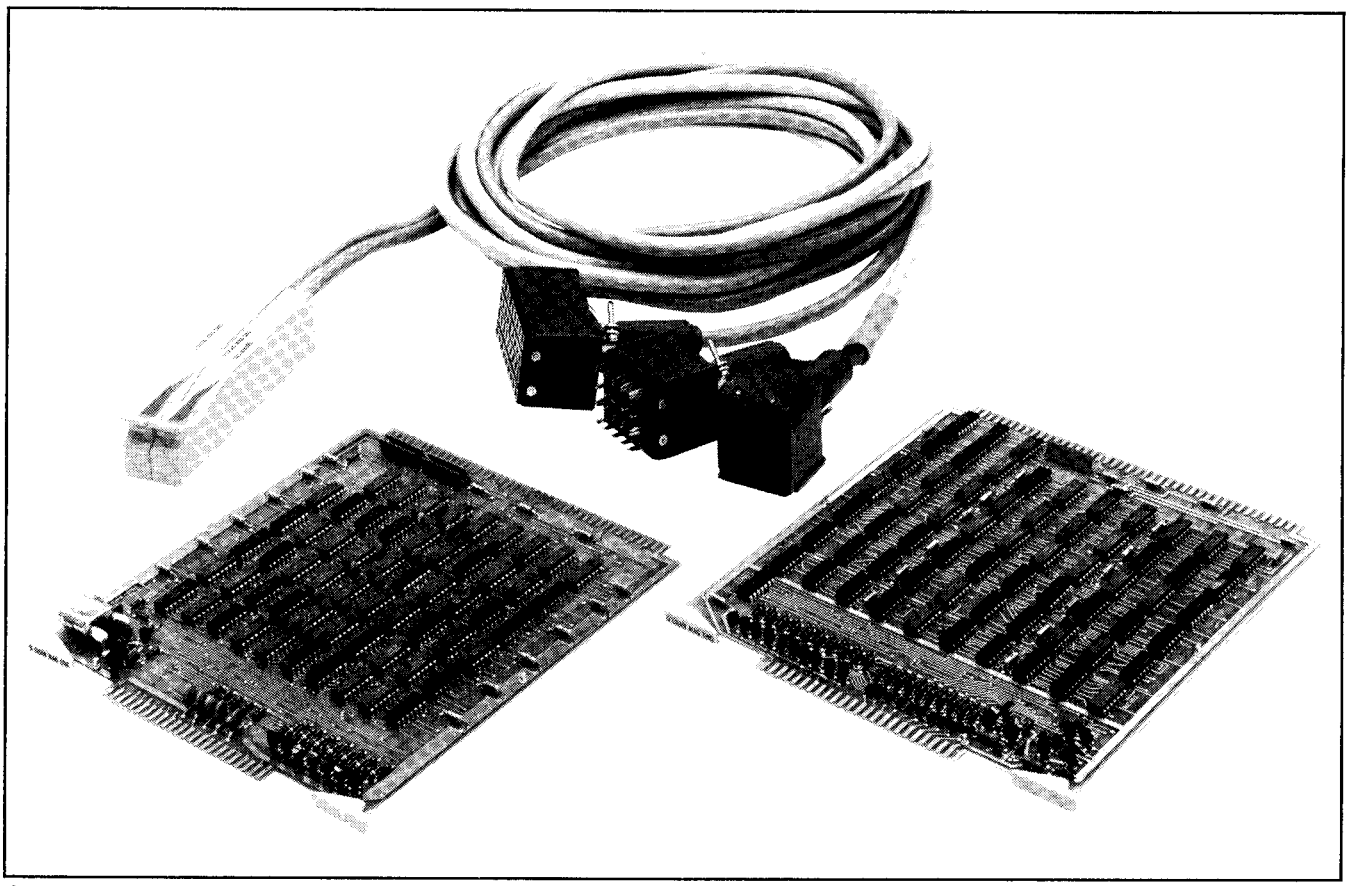

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Figure 1-1. HP 12559A Interface Kit

eight tracks contain data and one track is used for a parity bit. The parity bit indicates the accuracy of the data and is a logic 0 when the total number of bits in a data character is odd and a logic 1 when the total number of bits in a data character is even. A parity error occurs when there is an even number of logic 1's in the character.

1-7. Refer to the Digital Magnetic Tape Unit, Series 3030 manual for detailed information on the magnetic tape unit.

1-8. INTERFACE KIT CONTENTS.

1-9. The interface kit consists of the following:

a. Mag tape 1 card, part no. 02116-6159.
b. Mag tape 2 card, part no. 02116-6160.
c. Interconnecting cable, 15 feet, part no. 02116-6193.

Note

To prevent the malfunctioning of program instructions, always ensure that the interconnecting cable is connected. When the magnetic tape unit is disabled or not in use, do not remove the interconnecting cable without removing the interface cards.

d. Operating and service manual, part no. 12559-9001.

1-10. STANDARD ACCESSORIES AND SERVICE ITEMS.

1-11. The standard accessories and service items supplied with the magnetic tape unit are as follows:

a. Magnetic tape head cleaner, part no. 8500-0810.
b. Magnetic tape, 2400 feet, part no. 9162-0001.

1-12. IDENTIFICATION.

1-13. Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designations. Options to an interface kit are identified by a three-digit suffix following the model designation (00000A-000). If the designation and the option suffix of your kit do not agree with those on the title page of this manual, there are differences between your kit and the kit described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-14. In addition to a part number, each plug-in printed-circuit card is identified by a letter, a date code, and a division code (e.g. A-921-22). These are marked on the card beneath the part number. The letter identifies the version of the etched circuit on the card. The date code (three digits) refers to the electrical characteristics of the board with components mounted. The division code (two digits) identifies the Hewlett-Packard division which manufactured the board. If the date code on a printed-circuit card does not agree with the date code shown on the corresponding schematic diagram in this manual, the card differs from the one described in this manual. These differences are explained in change sheets or a manual supplement available at the nearest HP Sales and Service Office.

1-15. Diagnostic program tapes are identified by name and part number, marked on a label affixed to the beginning of the diagnostic tape.

1-16. Manuals and manual supplements are identified by title and part number on the title page of the document.

1-17. SPECIFICATIONS.

1-18. Table 1-1 lists the characteristics and specifications of the mag tape 1 and mag tape 2 interface cards.

Table 1-1. Mag Tape 1 and Mag Tape 2 Card Specifications

CHARACTERISTICS	SPECIFICATIONS		
Operating power required from computer:	Voltage	*Current	
	+4.5V	2.58A	
	+12V	180 mA	
	-12V	180 mA	
	-2V	240 mA	
Signal Logic Levels:			
Write Enable, Write Reset, Read Reset, Forward Drive, Reverse Drive, Rewind, Unload.	Negative True:	Logic 1:	-10V
		Logic 0:	0V
Write Clock, Read Clock, Read Tracks	Positive False:	Logic 1:	0V
		Logic 0:	+10V
Write Tracks	Positive True:	Logic 1:	+10V
		Logic 0:	0V
Card Dimensions:			
Width	7-3/4 inches (196,8 mm)		
Height	8-11/16 inches (220,7 mm)		

*An auxiliary HP 2160 Power Supply may be necessary for installations which use several I/O devices with high current requirements. Refer to Volume 3 of the computer documentation.

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides procedures and information for unpacking and inspection, installation, and programming of the mag tape 1 and mag tape 2 interface cards.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the cards are unpacked. Inspect the cards for damage (cracks, broken parts, etc.). If the cards are damaged and fail to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged cards without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. The magnetic tape unit and the computer are interconnected by use of a single cable assembly, see figure 2-1. Table 2-1 contains interconnecting cable lead-wire information. The hooded connectors of the cable which connect to the two interface cards are fastened together for ease of installation. Install the two interface cards as follows:

a. Turn off power at the computer and the magnetic tape unit.

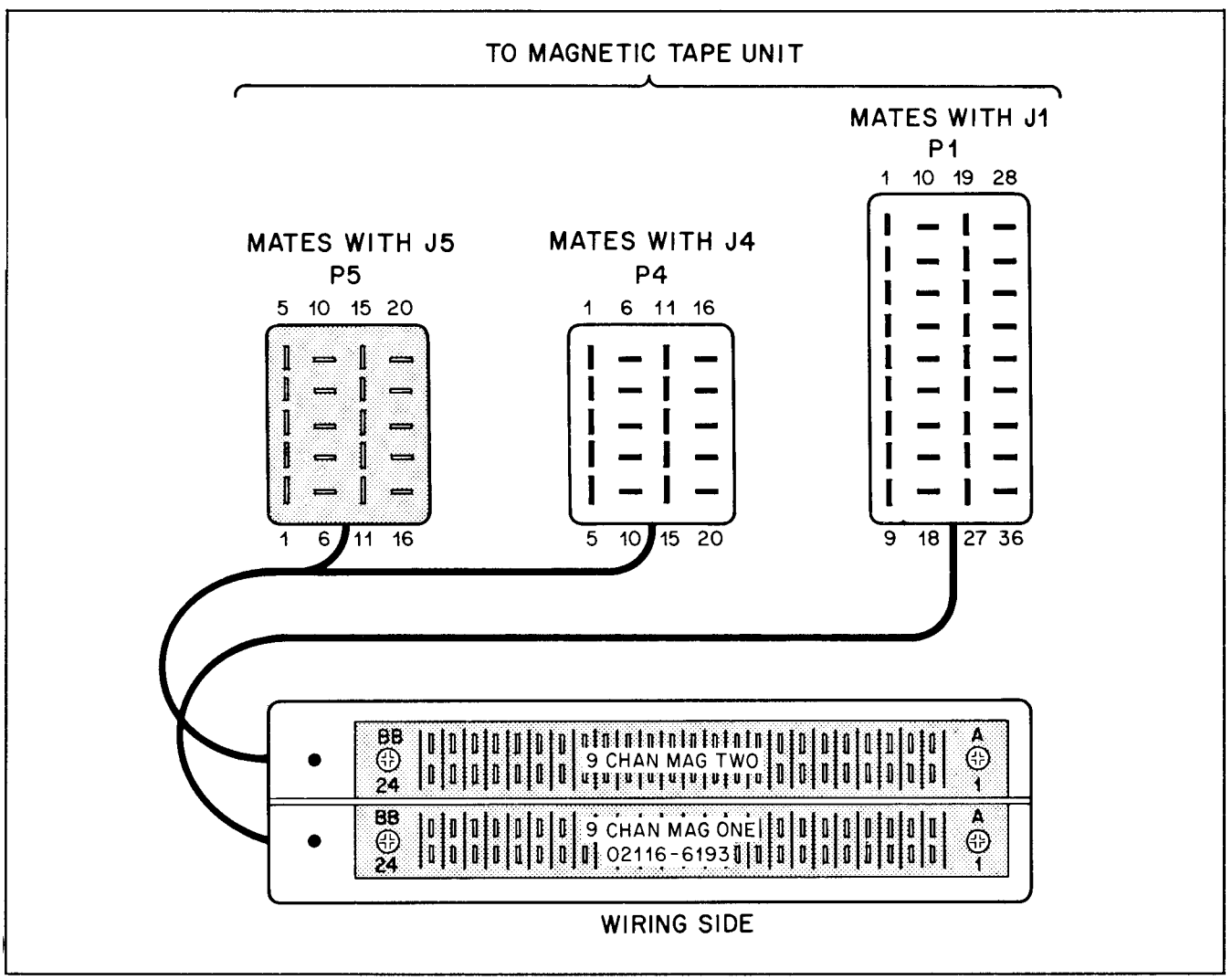

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Figure 2-1. Interconnecting Cable Diagram

Table 2-1. Interface Cards to Magnetic Tape Unit Connector Pin Assignments

*FROM	*TO	**SIGNAL	*FROM	*TO	**SIGNAL
MT1-1	MT2-A	Gnd	MT2-1	MT2-24	Bus Wire
MT1-2	NC		MT2-2	NC	
MT1-3	MT2-3	CCP	MT2-3	MT1-3	CCP
MT1-4	MT2-4	WFM	MT2-4	MT1-4	WFM
MT1-5	MT2-5	WRS	MT2-5	MT1-5	WRS
MT1-6	MT2-6	WRT	MT2-6	MT1-6	WRT
MT1-7	MT2-7	SRS	MT2-7	MT1-7	SRS
MT1-8	MT2-8	FWD	MT2-8	MT1-8	FWD
MT1-9	MT2-9	REV	MT2-9	MT1-9	REV
MT1-10	MT2-10	EOR	MT2-10	MT1-10	EOR
MT1-11	NC		MT2-11	NC	
MT1-12	NC		MT2-12	NC	
MT1-13	P1-8	Auto (Ready Status)	MT2-13	P5-2	RT2 (Track 2 Read)
MT1-14	NC		MT2-13	Cap.	
MT1-15	P1-15	Rewind (Rewind Status)	Cap.	Bus Wire	
MT1-16	NC		MT2-14	P5-8	RT8 (Track 8 Read)
MT1-17	P1-9	Load Point (Load Point Status)	MT2-14	Cap.	
MT1-18	NC		Cap.	Bus Wire	
MT1-19	P4-12	Write Reset	MT2-15	P5-1	RT1 (Track 1 Read)
MT1-20	NC		MT2-15	Cap.	
MT1-21	P1-2	Forward Drive (Forward)	Cap.	Bus Wire	
MT1-22	NC		MT2-16	P5-9	RT9 (Track 9 Read)
MT1-23	P1-4	Rewind	MT2-16	Cap.	
MT1-24	P1-36	Gnd (Ground)	Cap.	Bus Wire	
MT1-24	MT2-BB	Gnd	MT2-17	P5-3	RT3 (Track 3 Read)
MT1-24	MT1-BB	Gnd	MT2-17	Cap.	
MT1-24	MT2-24	Gnd	Cap.	Bus Wire	
			MT2-18	P5-5	RT5 (Track 5 Read)
MT1-A	NC		MT2-18	Cap.	
MT1-B	NC		Cap.	Bus Wire	
MT1-C	MT2-C	A2	MT2-19	P5-6	RT6 (Track 6 Read)
MT1-D	MT2-D	SPC	MT2-19	Cap.	
MT1-E	MT2-E	ADSD	Cap.	Bus Wire	
MT1-F	MT2-F	ACI	MT2-20	P5-7	RT7 (Track 7 Read)
MT1-H	MT2-H	DTF	MT2-20	Cap.	
MT1-J	MT2-J	SFB	Cap.	Bus Wire	
MT1-K	MT2-K	CLR	MT2-21	P5-4	RT4 (Track 4 Read)
MT1-L	MT2-L	WTC	MT2-21	Cap.	
MT1-M	NC		Cap.	Bus Wire	
MT1-N	P1-11	EOT (End of Tape Status)	MT2-22	P5-11	Read Clock
MT1-P	NC		MT2-23	NC	
MT1-R	P1-10	Write Enabled (Write Enable Status)	MT2-24	MT2-1	Bus Wire
			MT2-24	MT2-A	Bus Wire
MT1-S	NC		MT2-24	P5-10	Gnd (Common)
MT1-T	P5-12	Read Reset	MT2-24	MT2-BB	Gnd
MT1-U	NC		MT2-24	MT2-24	Gnd
MT1-V	P4-13	Write Enable (Write Permit)			
MT1-W	NC		MT2-A	MT2-24	Bus Wire
MT1-X	P1-3	Reverse Drive (Reverse)	MT2-A	MT1-1	Gnd
MT1-Y	NC		MT2-B	NC	
MT1-Z	P1-5	Unload	MT2-C	MT1-C	A2
MT1-AA	NC		MT2-D	MT1-D	SPC
MT1-BB	MT1-24	Gnd	MT2-E	MT1-E	ADSD
MT1-BB	MT2-BB	Gnd	MT2-F	MT1-F	ACI

* MT1 and MT2 refer to magnetic tape 1 and magnetic tape 2 interface cards, respectively.
** Signal names within parenthesis are those used in the magnetic tape unit documentation.

Table 2-1. Interface Cards to Magnetic Tape Unit Connector Pin Assignments (Continued)

*FROM	*TO	**SIGNAL
MT2-H	MT1-H	$\overline{\text{DTF}}$
MT2-J	MT1-J	$\overline{\text{SFB}}$
MT2-K	MT1-K	$\overline{\text{CLR}}$
MT2-L	MT1-L	WTC
MT2-M	NC	
MT2-N	NC	
MT2-P	P4-2	WT2 (Track 2 Write)
MT2-R	P4-8	WT8 (Track 8 Write)
MT2-S	P4-1	WT1 (Track 1 Write)
MT2-T	P4-9	WT9 (Track 9 Write)
MT2-U	P4-3	WT3 (Track 3 Write)
MT2-V	P4-5	WT5 (Track 5 Write)
MT2-W	P4-6	WT6 (Track 6 Write)
MT2-X	P4-7	WT7 (Track 7 Write)
MT2-Y	P4-4	WT4 (Track 4 Write)
MT2-Z	P4-11	Write Clock
MT2-AA	NC	
MT2-BB	P4-10	Gnd (Common)
MT2-BB	MT2-24	Gnd
P1-1	P1-36	Ground
P1-2	MT1-21	Forward Drive (Forward)
P1-3	MT1-X	Reverse Drive (Reverse)
P1-4	MT1-23	Rewind
P1-5	MT1-Z	Unload
P1-6	NC	
P1-7	NC	
P1-8	MT1-13	$\overline{\text{Auto}}$ (Ready Status)
P1-9	MT1-17	$\overline{\text{Load}}$ $\overline{\text{Point}}$ (Load Point Status)
P1-10	MT1-R	$\overline{\text{Write}}$ $\overline{\text{Enabled}}$ (Write Enable Status)
P1-11	MT1-N	$\overline{\text{EOT}}$ (End of Tape Status)
P1-12	NC	
P1-13	NC	
P1-14	NC	
P1-15	MT1-15	$\overline{\text{Rewind}}$ (Rewind Status)
P1-16	NC	
P1-17	NC	
P1-18	NC	
P1-19	NC	
P1-20	NC	
P1-21	NC	
P1-22	NC	
P1-23	NC	
P1-24	NC	
P1-25	NC	
P1-26	NC	
P1-27	NC	
P1-28	NC	
P1-29	NC	

*FROM	*TO	**SIGNAL
P1-30	NC	
P1-31	NC	
P1-32	NC	
P1-33	NC	
P1-34	NC	
P1-35	NC	
P1-36	P1-1	Ground
P1-36	MT1-24	Ground
P4-1	MT2-S	WT1 (Track 1 Write)
P4-2	MT2-P	WT2 (Track 2 Write)
P4-3	MT2-U	WT3 (Track 3 Write)
P4-4	MT2-Y	WT4 (Track 4 Write)
P4-5	MT2-V	WT5 (Track 5 Write)
P4-6	MT2-W	WT6 (Track 6 Write)
P4-7	MT2-X	WT7 (Track 7 Write)
P4-8	MT2-R	WT8 (Track 8 Write)
P4-9	MT2-T	WT9 (Track 9 Write)
P4-10	MT2-BB	Ground (Common)
P4-11	MT2-Z	Write Clock
P4-12	MT1-19	Write Reset
P4-13	MT1-V	Write Enable (Write Permit)
P4-14	NC	
P4-15	NC	
P4-16	NC	
P4-17	NC	
P4-18	NC	
P4-19	NC	
P4-20	NC	
P5-1	MT2-15	RT1 (Track 1 Read)
P5-2	MT2-13	RT2 (Track 2 Read)
P5-3	MT2-17	RT3 (Track 3 Read)
P5-4	MT2-21	RT4 (Track 4 Read)
P5-5	MT2-18	RT5 (Track 5 Read)
P5-6	MT2-19	RT6 (Track 6 Read)
P5-7	MT2-20	RT7 (Track 7 Read)
P5-8	MT2-14	RT8 (Track 8 Read)
P5-9	MT2-16	RT9 (Track 9 Read)
P5-10	MT2-24	Gnd (Common)
P5-11	MT2-22	Read Clock
P5-12	MT1-T	Read Reset
P5-13	NC	
P5-14	NC	
P5-15	NC	
P5-16	NC	
P5-17	NC	
P5-18	NC	
P5-19	NC	
P5-20	NC	

* MT1 and MT2 refer to magnetic tape 1 and magnetic tape 2 interface cards, respectively.
** Signal names within parenthesis are those used in the magnetic tape unit documentation.

b. Open the computer or extender for access to the I/O section.

c. Insert the two interface cards into the assigned computer or extender I/O card slots with the 02116-6159 Mag Tape 1 card assigned the higher priority (lower numbered select code).

Note

If used in conjunction with DMA, the interface cards must be installed in the I/O card slots in the computer card cage only.

d. Pass the end of the interconnecting cable that contains the hooded 48-pin connectors through the I/O cable access opening of the computer.

e. Attach the 9 CHAN MAG ONE 02116-6193 connector to the 02116-6159 Mag Tape 1 card (high priority card) and the 9 CHAN MAG TWO connector to the 02116-6160 Mag Tape 2 card.

Note

To prevent the malfunctioning of program instructions, always ensure that the interconnecting cable is connected. When the magnetic tape unit is disabled or not in use, do not remove the interconnecting cable without removing the interface cards.

f. At the back of the magnetic tape unit (lower left corner) remove the six screws from the access cover plate.

g. Attach the opposite end of the interconnecting cable to the appropriate magnetic tape unit connectors (see figure 2-1 and table 2-1).

h. Close all computer and magnetic tape unit access openings. This completes the installation.

i. Run the magnetic tape diagnostic program. Instructions for running the diagnostic program are outlined in the Diagnostic Program Procedure, part number 12559-90032, located in the Manual of Diagnostics.

2-7. PROGRAMMING.

2-8. GENERAL.

2-9. All commands to the magnetic tape unit initiate tape motion except for the Clear (CLR) instruction. Commands and status information are transferred through the computer A- or B-register to the command channel with standard I/O instructions. Data is transferred through the data channel to or from the A- or B-register. Data can also be transferred through the data channel to memory via Direct Memory Access (DMA). The Command Flag and Interrupt signals indicate the completion of operations requiring tape motion. If the Control FF in the command channel is not set by a Set Control (STC) instruction, interrupt requests from the magnetic tape unit will be inhibited.

Note

The two channels used by the magnetic tape unit are called data and command for software purposes. The data channel is the higher priority channel and corresponds to the address slot which the mag tape 1 interface card is plugged into. The command channel is the lower priority channel and corresponds to the address slot which the mag tape 2 interface card is plugged into. Therefore, when referring to software, the data channel is used in lieu of the mag tape 1 card and the command channel is used in lieu of the mag tape 2 card.

2-10. PROGRAM COMMANDS.

2-11. Figure 2-2 illustrates the eight-bit command word required for operation of the magnetic tape unit. These bits are the IOBO bits shown on the mag tape 1 and mag tape 2 interface card schematic diagrams. Before a program command is given, the status of the magnetic tape unit should be examined under program control to ascertain the condition of the magnetic tape unit before the operation is performed. The status of the magnetic tape unit should also be examined after the operation is performed. Table 2-2 identifies the functions to be performed by the magnetic tape unit when the respective bits of the eight-bit command word are a logic 1. Write bit 3 and Motion bit 0 results in forward motion of the tape during a write operation so that Forward bit 1 need not be programmed.

2-12. WRITE COMMAND. The Write Command (WC) initiates forward motion and sets up the necessary conditions for writing. This command prepares the data channel for each character to be written on the magnetic tape. Only bits 0 through 7 of the word loaded into the data channel are written on the magnetic tape. Command words written on the magnetic tape have bit and track assignments as shown in figure 2-3. (P denotes parity bit.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								REWIND	REWIND & STANDBY	REVERSE	TRANSFER DATA	WRITE	FILE MARK	FORWARD	MOTION

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Figure 2-2. Eight-Bit Command Word

conditions they represent are no longer true. The Busy bit is reset upon completion of any operation. The nine-bit status word may be examined at any time with a LIA or LIB instruction with the command channel select code.

Note

The status bits are the IOBI bits shown on the mag tape 1 and mag tape 2 interface card schematic diagrams.

2-24. BUSY. Busy bit 0 is a logic 1 when the tape is in motion or the magnetic tape unit is in the LOCAL mode of operation. When bit 0 is a logic 0, the command and data channels are ready to accept a command.

2-25. PARITY ERROR. Parity Error bit 1 is a logic 1 when a vertical or longitudinal parity error occurs during a read or write operation. The longitudinal parity of the entiry record is checked during read operations. Vertical parity is checked only during the data transfer portion (i.e., if the Data Flag FF is set when a character is read). Parity is not checked in FSR or BSR operations.

2-26. WRITE ENABLED. Write Enabled bit 2 is a logic 1 if the write ring is not inserted in the tape reel on the magnetic tape unit. The write ring must be inserted in the tape reel before a write operation can be performed.

2-27. REJECT. A command will be rejected and Reject bit 3 set to a logic 1 if tape motion is requested and the I/O interface cards are busy, backward tape motion is requested and the tape is at load point, or a write command is given and the tape reel does not have a write enable ring.

2-28. TIMING. Timing bit 4 is a logic 1 if the Data Channel Flag FF has not been reset before the next character is read and received by the command channel.

2-29. END-OF-TAPE. End-of-tape (EOT) bit 5 is a logic 1 when the EOT reflective marker is sensed while the tape is moving forward. Bit 5 remains a logic 1 until a Rewind command is given.

2-30. BEGINNING-OF-TAPE. Beginning-of-tape (BOT) bit 6 is a logic 1 while the beginning-of-tape reflective marker is under the photo-sense head on the magnetic tape unit.

2-31. END-OF-FILE. End-of-File (EOF) bit 7 is a logic 1 when a one-character file mark record (23 octal) is detected while reading, forward spacing, back spacing, or when a file mark record is written.

2-32. LOCAL. Local bit 8 is a logic 1 when the magnetic tape unit is in the LOCAL mode of operation.

2-33. SAMPLE PROGRAMS.

2-34. The magnetic tape unit may be programmed in HP Assembly language, FORTRAN, or ALGOL. A comprehensive software system is supplied with the magnetic tape unit. In addition, two types of drivers are included in the software supplied. The System Input/Output (SIO) magnetic tape unit driver permits read/write without interrupt control; the Basic Control System (BCS) magnetic tape unit driver is for input/output under interrupt control.

2-35. ASSEMBLY LANGUAGE PROGRAMMING. Three sample programs using assembly language are as follows:

a. The sample program shown in table 2-3 writes one record of 12 characters onto the magnetic tape. The data that is written onto the magnetic tape is obtained from the lower eight bits of the computer switch register. This record is written continuously until the EOT reflective marker is sensed and then the magnetic tape is automatically rewound. This program is repetitive unless switch 15 of the switch register is set.

b. The following sample program uses the SIO magnetic tape unit driver which reads and writes in binary only, without interrupt control.

OPERATION	OPERAND
LDA	Buffer length (1) or file count (2)
LDB	Buffer address (1) or record count (2)
JSB	107B,I
OCT	Command Code
End of file/End of tape return, Error return, or Normal return	

(1) Used for read/write operations
(2) Used for tape positioning.

c. The following sample program uses the BCS magnetic tape unit driver which inputs and outputs data under interrupt control. The BCD is converted to ASCII during a read operation and ASCII is converted to BCD during a write operation.

OPERATION	OPERAND
JSB	.IOC.
OCT	Function Subfunction Unit reference
JSB	Reflect Address
JMP	
DEF	Buffer Address
DEC	Buffer Length
OCT	
⋮	
EXT	.IOC.

Table 2-3. Sample Program

LABEL	OPERATION	OPERAND	COMMENTS
START	CLC	0C	DISABLE ALL I/O & TURN
	LDA	COUNT	OFF INTER.
	STA	TEMP	INITIALIZE COUNTER FOR 12 CHAR.
	LIB	1	INPUT DATA TO BE WRITTEN
	LDA	CMND	BITS 0-7
	OTA	COMCH	OUTPUT WRITE COMMAND TO
01A	SFS	DATCH	CMND. CH.
	JMP	*-1	TEST FOR DATA CH. FLAG
	OTB	DATCH,C	OUTPUT DATA TO DATA CHANNEL
	ISZ	TEMP	INCREMENT CHARACTER COUNTER
	JMP	01A	
	CLC	DATCH	CLEAR DATA TRANSFER FF
	LIA	1	INPUT SWITCH REGISTER
	SSA		SKIP IF BIT 15 = 0 CONTINUE OPER.
	HLT	77B	NORMAL HALT
	SFS	COMCH	CHECK COMMAND CHANNEL FLAG
	JMP	*-1	FOR END OF OPERATION
	LIA	COMCH	INPUT STATUS
	AND	MASK	EXTRACT EOT STATUS BIT
	SZA,RSS		SKIP IF EOT DETECTED
	JMP	START	REPEAT
	LDA	REW	
	OTA	COMCH,C	OUTPUT REWIND COMMAND
	SFS	COMCH	CHECK COMMAND CHANNEL FLAG
	JMP	*-1	FOR END OF OPERATION
	JMP	START	
COUNT	OCT	177764	NEGATIVE 12 DECIMAL
CMND	OCT	31	WRITE COMMAND
REW	OCT	201	REWIND COMMAND
MASK	OCT	000040	
TEMP	OCT	0	

NOTE: DATCH = LOWER SELECT CODE
COMCH = HIGHER SELECT CODE

2-36. FORTRAN PROGRAMMING. A sample program using FORTRAN is as follows:

READ, WRITE — (unit, format) List (1)

READ, WRITE — (unit, file count, record count) (2)

(1) - for BCD records
(2) - for tape positioning
REWIND, BACKSPACE, and END FILE are also available.

EXAMPLE: Write the contents of array DATA in one binary record on Unit 10.

```
DIMENSION DATA (100)
  WRITE (10) DATA
```

EXAMPLE: Backspace five records on Unit 13.

```
CALL PTAPE (13,0,-5)
```

2-37. ALGOL PROGRAMMING. A sample program using ALGOL is as follows:

READ, WRITE — (unit, format list) (1)

READ, WRITE — (unit, list) (2)

PTAPE — (unit, file count, record count) (3)

(1) for BCD records
(2) for binary records
(3) for tape positioning
REWIND, BACKSPACE, END FILE, and UNLOAD are also available.

EXAMPLE: Read 3 BCD values for variables A,B, and C from Unit 11.

```
FORMAT P1 (3F7.6)
READ (11,P1,A,B,C)
```

EXAMPLE: Forward space one file on Unit 8.

```
PTAPE (8,1,0) or SPACE (8)
```

SECTION III
THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. Interface circuits for controlling the transfer of data to and from the magnetic tape unit are located on the mag tape 1 and mag tape 2 interface cards which are installed in the I/O slots of the computer. The major function of the mag tape 1 card is to provide timing and control signals to the magnetic tape unit and to the mag tape 2 card. The mag tape 1 card also accepts command words from the computer, status signals from the magnetic tape unit, provides status bits to the computer, and controls end-of-operation interrupts.

3-3. The mag tape 2 card performs data handling functions, buffers the write data characters, generates the proper parity, generates the cyclic redundancy check character (CRCC), and provides write timing signals to the magnetic tape unit. During a read operation the data is buffered, parity is checked, and end-of-record (EOR) and end-of-file (EOF) detection is performed.

3-4. Figure 3-1 shows the signal lines between the magnetic tape unit and the interface cards, including direction of signal flow. The diagram also lists the main circuits contained on each interface card.

3-5. DETAILED THEORY OF OPERATION.

3-6. The following paragraphs describe operation of the mag tape 1 (data channel) interface card and the mag tape 2 (command channel) interface card. Operation of the magnetic tape unit and computer are described only to the extent required for explaining the functioning of the two interface cards. Refer to the computer and magnetic tape unit manuals for detailed descriptions of those instruments.

3-7. REFERENCE INFORMATION.

3-8. Paragraphs 3-9 through 3-18 present general information which is required for understanding the detailed theory discussion that follows.

3-9. BINARY VOLTAGE LEVELS. The binary signal levels on both interface cards are approximately +3.5 volts and +0.2 volt. The levels may vary from these approximate amounts, depending on the type of integrated circuit providing the signal. The input and output voltage levels for each type of integrated circuit are specified in section IV of this manual.

3-10. LOGIC CIRCUITS. The logic circuits on both interface cards principally employ positive logic. That is all inputs to an "and" or "nand" gate must be +3.5 volts for coincidence to occur. Similarly, if any input to an "or" or "nor" gate is +3.5 volts, the output is +3.5 volts for an "or" gate or +0.2 volt for a "nor" gate. The output from the set side of a flip-flop is approximately +3.5 volts when the flip-flop is set, and +0.2 volt when the flip-flop is clear. In accordance with established usage for positive-true logic circuits, the term "true" or logic 1 in this manual refers to a nominal signal level of +3.5 volts, and "false" or logic 0 refers to a nominal level of +0.2 volt.

3-11. ABBREVIATIONS. Signal-name abbreviations are listed in tables 3-1 and 4-1, together with the meanings of the abbreviated designations. Table 4-1 also lists the logic equation of the mnemonic and its source.

3-12. SIGNAL NAMES. Signals which enter or leave the two interface cards are named in one of the following ways:

a. As a condition which either exists or does not exist.

b. As a command or order, expressed in the imperative grammatical mode.

c. In accordance with the name of a flip-flop which is the source of the signal.

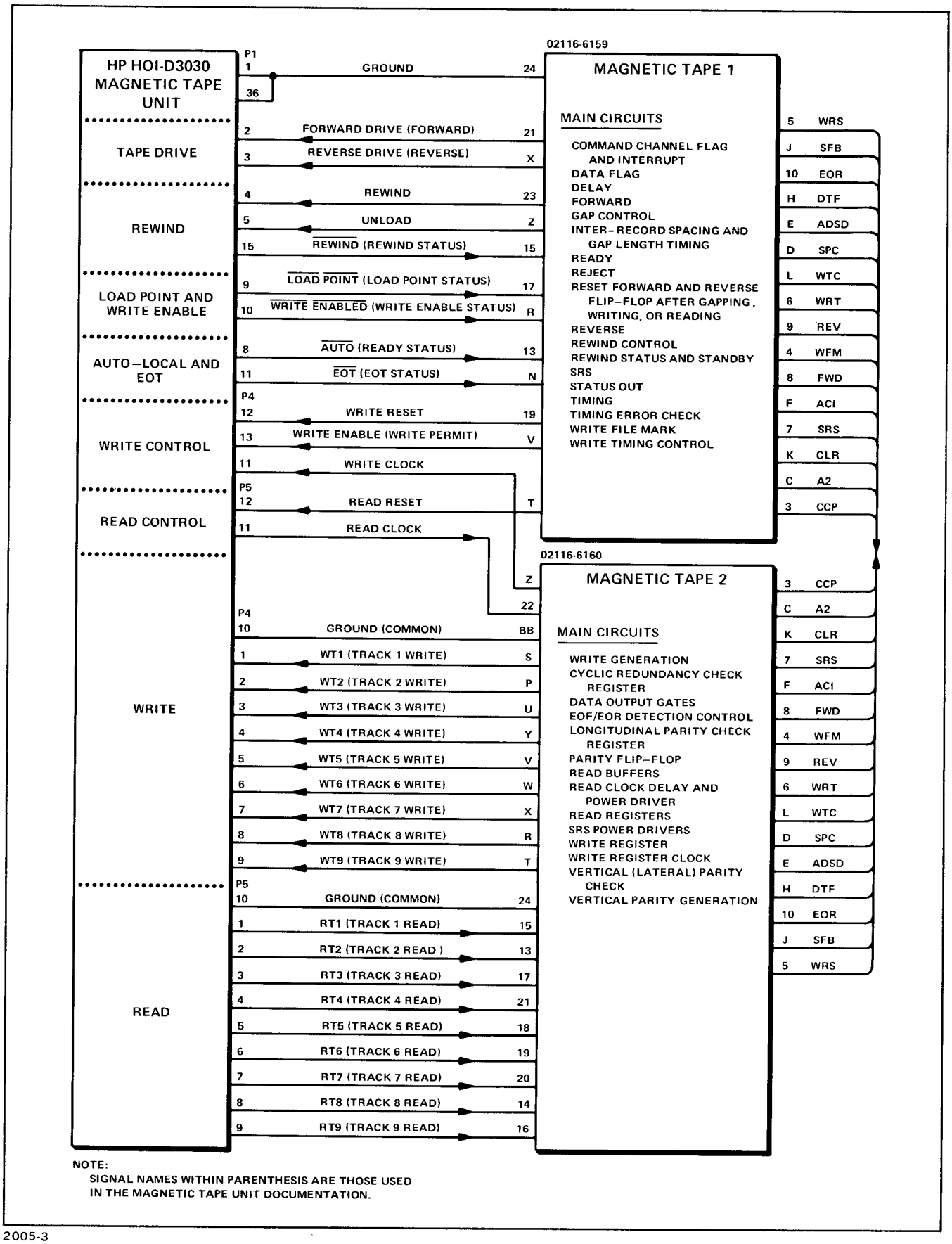
d. In accordance with the name of the bus which carries the signal.

3-13. Since the circuits on the two interface cards employ positive logic, signal names are positive-true. When a signal is named in accordance with a condition, the signal level is +3.5 volts when the condition exists, and +0.2 volt when the condition does not exist.

3-14. In further accordance with the principle of positive-true signal names, a signal which is named in the imperative mode becomes +3.5 volts to bring about the action commanded. For instance, the Flag FF is cleared when the CLF (clear flag) signal changes from +0.2 volt to +3.5 volts.

3-15. When a signal is named in accordance with the flip-flop which is its source, the signal taken from the set-side of the flip-flop is +3.5 volts when the flip-flop is in the set condition, and +0.2 volt when the flip-flop is in the clear condition.

3-16. When a signal is named in accordance with the bus which carries it, the signal is +3.5 volts when the bus carries a logic 1, and +0.2 volt when it carries a logic 0.



2005-3

Figure 3-1. Signals Between the Interface Cards and the Magnetic Tape Unit

Table 3-1. Glossary of Terms

MNEMONIC	DEFINITION
ACI	See ADSC
ADSC (ACI)	Address Command, Lower Priority Interrupt Location
ADSD	Address Data, Higher Priority Interrupt Location
A2	Counter 2 FF A
BOT	Beginning of Tape (Load Point)
BSR	Back Space Record
CCL	Command Control
CCP	Control Clock Pulse
CFB	Command Flag Buffer
CFL	Command Flag
CIR	Command Interrupt Request
CLC	Clear Control
CLF	Clear Flag
CLR	Clear
CRC	Cyclic Redundancy Check
CRCC	Cyclic Redundancy Check Character
CRS	Control Reset to I/O
DFB	Data Flag Buffer
DFL	Data Flag
DLY	Delay [counts off after all operations to allow settling after tape motion]
DTF	Data Transfer
ENF	Enable Flag (T2 buffered)
EOF	End of File
EOP	End of Operation
EOT	End of Tape
ERC	End of Record Control
FLGH	Flag
FWD	Forward
FSR	Forward Space Record
GAP	Three-Inch Gap. Automatically generates three inches of blank tape if a Write command is given at the start of tape or if a Gap command is issued.
HSCL	Higher Select Code Least Significant Digit
HSCM	Higher Select Code Most Significant Digit
IAK	Interrupt Acknowledge
IEN	Interrupt Enable
IOG(B)	Input/Output Group, buffered
IOI	I/O Input
IOO	I/O Output
IRG	Inter-Record Gap
IRQH	Interrupt Request
LPE	Longitudinal Parity Error
LPR	Longitudinal Parity Check Register
LRCC	Longitudinal Redundancy Check Character
LSCL	Lower Select Code Least Significant Digit
LSCM	Lower Select Code Most Significant Digit

Table 3-1. Glossary of Terms (Continued)

MNEMONIC	DEFINITION
MOT	Motion
NRZI	Non-Return to Zero with a flux reversal for every "1".
PE	Parity Error
POPIO	Power On Pulse to I/O
PRH	Priority High (Select Code)
PRL	Priority Low (Select Code)
PTC	Parity Control
PTY	Parity
RAS	Read After Start [time between initial motion and $\overline{\text{RRS}}$]
RCD	Read Clock Delayed
RDY	Ready [for next operation]
REJ	Reject [command not accepted]
REV	Reverse
REW	Rewind
RSB	Rewind and Standby
RRC	Read Record Control
RRS	Read Reset Control
RT	Read Track
RWS	Rewind Status [signal from tape unit]
SAG	Stop After Gap [time for gaps 40 us; 3 in. gap]
SAR	Stop After Read [time between EOR and motion stop]
SAW	Stop After Write [time between LPC and $\overline{\text{FWD}}$]
SCP	Spacing Clock Pulse
SFB	Set Data Flag Buffer
SFC	Skip if Flag Clear, decoded
SFS	Skip if Flag Set, decoded
SIR	Set Interrupt Request (T5 buffered)
SKF	Skip on Flag
SPC	Set Parity Control
SRS	Start-Reset [resets all FFs on the interface cards before a command is issued]
SRP	Stop Reset Pulse
SRQ	Service Request from Select Code Address
STC	Set Control, decoded
STF	Set Flag, decoded
TIM	Timing Error
TMC	Tape Mark Character
TM	Tape Mark
TRAS	*T Read After Start
TSAG	*T Stop After Gap
TSAR	*T Stop After Read
TSAW	*T Stop After Write
TWAS	*T Write After Start
VPE	Vertical Parity Error
VPC	Vertical Parity Check

*T denotes Time

Table 3-1. Glossary of Terms (Continued)

MNEMONIC	DEFINITION
WAS	Write After Start [time between initial motion and initial data]
WCC	Write Clock Control
WCP	Write Clock Pulse
WES	Write Enabled Status [write ring is in tape reel]
WFM	Write File Mark
WRS	Write Reset
WRT	Write
WT	Write Track
WTC	Write Timing Control

3-17. MAGNETIC TAPE SIGNALS. All control and data signals that enter or leave the magnetic tape unit pass through the two interface cards. The operating and service manual for the magnetic tape unit provides information on the timing of signals originating in the magnetic tape unit.

3-18. ADDITIONAL INFORMATION. Schematic diagrams for the two interface cards are furnished in figures 4-15 and 4-17 in section IV of this manual. In the schematic diagrams and tables, pins marked with an asterisk plug into the 48-contact interface connector. Pins without an asterisk plug into the 86-contact backplane connector. Reference designations preceded by MC (microcircuit package) are identified by part number and description in tables 4-3 and 4-4.

3-19. INPUT OPERATIONS.

3-20. To initiate the input of data from the magnetic tape unit, a Read Clock signal is applied to the mag tape 2 card. A flag checking routine or direct memory access (DMA) must be used to signal the mag tape 1 card. The interrupt system cannot be used to signal the computer that data is available from the magnetic tape unit.

3-21. When the magnetic tape unit is ready to transfer data, a Read Clock signal (see figures 3-2 and 4-17) is applied to the mag tape 2 card. This signal is transferred through the Read Clock Delay and Power Gates network and output 8 microseconds later as a Read Clock Delayed (RCD) signal. This signal is applied to the clock input of the Read Register FFs and the Longitudinal Redundancy Check Character Register FFs. The RCD signal transfers data into latching FFs of the Read Register so that the data is read at the mid-point of the data period.

3-22. At time T2 of the computer machine cycle, the ENF signal is supplied by the computer to set the Data Flag (DFL) FF (see figure 4-15). The output from the set-side of the DFL FF is the SRQ signal (pin 19) to indicate data readiness to the DMA. When the DMA option is not used, the computer checks the DFL FF with a SFS instruction to determine the data ready condition.

3-23. When the data input transfer is made, the DFL FF is cleared with a CLF instruction so that the mag tape 1 and mag tape 2 interface cards are ready to receive the next Control Clock Pulse (CCP) signal. When the DMA option is used, the DFL FF is automatically cleared when the data is input, except on the last word of a DMA transfer.

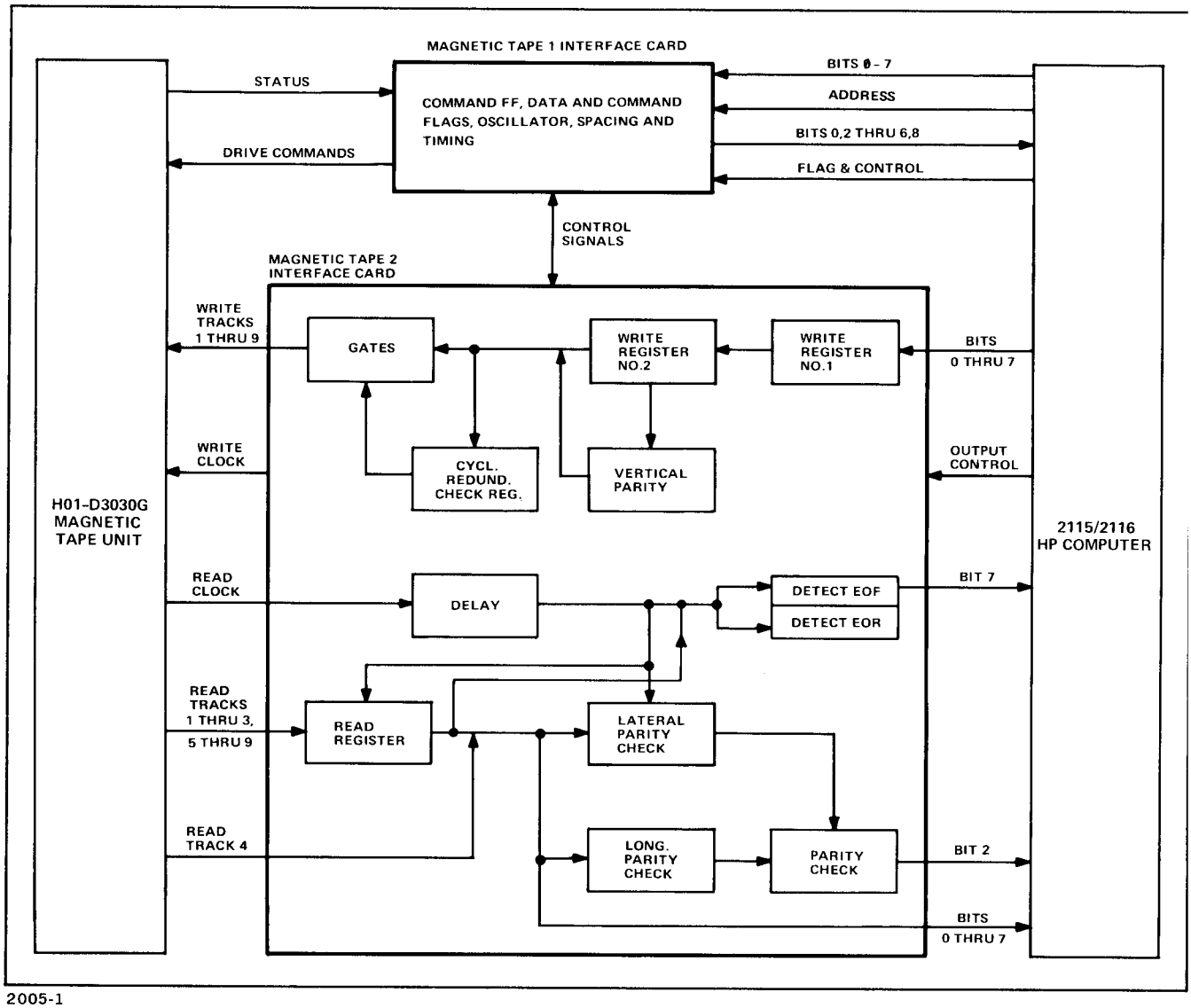
3-24. An end of record (EOR) detection is made when the current record of the magnetic tape no longer has any data characters to transfer. The absence of Read Clock signals from the magnetic tape unit causes the End of Record Control (ERC) FF (see figure 4-17) to set. The longitudinal redundancy check characters and cyclic redundancy check characters, at the end of the data record, are read from the magnetic tape and transferred to the interface cards but data flag signals are not generated. Once an EOR condition is sensed, the tape continuously advances into the Inter-Record Gap (IRG) where forward motion is automatically terminated.

3-25. The EOR signal initiates a 2.2-millisecond delay via MC53. During this delay the FWD motion command remains on. A 5-millisecond delay is then initiated after the motion command is cleared to allow the magnetic tape to come to a complete halt. After this period, the Command Flag Buffer (CFB) and Command Flag (CFL) FFs are set. If the interrupt system is enabled, these FFs cause an interrupt and the computer is alerted that the magnetic tape unit is ready for another operation. If the interrupt system is disabled, the CFL FF should be tested to determine magnetic tape unit readiness.

3-26. OUTPUT OPERATIONS.

3-27. A Write Command signal (true IOBO 0, 3, and 4) must be applied to the mag tape 1 card to initiate the output of data to the magnetic tape unit. The interrupt system will not signal the computer that the magnetic tape unit is ready to accept data. The DMA options or a flag-checking routine is used with the mag tape 1 card.

3-28. Once a Write Command signal is given, the interface cards initiate forward motion of the magnetic tape. After the remainder of a 0.6-inch IRG has been placed on the magnetic tape, a Flag signal is generated which sets the Data Flag Buffer (DFB) FF (see figure 4-15). This signal is combined with the ENF signal at time T2 of the computer



2005-1

Figure 3-2. Magnetic Tape Interface Block Diagram

machine cycle to set the DFL FF. The computer responds with the character to be written and the data is automatically written on the magnetic tape.

3-29. Once the transfer of the character has been made, the DFL FF must be cleared by a CLF instruction or an SRS signal from "nand" gate MC75. This prepares the two interface cards for the next data transfer.

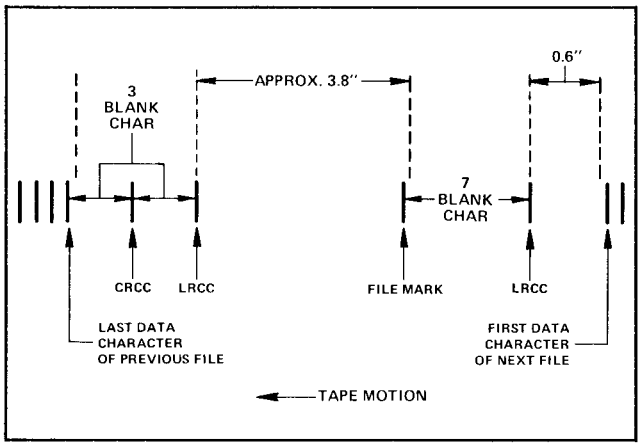
3-30. When the last data character has been output from the computer to the interface cards, the interface cards must signal that no more data will be sent. This is done by clearing the Command Control (CCL) FF on the mag tape 1 card. Three blank characters and the cyclic redundancy check character (CRCC) are automatically placed on the magnetic tape (see figure 3-3). The mag tape 2 card generates three blank characters and writes the longitudinal redundancy check character (LRCC).

3-31. When all cyclic and longitudinal redundancy check characters have been written on tape, a delay allows the magnetic tape to advance into an inter-record gap. The tape is allowed to move forward so that all characters will pass over the read head and a read-after-write parity check can be performed. The magnetic tape is then stopped.

3-32. When a motion command is completed, a 5-millisecond delay is initiated (via MC112 and MC96A) to allow the magnetic tape to come to a complete halt. After this delay, the CFL and CFB FFs are set. If the interrupt system is enabled, an interrupt occurs, indicating that the tape unit is ready for another operation. If the interrupt system is disabled, the CFL FF can be tested to determine tape unit readiness.

3-33. RECORDING (NRZI) TECHNIQUE.

3-34. In NRZI recording (non-return to zero with a flux reversal for every "1"), a flux change represents a logic 1 and a no flux change represents a logic 0. This means that the magnetic tape is magnetized in one direction in all



2005-4

Figure 3-3. Nine-Track File Gap Format

tracks during a gap. Every time a logic 1 is to be recorded in a particular track, the magnetic write-head current is reversed and the tape track is magnetized in the opposite direction. Since the 9-track magnetic tape uses odd vertical parity, there is always at least one flux reversal per character across the magnetic tape. The magnetic tape does not use clock tracks.

3-35. TRACK SPACING AND BIT LOCATIONS.

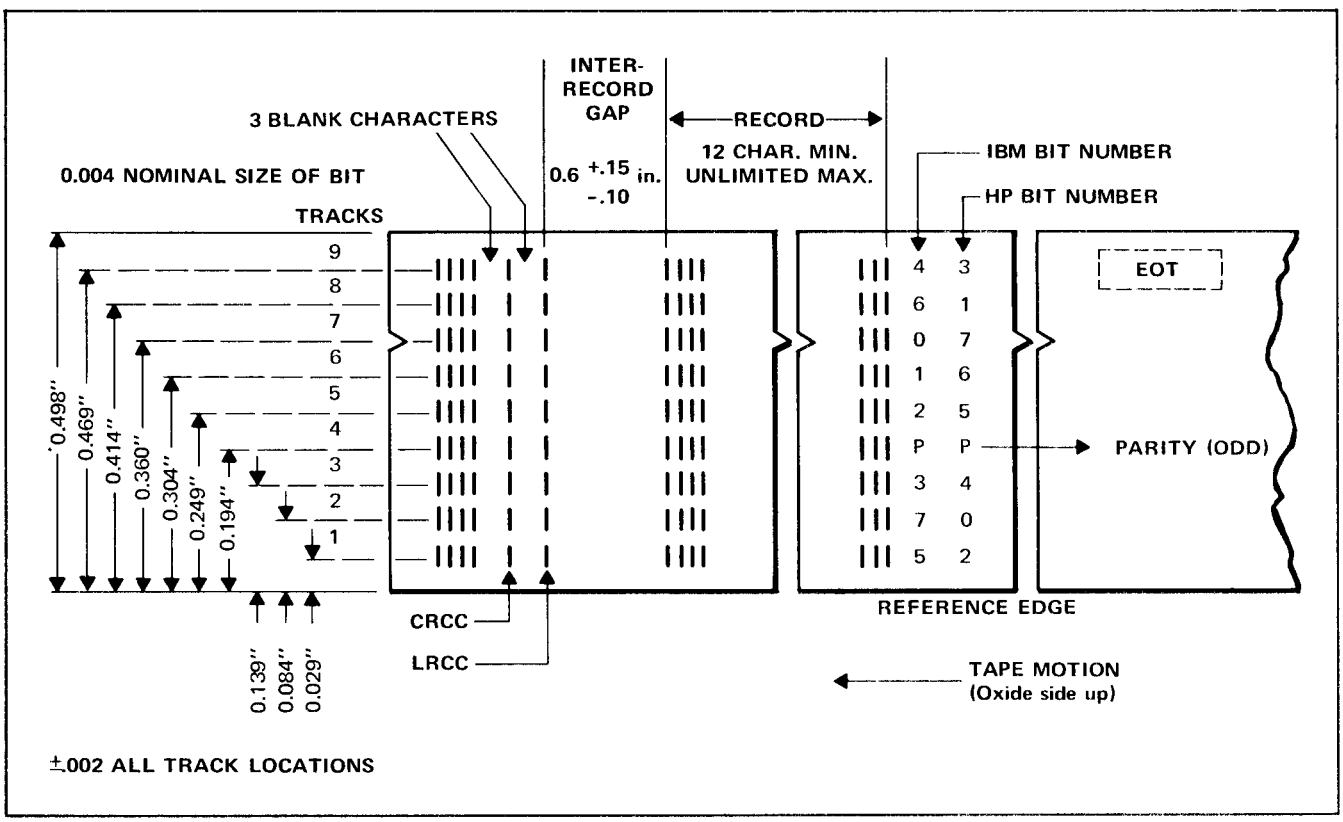
3-36. The nominal spacing from the center of one track to the center of the next track is 0.055 inch. The nominal bit width is 0.048 inch with the bits on the outer edge coming within 0.029 inch of the edge. Since the bits on the outer edge of the tape are less reliable, the least used bits are placed on the outer edges. Figure 3-4 illustrates the spacing, track location, and corresponding HP computer and IBM bit numbers of the magnetic tape.

3-37. RECORD AND GAP LENGTH.

3-38. A record must contain at least 12 data characters. Each record contains a data block, cyclic redundancy check character (CRCC), and a longitudinal redundancy check character (LRCC). The CRCC is spaced four characters from the end of the data block. The LRCC is spaced four characters past the CRCC. Between each record is a 0.6-inch (nominal) IRG.

3-39. VERTICAL PARITY.

3-40. Each nine bits recorded across the width of the tape include eight data bits and a parity bit. Since the number of "ones" in the nine bits are always odd, parity is odd.



2005-5

Figure 3-4. Magnetic Tape Characteristics

3-41. CYCLIC REDUNDANCY CHECK CHARACTER.

3-42. The cyclic redundancy check character (CRCC) (see figure 4-17) consists of nine bits. Figure 3-5 illustrates the relationship between the CRCC bits and the data bits during the addition phase of the CRCC generation. When the CRCC is written on tape, all bits except 3 and 5 are inverted and gated to the data lines. If an even number of characters are written in a record the CRCC will have an odd number of "1" bits. If an odd number of characters are written in a record the CRCC will have an even number of "1" bits. If bit 0 of the CRCC is a logic 0, then a half-add of all data bits and CRCC bits is performed. When the half-add is completed, the CRCC register is rotated to the right one position. If bit 0 of the CRCC is a logic 1, then an addition with a forced carry into bits 3, 4, 5, and 6 is accomplished. Bits 0, 1, 2, 7, and 8 are half-added. At the completion of the process the CRCC register is rotated right one position. Figure 3-6 illustrates how a CRCC is generated.

DATA	7	6	5	4	3	2	1	0	P
CRCC	8	7	6	5	4	3	2	1	0

2005-27

Figure 3-5. Data and CRCC Bit Relationships

3-43. LONGITUDINAL REDUNDANCY CHECK CHARACTER.

3-44. The last check character in a record is the longitudinal redundancy check character (LRCC) and is 9 bits wide. The LRCC register (see figure 4-17) ensures that the number of logic 1's in each track is even for each record. A vertical parity bit is not generated for the LRCC.

3-45. SIGNALS REQUIRED BY THE MAGNETIC TAPE UNIT.

3-46. The magnetic tape unit receives signals from the mag tape 1 and mag tape 2 interface cards through the interconnecting cable. These signals are explained in paragraphs 3-47 through 3-55. Some signals are identified by two names. In these cases, the name within parentheses is that used in the magnetic tape unit documentation.

3-47. FORWARD DRIVE (FORWARD). When this negative-true signal is true, the forward actuator of the magnetic tape unit is pressed against the capstan which moves the magnetic tape from the supply reel, past the read/write head, toward the take-up reel at a speed of 75 inches per second.

CRCR	8 7 6 5 4 3 2 1 0	
WRITE REGISTER	7 6 5 4 3 2 1 0 P	The parity bit (P) is generated whenever there is an even number of logic 1's in the Write Register.
CRCR Contents	0 0 0 0 0 0 0 0 0	CRCR cleared to all logic 0's.
WRITE REGISTER Contents	1 0 1 0 1 0 1 0 1	Bits 0 thru 7 are typical.
CRC ADDER Contents	1 0 1 0 1 0 1 0 1	Half-add the contents of the CRCR and Write Register (see note 2).
CRCR Contents	1 1 0 1 0 1 0 1 0	Rotate the CRC Adder contents to the right one bit.
WRITE REGISTER Contents	0 1 0 1 0 1 0 1 1	Bits 0 thru 7 are typical.
CRC ADDER Contents	1 0 0 0 0 0 0 0 1	Half-add the contents of the CRCR and Write Register (see note 2).
CRCR Contents	1 1 0 0 0 0 0 0 0	Rotate the CRC Adder contents to the right one bit.
WRITE REGISTER Contents	1 1 1 1 1 0 0 0 0	Bits 0 thru 7 are typical.
CRC ADDER Contents	0 0 1 1 1 0 0 0 0	Half-add the contents of the CRCR and Write Register (see note 2).
CRCR Contents	0 0 0 1 1 1 0 0 0	Rotate the CRC Adder contents to the right one bit.
WRITE REGISTER Contents	1 1 1 1 1 1 1 1 1	Bits 0 thru 7 are typical.
CRC ADDER Contents	1 1 1 0 0 0 1 1 1	Half-add the contents of the CRCR and Write Register (see note 2).
CRCR Contents	1 1 1 1 0 0 0 1 1	Rotate the CRC Adder contents to the right one bit.
WRITE REGISTER Contents	0 0 0 0 1 1 1 1 1	Bits 0 thru 7 are typical.
CRC ADDER Contents	1 1 0 0 0 0 1 0 0	See note 3.
CRCR Contents*	0 1 1 0 0 0 0 1 0	Rotate the CRC Adder contents to the right one bit.

NOTES:

1. Shaded areas denote the registers to be added.
2. When bit 0 of the CRCR is a logic 0, half-add the contents of the CRCR and the Write Register.
3. When bit 0 of the CRCR is a logic 1, half-add bits 0, 1, 2, 7, and 8 of the CRCR and the Write Register and add with a forced carry into bits 3, 4, 5, and 6.

* The CRCR will always contain an octal 302 after a good read operation. The contents of the CRCR is unpredictable after a write operation.

2005-23

Figure 3-6. CRCC Generation

3-48. REVERSE DRIVE (REVERSE). When this negative-true signal is true, the reverse actuator of the tape unit is pressed against the capstan which moves the tape from the take-up reel, past the read/write head, toward the supply reel at a speed of 75 inches per second.

3-49. REWIND. When this negative-true signal is true, the tape is wound onto the supply reel until a load point marker is detected. Depending upon the amount of tape on the take-up reel, the tape is moved to the load point at 75 inches per second, or removed from the vacuum chambers and rewound at high speed. The rewind operation is controlled by the magnetic tape unit. The CFB and CFL FFs on the mag tape 1 card are set upon completion of this operation.

3-50. UNLOAD. When this negative-true signal is true, the magnetic tape unit switches to the LOCAL mode and rewinds the tape to the beginning-of-tape (BOT) marker.

3-51. WRITE TRACKS. Each write track driver controls the bit written in that track on the tape during a write operation. The Write Track signals are positive-true.

3-52. WRITE CLOCK. The positive-false Write Clock signal provides the magnetic tape unit with the appropriate data rate. An internal tape unit strobe is triggered on the trailing edge of the Write Clock signal.

3-53. WRITE RESET. When this negative-true signal is true, the write cards in the magnetic tape unit are held in the logic 0 state. When this signal is false, the write cards in the magnetic tape unit are enabled for switching.

3-54. WRITE ENABLE (WRITE PERMIT). When this negative-true signal is true, current flows in the write head so the magnetic tape can be magnetized.

3-55. READ RESET. When this negative-true signal is true, the read cards located in the magnetic tape unit are held in the reset state in order to space over gaps.

3-56. SIGNALS SUPPLIED BY THE MAGNETIC TAPE UNIT.

3-57. The magnetic tape unit supplies signals to the computer through the interconnecting cable to the mag tape 1 and mag tape 2 cards. These signals are explained in paragraphs 3-58 through 3-64. Some signals are identified by two names. In these cases, the name within parentheses is that used in the magnetic tape unit documentation.

3-58. $\overline{\text{AUTO}}$ (READY STATUS). This positive-false signal is true when the magnetic tape unit is in the AUTO mode and false when the magnetic tape unit is in the LOCAL mode. When the magnetic tape unit is in the AUTO mode, the computer can write or read from the magnetic tape unit. When the magnetic tape unit is in the LOCAL mode, the magnetic tape will not move and the writing or reading of data is inhibited.

3-59. $\overline{\text{LOAD POINT}}$ (LOAD POINT STATUS). When this positive-false signal is true, the tape is positioned so that the reflective beginning-of-tape (BOT) marker is under the photo cell. There may be more than one BOT marker on the magnetic tape.

3-60. $\overline{\text{WRITE ENABLED}}$ (WRITE ENABLE STATUS). This positive-false signal is true when there is a write ring installed in the magnetic tape supply reel.

3-61. $\overline{\text{EOT}}$ (END-OF-TAPE STATUS). This positive-false signal is true when the photo cell detects a reflective end-of-tape (EOT) marker and until the tape unit receives a Rewind Command signal. There may be more than one EOT marker on the magnetic tape.

3-62. $\overline{\text{REWIND}}$ (REWIND STATUS). This positive-false signal is true during a rewind operation.

3-63. READ CLOCK. The positive-false Read Clock signal is a data rate pulse generated from an "or" function of all read cards in the magnetic tape unit. A Read Clock signal occurs each time a single data bit is detected by the tape unit.

3-64. READ TRACKS. The positive-false Read Track signals are transferred from the magnetic tape unit to the mag tape 2 card.

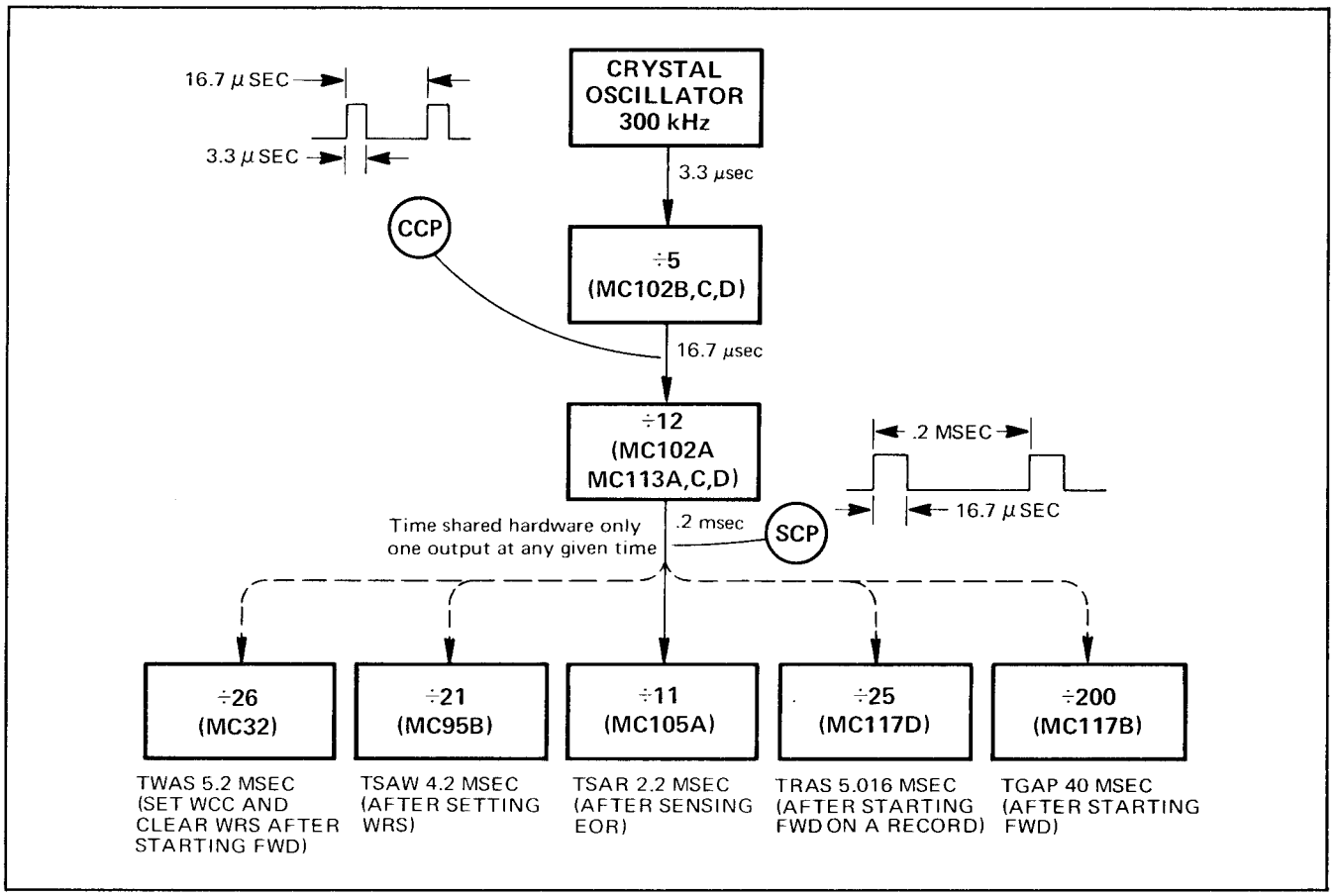
3-65. MAGNETIC TAPE INTERFACE TIMING FORMAT.

3-66. Figure 3-7 is a block diagram of the magnetic tape interface timing format. The operating frequency of the crystal oscillator on the mag tape 1 card is 300 kHz. This oscillator generates all clock signals used by the magnetic tape unit. The 300-kHz signal is reduced to 60 kHz by the divide-by-five circuit (see figure 4-15) MC102B, C, and D which forms the Clock Control Pulse (CCP) signal. This signal is further reduced to 5 kHz by the divide-by-twelve circuits MC102A and MC113A, C, and D. The 5-kHz signal is transferred through "nand" gates MC114C and MC92C and forms Spacing Clock Pulse (SCP) signal. The SCP signal is transferred through spacing counters MC112 and MC103B, C, D, forming various clock pulses which are used with time-shared hardware on the interface cards.

3-67. WRITE OPERATION.

3-68. A flow chart illustrating a write operation is shown in figure 4-8. Refer to this flow chart and the write operation timing diagram shown in figure 3-8 for a better understanding of a write operation.

3-69. Under program control, a write command is applied to the mag tape 1 card. This command word consists of IOBO 0 (Motion), IOBO 3 (Write), and IOBO 4 (Transfer Data) of the eight-bit command word. These bits are a logic 1 (octal 31 of the eight-bit command word) after the write command is executed.



2005-6

Figure 3-7. Magnetic Tape Interface Timing Format

3-70. Motion bit 0 is applied to pin 35 of the mag tape 1 card (see figure 4-15) and transferred through "nand" gates MC55C and MC55D. The output from gate MC55D is applied to pin 12 of "nand" gate MC56B. This gate determines if the magnetic tape unit is in the LOCAL mode of operation and if the mag tape 1 card is ready to accept a new instruction. If the magnetic tape unit is in the LOCAL mode of operation or the mag tape 1 card is not ready to accept the write command, the Reject FF is set. When this occurs, the logic 1 output from the set-side of the Reject FF is transferred through "and" gate MC107A to the computer (IOBI 3 true), inhibiting the command word. If the magnetic tape unit is in the AUTO mode of operation and the mag tape 1 card is ready to accept the write command, "nand" gate MC46B is enabled. The output from this gate is transferred through "nand" gate MC54D, forming the Motion (MOT) signal. The MOT signal is applied as one true input to "nand" gate MC62B. This gate is enabled when the Write bit (IOBO 3) is a logic 1 and the Write Enabled Status (WES) signal is a logic 1 (write ring is installed on the supply reel which is mounted on the magnetic tape unit). The output of MC62B is applied to the set-side input of the Write (WRT) FF, causing the FF to be set. The output from the set-side of the WRT FF and the MOT signal are transferred through "and" gate MC53D and "nor" gate MC53F. The logic 0 output from "nor" gate MC53F is transferred to the direct-set input of the Forward FF, setting the FF. The output from the set-side of the Forward FF (pin 15), is transferred through pin 8 of the 48-pin connector to the mag tape 2 card as the Forward (FWD) signal. The output from pin 15 of MC115 is also transferred through transistor Q5 and pin 21 of the 48-pin connector to pin 2 of connector P1 of the magnetic tape unit as the Forward Drive signal. The same signal from "nor" gate MC53F which set the Forward FF is also applied to pin 6 of "nand" gate MC75. The output from this gate is the Start-Reset (SRS) signal which has a pulse width of 200 nanoseconds. The SRS signal does the following (see figure 4-15):

a. Resets the divide-by-two counter MC102A.

b. Resets the divide-by-five counter MC102B,C, and D.

c. Clocks the Ready (RDY) FF to the clear state.

d. Sets the Three-Inch Gap Control FF (MC116A) if the magnetic tape is positioned at the load point. If MC116A becomes set, the Write Timing Control (WTC) signal is inhibited by "nand" gate MC86D and clearing of the Read Reset (RRS) FF is inhibited by gate MC117C. This allows 3-1/2 inches of tape to be moved prior to attempting to write data.

e. Clears the Timing (TIM) FF through gates MC42B and MC42C.

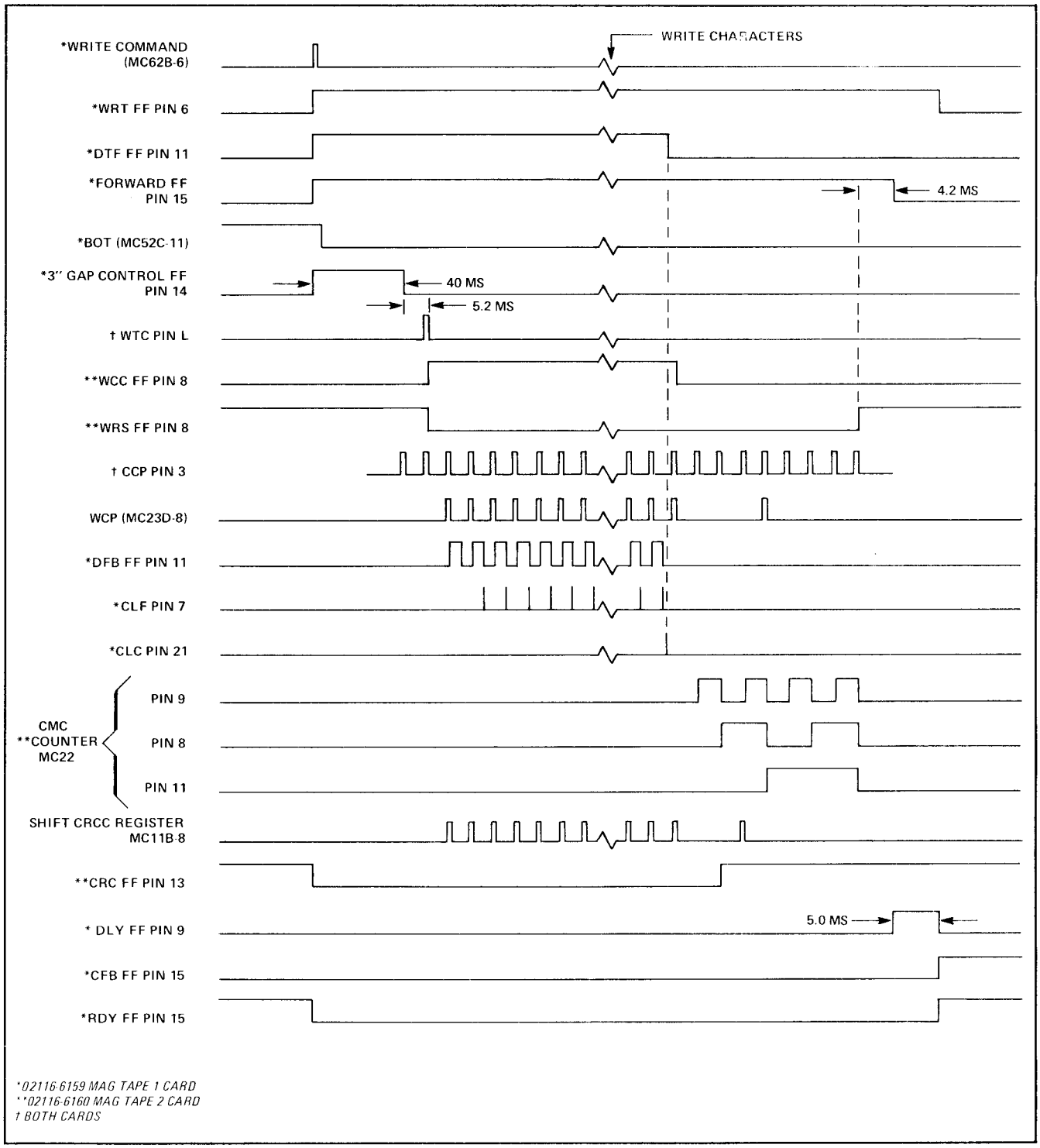


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Figure 3-8. Write Operation Timing Diagram

f. The SRS signal is gated with the Transfer Data signal (bit 4 of the command word) at "nand" gate MC32D; the output of which directly sets the Data Transfer (DTF) FF and generates the $\overline{\text{Set Parity Control}}$ ($\overline{\text{SPC}}$) signal.

g. The $\overline{\text{SPC}}$ signal from pin D of the mag tape 1 card is transferred through pin D of the mag tape 2 card (see figure 4-17) and does the following:

(1) Sets the Parity Control (PTC) FF.

(2) Clears the Data Flag Buffer (DFB) FF through gates MC34B, MC34C, MC23D and MC23C.

(3) Clears the Command Flag (CFL) FF through gates MC36D and MC36F.

h. The SRS signal is transmitted to the mag tape 2 card through pin 7, where it resets the divide-by-sixteen counter, MC63, and is applied to "nand" gates MC74A and MC74B. The $\overline{SRS}$ output of "nand" gates MC74A and MC74B does the following:

(1) Clears the Cyclic Redundancy Check Character (CRCC) Register.

(2) Clears the Cyclic Redundancy Character (CRC) FF.

(3) Clears the Write Clock Control (WCC) FF.

(4) Sets the Write Reset (WRS) FF.

(5) Clears the Parity (PTY) FF.

(6) Clears the Longitudinal Redundancy Check Character (LRCC) Register.

(7) Clears the Read Record Control (RRC) FF.

(8) Clears the End-of-Record Control (ERC) FF.

(9) Clears the End-of-File (EOF) FF.

(10) Clears the End-of-Record (EOR) FF.

3-71. The WRS and WRT signals (see figure 4-15) are applied to the input of "and" gate MC94D. When these signals are true, "and" gate MC94D is enabled. The output from this gate is transferred through "nor" gate MC94F, inverted and transferred to the input of "nand" gate MC104A where the signal is again inverted. The true output from "nand" gate MC104A is transferred to the input of "and" gate MC94B. This gate is then enabled when the FWD signal is true. The output from "and" gate MC94B is inverted in "nor" gate MC94C and resets the divider network consisting of MC93, MC103, and MC113A, B, and C.

3-72. The Three-Inch Gap Control FF is set when the magnetic tape is positioned at the load point and cleared by the output signal from "nand" gate MC117B and the CCP signal after 3-1/2 inches of magnetic tape has been moved. When this FF is clear, the WTC signal is enabled by "nand" gates MC86D and MC85D and "nand" gate MC117C is enabled. On receipt of the next A2 timing signal the RRS FF is cleared (via "nand" gates MC117C and MC117D) which removes the Read Reset signal to the magnetic tape unit. This allows the read circuits to detect the presence of data on the magnetic tape. Even though a write operation is being processed, the magnetic tape unit is capable of reading data immediately after it has been written.

3-73. When the next 200-microsecond SCP signal is generated, the WTC signal is transferred through pin L of the mag tape 1 card to pin L of the mag tape 2 card and to the set-side of the WCC FF (see figure 4-17). The other inputs to the set-side of the WCC FF are the A2 timing signal and the output from "nand" gate MC42A. The WCC FF is then clocked set by the CCP signal. The output from the clear-side of the WCC FF is transferred through "nand" gates MC23C and MC23D to the base of transistor Q10, turning the transistor on. With Q10 on, the Write Clock signal is transferred through connector pin Z of the mag tape 2 card to pin 11 of connector P4 of the magnetic tape unit enabling the write character timing signals.

3-74. At the same time that the WCC FF is set the WRS FF is cleared. When this occurs, a logic 0 signal is transferred through connector pin 5 of the mag tape 2 card to connector pin 5 of the mag tape 1 card and applied to pin 13 of "and" gate MC94D (see figure 4-15). This gate is disabled and the output transferred through "nor" gate MC94F and "nand" gate MC104A. The logic 0 output from "nand" gate MC104A is transferred through "and" gate MC94B and "nor" gate MC94C, resetting the divider network consisting of MC93, MC103, and MC113.

3-75. The false (logic 0) WRS signal also disables "nand" gate MC86D and turns transistor Q3 on. The output from Q3 is transferred through connector pin 19 of the mag tape 1 card to pin 12 of connector P4 of the magnetic tape unit. This allows the write circuit to change states, depending on the data being written.

3-76. The output from "nand" gate MC86D is transferred through "nand" gate MC85D as a logic 0 signal. This signal is then transferred through connector pin L of the mag tape 1 card to connector pin L of the mag tape 2 card. The WTC signal is then transferred to the set-side of the WCC FF (see figure 4-17) disabling the FF. The logic 0 WTC signal is also applied to the clear-side of the WRS FF, clearing the FF. At the same time that the WRS FF is cleared, a Set Flag Buffer (SFB) signal is generated at the output of "nand" gate MC12C. This signal is transferred through connector pin J of the mag tape 2 card to connector pin J of the mag tape 1 card. The SFB signal clocks the Data Flag Buffer (DFB) FF (see figure 4-15) to the set state when the Data Transfer (DTF) FF is set. At the next time T2 of the computer machine cycle, the Data Flag (DFL) FF is set. The mag tape 1 and mag tape 2 interface cards are now ready to accept the first character of data under program control.

3-77. When a write operation is completed and an interrupt request is desired, the program must execute a Set Control (STC) command to the command channel (mag tape 2 card). Each time a data character is transferred to the data channel (mag tape 1 card) the Data Flag (DFL) must be cleared. The data character is transferred via the IOBO lines into Write Register 1 (see figure 4-17) which consists of eight FFs. The outputs from the set-side of these FFs are applied to the set-side inputs of Write Register 2 and to the adder circuits in the CRCC Register. When the next CCP is generated, the data in Write Register 2 is transferred through the Data Output Gates and the Write Track Inverters to the magnetic tape unit. The adders in the CRCC Register are also clocked into the CRCC Register FFs.

3-78. When the WCC FF is clear, a logic 0 signal is transferred through "nand" gates MC12B and MC12C, generating the SFB signal. This signal is transferred through connector pin J of the mag tape 2 card to connector pin J of the mag tape 1 card. The SFB signal clocks the DFB FF (see figure 4-15) to the set state when the DTF FF is set. At the next time T2 of the computer machine cycle, the DFL FF is set, again indicating that the mag tape 1 and mag tape 2 interface cards are ready to accept another data character under program control. Once the last data character has been transferred, it must be followed by a Clear Control (CLC) instruction to the data channel (mag tape 1 card). The CLC instruction resets the DTF FF, indicating the end of the transmission of data.

3-79. When the next CCP signal occurs, the WCC FF (see figure 4-17) is cleared. This inhibits the Write Clock signal to the magnetic tape unit through "nand" gates MC23C and MC23D and transistor Q10. With the WCC FF and the WRS FF clear, the reset input to the CMC divide-by-eight counter (MC22 pin 2) is removed. This allows the counter to begin counting the CCP signals. After two CCP signals have been counted, the Cyclic Redundancy Character (CRC) FF is set. This allows the contents of the CRCC Register to be transferred to the Data Output Gates (replacing the outputs from the FFs of Write Register 2). During this transfer, all bits of the CRCC Register are inverted except bits three and five. When the CMC counter (MC22) has counted three CCP signals, "nand" gate MC11A outputs a logic 0 which is transferred to the direct-clear inputs of the Write Register 1 FFs. All FFs in the register are then cleared. The logic 0 output from "nand" gate MC11A is inverted through "nand" gate MC18B and applied as a clock input to the Write Register 2 FFs. The outputs from the Write Register 1 FFs are then shifted into the Write Register 2 FFs. This ensures that both write registers are reset to the logic 0 state and that the CRC signal is the only signal present in the Data Output Gates.

3-80. The Write Clock signal is again enabled via "nand" gates MC43A, MC23C, and MC23D and transistor Q10. This allows a Write Clock signal to be generated in order to write the CRCC onto the magnetic tape. When the fourth CCP signal has been counted the Write Clock signal is disabled again. When the eighth CCP signal has been counted the WRS FF is set. The set-side output of the WRS FF is transferred through connector pin 5 of the mag tape 2 card to connector pin 5 of the mag tape 1 card. This true WRS signal is applied to the base of transistor Q3 (see figure 4-15), turning the transistor off. This allows the Write Reset signal to change the write circuits in the magnetic tape unit to the logic 0 state and allows the LRCC to be written onto the magnetic tape.

3-81. The true WRS and WRT signals are applied to the input of "and" gate MC94D, enabling the gate. The true output from this gate is transferred through "nor" gate MC94F and "nand" gate MC104A and applied to the input of "and" gate MC94B. The other true input to "nand" gate MC94B is the FWD signal. The gate is then enabled and the true output is transferred through "nor" gate MC94C where the output on pin 6 is inverted and applied to the reset-side of counters MC93, MC103, and MC113E. This removes the reset level that had been applied to the counters. When the output of the divide-by-two counter (MC93B, C, D) is true, "nand" gate MC95B is enabled. The output from this gate is inverted in "nand" gate MC105B, forming the "not" Stop After Write ($\overline{SAW}$) signal. This signal is applied to the clear input of the Reverse FF, the Forward FF, and the DLY FF. When the next CCP signal is generated, the Forward FF is clocked clear which removes the Forward Drive signal to the magnetic tape unit through transistor Q5 and connector pin 21 of the mag tape 1 card. The tape movement stops within 2 milliseconds.

3-82. The DLY FF is cleared at the same time that the Forward FF is cleared. When this occurs the reset input to the divide-by-sixteen counter MC112 is removed and the counter begins counting the Spacing Clock Pulse (SCP) signals. After 16 SCP signals have been counted, FF MC96A is set and the set-side output is applied to "nand" gate MC86A. After nine more SCP signals are counted, "nand" gate MC86A is enabled. The logic 0 output from this gate is applied to the input of "nand" gate MC76D. The logic 1 output from this gate is the Set-Reset Pulse (SRP) signal. This signal is applied to the set-side input of the DLY FF and to "and" gate MC72A. The SRP signal is transferred through "and" gate MC72A and input to "nor" gate MC72C. The output from this gate is the $\overline{SRP}$ signal which clears the WRT FF and direct-sets the RRS FF.

3-83. When the RRS FF is set, the output from the clear-side of the FF is transferred through "nand" gate MC106D as a logic 1 and applied to the base of transistor Q1, turning it off. With Q1 turned off, a negative-true Read Reset signal is applied through connector pin T of the mag tape 1 card to the magnetic tape unit. When this occurs, the read circuits in the magnetic tape unit are held in the reset state.

3-84. When the WRT FF is cleared, the output from the set-side of the FF disables "and" gate MC94D, thereby restoring the reset inputs to the divider network consisting of MC93, MC103, and MC113. On the next CCP signal, the DLY FF is set. The SRP signal from the output of "nand" gate MC76D is applied as a clock input to the CFB FF. Since the input to the set-side of the FF is connected to +4.5 volts, the FF will switch to the set state. At the next time period T2 of the computer machine cycle, the ENF signal is inverted and applied to the set-side of the CFL FF, setting the FF. If the end-of-operation interrupt feature has been selected, the Command Control (CCL) FF is set by program control. If the interrupt system is enabled and the magnetic tape interface cards have the highest priority on the interrupt chain, the SIR signal becomes true at the next time period T5 of the computer machine cycle. When this occurs "nand" gate MC25 is enabled, making the output on pin 8 a logic 0. This logic 0 is applied to the set-side of the Command Interrupt (CIR) FF, setting the FF. Once this FF is set, the necessary Flag and IRQ signals are generated and transferred to the I/O Address card located in the computer. The computer will then enter an interrupt sequence.

Note

During a write or a read operation, the DTF FF must be cleared each time a data character is output from the computer. If this sequence is not followed, the TIM FF sets and causes a timing error status indication (IOBI 0) to the computer.

3-85. READ OPERATION.

3-86. A flow chart illustrating a read operation is shown in figure 4-10. Refer to this flow chart and the read operation timing diagram shown in figure 3-9 for a better understanding of a read operation.

3-87. Under program control a read command is applied to the mag tape 1 card. This command word consists of IOBO 0 (Motion), IOBO 1 (Forward), and IOBO 4 (Transfer Data) of the eight-bit command word. These bits are a logic 1 (octal 23 of the eight-bit command word) when the RCC command is enabled.

3-88. Motion bit 0 is applied to pin 35 of the mag tape 1 card (see figure 4-15) and transferred through "nand" gates MC55C and MC55D. The output from gate MC55D is applied to pin 12 of "nand" gate MC56B. This gate determines if the magnetic tape unit is in the LOCAL mode of operation and if the mag tape 1 card is ready to accept a new instruction. If the magnetic tape unit is in the LOCAL mode of operation or the mag tape 1 card is not ready to accept the read command, the Reject FF is set. When this

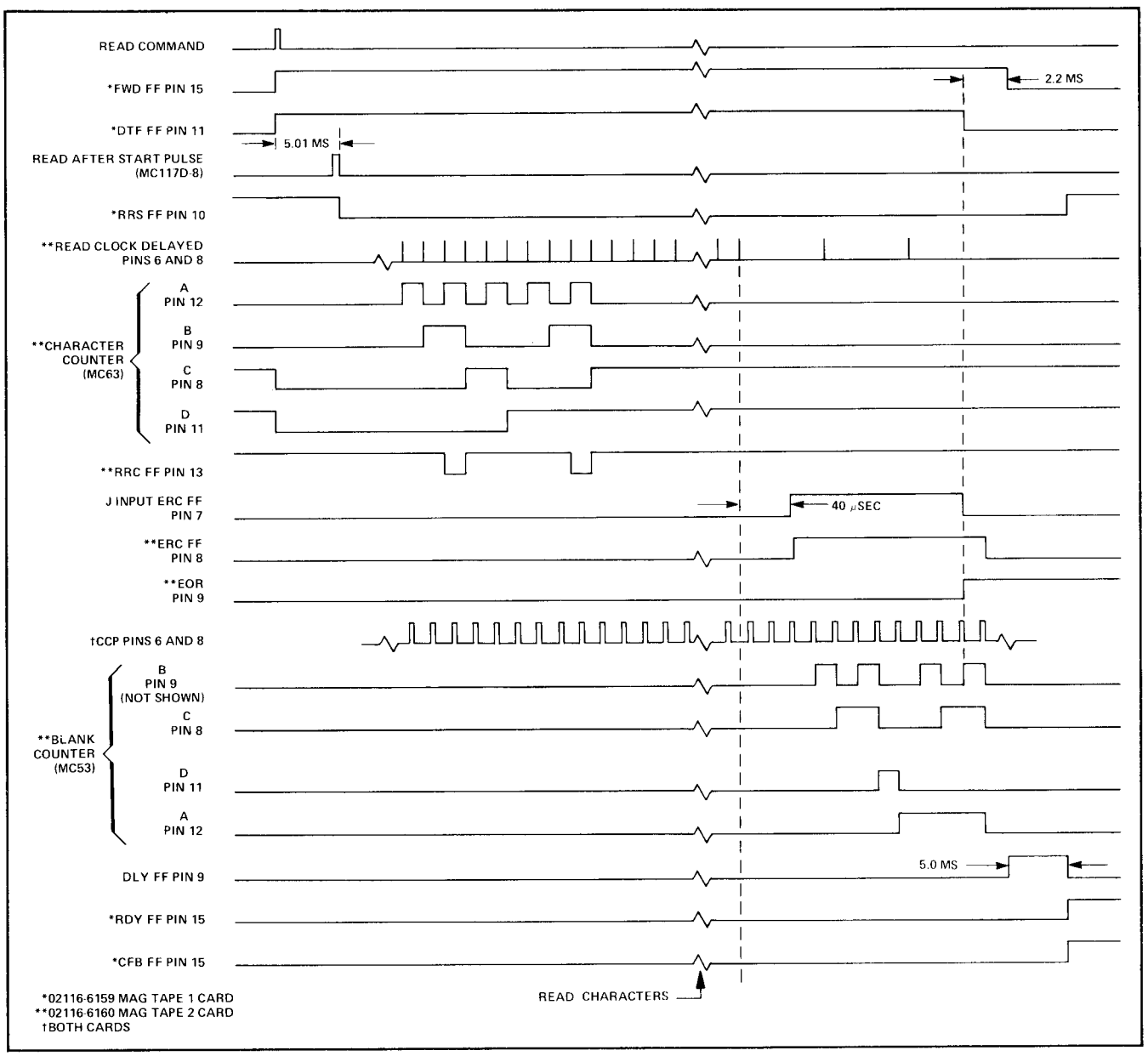

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Figure 3-9. Read Operation Timing Diagram

occurs, a logic 1 output from the set-side of the Reject FF is transferred through "and" gate MC107A to the computer (IOBI 3 true), inhibiting the command word. If the magnetic tape unit is in the AUTO mode of operation and the mag tape 1 card is ready to accept the read command, "nand" gate MC46B is enabled. The output from this gate is transferred through "nand" gate MC54D, forming the Motion (MOT) signal. This signal is applied as one true input to "and" gate MC53E. The other input to this gate is the Forward bit (IOBO 1). When both of these inputs are a logic 1, "and" gate MC53E is enabled. The output from this gate is transferred through "nor" gate MC53F and applied to the direct-set input of the Forward FF, setting the FF. The output from the set-side of this FF is transferred to the base of transistor Q5, turning the transistor off. With transistor Q5 turned off, the Forward Drive signal is transferred through pin 21 of the 48-pin connector to pin 2 of connector P1 of the magnetic tape unit. The same signal from "nor" gate MC53F which set the Forward FF is also applied to pin 6 of "nand" gate MC75. The output from this gate is the SRS signal which has a pulse width of 200 nanoseconds. Refer to paragraph 3-70, steps "a" through "h" for a list of functions that the SRS signal performs.

3-89. If the tape is positioned at the load point, the Load Point Status signal is transferred through pin 17 of the 48-pin connector of the mag tape 1 card and applied to "nand" gate MC52C. The output on pin 11 of this gate is the Beginning of Tape (BOT) signal. This signal is transferred through "nand" gates MC52D, MC106B, and MC95A to the direct-set input (pin 2) of the Three-Inch Gap Control FF, setting the FF. This causes the magnetic tape to move forward 3-1/2 inches before any attempt is made to check the presence of data on the magnetic tape. If the magnetic tape is not positioned at the load point, the Three-Inch Gap Control FF is direct-cleared at pin 3 of the FF via "nand" gates MC52C, MC52D, MC106B, MC106A, and MC106C. The output from the clear-side (pin 14) of the Three-Inch Gap Control FF is applied to pin 12 of "nand" gate MC117C. The other input to pin 13 of this gate is the A2 signal. When both signals are true, "nand" gate MC117C is enabled. The output from this gate is inverted and transferred to pins 8 and 9 of "nand" gate MC117D. The output from this gate is inverted and applied to the clear-side of the RRS FF, resetting the FF. On the generation of the next CCP signal the RRS FF is cleared. The output from the clear-side of the FF is transferred through "nand" gate MC106D where the signal is inverted and applied to the base of transistor Q1, turning the transistor on. With transistor Q1 turned on, a Read Reset signal of approximately 4 volts is transferred through pin T of the 48-pin connector to pin 12 of connector P5. This allows the read circuits in the magnetic tape unit to detect the presence of data on the magnetic tape.

3-90. As the magnetic tape is moved past the read head in the magnetic tape unit, the first data bit detected causes the magnetic tape unit to generate a Read Clock signal. This positive-false signal is transferred through pin 11 of connector P5 to pin 22 of the 48-pin connector of the mag tape 2 card (see figure 4-17). When a positive Read Clock signal (+10 volts) is applied, the +10 volts is transferred through resistor R41, placing approximately +5 volts at the cathode of diode CR10. The 22-volt potential between the +10 volt signal and the -12 volt supply is dropped between resistors R41 and R42, causing CR10 to go toward a back-biasing condition. This causes a higher positive potential to appear at the base of transistor Q11, turning it on. With Q11 on, transistor Q12 is turned off. As Q12 turns off, a variation in voltage across resistor R43 and capacitor C1 keeps Q11 on for 8 microseconds. This 8-microsecond delay allows the read amplifiers in the magnetic tape unit to settle. When Q11 changes state there is a 5.5-volt drop across capacitor C2 for 1.2 microseconds. A negative potential on the base of transistor Q13 turns the transistor off. With Q13 off, transistor Q14 is turned on. With Q14 on, a negative potential is transferred to the input of "nand" gates MC105A and MC105B. The output from these gates is inverted and called the Read Clock Delayed (RCD) signal. Data is shifted into the Read Register on the leading edge of the RCD signal. The RCD signal does the following:

a. Clocks the Longitudinal Redundancy Check Character Register FFs.

b. Clocks the Read Register FFs.

c. Clocks the Parity (PTY) FF.

d. Clocks the Read Record Control (RRC) FF.

e. Generates the Set Flag Buffer (SFB) signal through "nand" gates MC72C and MC12C.

f. Steps divide-by-sixteen counter MC63 via "nand" gates MC92A and MC92B.

3-91. The positive-false Read Track signals (RT1 through RT9) are transferred from the magnetic tape unit to the mag tape 2 card. These signals are transferred through the Read buffers and applied to the following circuits:

a. The Vertical Parity Check circuit.

b. The Longitudinal Redundancy Check Character Register.

c. The Read Register.

3-92. The Read Control circuit detects the absence of two consecutive Read Clock signals. A Read Clock signal is transferred through the Read Clock Delay and Power Gates circuit and output on the collector of transistor Q14 as a $\overline{\text{RCD}}$ signal. This signal is transferred to pin 11 of "nand" gate MC103C, disabling the gate and making the output on pin 8 a logic 1. At the same time that the $\overline{\text{RCD}}$ signal is applied to "nand" gate MC103C, the RCD signal is transferred through "nand" gates MC92A and MC92B and applied to pin 14 of divide-by-sixteen counter MC63. This steps the counter one count.

3-93. The logic 1 output on pin 8 of "nand" gate MC103C is transferred to the base of transistor Q15, turning it on. The output (gnd) on the collector of Q15 is transferred to the base of transistor Q16, turning it on. With Q16 on, transistor Q17 is turned off which applies a negative potential to the set-side input of the ERC FF. The output from the clear-side of this FF is transferred to pin 10 of "nand" gate MC72C. The other two inputs to this gate are the WRT signal and the RCD signal. When these signals are in a true state, "nand" gate MC72C is enabled. The logic 0 output from this gate is applied to "nand" gate MC12C. The logic 1 output from this gate is transferred to pin J of the 48-pin connector as the Set Flag Buffer (SFB) signal. This signal is transferred from pin J of the mag tape 2 card to pin J of the mag tape 1 card. The SFB signal is then transferred from pin J of the mag tape 1 card to the clock input of the DFB FF (see figure 4-15) and the Timing (TIM) FF, setting the FFs. The output from the set-side of the DFB FF is transferred to pin 9 of "nand" gate MC35D. The other input to this gate is the ENF signal. At the next time period T2 of the computer machine cycle the DFL FF is set. The output from the set-side of this FF is transferred to pin 1 of "nand" gate MC57A. The other true inputs of this gate are the SFS signal on pin 2 and the ADSD signal on pin 13, enabling the gate. The output on pin 12 of "nand" gate MC57A is transferred through "nand" gate MC46A and "and" gate MC47A and output on pin 12 of the 86-pin connector as the SKF signal. This indicates to the computer that a data character is in the Read Register (see figure 4-17). If the computer is under DMA control, the output from the set-side of the DFL FF (see figure 4-15) is output on pin 19 of the 86-pin connector as the SRQ signal. This indicates to the DMA that a data character is in the Read Register (see figure 4-17).

3-94. The data character read from the magnetic tape is checked for a vertical parity which should always be odd. If a vertical parity is detected, the Parity (PTY) FF is set on the trailing edge of current RCD signal. If the first data character within a record is an octal 23, then it is possible that the record being read is a file mark record. If this record is a file mark record, then the next two consecutive frames will be blank, causing the ERC FF to be set. If the next two frames are not blank, then the character will be read as data. Succeeding data characters are read in the same manner.

3-95. If less than 12 data characters are read before the two blank frames are detected, an illegal record length occurs, parity errors are generated, and more than one record of data will be read (see figure 4-11). If 12 or more characters are read, the RCD signal is transferred through "nand" gate MC103C and applied to the base of transistor Q15. The signal is then transferred through transistors Q16 and Q17 to the set-side of the ERC FF, setting the FF. When the ERC FF is set the output from the clear-side of the FF is transferred through "nand" gates MC72C and MC12C, inhibiting the SFB signal. The output from the clear-side of the ERC FF also inhibits the Parity (PTY) FF. With the ERC FF in the set state, divide-by-ten counter MC53 is also enabled. After seven CCP signals have been counted, the End-of-File (EOF) FF is set and the longitudinal parity is checked. If an error occurs, the PTY FF is set and Parity Error status bit IOBI 1 at pin 29 of the 86-pin connector becomes true. Since the ERC FF is set, the End-of-Record (EOR) FF is set via pin 12 of divide-by-ten counter MC53 and the output of "nand" gate MC43B. When the EOR FF is set, the clear-side output is transferred through "nand" gate MC23A, clearing the ERC FF on the next CCP signal. When the ERC FF is cleared, divide-by-ten counter MC53, the EOR FF, and the Parity Control (PTC) FF are cleared.

3-96. The set-side output of the EOR FF is transferred through pin 10 of the 48-pin connector of the mag tape 2 card to pin 10 of the 48-pin connector of the mag tape 1 card. The EOR signal is applied to pin 9 of "and" gate MC42E (see figure 4-15). The other true input to this gate is the $\overline{\text{WRT}}$ signal which is applied to pin 10, enabling the gate. The true output is transferred through "nor" gate MC42F where the signal is inverted and applied to the direct-clear input (pin 8) of the Data Flag (DTF) FF, clearing the FF. The EOR and $\overline{\text{WRT}}$ signals are also applied to "and" gate MC94E, enabling the gate. The true output is transferred through "nor" gate MC94F where the signal is inverted and applied to pin 1 of "nand" gate MC104A. The output on pin 3 of "nand" gate MC104A is again inverted and applied to pin 4 of "and" gate MC94B. The other input on pin 5 of this gate is the Forward (FWD) signal, which enables the gate. The output from this gate is transferred through "nor" gate MC94C, inverted and applied to the divider network. A logic 0 is then applied to pin 2 of dividers MC93 and MC103 and pin 6 of divider MC113, removing the reset condition of the dividers.

3-97. The Spacing Clock Pulse (SCP) signal is generated at the output of "nand" gate MC92C. This signal is applied to pin 4 of "nand" gate MC105A. The other inputs to this gate are the EOR signal, $\overline{\text{WRT}}$ signal, and the C output from the divide-by-two counter (MC93B, C, D). The output on pin 6 of "nand" gate MC105A is the Stop After Read (SAR) signal and is applied to pin 9 of "nand" gate MC105B. The other inputs to this gate are the Stop After Gap (SAG) signal, the Stop After Write (SAW) signal, and the output from "nand" gate MC104B. When "nand" gate MC105B is enabled, the logic 1 output on pin 8 is applied to the clear input of the Reverse FF, the Forward FF, and the Delay (DLY) FF. These FFs are cleared when the next CCP signal is received at the clock inputs of the FFs.

3-98. When the Forward FF is cleared, a logic 0 is output on pin 15 of the set-side of the FF and transferred to the base of transistor Q5, turning the transistor on. With Q5 on, a logic 0 (ground potential) is transferred through pin 21 of the 48-pin connector to pin 8 of connector P1 of the magnetic tape unit. This stops the forward motion of the magnetic tape within 2 milliseconds.

3-99. When the Delay (DLY) FF is cleared, a logic 0 is output on pin 9 of the set-side of the FF and is transferred to pin 2 of the divide-by-sixteen counter (MC112). This removes the reset level from the counter, allowing the

Spacing Clock Pulse (SCP) signal to begin counting. After 16 SCP signals have been counted, the DLY FF is set. After nine more SCP signals have been counted, "nand" gate MC86A is enabled and the output on pin 6 becomes a logic 0. This logic 0 is transferred to the direct-set input (pin 2) of the Ready (RDY) FF, setting the FF.

3-100. The output from "nand" gate MC86A is also transferred through "nand" gate MC76D. The logic 1 output on pin 8 of this "nand" gate is the Stop Reset Pulse (SRP) signal. This signal provides a set input to the DLY FF which is clocked to the set-state on the trailing edge of the next CCP signal. The SRP signal is also applied to "and" gate MC72A, enabling the gate. The output from this gate is transferred through "nor" gate MC72C and applied to the direct-set input (pin 7) of the Read Reset (RRS) FF, setting the FF. With the FF set, a logic 0 is output on pin 10 of the clear-side of the FF and transferred to pin 9 of "nand" gate MC106D. The logic 1 output on pin 8 of this gate is transferred to the base of transistor Q1, turning the transistor on. With Q1 on, a logic 0 (positive potential) is transferred through pin T of the 48-pin connector to pin 12 of connector P5 of the magnetic tape unit. This negative-true signal causes the read circuits in the magnetic tape unit to be disabled.

3-101. The SRP signal is also transferred to pin 1 of the Command Flag Buffer (CFP) FF as a clock input, setting the FF. The set-side output on pin 15 is applied to pin 5 of "nand" gate MC45B. The other input on pin 4 of this gate is the ENF signal. At time period T2 of the next computer machine cycle, "nand" gate MC45B is enabled. The output from this gate sets the Command Flag (CFL) FF. If the Command Control (CCL) FF is set under program control and the mag tape 1 and mag tape 2 interface cards have the highest priority on the interrupt chain, the interrupt system is enabled. At time period T5 of the computer machine cycle, the SIR signal is applied to "nand" gate MC25, enabling the gate. The output on pin 8 of "nand" gate MC25 is transferred to the set-side of the Control Interrupt (CIR) FF, setting the FF. With the FF in the set condition, a logic 1 is output on pin 9 and transferred to "and" gates MC37A and MC37B, enabling the gates. The output from these gates generate the Interrupt Request (IRQ) and Flag (FLG) signals. These signals are transferred to the computer circuits and the interrupt sequence begins.

SECTION IV
MAINTENANCE

4-1. INTRODUCTION.

4-2. This section contains maintenance information for the 12559A 9-Track Magnetic Tape Interface Kit. Included are preventive maintenance instructions, corrective maintenance instructions, and maintenance data consisting of a table of interface card logic equations, flow charts pertaining to specific operations, integrated circuit characteristics and connections, replaceable parts lists, part location views, and schematic diagrams.

4-3. PREVENTIVE MAINTENANCE.

4-4. Preventive maintenance for the interface kit is conducted by running the entire magnetic tape diagnostic program once each month. Instructions for running the diagnostic program are outlined in the Diagnostic Program Procedures, part number 12559-90032, located in the Manual of Diagnostics.

4-5. Perform the following preventive maintenance procedures every three months:

a. Visually inspect all cables and cable connectors associated with the interface kit for fraying or chafing. Repair or replace all cables and cable connectors found to be damaged.

b. Visually inspect components or the two magnetic tape interface cards for damage caused by excessive heat.

4-6. CORRECTIVE MAINTENANCE.

4-7. When performing troubleshooting, refer to figures 4-1 through 4-17 and tables 4-1 through 4-4 in this section, and to figures 3-1 through 3-9 in section III.

4-8. INTERCONNECTIONS.

4-9. For connections to the 86-pin connector on each interface card, refer to the computer or extender backplane wiring list. For connections to the 48-pin connector on each card, refer to the schematic diagrams.

4-10. REPLACEABLE PARTS.

4-11. The replaceable parts lists, tables 4-3 and 4-4, provide a listing of all components on the two magnetic tape interface cards by their reference designations. This table also provides the HP part number, description, manufacturer's code number, and manufacturer's part number for each component. Abbreviations used in the DESCRIPTION column are listed in table 5-2. Manufacturer's codes are listed in table 5-3. Refer to section V for parts ordering information.

Table 4-1. Logic Equations for Magnetic Tape Interface Cards

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
ADSC = HSCL · HSCM · IOG	Address command - lower priority interrupt location.	MC66C Mag Tape 1
ADSD = LSCL · LSCM · IOG	Address data - higher priority interrupt location.	MC92B Mag Tape 1
BOT = $\overline{\text{LOAD}}$ $\overline{\text{POINT}}$ (pin 17, 48-pin connector)	Beginning of Tape.	MC52C Mag Tape 1
CCL – JK FF (dual rank) J = STC K = CLC C = ADSC DS = None DC = $\overline{\text{CRS}}$	Command Control FF.	MC33B Mag Tape 1
CCP = D Output of counter	Control Clock Pulse. A general clock pulse used with both interface cards; 60 kHz clock rate with a 3.3 usec pulse width.	MC82A MC82B Mag Tape 1
CFB – JK FF (dual rank) J = 4.5V K = Ground C = SRP DS = STF · ADSC DC = (IAK · CIR) · (ADSC · CLF) + SRS	Command Flag Buffer FF.	MC24A Mag Tape 1
CIR – RS FF S = SIR · IEN · PRH · CCL · CFB · CFL R = ENF	Command Interrupt Request FF.	MC26C and MC26D Mag Tape 1
CLF – RS FF S = ENF · CFB R = SRS + CLF · ADSC	Command Flag FF.	MC45C and MC45D Mag Tape 1
CLR = ADSC · IOO · IOBO 6 · IOBO 7	Clear (pseudo control function). One of the command repertoire.	MC54C Mag Tape 1
CRC – JK FF (dual rank) J = B output of CMC counter MC22 K = Ground C = CCP DS = None DC = $\overline{\text{SRS}}$	Cyclic Redundancy Check control: write data gates for putting either data or CRCC onto tape.	MC52A Mag Tape 2
CRCC Register	Cyclic Redundancy Check Character Register. 9 FFs and 9 Adders. FFs = Adders =	MC25,34,45, 55,65A MC26,36,46, 56,66A Mag Tape 2

Table 4-1. Logic Equations for Magnetic Tape Interface Cards (Continued)

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
DFB – JK FF J = DTF K = Ground C = SFB DS = ADSD · STF DC = (CLF · ADSD) + SRS	Data Flag Buffer FF.	MC24B Mag Tape 1
DFL – RS FF S = DFB · ENF R = SRS + CLF · ADSD	Data Flag FF.	MC35A and MC35B Mag Tape 1
DLY – JK FF K = SRP J = SAW + SAG + SAR + BOT · REV C = CCP DC = None DS = (BOT · RWS) + ($\overline{\text{RWS}}$ · CLR)	Delay: This FF changes state to gain a direct set input. It is set to control a 5-millisecond time inserted after the completion of any operation before the interface cards are set ready.	MC96B Mag Tape 1
DTF – JK FF J = Ground K = +4.5V C = (ADSD · CLC) + (A2 · SCP · WFM) DS = SPC DC = CLR + EOR · $\overline{\text{WRT}}$	Data Transfer FF. Clocks on leading edge. Set for any operation requiring data transfer. Note Data transfer is command bit 4.	MC22B Mag Tape 1
EOF – RS FF S = RRC · T EOR · B (output of counter MC63) R = SRS	End of File. File mark is detected if an end of record is given with only two characters in the record.	MC62B MC62A Mag Tape 2
EOR – Latching FF (dual rank) S = $\overline{\text{A}}$ output of control counter MC53 R = A output of control counter MC53 DS = +4.5V DC = SRS C = T EOR	End of Record.	MC65B Mag Tape 2
ERC – JK FF (dual rank) J = Q17 collector output K = EOR + $\overline{\text{RRC}}$ C = CCP DS = None DC = SRS	End of Record Control. If this FF remains set for seven CCP pulses, an EOR will be detected.	MC52B Mag Tape 2
FWD – JK FF (dual rank) J = Ground K = SAW · SAG · SAR + BOT · REV C = CCP DS = MOT · IOBO 1 + MOT · WRT DC = $\overline{\text{CLR}}$	Forward. This FF drives the tape unit forward. Forward motion is caused by a command having IOBO 0 and IOBO 1, or a command to write.	MC115A Mag Tape 1
LPE = PTC · T EOR · LPC	Longitudinal Parity Error. If any of the longitudinal parity register FFs are set at the end of record, a longitudinal parity error occurs.	MC103A Mag Tape 2

Table 4-1. Logic Equations for Magnetic Tape Interface Cards (Continued)

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
LRCC – Outputs from LRCC Register FFs	Longitudinal Redundancy Check Character. Ensure that there are an even number of one bits in each track. All LRCC register FFs should be clear at end of record.	MC64 Mag Tape 2
LRCC Register = JK FFs (dual rank) 9-bit register J = Read Buffer output bit K = Read Buffer output bit C = RCD DS = None DC = SRS	Longitudinal Redundancy Check Character Register. Register consists of 9 FFs. One FF per read track.	MC75,76,85, 95,102B Mag Tape 2
MOT = RDY · AUTO · ADSC · IOO · IOBO 0	Motion. Any legal command calling for tape unit motion will make this signal true.	MC54D Mag Tape 1
PTC – RS FF (dual rank) S = SPC R = $\overline{CLR}$ · $\overline{EOR}$	Parity Control. Set if longitudinal parity is to be checked in this operation.	MC92C MC103B Mag Tape 2
PTY – JK FF (dual rank) J = (WRT + DTF) · VPC · $\overline{ERC}$ K = Ground C = RCD DS = LRCC · PTC · T EOR DC = SRS	Parity. If this FF is set, there is a parity error. The FF remains set until a new command is given. Longitudinal parity error sets the FF by a direct-set input. Vertical parity error sets the FF by clocked input.	MC82 Mag Tape 2
RAS = $\overline{Gap}$ · CCP · A2 (5.01 milliseconds)	Read After Start. Time between initial motion and RRS cleared is 5.016 milliseconds.	MC117D Mag Tape 1
RCD = Output of Read Clock Circuit, Collector of Q14	Read Clock Delayed 0.2 usec pulse width.	MC105A MC105B Mag Tape 2
RDY – JK FF (dual rank) J = Ground K = +4.5V C = SRS DS = SRP DC = +4.5V	Ready FF (format operation). Ready is set when tape unit is prepared to accept a new command. Not ready or LOCAL mode will make the status bit "busy" true.	MC22A Mag Tape 1
REJ – RS FF S = ADSC · IOO · IOBO 0 · ($\overline{AUTO}$ + $\overline{RDY}$ + $\overline{WES}$ · IOBO 3 + BOT · IOBO 5) R = $\overline{SRS}$	Reject FF. Command not accepted. Reason can be found from status. Either not write ring, load point, or already busy.	MC66B MC66A Mag Tape 1
REV – JK FF J = Ground K = SAW · SAG · SAR + BOT · REV C = CCP DS = MOT · BOT · IOBO 5 DC = CLR	Reverse. Drives the tape in reverse.	MC116B Mag Tape 1

Table 4-1. Logic Equations for Magnetic Tape Interface Cards (Continued)

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
REW – RS FF S = MOT · IOBO 7 R = BOT + CLR	Rewind FF.	MC64D MC74B Mag Tape 1
RRC – JK FF J = B output of counter MC63 K = $\overline{\text{CD}}$ output of counter MC63 C = RCD DS = None DC = SRS	Read Record Control. Aids in the detection of a file mark record.	MC102A Mag Tape 2
RRS – JK FF J = Ground K = A2 · $\overline{\text{3-Inch Gap}}$ C = CCP DS = SRP + CLR DC = +4.5V	Read Reset Control. Read reset holds the read track cards in the "0" state while it is true.	MC115B Mag Tape 1
RSB – RS FF S = MOT · IOBO 6 R = $\overline{\text{BOT}}$ · CLR · $\overline{\text{REWIND}}$	Rewind and Standby. Rewinds the tape to load point and switches the tape unit to local mode.	MC64A MC74A Mag Tape 1
RWS – RS FF S = MOT · IOBO 7 R = T (3.2 ms) + CLR · $\overline{\text{REWIND}}$	Rewind Status (signal from tape unit). Holds the status of the magnetic tape unit while in REWIND mode.	MC64C MC74C Mag Tape 1
SAG = $\overline{\text{WFM}}$ · $\overline{\text{DTF}}$ · TSAG	Stop After Gap. Reset FWD and gap FFs after 40 milliseconds.	MC95C Mag Tape 1
SAR = SCP · $\overline{\text{WRT}}$ · EOR · (÷ 2 C output)	Stop After Read. Time between EOR and motion stop.	MC105A Mag Tape 1
SAW = WTC · $\overline{\text{DTF}}$ · D (from MC93) 2.2 milliseconds	Stop After Write. Stops motion on write operation. Time between clearing control on data channel (to terminate write operation) and reset FWD FF.	MC95B Mag Tape 1
SCP = 0.2-millisecond period, 16.7-usec clock width	Spacing Clock Pulse.	MC92C Mag Tape 1
SFB = A2 · WTC · CCP + WCC · $\overline{\text{WRS}}$ · CCP + RCD · $\overline{\text{ERC}}$ · $\overline{\text{WRT}}$	Set Flag Buffer. Clocks data flag buffer FF.	MC24B Mag Tape 1
SPC = SRS · IOBO 4	Set Parity Control.	MC32D Mag Tape 1
SRS = POPIO + CLR + RSB + REW + FWD + REV	Start-Reset. Resets all FFs before a command is undertaken.	MC75 Mag Tape 1
T EOR = CCP · A (from MC53) · C (from MC53)	T End of Record. Pulse is sent 7 CCPs after ERC is set. Refer to EOR.	MC65B Mag Tape 2

Table 4-1. Logic Equations for Magnetic Tape Interface Cards (Continued)

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
TIM – JK FF (dual rank) J = DTF · DFB K = Ground C = SFB DS = None DC = SRS + $\overline{TIM}$ · [(SRS + ADSD · CLF) + DTF · (CLC · ADSD + WFM · SCP · A2)]	Timing Error. If data flag buffer FF is not cleared by the time the next flag is ready, a timing error occurs.	MC43 Mag Tape 1
3-Inch Gap Control – JK FF (dual rank) J = Ground K = TSAG C = CCP DS = WRT · SRS · (BOT + $\overline{DTF}$) DC = SRS + (DTF · $\overline{BOT}$ + $\overline{WRT}$)	3-Inch Gap Control. Erase tape by moving forward, turning on write current, but holding the Write FF clear.	MC116A Mag Tape 1
$\overline{TM}$ = $\overline{b0}$ · $\overline{b1}$ · $\overline{b2}$ · $\overline{b3}$ · $\overline{b4}$ · $\overline{b5}$ · $\overline{b6}$ · $\overline{b7}$	"Not" Tape Mark.	MC106 Mag Tape 2
TMC = 23_8	Tape Mark Character.	MC106 Mag Tape 2
TRAS = 5.016 milliseconds	T Read After Start pulse. Refer to RAS.	MC117D Mag Tape 1
TSAW = 4.2 milliseconds	T Stop After Write pulse. Refer to SAW.	MC95B Mag Tape 1
TWAS = 5.2 milliseconds	T Write After Start. Refer to WAS.	MC32 Mag Tape 1
T3.2 – JK FF J = +4.5V K = Ground C = D output of ÷6 counter DS = None DC = $\overline{DLY}$	Timing 3.2 milliseconds.	MC96A Mag Tape 1
VPE = VPC · (WRT + DTF) · $\overline{ERC}$ · RCD	Vertical Parity Error.	MC82 Mag Tape 2
VPC = $\overline{b0}$ · $\overline{b1}$ · $\overline{b2}$ · $\overline{b3}$ · $\overline{b4}$ · $\overline{b5}$ · $\overline{b6}$ · $\overline{b7}$ · $\overline{Parity\ Bit}$ A2 = $\overline{S2}$ (output of adder MC93B) B2 = S1 (output of adder MC93A) CIN2 = S1 (output of adder MC83A)	Vertical Parity Check – S2 output adder.	MC83B Mag Tape 2
WAS = A2 · WTC · CCP	Write After Start. Time between start of motion and first data character.	MC32 Mag Tape 1
WCC – JK FF J = A2 · WTC · (DTF + WFM) K = $\overline{DTF}$ · $\overline{WRS}$ DS = +4.5V DC = SRS	Write Clock Control. This FF is true for the time that data write clocks are being transmitted to the tape unit.	MC32 Mag Tape 2
WCP = WCC · CCP + ($\overline{B}$ · C · $\overline{D}$ · CCP)	Write Clock Pulse. Shifts the CRCC register on the trailing edge of the write clocks.	MC23D Mag Tape 2

Table 4-1. Logic Equations for Magnetic Tape Interface Cards (Continued)

SIGNAL MNEMONIC AND EQUATION	DEFINITION	SOURCE AND I/O BOARD
WES = WRITE ENABLED (pin R, 48-pin connector)	Write Enabled Status (write ring in tape reel).	MC52B Mag Tape 1
WFM – RS FF S = MOT · IOBO 2 R = SAW	Write File Mark. Writes a tape mark character on the tape.	MC84D MC84C Mag Tape 1
WRS – JK FF J = B · C · (D + WFM) K = A2 · WTC · (DTF + WFM) C = CCP DS = SRS DC = +4.5V	Write Reset (control FF). Holds the write tracks in the "0" state.	MC33 Mag Tape 2
WRT – RS FF S = WES · IOBO 3 · MOT R = SRP + CLR	Write. When in true state, current is flowing in the write head on the tape unit.	MC84B and MC84A Mag Tape 1
WTC = WRT · $\overline{\text{GAP}}$ · SCP · FWD · WRS	Write Timing Control.	MC85D Mag Tape 1

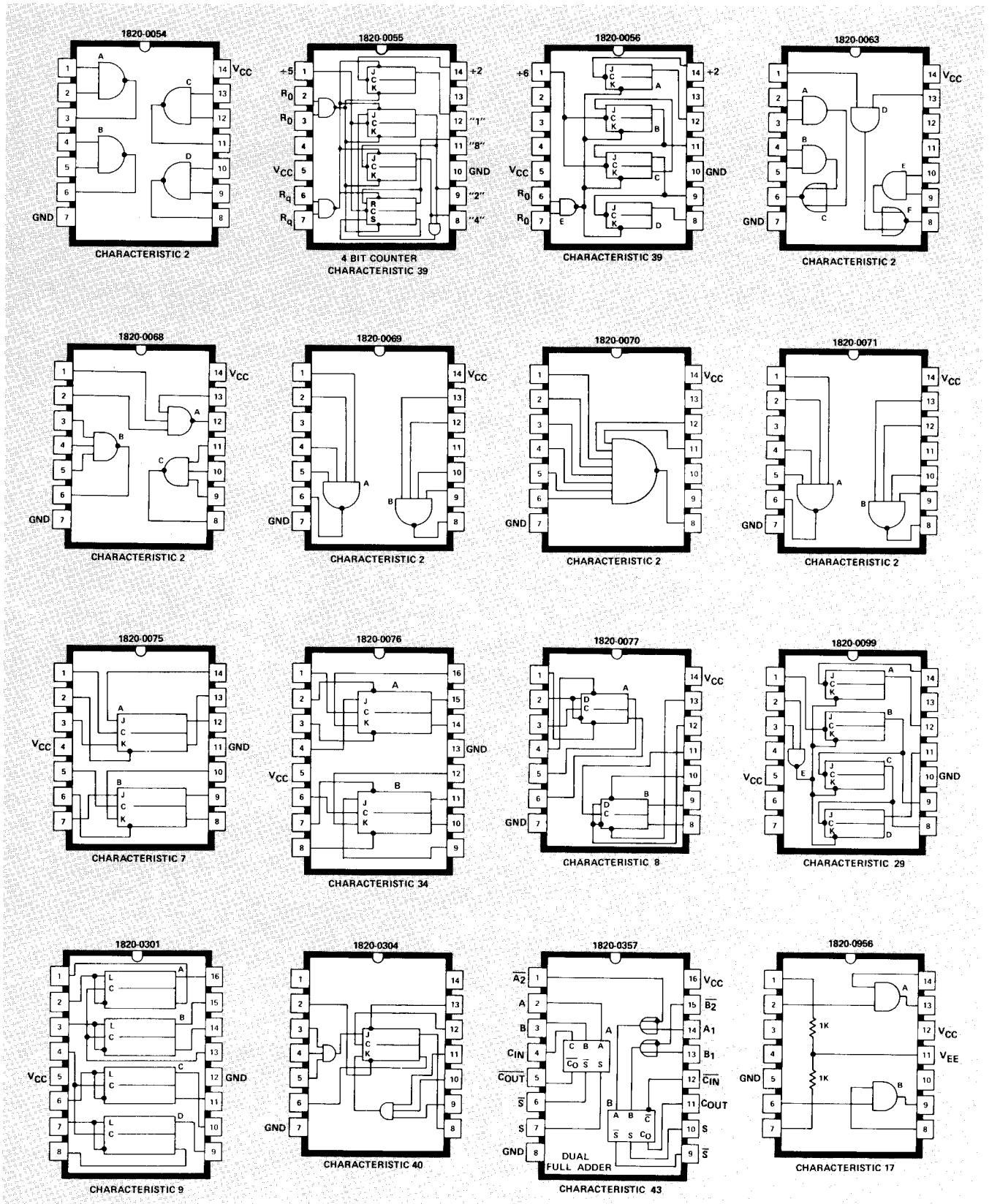

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Figure 4-1. Integrated Circuit Logic Diagrams

Table 4-2. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECOND)	TO LOGIC 0 (NANOSECOND)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
7	+2.0 (see note 1)	+0.8	+2.4	+0.4	Logic 1	50	50
8	+2.0 (see note 2)	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0 (see note 3)	+0.8	+2.4	+0.4	Logic 1	40	25
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
29	+2.0 (see note 4)	+0.8 (see note 5)	+2.4	+0.4	Logic 1	135	135
34	+2.0 (see note 6)	+0.8	+2.4	+0.4	Logic 1	30	45
39	+2.0 (see note 7)	+0.8	+2.4	+0.4	Logic 1	100	100
40	+2.0	+0.8	+2.4	+0.4	Logic 1	21	27
43	+1.8	+0.8	+2.4	+0.4	Logic 1	45	40

NOTES:
1. Required pulse widths; 20 ns minimum for clock, 25 ns minimum for set and clear.
2. Required pulse widths are 30 ns minimum.
3. Required pulse widths; 30 ns minimum for clock, 75 ns minimum for set and clear.
4. +2.2V for pin 1.
5. +0.6V for pin 1.
6. Required clock pulse width is 20 ns minimum.
7. Required input pulse width is 50 ns minimum.

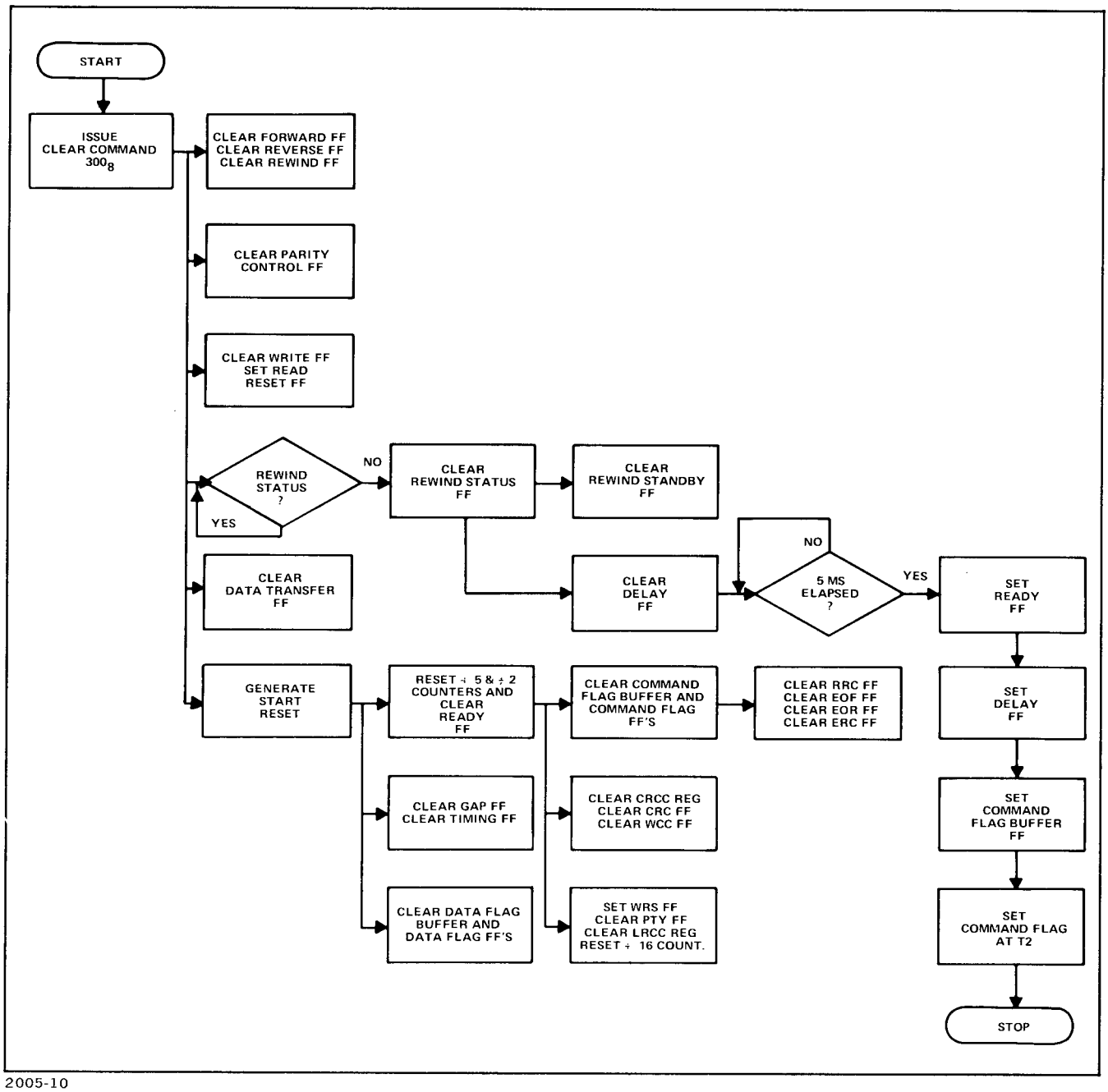

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Figure 4-2. Clear Command Flow Chart

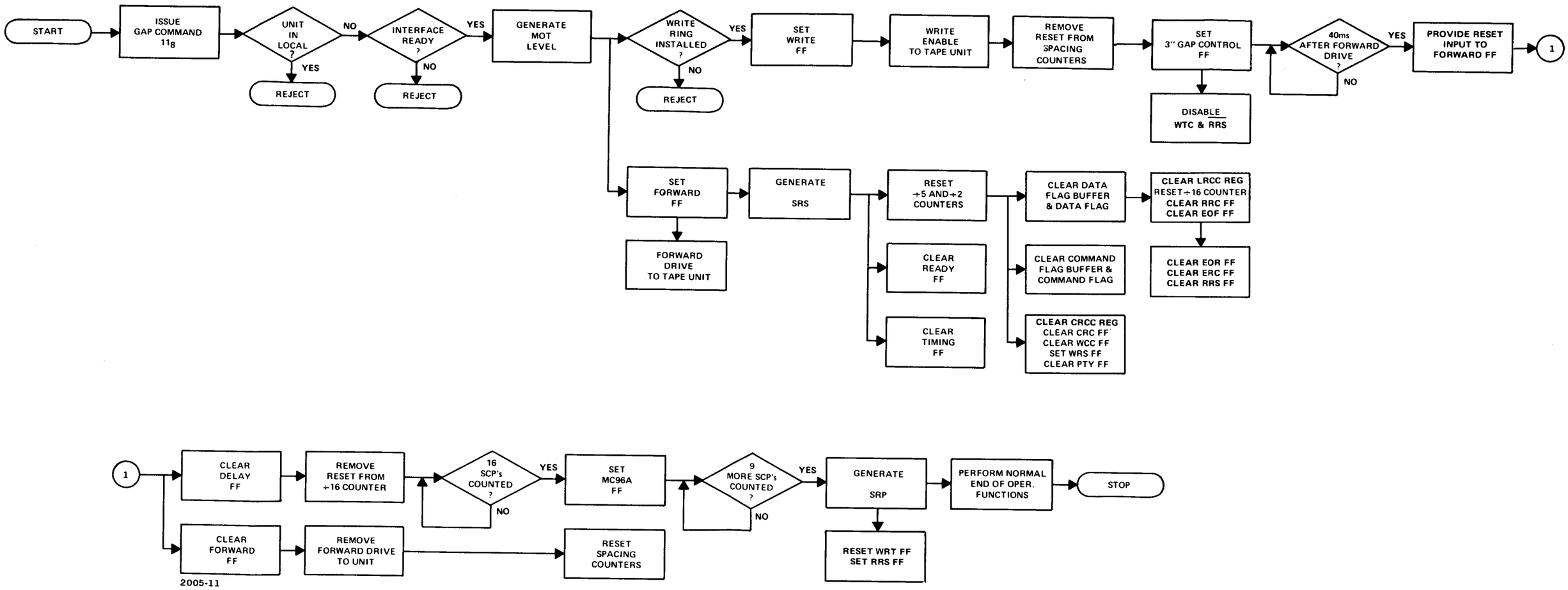
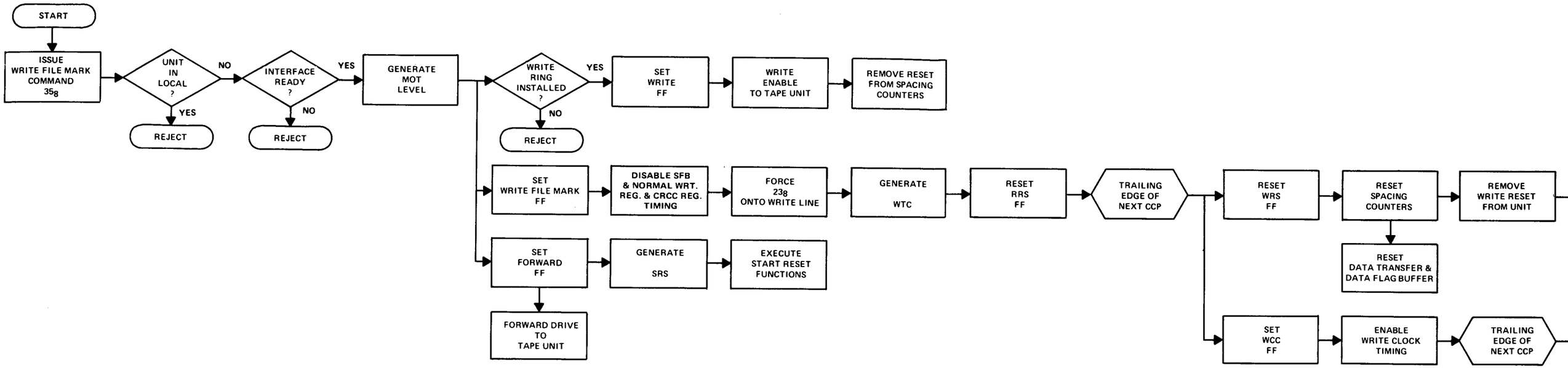


Figure 4-3. Three-Inch Gap Operation Flow Chart


START
ISSUE WRITE FILE MARK COMMAND 35_8
UNIT IN LOCAL ?
NO
YES
REJECT
INTERFACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
WRITE RING INSTALLED ?
YES
NO
REJECT
SET WRITE FF
WRITE ENABLE TO TAPE UNIT
REMOVE RESET FROM SPACING COUNTERS
SET WRITE FILE MARK FF
DISABLE SFB & NORMAL WRT. REG. & CRCC REG. TIMING
FORCE 23_8 ONTO WRITE LINE
GENERATE WTC
RESET RRS FF
TRAILING EDGE OF NEXT CCP
RESET WRS FF
RESET SPACING COUNTERS
REMOVE WRITE RESET FROM UNIT
RESET DATA TRANSFER & DATA FLAG BUFFER
SET FORWARD FF
GENERATE SRS
EXECUTE START RESET FUNCTIONS
FORWARD DRIVE TO TAPE UNIT
SET WCC FF
ENABLE WRITE CLOCK TIMING
TRAILING EDGE OF NEXT CCP
1
DISABLE WRITE CLOCK TIMING
8 CCP's COUNTED ?
YES
NO
SET WRS FF
SEND WRITE RESET TO UNIT TO WRITE LRCC
REMOVE RESET FROM SPACING COUNTERS
GENERATE WTC
PROVIDE RESET INPUT TO DELAY FORWARD & REVERSE FF's
EXECUTE NORMAL EOP SEQUENCE
STOP

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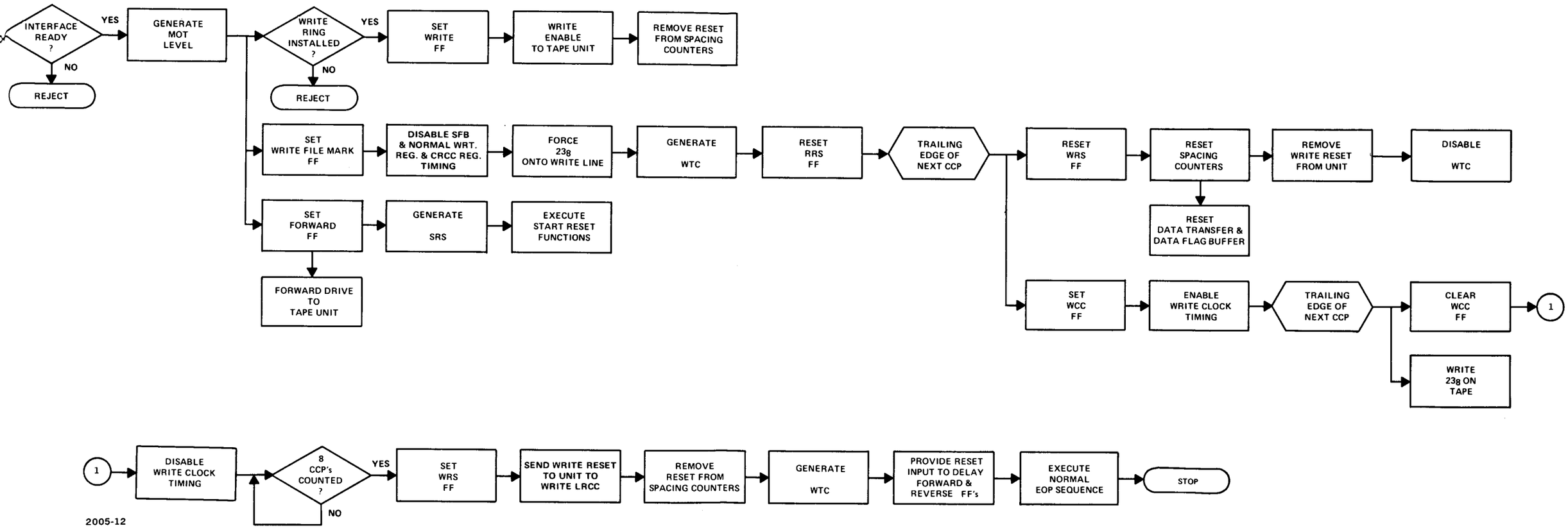


Figure 4-4. Write File Mark Flow Chart

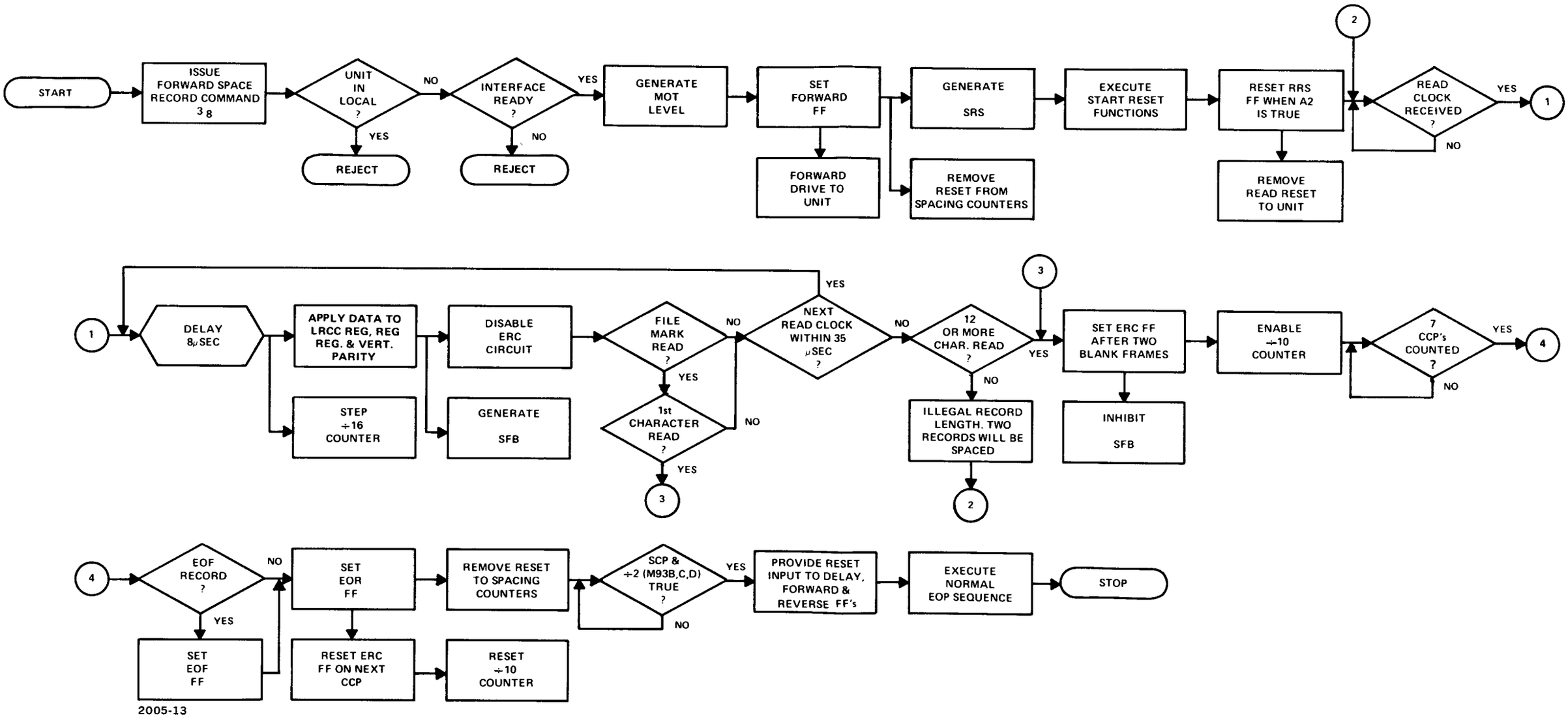


Figure 4-5. Forward Space Record Flow Chart

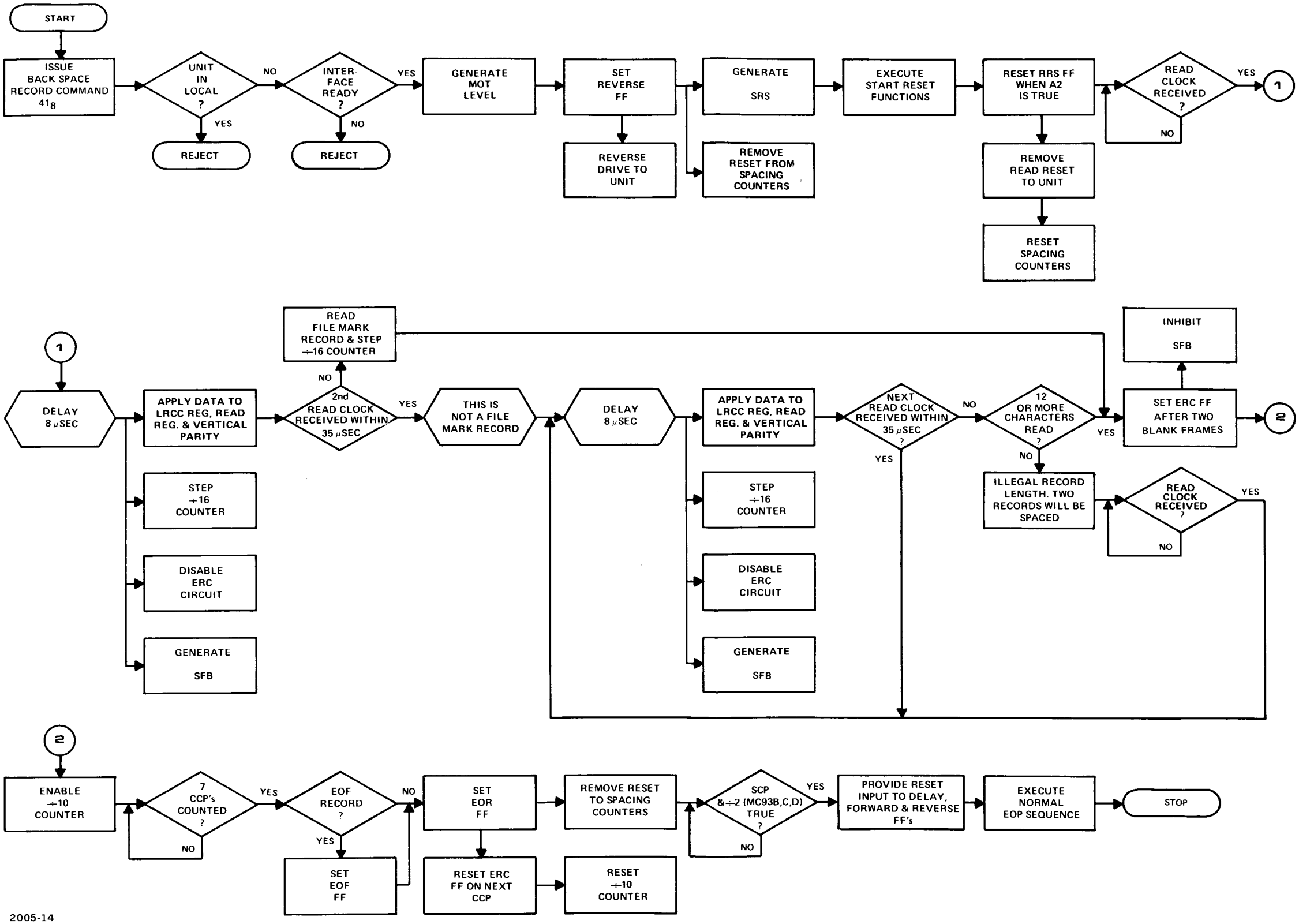


Figure 4-6. Back Space Record Flow Chart

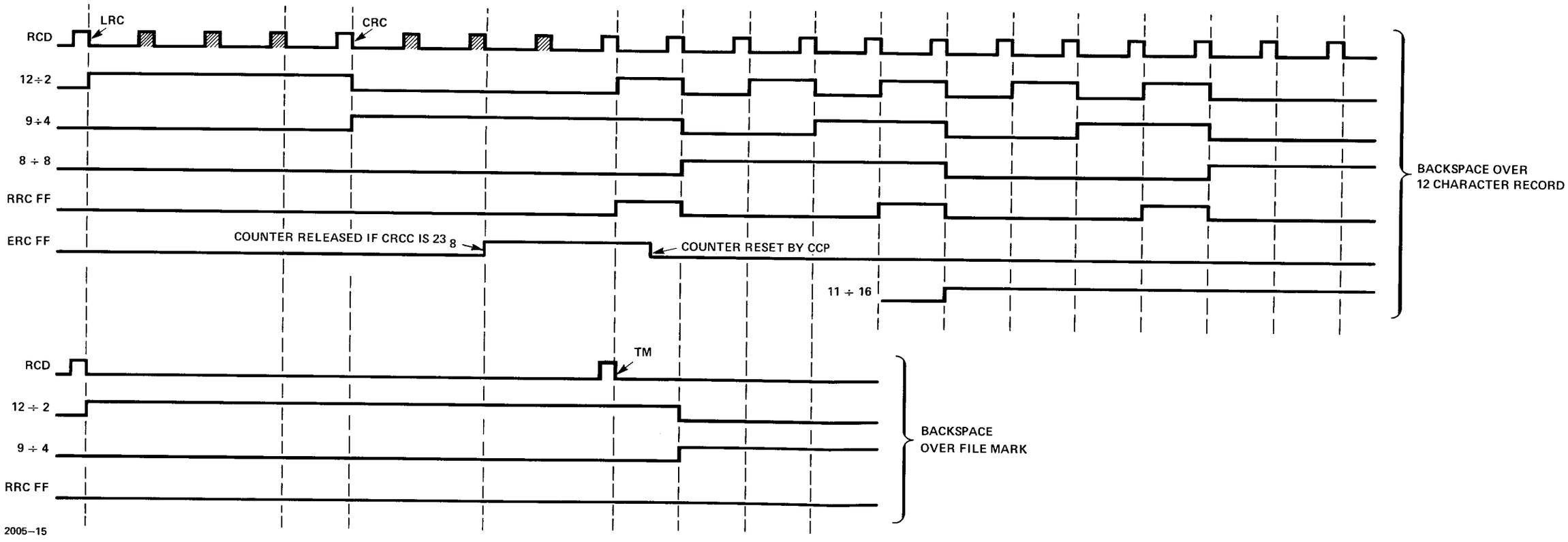
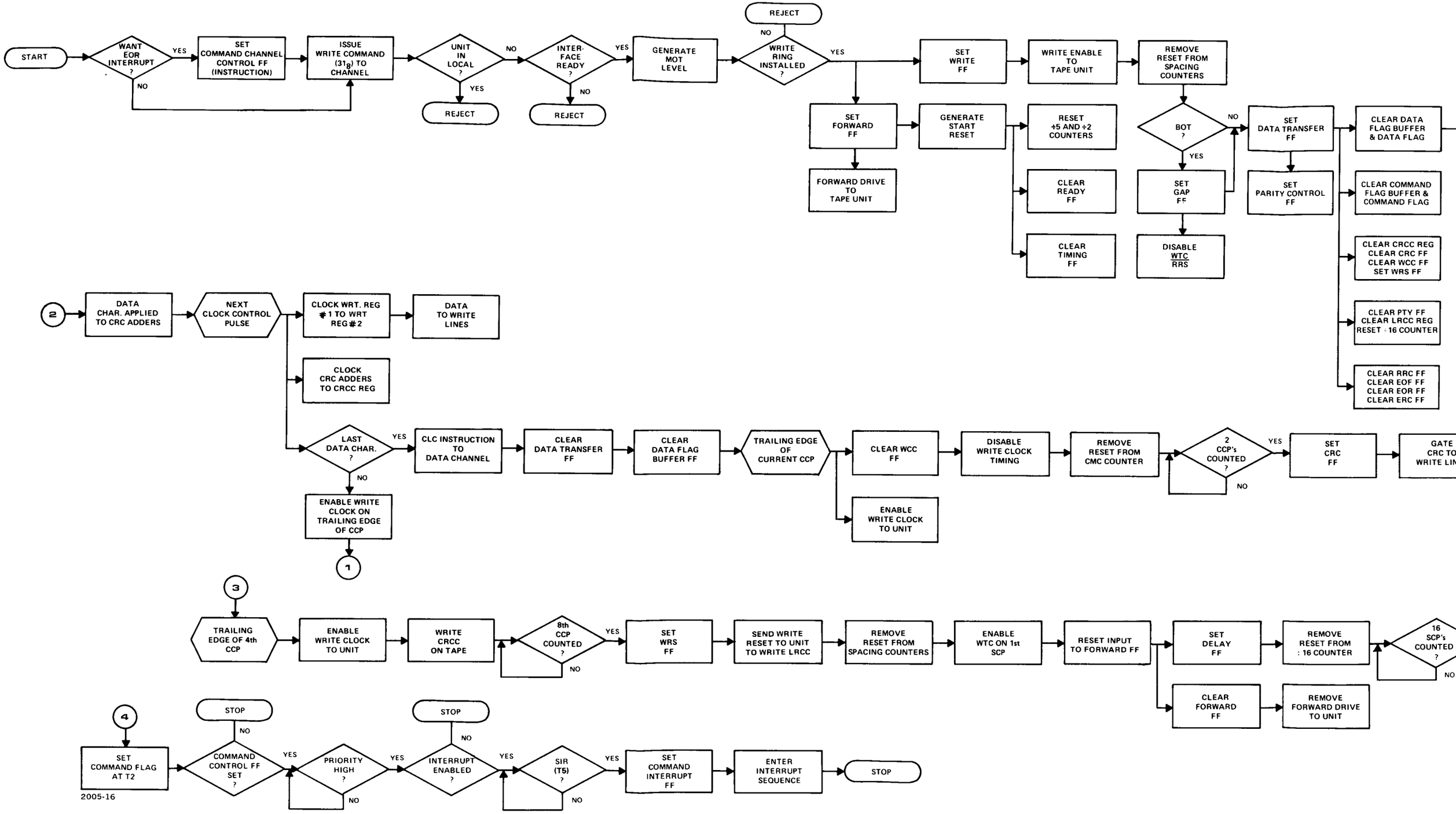


Figure 4-7. Back Space Operation Timing Diagram


START
WANT EOR INTERRUPT ?
YES
NO
SET COMMAND CHANNEL CONTROL FF (INSTRUCTION)
ISSUE WRITE COMMAND (31_8) TO CHANNEL
UNIT IN LOCAL ?
NO
YES
REJECT
INTER-FACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
REJECT
NO
WRITE RING INSTALLED ?
YES
SET WRITE FF
WRITE ENABLE TO TAPE UNIT
REMOVE RESET FROM SPACING COUNTERS
SET FORWARD FF
FORWARD DRIVE TO TAPE UNIT
GENERATE START RESET
RESET ÷5 AND ÷2 COUNTERS
CLEAR READY FF
CLEAR TIMING FF
BOT ?
NO
YES
SET GAP FF
DISABLE WTC/RRS
SET DATA TRANSFER FF
SET PARITY CONTROL FF
CLEAR DATA FLAG BUFFER & DATA FLAG
CLEAR COMMAND FLAG BUFFER & COMMAND FLAG
CLEAR CRCC REG
CLEAR CRC FF
CLEAR WCC FF
SET WRS FF
CLEAR PTY FF
CLEAR LRCC REG
RESET ÷16 COUNTER
CLEAR RRC FF
CLEAR EOF FF
CLEAR EOR FF
CLEAR ERC FF
2
DATA CHAR. APPLIED TO CRC ADDERS
NEXT CLOCK CONTROL PULSE
CLOCK WRT. REG #1 TO WRT REG #2
DATA TO WRITE LINES
CLOCK CRC ADDERS TO CRCC REG
LAST DATA CHAR. ?
YES
NO
CLC INSTRUCTION TO DATA CHANNEL
CLEAR DATA TRANSFER FF
CLEAR DATA FLAG BUFFER FF
TRAILING EDGE OF CURRENT CCP
CLEAR WCC FF
ENABLE WRITE CLOCK TO UNIT
DISABLE WRITE CLOCK TIMING
REMOVE RESET FROM CMC COUNTER
2 CCP's COUNTED ?
YES
NO
SET CRC FF
GATE CRC TO WRITE LIN
ENABLE WRITE CLOCK ON TRAILING EDGE OF CCP
1
3
TRAILING EDGE OF 4th CCP
ENABLE WRITE CLOCK TO UNIT
WRITE CRCC ON TAPE
8th CCP COUNTED ?
YES
NO
SET WRS FF
SEND WRITE RESET TO UNIT TO WRITE LRCC
REMOVE RESET FROM SPACING COUNTERS
ENABLE WTC ON 1st SCP
RESET INPUT TO FORWARD FF
SET DELAY FF
REMOVE RESET FROM : 16 COUNTER
16 SCP's COUNTED ?
NO
CLEAR FORWARD FF
REMOVE FORWARD DRIVE TO UNIT
4
SET COMMAND FLAG AT T2
STOP
NO
COMMAND CONTROL FF SET ?
YES
PRIORITY HIGH ?
YES
NO
STOP
NO
INTERRUPT ENABLED ?
YES
SIR (T5) ?
YES
NO
SET COMMAND INTERRUPT FF
ENTER INTERRUPT SEQUENCE
STOP

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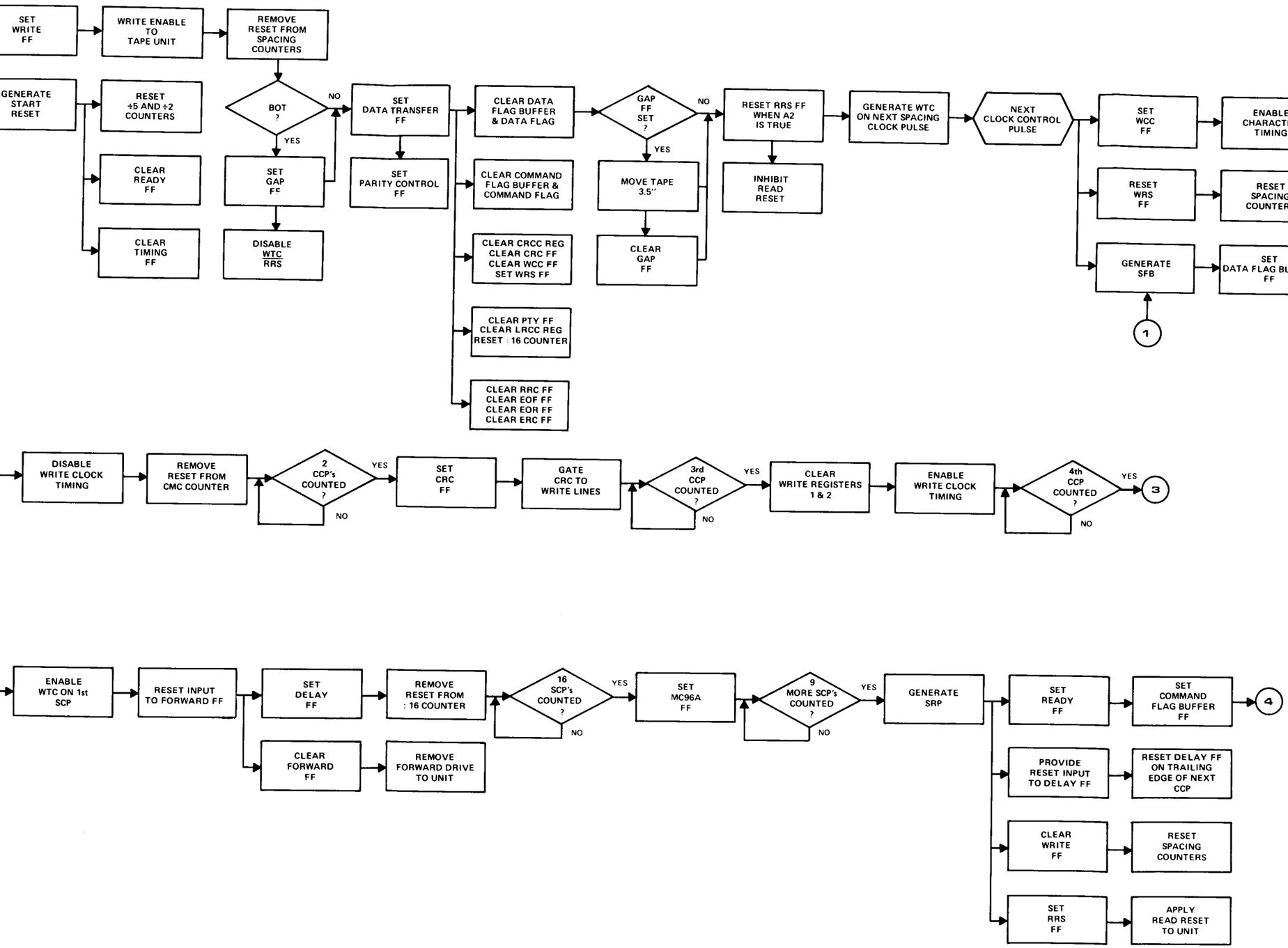
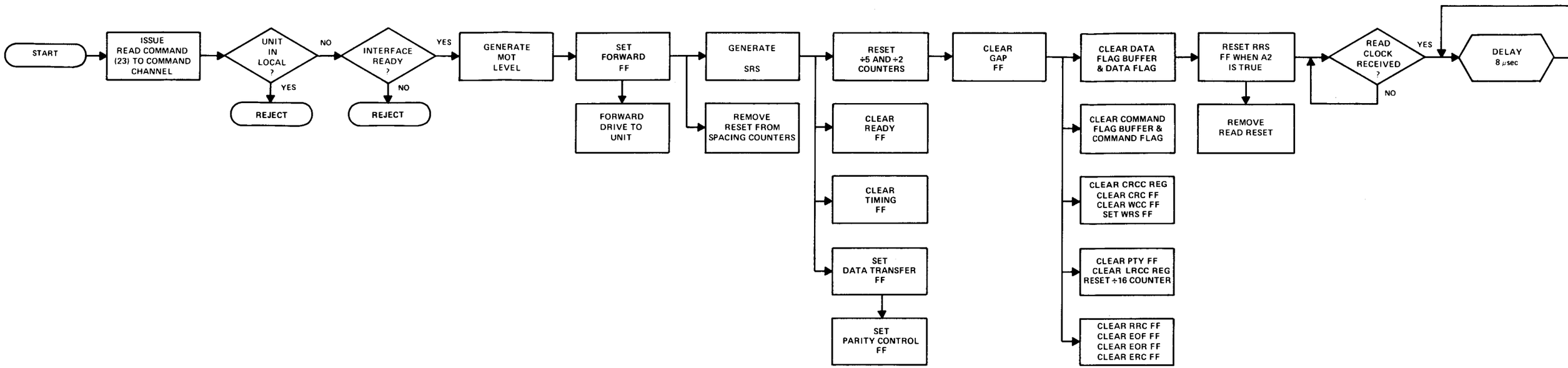
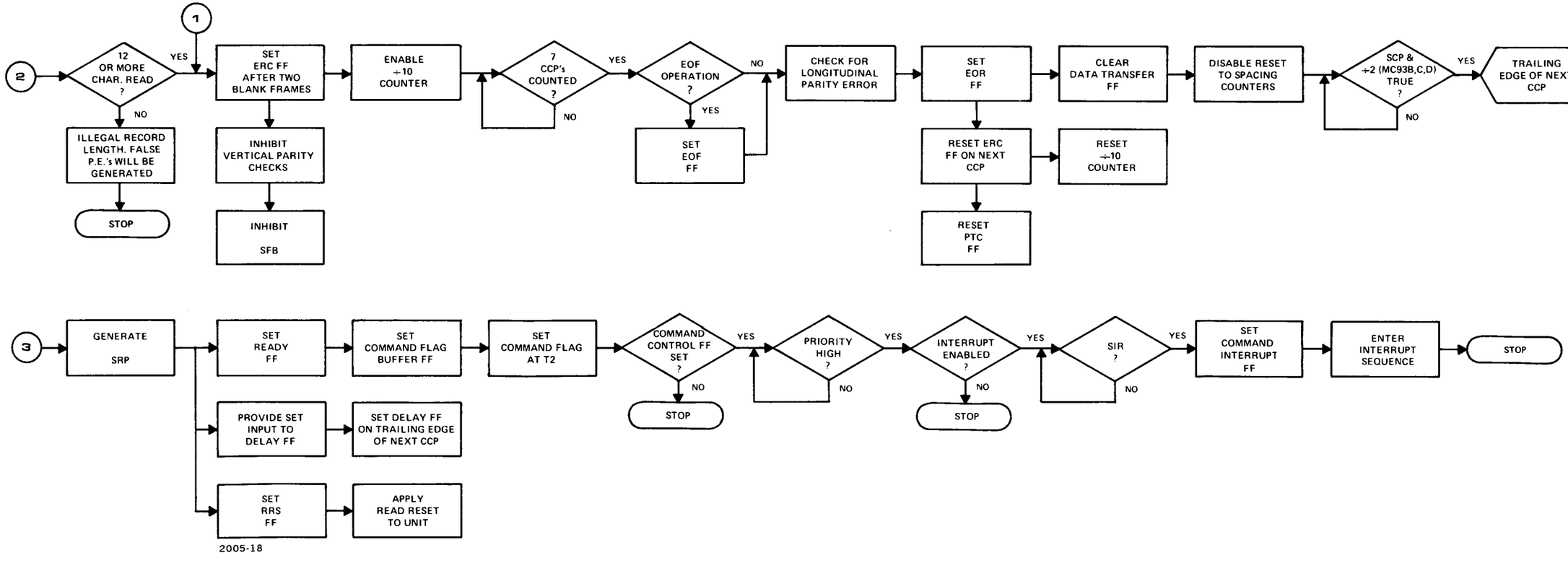


Figure 4-8. Write Operation Flow Chart


START
ISSUE READ COMMAND (23) TO COMMAND CHANNEL
UNIT IN LOCAL ?
YES
REJECT
NO
INTERFACE READY ?
YES
NO
REJECT
GENERATE MOT LEVEL
SET FORWARD FF
FORWARD DRIVE TO UNIT
GENERATE SRS
REMOVE RESET FROM SPACING COUNTERS
RESET ÷5 AND ÷2 COUNTERS
CLEAR READY FF
CLEAR TIMING FF
SET DATA TRANSFER FF
SET PARITY CONTROL FF
CLEAR GAP FF
CLEAR DATA FLAG BUFFER & DATA FLAG
CLEAR COMMAND FLAG BUFFER & COMMAND FLAG
CLEAR CRCC REG
CLEAR CRC FF
CLEAR WCC FF
SET WRS FF
CLEAR PTY FF
CLEAR LRCC REG
RESET ÷16 COUNTER
CLEAR RRC FF
CLEAR EOF FF
CLEAR EOR FF
CLEAR ERC FF
RESET RRS FF WHEN A2 IS TRUE
REMOVE READ RESET
READ CLOCK RECEIVED ?
YES
NO
DELAY 8 μsec


1
2
12 OR MORE CHAR. READ ?
YES
NO
ILLEGAL RECORD LENGTH. FALSE P.E.'s WILL BE GENERATED
STOP
SET ERC FF AFTER TWO BLANK FRAMES
INHIBIT VERTICAL PARITY CHECKS
INHIBIT SFB
ENABLE ÷10 COUNTER
7 CCP's COUNTED ?
YES
NO
EOF OPERATION ?
YES
SET EOF FF
NO
CHECK FOR LONGITUDINAL PARITY ERROR
SET EOR FF
RESET ERC FF ON NEXT CCP
RESET PTC FF
CLEAR DATA TRANSFER FF
RESET ÷10 COUNTER
DISABLE RESET TO SPACING COUNTERS
SCP & ÷2 (MC93B,C,D) TRUE ?
YES
NO
TRAILING EDGE OF NEXT CCP
CLEAR DLY FF
CLEAR FORWARD FF
3
GENERATE SRP
SET READY FF
SET COMMAND FLAG BUFFER FF
SET COMMAND FLAG AT T2
COMMAND CONTROL FF SET ?
YES
NO
STOP
PRIORITY HIGH ?
YES
NO
INTERRUPT ENABLED ?
YES
NO
STOP
SIR ?
YES
NO
SET COMMAND INTERRUPT FF
ENTER INTERRUPT SEQUENCE
STOP
PROVIDE SET INPUT TO DELAY FF
SET DELAY FF ON TRAILING EDGE OF NEXT CCP
SET RRS FF
APPLY READ RESET TO UNIT

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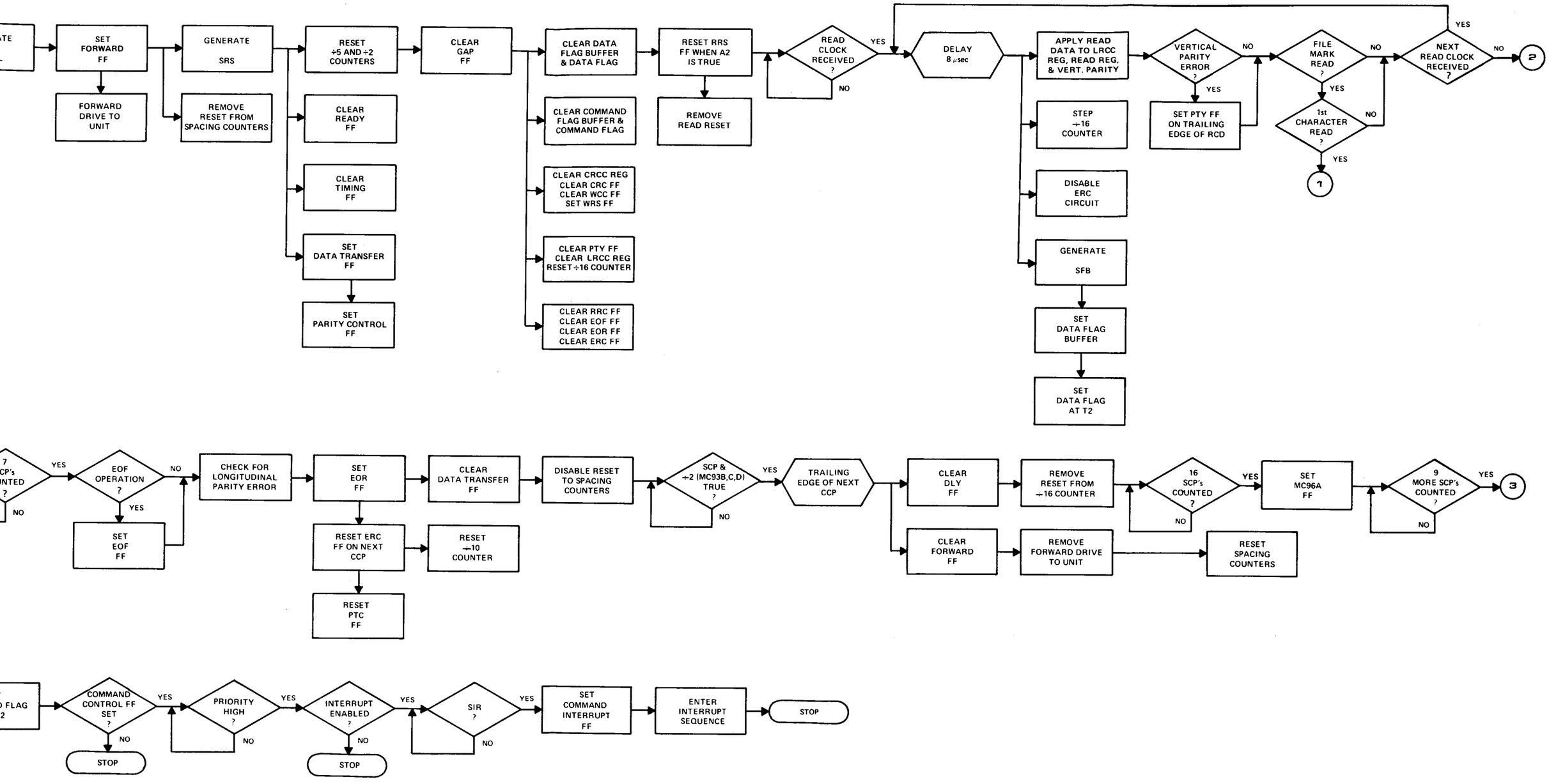
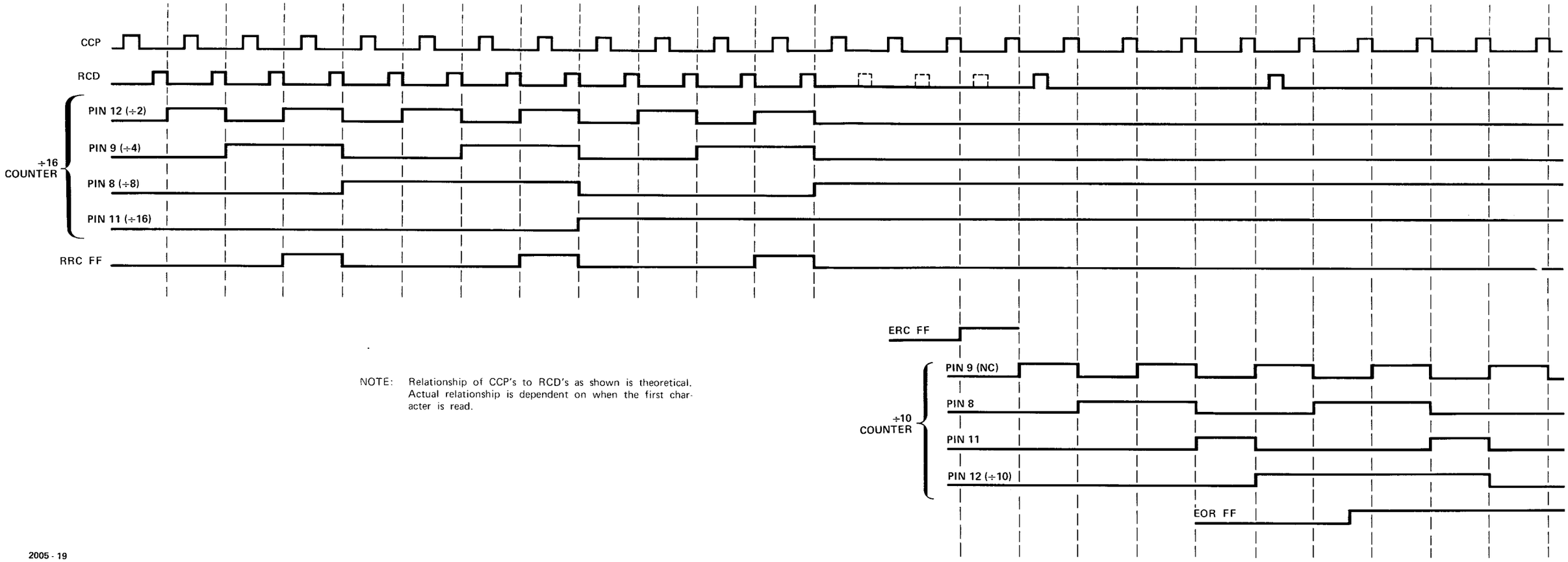


Figure 4-10. Read Operation Flow Chart



NOTE: Relationship of CCP's to RCD's as shown is theoretical. Actual relationship is dependent on when the first character is read.

Figure 4-11. Read Operation of 12 Characters Timing Diagram

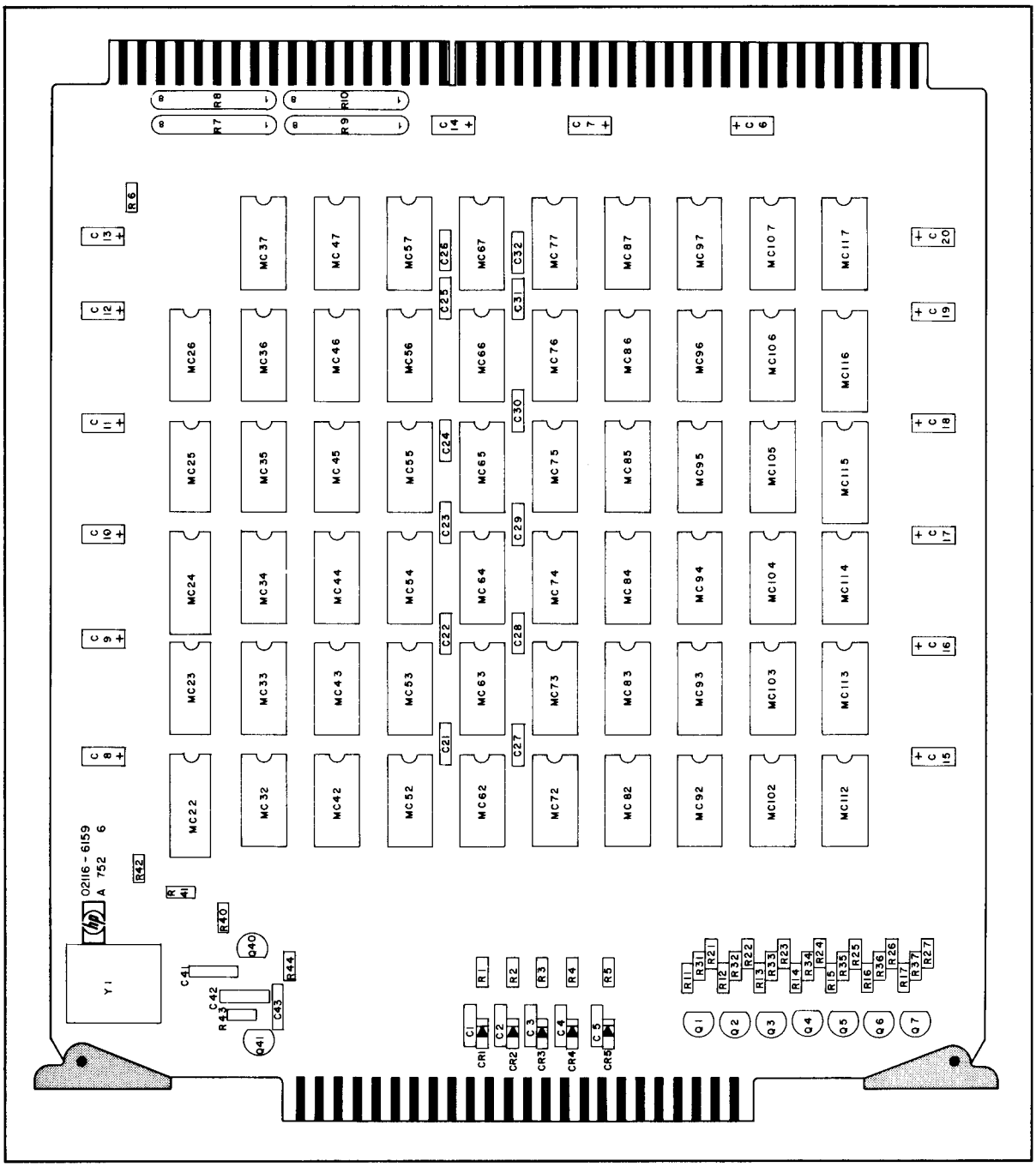


Figure 4-14. Mag Tape 1 Card (02116-6159) Parts Location Diagram

MAGNETIC TAPE 1 INTERFACE (02116-6159, REV. 752)

TIMING

C41 22PF
Y1
TP1
+4.5V
R40 15K
R41 820
C42 75PF
R42 820
R44 2.2K
R43 4.7K
Q40
Q41
C43 .001UF
MC92D
MC102B,C,D ÷5
MC92A
MC82A
MC82B
MC102A ÷2
MC113E
MC113A,C,D ÷6
MC114C
MC92C
MC103A ÷2
MC93A ÷2
MC103B,C,D ÷5
MC93B,C,D ÷2
MC112 ÷16
MC96A
DLY FF
MC96B
MC86A
MC76D
FROM MC94C-6
SCP
SRP
CCP
RDY FF
MC22A
MC83
MC117C
MC117B
MC117D
RRS FF
MC115B
MC106D
MC85D
MC104C
MC104D
WRS
FWD
TO MC104-2
R21 1.5K
R31 390
Q1
R11 1K
READ RESET
R22 1.5K
R32 390
Q2
R12 1K
WRITE ENABLE
WTC
R23 1.5K
R33 390
Q3
R13 1K
WRITE RESET
AUTO (READY STATUS)
CR2
C2 .01UF
R2 2.7K
MC26B
MC26A
MC85B
AUTO
IOI 24
EOT (END OF TAPE STATUS)
CR1
C1 .01UF
R1 2.7K
MC85C
EOT
WRITE ENABLED WRITE ENABLE STATUS
CR3
C3 .01UF
R3 2.7K
MC52B
WES
MC52A
MC53B
MC53C
MC53A
MC62B
MOT
LOAD POINT (LOAD POINT STATUS)
CR5
C5 .01UF
R5 2.7K
MC52C
BOT
MC52D
IOBO3
IOO 20
R9G 1.5K
R10F 1.5K
MC55A
MC55B
IOBO 2 FILE MARK
POPIO
R10G 1.5K
MC54A
IOBO 5 REVERSE
IOBO 3 WRITE
IOBO 0 MOTION
IOBO 7 REWIND
MC63C
MC63A
MC63D
MC63B
MC62A
MC55C
MC55D
MC65A
MC65B
MC66D
MC56B
REJECT FF
MC66B
MC66A
SRS
MC46B
MC54D
MC54B
MC54C
CLR
MC46A
MC72A
MC72C
MC72B
MC87B
IOBI 4
MC97A
IOBI 0
MC97B
IOBI 8
ACI
MC107B
IOBI 5
MC77A
IOBI 6
MC87A
IOBI 2
MC107A
IOBI 3
MC85A
MC77-R1
-2V
MC77B
MC117A
MC1068
MC106A
MC76A
MC95A
MC106C
FORWARD FF
MC115A
REVERSE FF
MC116B
WRT FF
MC84B
MC84A
3" GAP CONTROL FF
MC116A
WFM FF
MC84D
MC84C
MC75
MC76C
SRS
MC114A
A2
R25 1.5K
R35 390
Q5
R15 1K
FORWARD DRIVE (FORWARD)
R24 1.5K
R34 390
Q4
R14 1K
REVERSE DRIVE (REVERSE)
WFM
REV
WRT
ACI
C_R
SRS
FWD
IOBI 0 BUSY
IOBI 2 WRITE ENABL
IOBI 3 REJECT
IOBI 4 TIMING
IOBI 5 EOT
IOBI 6 BOT
IOBI 8 LOCAL

(END OF TAPE STATUS)

WRITE ENABLED (WRITE ENABLE STATUS)

LOAD POINT (LOAD POINT STATUS)

IOO

IOBO 2 FILE MARK

POPIO

IOBO 5 REVERSE

IOBO 3 WRITE

IOBO 0 MOTION

IOBO 7 REWIND

IOBO 6 REWIND & STANDBY

IOBO 1 FORWARD

REWIND (REWIND STATUS)

WRS

SFB

EOR

TRANSFER DATA IOBO 4

LSCL

LSCM

DATA FLAG CIRCUIT

TIMING

REJECT FF

TIM FF

FORWARD FF

REVERSE FF

WRT FF

3" GAP CONTROL FF

WFM FF

REW FF

RWS FF

RSB FF

DFB FF

DTF FF

DFL FF

FORWARD DRIVE (FORWARD)

REVERSE DRIVE (REVERSE)

REWIND

UNLOAD

CLR

SRS

FWD

WFM

REV

WRT

DTF

DATA FLAG CIRCUIT

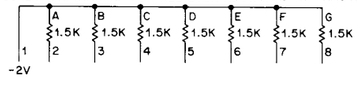
COMMAND FLAG AND INTERRUPT CIRCUIT

TIMING

WRS 5*
SFB J*
EOR 10*
TRANSFER DATA IOBO 4 42
LSCL 141
LSCM 16
SFC 5
SFS 25
CLF 7
ENF 46
IAK 10
STF 9
STC 22
HSCL 34
HSCM 35
IOG(B) 15
CLC 21
CRS 13
PRH 23
IEN 8
SIR 32

MC42B MC42F MC42E MC34D MC34F MC34E MC23D MC23C DFB FF MC24B MC35D DFL FF MC35B MC35A
MC32D SRS MC62C MC92B MC34A MC34C MC34B MC32C MC23A ADSD
R7A 1.5K -2V R8A 1.5K -2V
R7G 1.5K R8G 1.5K R9C 1.5K R10C 1.5K R7F 1.5K R8F 1.5K -2V
MC36D MC36F MC36E +4.5V ADSC
MC45A MC35C MC44D MC44A MC44B MC45B CFL FF MC45C MC45D
R9B 1.5K -2V R7C 1.5K R8D 1.5K -2V
MC23B +4.5V CFB FF MC24A
R7D 1.5K R8E 1.5K -2V R9D 1.5K R9E 1.5K -2V
MC67C MC66C ADSC CCL FF MC33B
R10A 1.5K R9A 1.5K R8B 1.5K R8C 1.5K -2V
R9F 1.5K R10E 1.5K -2V
MC32A R7B 1.5K -2V R10C 1.5K -2V R7E 1.5K -2V R10B 1.5K -2V
MC25 MC57A MC46A MC67B MC57C MC57B MC47A R6 270 +4.5V
MC37A IRQH MC37B FLGH CIR FF MC26C MC26D MC36A MC36C MC36B MC47B PRL
RSB FF MC64A MC74A MC74C
WRS
-12V R16 1K R26 1.5K Q6 R36 390 +4.5V Z* UNLOAD
WFM MC95C SAG MC105B DTF MC104B BOT REV H* DTF
WTC MC95B SAW
SCP MC105A SAR EOR
MC94E MC94F MC104A MC94D WRS WRT RRS FROM MC115-10
MC94B MC94C MC94A FWD REV DIVIDER NETWORK TO MC103-2 MC93-2 MC113-6
SPC SRQ SKF ADSD
D* SPC 19 SRQ 12 SKF E* ADSD 33 IRQH 49 FLGH 3 PRL
C8-C20 1UF C21-C32 .001UF 39 +4.5V 40 C6 1UF 69 70 -12V C7 1UF 47 48 -2V 1* A 24 BB GND

NOTES:
1. * INDICATES SIGNALS FROM/TO MAG TAPE CARD VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO 86-PIN CONNECTOR.
2. SIGNAL NAMES WITHIN PARENTHESIS ARE THOSE USED IN THE MAG TAPE UNIT DOCUMENTATION.
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R7 THRU R10:



DWG REV F

Figure 4-15. Mag Tape 1 Card (Data Channel)

Table 4-4. Mag Tape 2 Card Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0160-0298	Capacitor, Fxd, My, 0.0015 uF, 10%, 200 VDCW	56289	192P15292-PTS
C2	0160-2094	Capacitor, Fxd, Cer, 200 pF, 10%, 200 VDCW	72982	865-024-Y5E-201K
C3	0160-0155	Capacitor, Fxd, My, 3300 pF, 10%	28480	0160-0155
C4 thru C23	0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	28480	0180-0291
CR1 thru CR9	1901-0460	Diode, Si, 3 junction stabistor	28480	1901-0460
CR10,11	1901-0040	Diode, 30 mA, 30 WV	07263	FDG1088
MC11,17,18,74,105	1820-0071	Integrated Circuit, TTL	56289	USN7440A
MC12,72,103	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC13,24,34,44,54	1820-0063	Integrated Circuit, TTL	56289	USN7451A
MC14,23,42,62,73,84,92, 94,104	1820-0054	Integrated Circuit, TTL	56289	USN7400A
MC15,16,26,36,46,56,66,83,93	1820-0357	Integrated Circuit, TTL	07263	U5B930459X
MC22,63	1820-0099	Integrated Circuit, TTL	01295	SN7495N
MC25,28,35,37,38,45,55,57,65	1820-0077	Integrated Circuit, TTL	01295	SN4354
MC27,47,86,96	1820-0301	Integrated Circuit, TTL	01295	SN7475N
MC32,33,82	1820-0304	Integrated Circuit, TTL	01295	SN7472N
MC43	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC52,75,76,85,95,102	1820-0075	Integrated Circuit, TTL	01295	SN7473N
MC53	1820-0055	Integrated Circuit, TTL	01295	SN7490N
MC64,106	1820-0070	Integrated Circuit, TTL	01295	SN7430A
MC67,77,87,97,107	1820-0956	Integrated Circuit, CTL	07263	SL3459
Q1 thru Q15	1854-0215	Transistor, Si, NPN	28480	1854-0215
Q16,17	1853-0036	Transistor, Si, PNP	04713	SP-3612
R1 thru R9	0683-2725	Resistor, Fxd, Comp, 2700 ohms, 5%, 1/4W	01121	CB2725
R11 thru R20,50,51,54	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R21 thru R30,49	0683-1525	Resistor, Fxd, Comp, 1500 ohms, 5%, 1/4W	01121	CB1525
R31 thru R40	0683-5125	Resistor, Fxd, Comp, 5100 ohms, 5%, 1/4W	01121	CB5125
R41	0683-2225	Resistor, Fxd, Comp, 2.2k, 5%, 1/4W	01121	CB2225
R42	0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4W	01121	CB4725
R43	0683-1235	Resistor, Fxd, Comp, 12k, 5%, 1/4W	01121	CB1235
R44	0683-3925	Resistor, Fxd, Comp, 3900 ohms, 5%, 1/4W	01121	CB3925
R45,46	0683-3325	Resistor, Fxd, Comp, 3300 ohms, 5%, 1/4W	01121	CB3325
R47	0683-6825	Resistor, Fxd, Comp, 6800 ohms, 5%, 1/4W	01121	CB6825
R48	0683-1035	Resistor, Fxd, Comp, 10k, 5%, 1/4W	01121	CB1035
R52	0683-2235	Resistor, Fxd, Comp, 22k, 5%, 1/4W	01121	CB2235
R53	0683-1225	Resistor, Fxd, Comp, 1200 ohms, 5%, 1/4W	01121	CB1225
R55	1810-0020	Resistor Network (7 fxd film resistors)	28480	1810-0020

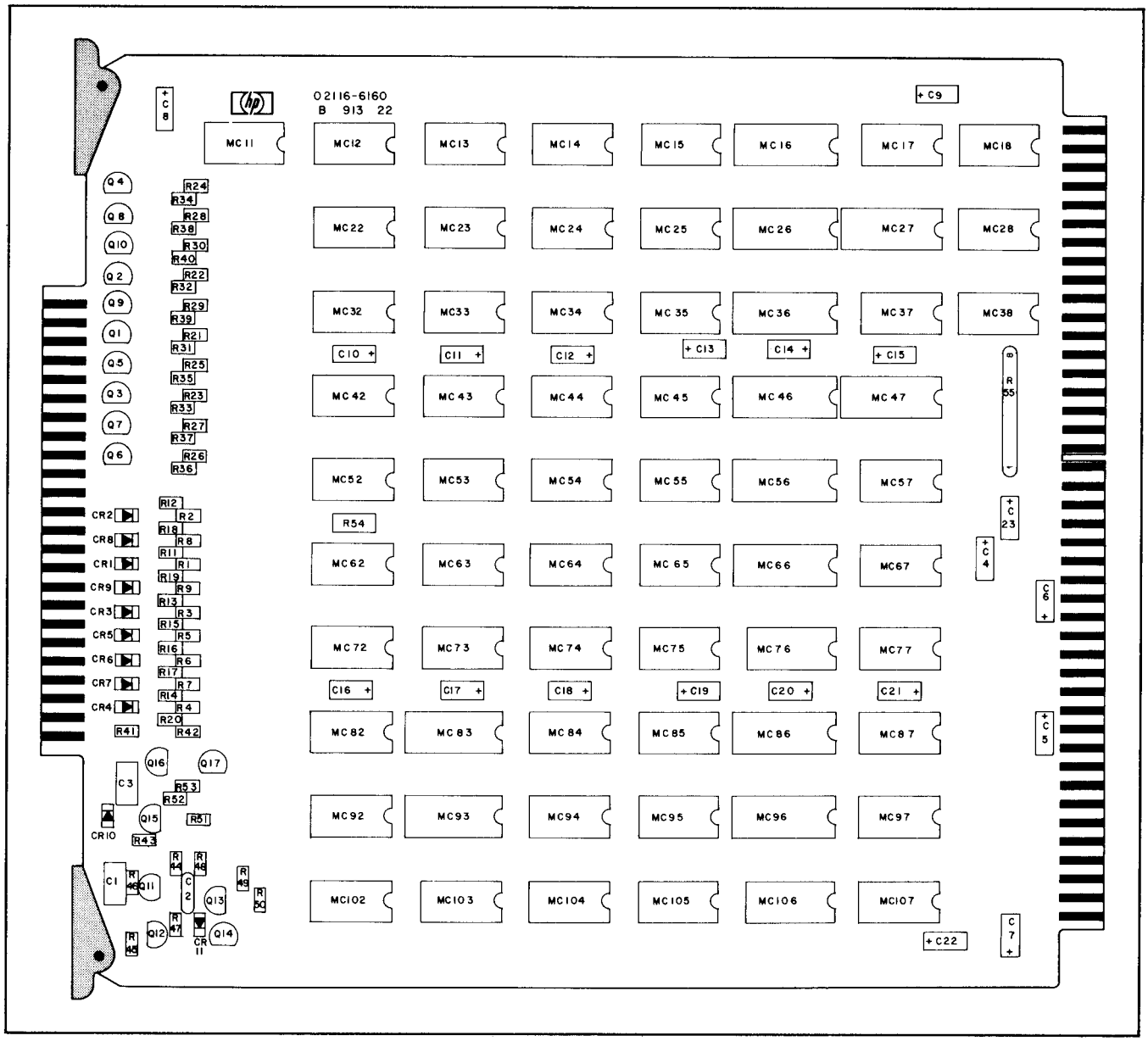
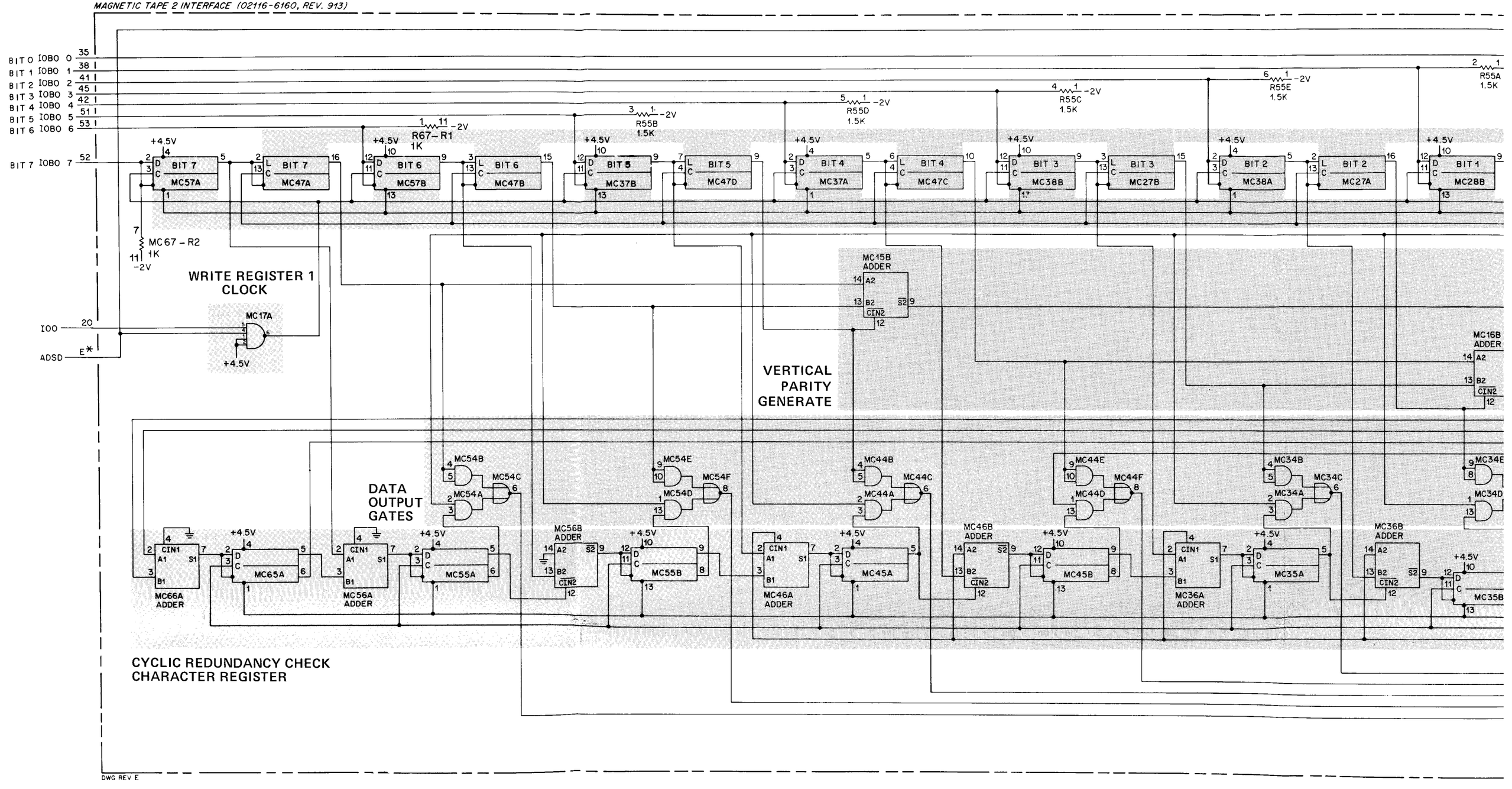


Figure 4-16. Mag Tape 2 Card (02116-6160) Parts Location Diagram

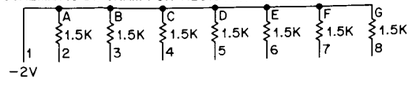
12559A


MAGNETIC TAPE 2 INTERFACE (02116-6160, REV. 913)
BIT 0 IOBO 0
BIT 1 IOBO 1
BIT 2 IOBO 2
BIT 3 IOBO 3
BIT 4 IOBO 4
BIT 5 IOBO 5
BIT 6 IOBO 6
BIT 7 IOBO 7
R67-R1 1K
R55B 1.5K
R55D 1.5K
R55C 1.5K
R55E 1.5K
R55A 1.5K
MC67-R2 1K
WRITE REGISTER 1 CLOCK
MC17A
IOO
ADSD
E*
MC15B ADDER
VERTICAL PARITY GENERATE
MC16B ADDER
DATA OUTPUT GATES
MC54B
MC54C
MC54A
MC54E
MC54F
MC54D
MC44B
MC44C
MC44A
MC44E
MC44F
MC44D
MC34B
MC34C
MC34A
MC34E
MC34D
MC66A ADDER
MC65A
MC56A ADDER
MC56B ADDER
MC55A
MC55B
MC46A ADDER
MC45A
MC46B ADDER
MC45B
MC36A ADDER
MC35A
MC36B ADDER
MC35B
CYCLIC REDUNDANCY CHECK CHARACTER REGISTER
DWG REV E

WRITE REGISTER 2

WRITE TRACK INVERTERS

NOTES:
1. * INDICATES SIGNALS FROM/TO MAG TAPE CARD VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO 86-PIN CONNECTOR.
2. SIGNAL NAMES WITHIN PARENTHESIS ARE THOSE USED IN THE MAG TAPE UNIT DOCUMENTATION.
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORK R55:



Y* WT4
P* WT2
R* WT8
S* WT1
T* WT9
U* WT3
V* WT5
W* WT6
X* WT7

SPC D*
CLR K*
SRS 7*
A2 C*
WTC L*
WFM 4*
WRT 6*
CCP 3*
DTF H*
FWD 8*
IOI 24

MC74A
MC74B
+4.5V
SRS

ADDER MC83B
ADDER MC83A
MC93A ADDER
MC93B ADDER
CIN1 A1 S1 A2 B1 B2 CIN2 S2

VERTICAL PARITY CHECK

PTC FF
MC92C
MC103B
MC92D

MC82
PTY FF

WRITE CONTROL
MC12A
CCP
A2
WTC
MC42A
RCD
+4.5V

MC104A
MC104C
MC104B
R55G 1.5K -2V
+4.5V

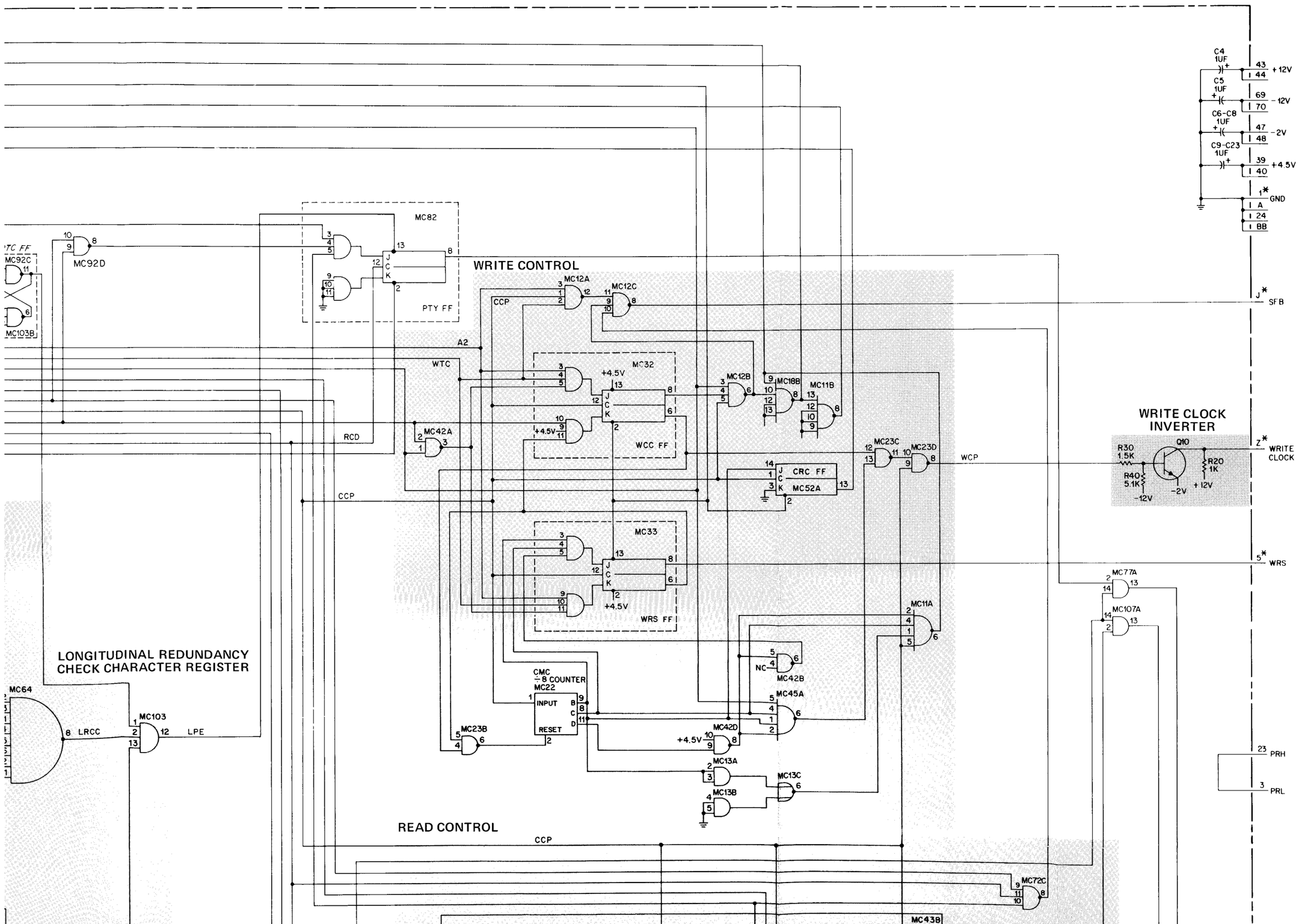
RT2 13* b0 CR2 R2 2.7K -12V MC84B
RT8 14* b1 CR8 R8 2.7K -12V MC84A
RT1 15* b2 CR1 R1 2.7K -12V MC84D
RT9 16* b3 CR9 R9 2.7K -12V MC84C
RT3 17* b4 CR3 R3 2.7K -12V MC94A
RT5 18* b5 CR5 R5 2.7K -12V MC94B
RT6 19* b6 CR6 R6 2.7K -12V MC94D
RT7 20* b7 CR7 R7 2.7K -12V MC94C
RT4 21* P CR4 MC104B

MC102B
MC75A
MC75B
MC85A
MC85B
MC95A
MC95B
MC76A
MC66
A2 C02

LONGITUDINAL REDUNDANCY CHECK CHARACTER REGISTER
MC64
LRCC
MC103
LPE

CMC ÷8 COUNTER
MC22
INPUT RESET
MC23B

READ CONTROL
CCP


C4 1UF
C5 1UF
C6-C8 1UF
C9-C23 1UF
43
44
+12V
69
70
-12V
47
48
-2V
39
40
+4.5V
1*
GND
A
24
BB
J*
SFB
WRITE CONTROL
MC82
PTY FF
MC92D
MC92C
MC103B
MC12A
MC12C
CCP
A2
WTC
MC32
+4.5V
WCC FF
MC42A
RCD
MC12B
MC18B
MC11B
MC23C
MC23D
WCP
CRC FF
MC52A
WRITE CLOCK INVERTER
R30 1.5K
Q10
R40 5.1K
R20 1K
-12V
-2V
+12V
Z*
WRITE CLOCK
MC33
WRS FF
5*
WRS
MC77A
MC107A
MC11A
LONGITUDINAL REDUNDANCY CHECK CHARACTER REGISTER
CMC ÷8 COUNTER MC22
INPUT
RESET
NC
MC42B
MC45A
MC42D
MC23B
MC13A
MC13C
MC13B
MC64
MC103
LRCC
LPE
23
PRH
3
PRL
READ CONTROL
MC72C
MC43B
MC42C
MC66

V* WT5

W* WT6

X* WT7

RT2 13* b0 CR2 R2 2.7K −12V MC84B

RT8 14* b1 CR8 R8 2.7K −12V MC84A

RT1 15* b2 CR1 R1 2.7K −12V MC84D

RT9 16* b3 CR9 R9 2.7K −12V MC84C

RT3 17* b4 CR3 R3 2.7K −12V MC94A

RT5 18* b5 CR5 R5 2.7K −12V MC94B

RT6 19* b6 CR6 R6 2.7K −12V MC94D

RT7 20* b7 CR7 R7 2.7K −12V MC94C

RT4 21* P CR4 R4 2.7K −12V +4.5V MC104B

READ BUFFERS

ACI F*

MC102B

MC75A

MC75B

MC85A

MC85B

MC95A

MC95B

MC76A

MC76B

MC64

LONGITUDINAL REDUNDANCY CHECK CHARACTER REGISTER

MC103

LRCC

LPE

MC66

CCP

CMC ÷8 COUNTER MC22

INPUT

RESET

MC23B

READ CONTROL

+12V

R52 22K

Q15

Q16

R51 1K

C3 3300PF

READ CLOCK DELAY AND POWER GATES

READ CLOCK 22* R41 2.2K CR10 R42 4.7K −12V

+12V R43 12K R44 3.9K R45 3.3K C1 1500PF R46 3.3K C2 200PF R48 10K TP1 R47 6.8K CR11 Q11 Q12

+4.5V R50 1K Q13 Q14 R49 1.5K −12V

MC105A MC105B RCD

READ REGISTER

MC96A MC96B MC96C MC96D MC86A MC86B MC86C MC86D

MC107B MC97B MC97A MC87B MC87A MC67B MC77B MC67A

MC106 TM

MC73A

MC92A MC92B

÷16 COUNTER MC63

RCD SRS FWD

LONGITUDINAL REDUNDANCY CHECK CHARACTER REGISTER

READ CONTROL

MC64 MC103 LRCC LPE

MC66 MC106 TM

MC107B MC97B MC97A MC87B MC87A MC67B MC77B MC67A

MC33 WRS FF +4.5V

CMC ÷8 COUNTER MC22 INPUT RESET

MC23B MC42B MC45A MC42D MC13A MC13B MC13C MC11A

MC77A MC107A

5* WRS

23 PRH

3 PRL

CCP

MC72C

MC73A TM

MC92A MC92B ÷16 COUNTER MC63 RCD SRS FWD

MC62C

RRC FF MC102A

Q15 Q16 Q17 R51 1K R52 22K R53 1.2K R54 1K C3 3300PF +12V -2V +4.5V

ERC FF MC52B

MC53 ÷10 COUNTER

MC43B MC42C MC23A MC72A MC62D MC103C MC73D MC73B MC73C MC72B

EOF FF MC62B MC62A

EOR FF MC65B

10* EOR

84 IOBI 7 BIT 7 OR EOF
81 IOBI 6 BIT 6
80 IOBI 5 BIT 5
77 IOBI 4 BIT 4
64 IOBI 3 BIT 3
30 IOBI 2 BIT 2
29 IOBI 1 BIT 1 OR PARITY ERROR
26 IOBI 0 BIT 0

Figure 4-17. Mag Tape 2 Card (Command Channel) Schematic Diagram

SECTION V

REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the interface kit. Table 5-1 lists parts in alphanumeric order of the HP part numbers and lists the following information on each part:

a. Description of the part. (Refer to table 5-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. Separate parts lists are provided along with the parts location diagram for the interface cards in section IV of this manual. The parts list in section IV lists the parts in alphanumeric order of reference designations.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.
b. Hewlett-Packard part number for each part.
c. Description of each part.
d. Circuit reference designation.

Table 5-1. HP 12559A Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0145	Capacitor, Fxd, Mica, 22 pF, 5%	28480	0140-0145	1
0150-0050	Capacitor, Fxd, Cer, 1000 pF, 600 VDCW	77630	OBD	22
0160-0155	Capacitor, Fxd, My, 3300 pF, 10%	28480	0160-0155	1
0160-0298	Capacitor, Fxd, My, 0.0015 uF, 10%, 200 VDCW	56289	192P15292-PTS	1
0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	56289	C023F101F103 ZE12-CHD	5
0160-2094	Capacitor, Fxd, Cer, 200 pF, 10%, 200 VDCW	72982	865-024-Y5E-201K	1
0160-2202	Capacitor, Fxd, Mica, 75 pF, 5%	28480	0160-2202	1
0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	28480	0180-0291	35
0410-0163	Crystal, Quartz, 300 kHz	75378	CR46A/V	1
0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025	20
0683-1035	Resistor, Fxd, Comp, 10k, 5%, 1/4W	01121	CB1035	1
0683-1225	Resistor, Fxd, Comp, 1200 ohms, 5%, 1/4W	01121	CB1225	1
0683-1235	Resistor, Fxd, Comp, 12k, 5%, 1/4W	01121	CB1235	7
0683-1525	Resistor, Fxd, Comp, 1500 ohms, 5%, 1/4W	01121	CB1525	11
0683-1535	Resistor, Fxd, Comp, 15k, 5%, 1/4W	01121	CB1535	1
0683-2225	Resistor, Fxd, Comp, 2.2k, 5%, 1/4W	01121	CB2225	2
0683-2235	Resistor, Fxd, Comp, 22k, 5%, 1/4W	01121	CB2235	1
0683-2715	Resistor, Fxd, Comp, 270 ohms, 5%, 1/4W	01121	CB2715	1
0683-2725	Resistor, Fxd, Comp, 2700 ohms, 5%, 1/4W	01121	CB2725	14
0683-3325	Resistor, Fxd, Comp, 3300 ohms, 5%, 1/4W	01121	CB3325	2
0683-3915	Resistor, Fxd, Comp, 390 ohms, 5%, 1/4W	01121	CB3915	7
0683-3925	Resistor, Fxd, Comp, 3900 ohms, 5%, 1/4W	01121	CB3925	1
0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4W	01121	CB4725	2
0683-5125	Resistor, Fxd, Comp, 5100 ohms, 5%, 1/4W	01121	CB5125	10
0683-6825	Resistor, Fxd, Comp, 6800 ohms, 5%, 1/4W	01121	CB6825	1
0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4W	01121	CB8215	2
1200-0199	Socket, Crystal	91506	8000-AG9	1
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	5
1820-0054	Integrated Circuit, TTL	56289	USN7400A	30
1820-0055	Integrated Circuit, TTL	01295	SN7490N	4
1820-0056	Integrated Circuit, TTL	01295	SN7492N	1
1820-0063	Integrated Circuit, TTL	56289	USN7451A	11
1820-0068	Integrated Circuit, TTL	56289	USN7410A	9
1820-0069	Integrated Circuit, TTL	56289	USN7420A	5
1820-0070	Integrated Circuit, TTL	01295	SN7430A	5
1820-0071	Integrated Circuit, TTL	56289	USN7440A	6
1820-0075	Integrated Circuit, TTL	01295	SN7473N	8
1820-0076	Integrated Circuit, TTL	01295	SN7474N	4
1820-0077	Integrated Circuit, TTL	01295	SN4354	9
1820-0099	Integrated Circuit, TTL	01295	SN7495N	3
1820-0301	Integrated Circuit, TTL	01295	SN7475N	4
1820-0304	Integrated Circuit, TTL	01295	SN7472N	1
1820-0357	Integrated Circuit, TTL	07263	U5B930459X	9
1820-0956	Integrated Circuit, CTL	07263	SL3459	11
1853-0036	Transistor, Si, PNP	04713	SP-3612	9
1854-0215	Transistor, Si, NPN	28480	1854-0215	17
1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088	2
1901-0460	Diode, Si, 3 junction stabistor	28480	1901-0460	14
02116-6159	Mag Tape 1 Card	28480	02116-6159	1
02116-6160	Mag Tape 2 Card	28480	02116-6160	1
02116-6193	Cable, Interconnecting	28480	02116-6193	1
12559-9001	Operating and Service Manual	28480	12559-9001	1