HP 12791A
FIRMWARE EXPANSION MODULE

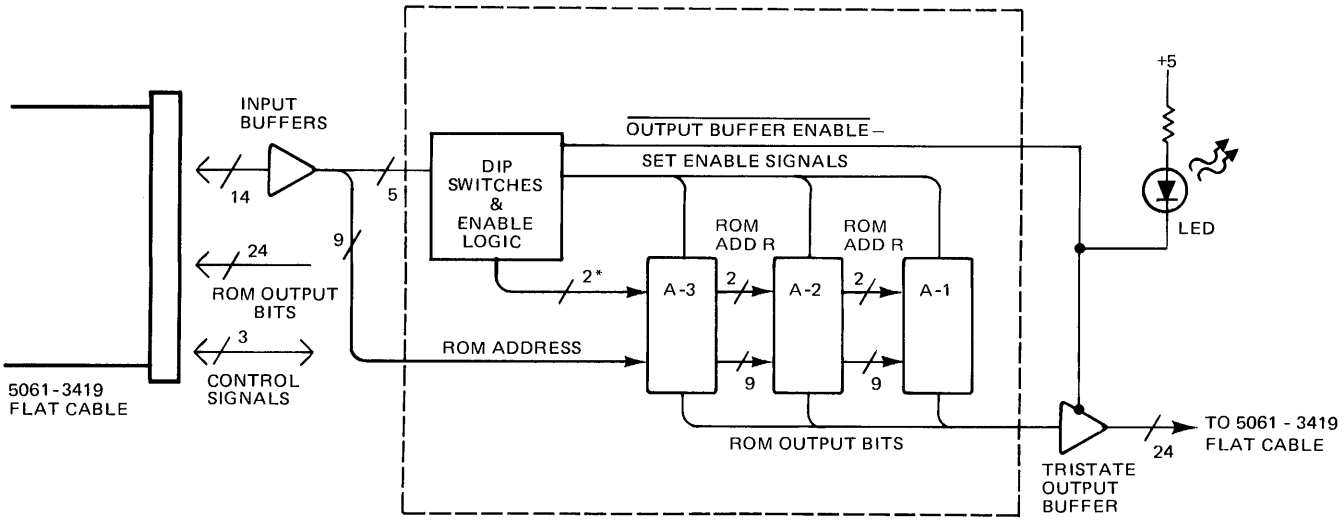
THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

GENERAL OPERATION

The 12791A Firmware Expansion Module (FEM) replaces the 13047A User Control Store Board in M/E/F-Series computers. The board occupies one I/O slot, either select code 10 or 11. A flat ribbon cable provides signal connection between the FEM, CPU, FAB, and WCS. The board contains 8 sets of three 24 pin sockets. Each set of sockets can contain either 4k, 8k, or 16k ROMs (512 x 8, 1024 x 8, or 2048 x 8). Each set of three sockets has a corresponding set of configuration switches. These switches allow the control memory located in the particular set to be configured for ROM size and logical address location. One of the eight identical sections of the FEM is shown in the following diagram.



* IF 8K OR 16K ROMs ARE USED, ONE OR TWO ADDITIONAL ADDRESS BITS RESPECTIVELY WILL BE ENABLED TO THE ROMs.

7700-557

The functional blocks in dotted section are duplicated 8 times on the FEM, once each for sets A through H (see schematic diagram 12791-60001-51 and -52).

* If 8k or 16k ROMs are used, one or two additional address bits respectively will be enabled to the ROMs.

BACKPLANE CONNECTOR P1 SIGNAL INTERCONNECTION

The FEM has only the following connections to the I/O backplane.

P1 pins 39,40	+5V I/O
P1 pins 1,2,85,86	GND
P1 pin 3	PRL (priority low)
P1 pin 23	PRH (priority high)
P1 pin 18	BIOS- (P4-)

The priority signal is passed directly between pins 3 and 23. The BIOS- is buffered and inverted to be used as a timing signal on test connector J2.

FLAT CABLE CONNECTOR J1 SIGNAL CONNECTIONS

Connector J1 connects to the CPU and any other control store boards (WCS, FAB, or additional FEM) with the following signals.

ROM output bits 0 through 23
CMAR address bits 0 through 13
Ground
WCSEN- (When asserted, a WCS board is enabled, and this signal will disable the FEM output buffer.)
RMX- (When asserted, a user external control store board is enabled, and this signal will disable the FEM output buffer.)
ECSEN- (When asserted, no higher priority control store board is enabled, and control memory on the FEM is being addressed. The output buffers are then enabled.)

TEST CONNECTOR J2 SIGNAL CONNECTIONS

Connector J2 contains the following signals which can be utilized for troubleshooting purposes.

CMAR address bits 0 through 13
The set enable signals for sets A through H
BIOS (timing signal P4)
Output Buffer Enable
CSB Disable
Ground

THEORY OF OPERATION

The CMAR bits from the CPU are buffered by 74S241 U41 and U71. The lower 9 bits, A0 through A8 are presented to all the ROMS as an address. 8k ROMs require address bits A0 through A9, and 16k ROMs require address bits A0 through A10.

Selection of a PROM set is determined by bits A9-A13 for 4k ROMs, A10-A13 for 8k ROMs and A11-A13 for 16k ROms

The function of the switches for each switch pack (SWA-SWH) is as follows:

SWITCH NO.

1 When closed, grounds the X-NOR gates output line to prevent the set from being enabled. When open, there is no connection to the X-NOR gates common output line.

2 When open, removes both A9 and A10 X-NOR gate ouput from the other X-NOR gates common ouput line. When closed, for 4k or 8k ROMs, A9 and A10 are connected.

3 When open, removes the A9 X-NOR gate output from the other X-NOR gates common output line. When closed, for 4k ROMs, A9 is connected.

4 When closed, connects A9 line to pin 22 of the ROM set as an address bit for 8k and 16k ROMs. When open, for 4k ROMs, A9 is disconnected from pin 22.

5 When closed, connects A10 line to pin 21 of the ROM set as an address bit for 16 k ROMs. When open, allows pin 21 to go low, thereby providing one of the required enabling signal for 4k or 8k ROMs.

Switches 6 through 10 determine the input which the X-NOR gates compare to the upper control memory address bits. If the control memory address matches the switch settings, the corresponding socket set is enabled.

6 When closed, provides low input to X-NOR gate to compare with bit A13. When open, provides high input to X-NOR gate.

7 When closed, provides low input to X-NOR gate to compare with bit A12. When open, provides high input to X-NOR gate.

8 When closed, provides low input to X-NOR gate to compare with bit A11. When open, provides high input to X-NOR gate.

9 When closed, provides low input to X-NOR gate to compare with bit A10. When open, provides high input to X-NOR gate.

10 When closed, provides low input to X-NOR gate to compare with bit A9. When open, provides high input to X-NOR gate.

ROM SET LOGICAL CONTROL MEMORY ADDRESS PROGRAMMING

The programming table is located in the HP 1000 M/E/F-Series Firmware Installation and Reference Manual, P/N 12791-90001. If 4k ROMs are used, any of the 32 discrete 512 word block may be programmed. If 8k ROMs are used, any of the 16 discrete 1024 word blocks may be programmed. If 16k ROMs are used in the set, any of the 8 discrete 2048 word blocks may be programmed.

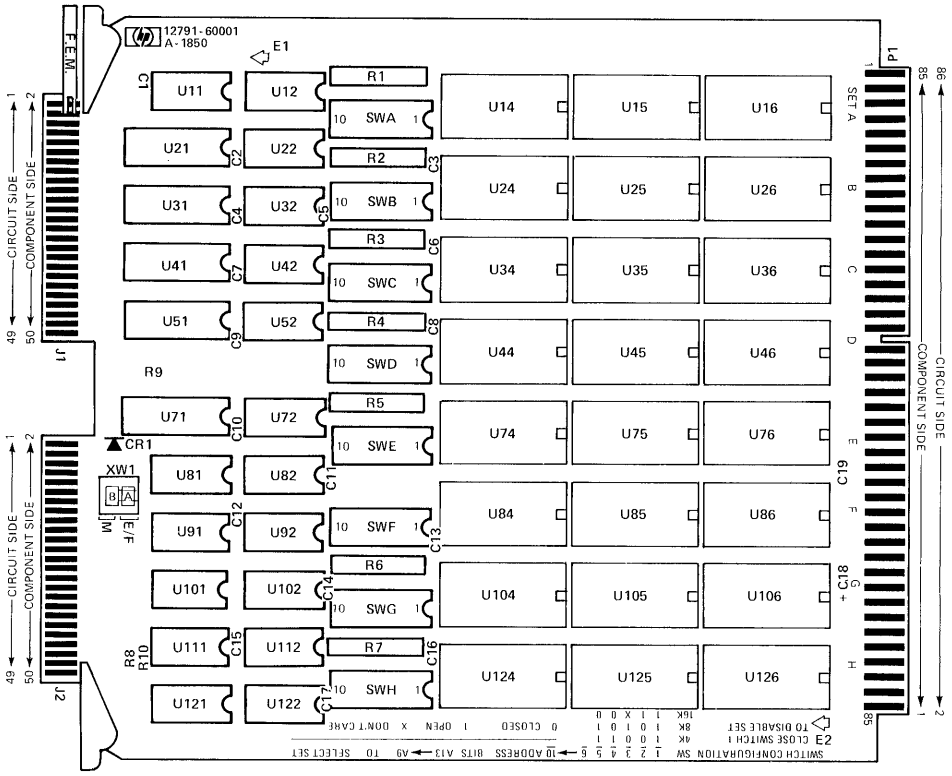
ROM ACCESS REQUIREMENTS

The time delay between address input to data output from the FEM does not exceed 120ns. The delay in the input and output buffer gates and traces total 40ns. Therefore the maximum acceptable address access delay time for the ROMs is 80ns. The maximum acceptable chip enable delay time for the ROMs is 40ns.

CONTROL MEMORY BOARD PRIORITY

The FEM receives two inputs from other physical locations of control memory. The signal WCSEN- emanates from the 13197A WCS card. The signal RMX- is issued from a user designed control store board. If either WCSEN- or RMX- is asserted, the signal CSB DISABLE will disable the output buffers on the FEM.

When control memory located on the FEM is addressed, the common output of the X-NOR gates will go high and enable the appropriate ROM set via enable E3. The common output is inverted to become ENRMX-. If ENRMX- is valid, the output buffers will be enabled, and the LED on the board will be lit. ENRMX- is then buffered to become ECSEN-. When control memory on the FEM is accessed, the assertion of ECSEN- will disable all lower priority control memory boards (FAB board, and CPU board).

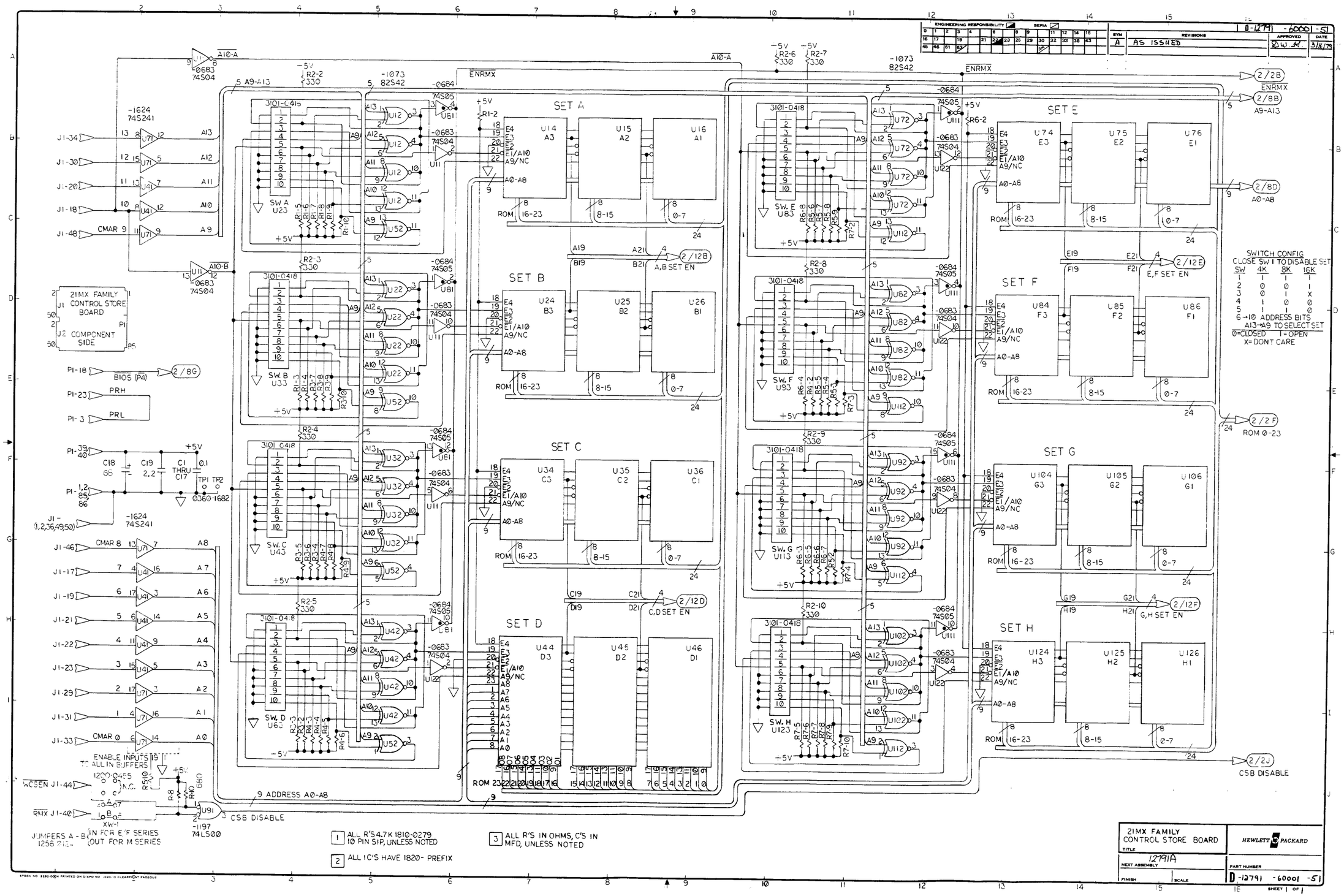


12791A Firmware Expansion Module Assembly
12791-60001

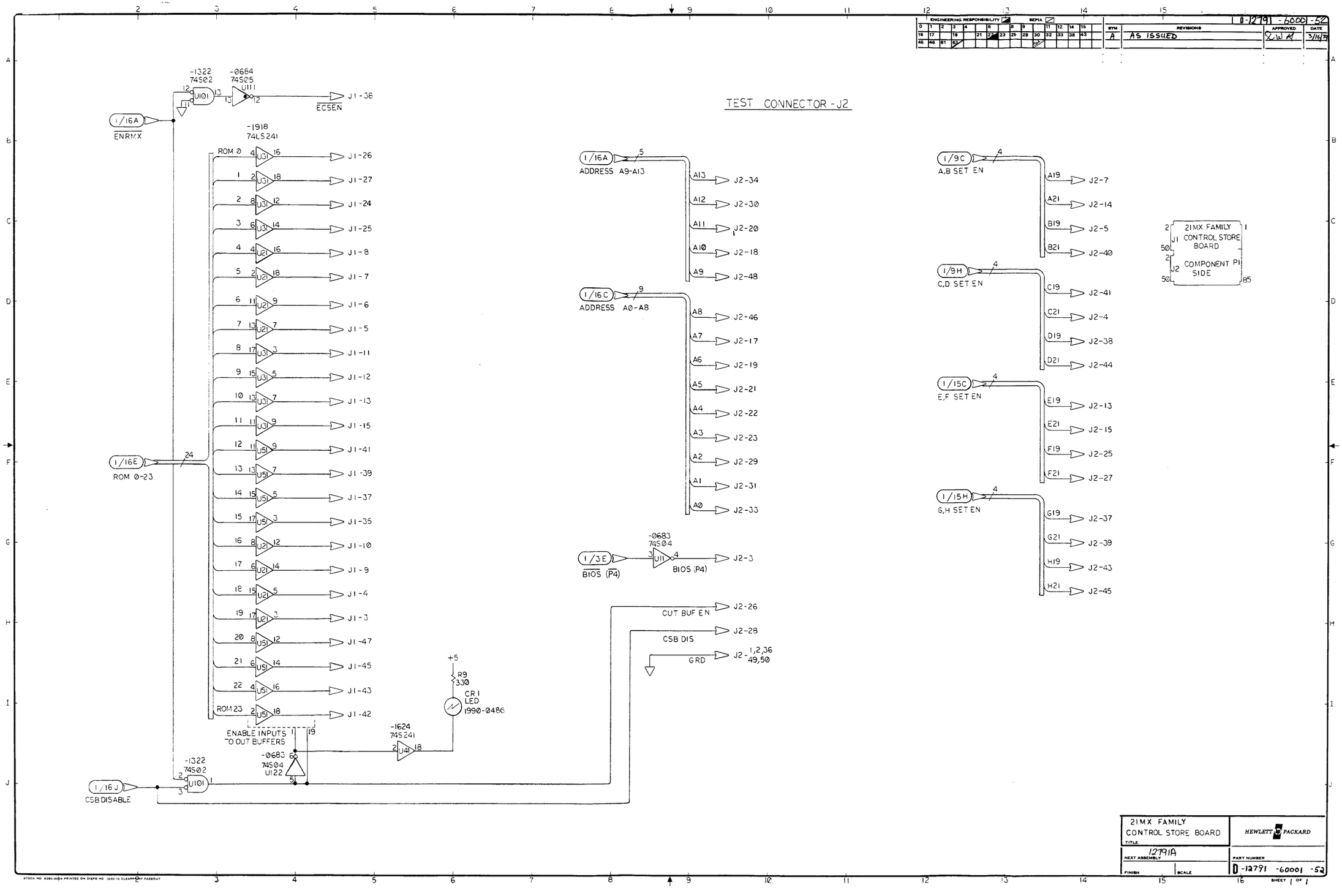
12791A Firmware Expansion Module Parts List (12791-60001) Sht. 1 of 2

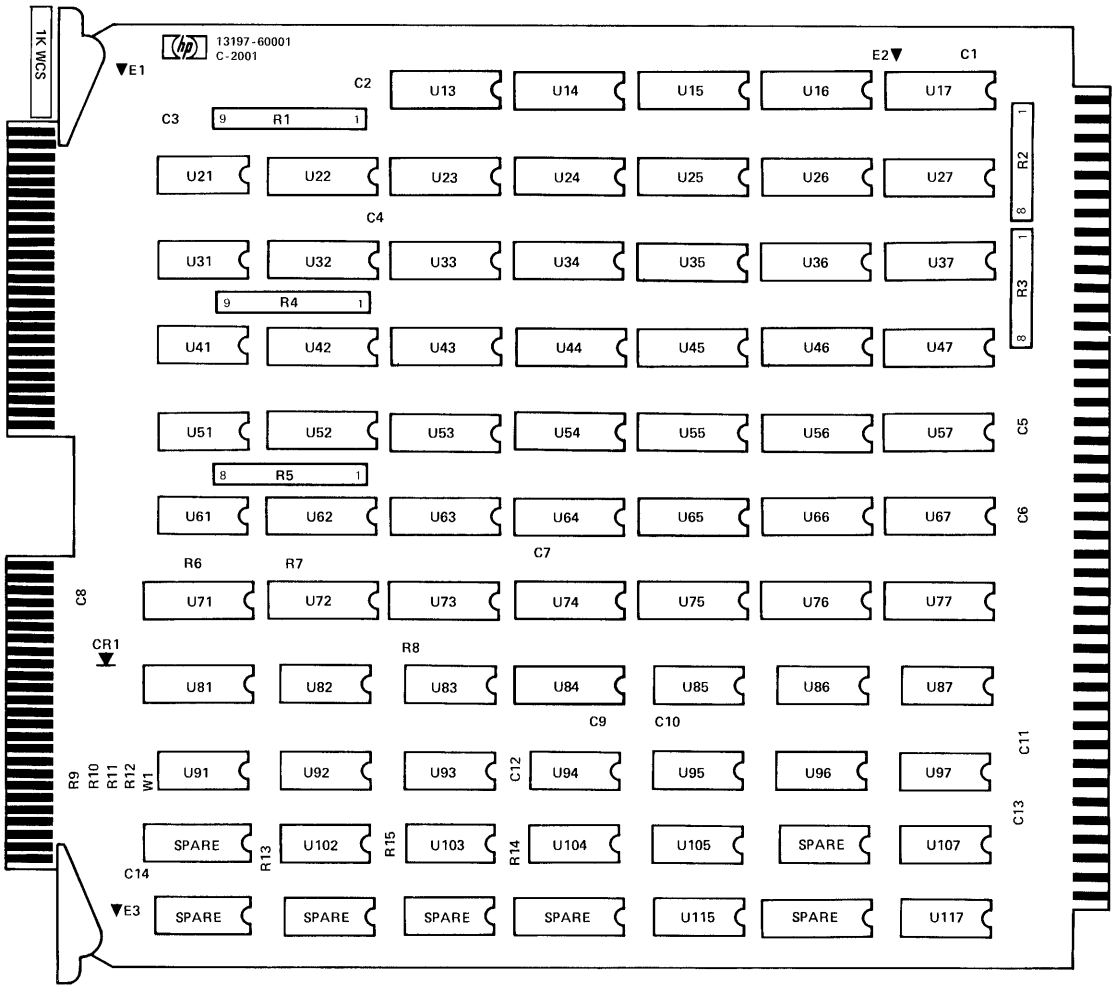
ITEM NO	REFERENCE DESIGNATOR FIRST SIX	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	C19	CAP. 2.2UF		0160-0128		U	1
01	C1-17	CAP .1UF 20% 50V		0160-0576		U	17
01	C18	CAP 68UF 20%		0180-1835		D	1
01	E1,2	TERM-STUD SGL		0360-1682		U	2
01	R9	RES 330 5% .25		0683-3315		U	1
01	R8,10	RES 680 5% .25		0683-6815		U	2
		SOCKET 8 DIP LO		1200-0455		U	1
		SOCKET 24 PIN		1200-0541		U	24
01	W1,2	JMPR PLUG .3"C-C		1258-0124		U	2
		PIN GRV .062X.25		1460-0116		U	2
01	R2	NTWK RES 9X330		1810-0272		U	1
01	R1,3-7	NTWK RES 9X4.7K		1810-0279		U	6
01	U11,122	IC SN74S04N		1820-0683		U	2
01	U8,111	IC SN74S05N		1820-0684		U	2
01 03	U12,22,32,42,52,72,82 92,102,112	IC N82S42A		1820-1073		U	10
01	U91	IC SN74LS00N		1820-1197		U	1
01	U101	IC SN74S02N		1820-1322		U	1
01	U41,71	ICSN74S241N		1820-1624		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U21,31,51	IC SN74LS241N		1820-1918		U	3
01	CR1	DIODE-LIGHT EMIT		1990-0486		U	1
01 03	U23,33,43,63,83,93 113,123	SW DIP 10 ROCKER		3101-0418		U	8
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-RED		5040-6073		W	1
		PC BOARD-ETCHED		12791-80001		W	1
01	TEST FIXTURE	BED OF NAILS		ET13433		1	0
		UNIVERSL FIXTURE		ET13448		1	0


21MX FAMILY CONTROL STORE BOARD
J1 COMPONENT SIDE
P1
SET A
SET B
SET C
SET D
SET E
SET F
SET G
SET H
SW A U23
SW B U33
SW C U43
SW D U63
SW E U83
SW F U93
SW G U113
SW H U123
ROM 16-23
8-15
0-7
A,B SET EN
C,D SET EN
E,F SET EN
G,H SET EN
ROM 0-23
CSB DISABLE
9 ADDRESS A0-A8
3 CSB DISABLE
ENABLE INPUTS TO ALL IN BUFFERS
JUMPERS A-B 1256-2182- IN FOR E/F SERIES OUT FOR M SERIES
SWITCH CONFIG
CLOSE SW 1 TO DISABLE SET
SW 4K 8K 16K
1 1 1 1
2 0 0 1
3 0 1 X
4 1 0 0
5 1 1 0
6→10 ADDRESS BITS A13→A9 TO SELECT SET
0=CLOSED 1=OPEN X=DONT CARE
1 ALL R'S 4.7K 1810-0279 10 PIN SIP, UNLESS NOTED
2 ALL IC'S HAVE 1820- PREFIX
3 ALL R'S IN OHMS, C'S IN MFD, UNLESS NOTED
21MX FAMILY CONTROL STORE BOARD
HEWLETT PACKARD
12791A
D-12791 -60001 -51
REVISIONS
A AS ISSUED
3/16/79

VIA -11/ -12


TEST CONNECTOR - J2
-1322 74S02 U101
-0684 74S05 U111
ECSEN
J1-36
1/16A
ENRMX
-1918 74LS241
ROM Ø
J1-26
J1-27
J1-24
J1-25
J1-8
J1-7
J1-6
J1-5
J1-11
J1-12
J1-13
J1-15
J1-41
J1-39
J1-37
J1-35
J1-10
J1-9
J1-4
J1-3
J1-47
J1-45
J1-43
ROM 23
J1-42
1/16E
ROM Ø-23
ENABLE INPUTS TO OUT BUFFERS
-1624 74S241 U41
-0683 74S04 U122
-1322 74S02 U101
1/16J
CSB DISABLE
+5
R9 330
CR1 LED 1990-0486
1/16A
ADDRESS A9-A13
A13 J2-34
A12 J2-30
A11 J2-20
A10 J2-18
A9 J2-48
1/16C
ADDRESS A0-A8
A8 J2-46
A7 J2-17
A6 J2-19
A5 J2-21
A4 J2-22
A3 J2-23
A2 J2-29
A1 J2-31
A0 J2-33
1/3E
BIOS (P4)
-0683 74S04 U11
BIOS (P4) J2-3
CUT BUF EN J2-26
CSB DIS J2-28
GRD J2-1,2,36 49,50
1/9C
A,B SET EN
A19 J2-7
A21 J2-14
B19 J2-5
B21 J2-40
1/9H
C,D SET EN
C19 J2-41
C21 J2-4
D19 J2-38
D21 J2-44
1/15C
E,F SET EN
E19 J2-13
E21 J2-15
F19 J2-25
F21 J2-27
1/15H
G,H SET EN
G19 J2-37
G21 J2-39
H19 J2-43
H21 J2-45
21MX FAMILY CONTROL STORE BOARD
J1
J2
COMPONENT PI SIDE
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
SYM
A
AS ISSUED
APPROVED
DATE
3/16/79
D-12791-60001-52
21MX FAMILY CONTROL STORE BOARD
TITLE
12791A
NEXT ASSEMBLY
FINISH
SCALE
HEWLETT PACKARD
PART NUMBER
D-12791-60001-52
SHEET 1 OF 1

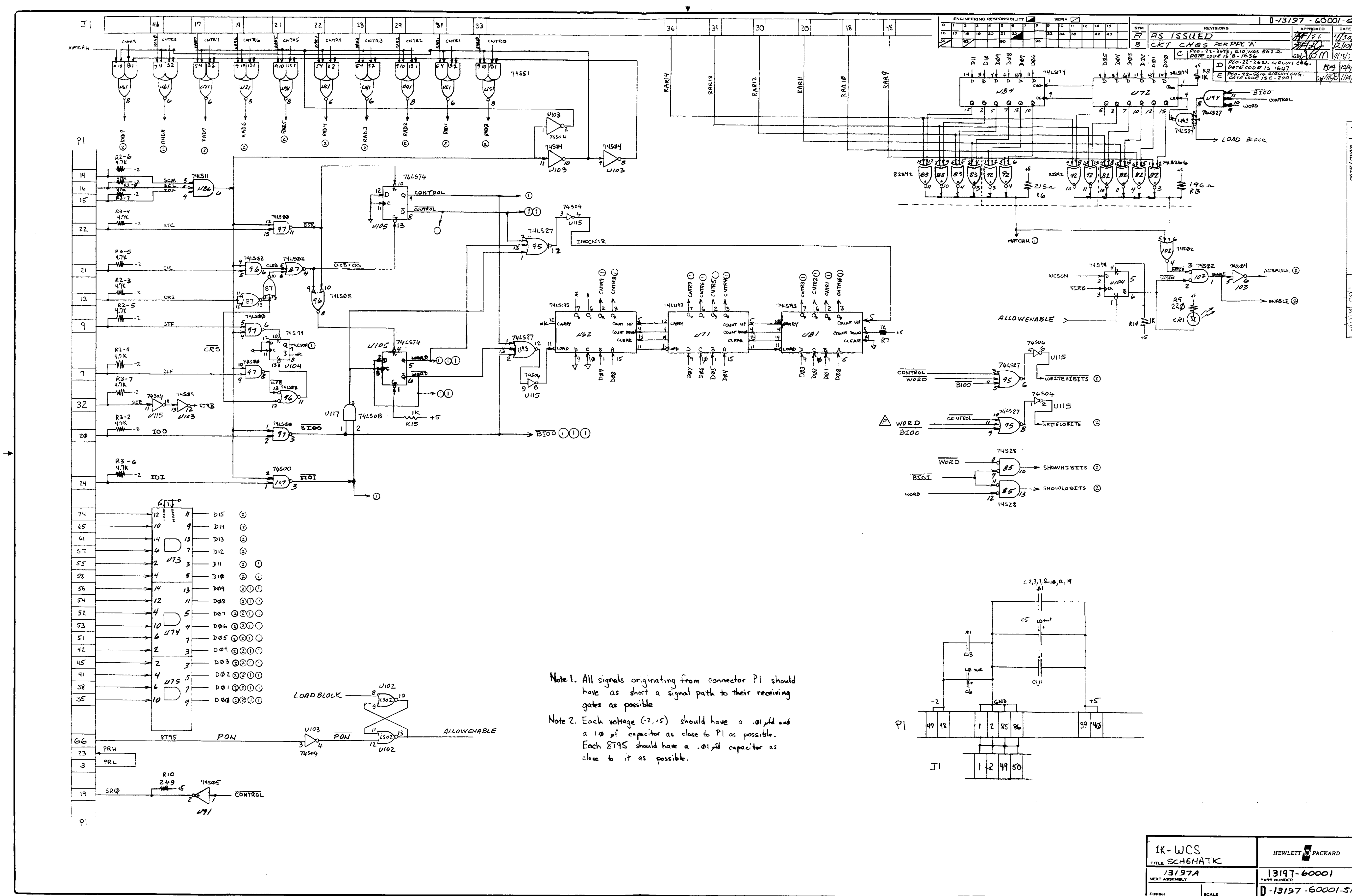


13197A Writable Control Store Assembly
13197-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	C1,11	CAP 0.1UF		0150-0121		U	2	
01 03	C2,3,4,7,8,9,10,12 13,14	CAP .01UF		0160-2055		U	10	
00	C5,6	CAP 1UF 10%		0180-0291		D	2	
00	E1-4	STUD SOLDER TERM		0360-0294		U	4	
00	R13	RES 196 1%.125		0698-3440		D	1	
00	R6	RES 215 1%.125		0698-3441		D	1	
00	R10	RES 249 1%.125		0698-4421		U	1	
01	R7,8,11,14,15	RES 1K 1%.125		0757-0280		D	5	
00	R12	RES 10K 1%.125		0757-0442		D	1	
00	R9	RES 221 1% .25		0757-0719		U	1	
		JMPR PLUG .3"C-C		1258-0124		U	2	
		PIN GRV .062X.25		1480-0116		U	2	
00	R2,3	RES NET 7X4.7K		1810-0125		U	2	
01	R1,4,5	RES NET 8X500		1810-0132		U	3	
01 03	U13-16,23-26,33-36 43-46,53-56,63-66	RNDM ACS MEM		1816-0723		U	24	
00	U107	IC SN74S00N		1820-0681		U	1	
01	U103,115	IC SN74S04N		1820-0683		U	2	
		IC SN74S05N		1820-0684		U	1	

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	U91			1820-0684				
01	U104	IC SN74S74N		1820-0693		U	1	
01	U82,83,92	IC N82S42A		1820-1073		U	3	
01 03	U17,27,37,47,57,67 76,77	IC 8T13B		1820-1080		U	8	
01	U105	IC SN74LS74N		1820-1112		U	1	
00	U87	IC SN74LS02N		1820-1144		U	1	
01	U21,31,41,51,61	IC SN74S51N		1820-1158		U	5	
00	U85	IC SN7428N		1820-1184		U	1	
01	U62,71,81	IC SN74LS193N		1820-1194		U	3	
01	U84,72	IC SN74LS174N		1820-1196		U	2	
00	U97	IC SN74LS00N		1820-1197		U	1	
01	U96,117	IC SN74LS08N		1820-1201		U	2	
00	U86	IC SN74LS11N		1820-1203		U	1	
01	U93,94,95	IC SN74LS27N		1820-1206		U	3	
00	U102	IC SN74S02N		1820-1322		U	1	
01 03	U22,32,42,52,73, 74,75	IC 8T95B		1820-1477		U	7	
00	CR1	DIODE-LIGHT EMIT		1990-0327		U	1	
		EXTRACTOR-PC GRY		5040-6006		W	1	

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
		EXTRACTOR-RED		5040-6073		W	1	

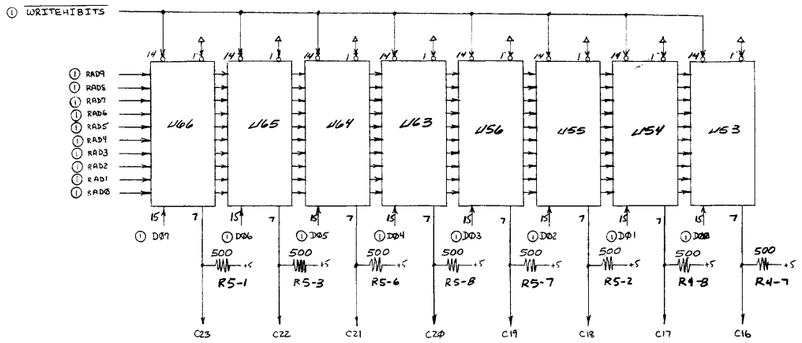

Note 1. All signals originating from connector P1 should have as short a signal path to their receiving gates as possible.
Note 2. Each voltage (-2, +5) should have a .01 µfd and a 1.0 µf capacitor as close to P1 as possible. Each 8T95 should have a .01 µfd capacitor as close to it as possible.
1K-WCS
TITLE SCHEMATIC
13197A
NEXT ASSEMBLY
13197-60001
PART NUMBER
D-13197-60001-51
HEWLETT PACKARD

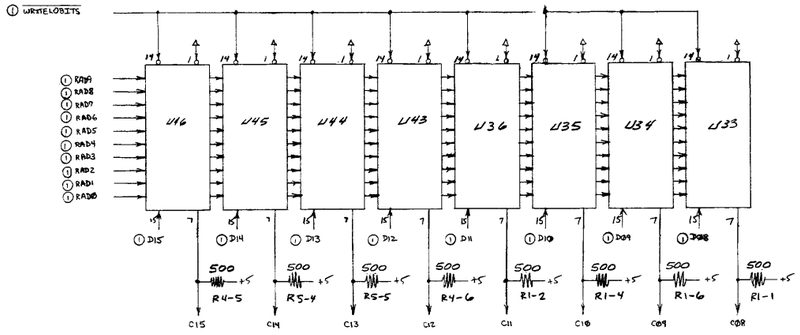
D-13197-60001-52

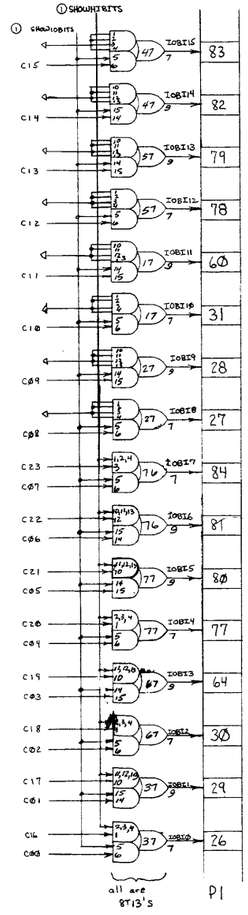
ENGINEERING RESPONSIBILITY															
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15
16	17	18	19	20	21	22			33	34	38		42	43
S		65				90		93						

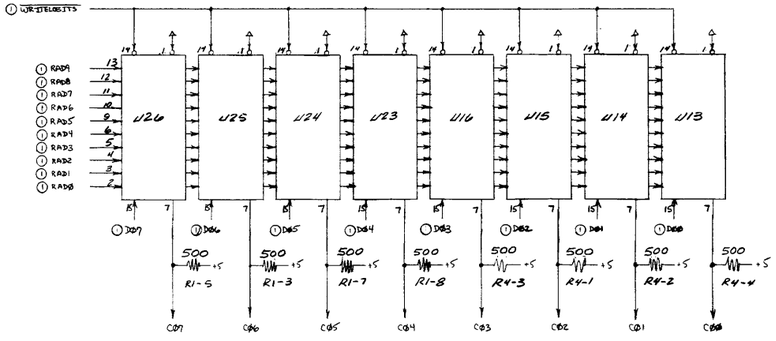
SEPIA

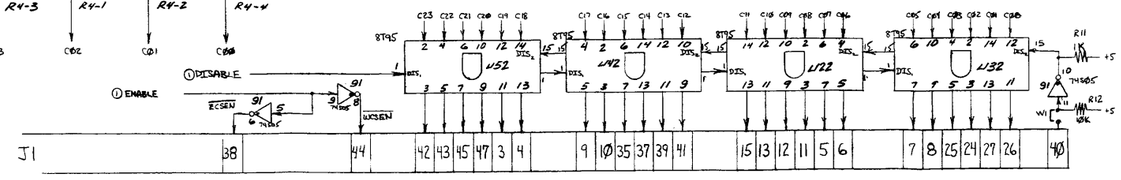
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	BF/KF	4/30/76
B	PCO-22-3473 - DATE CODE IS 8-1636	GD/JWM	9/17/76
C	PCO-22-3621. 500 WAS 1K, DATE CODE IS 1647	GD/BBB	12/3/76



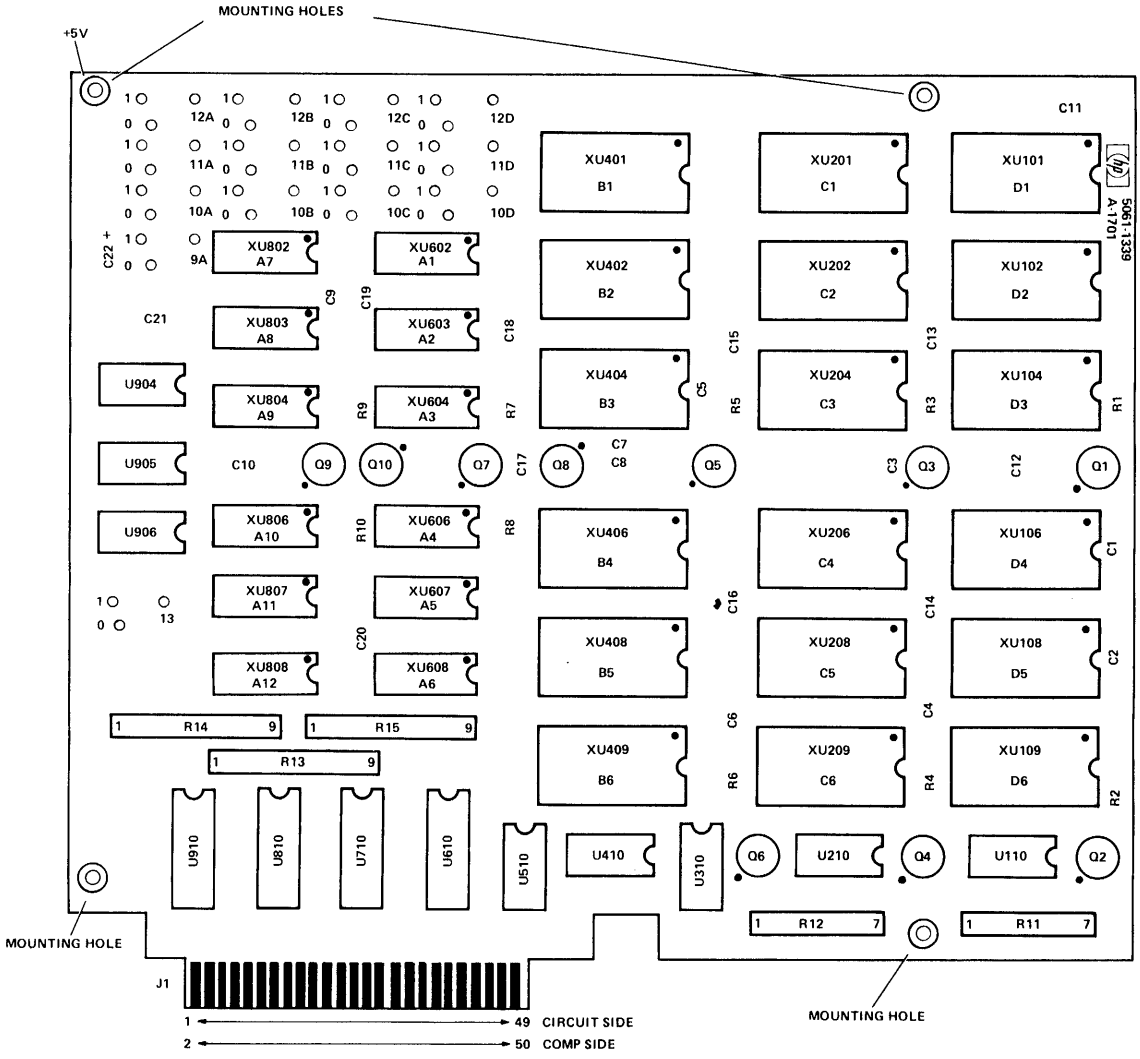








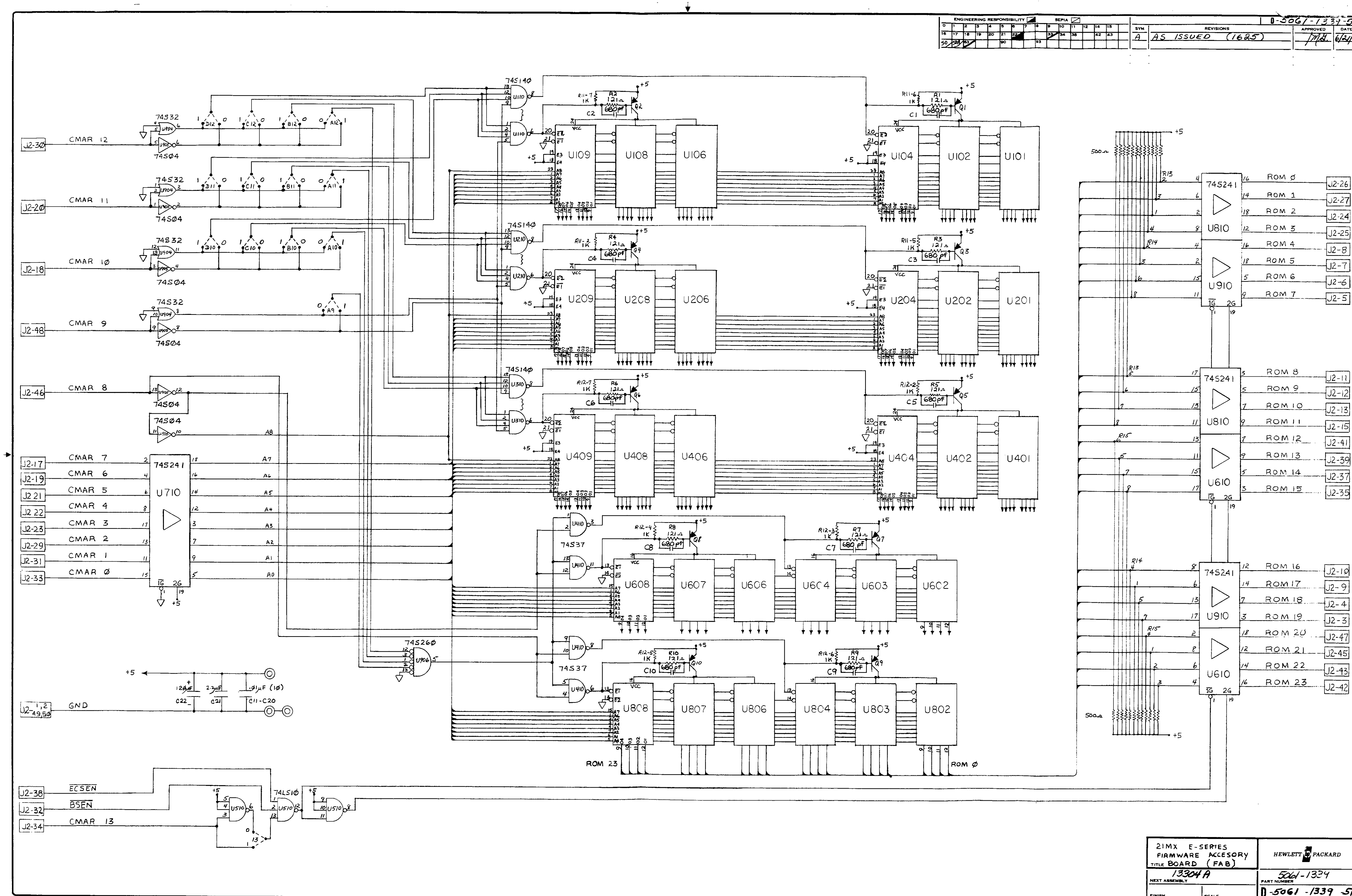
1K WCS TITLE SCHEMATIC	HEWLETT PACKARD
13197A NEXT ASSEMBLY	13197-60001 PART NUMBER
FINISH / SCALE	D-13197-60001-52 SHEET 1 OF 1

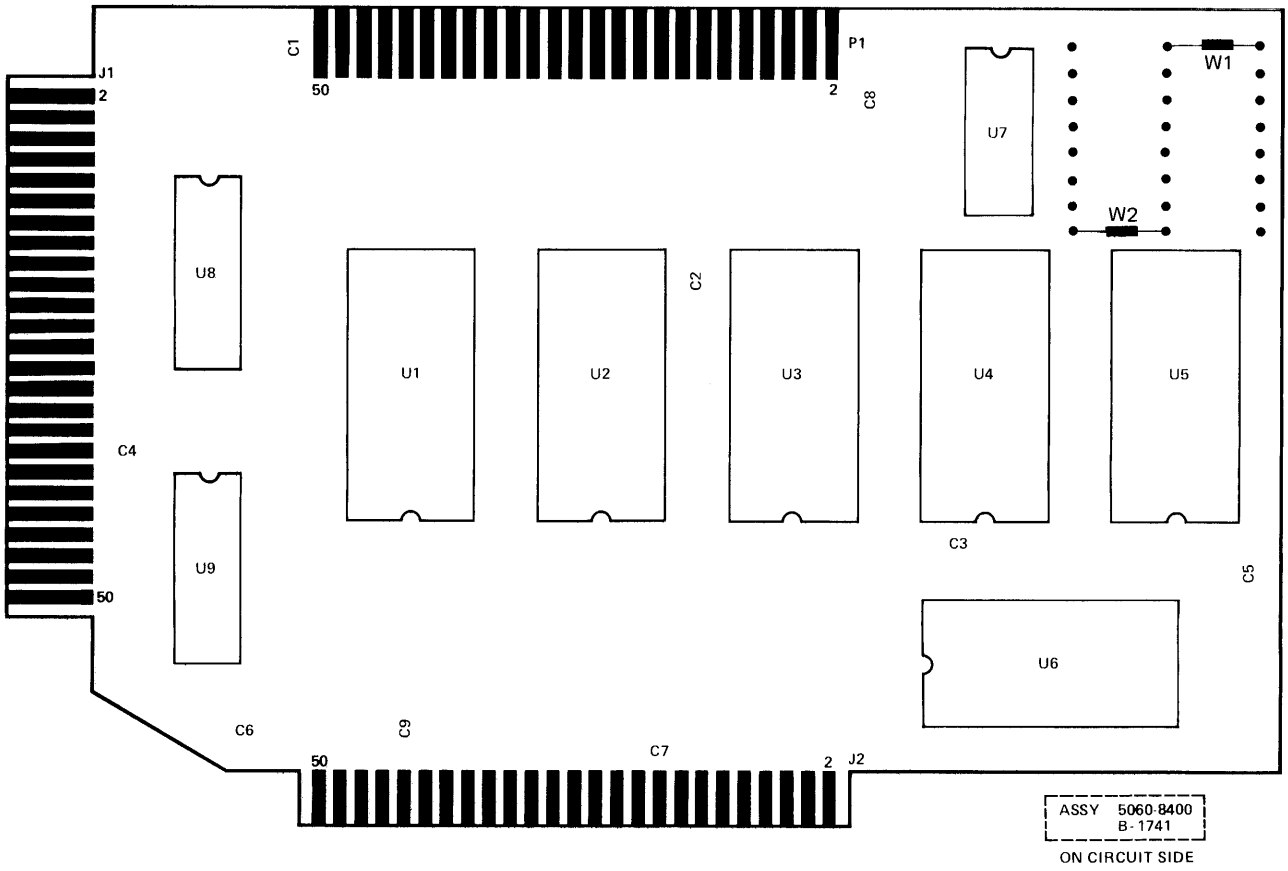


13304A Firmware Accessory Board Assembly
5061-1339

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	C21	CAP. 2.2UF		0160-0128		D	1	
01	C11-20	CAP .01UF		0160-2055		U	10	
00	C1-10	CAP 680PF 10%		0160-3573		U	10	
00	C22	CAP 120UF 10%		0180-2145		U	1	
		PAD-MTG TO5		0340-0164		U	10	
00	F1	STUD SOLDER TERM		0360-0294		U	1	
00	R1-10	RES 121 1%.125		0757-0403		D	10	
		SOCKET 24 PIN		1200-0541		U	18	
		SKT 16DIP LO DS		1200-0607		U	12	
		SOCKET PC SINGLE		1251-1556		U	42	
		JMPR PLUG .3"C-C		1258-0124		U	14	
01	R11,12	RES NET 7X1K		1810-0030		U	2	
01	R13-15	RES NET 8X500		1810-0132		U	3	
00	U905	IC SN74S04N		1820-0683		U	1	
01	U110,210,310	IC SN74S140N		1820-0697		U	3	
00	U510	IC SN74LS10N		1820-1202		U	1	
00	U906	IC SN74S260N		1820-1275		U	1	
00	U904	IC SN74S32N		1820-1449		U	1	

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	U410	IC SN74S37N		1820-1450		U	1	
01	U610,710,810,910	ICSN74S241N		1820-1624		U	4	
00	Q1-10	XSTR PNP 2N3467		1853-0399		U	10	

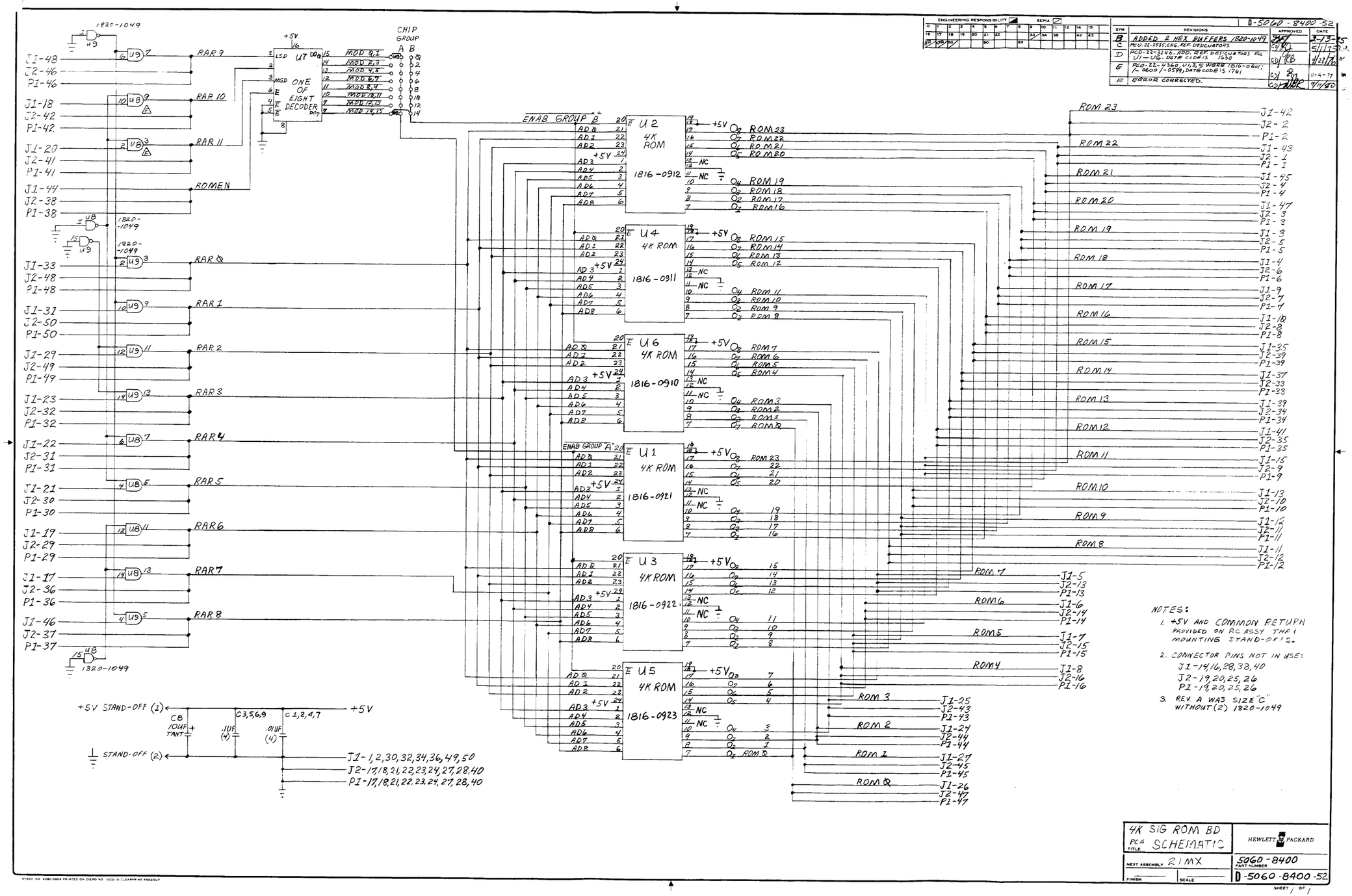

D-5061-1339-51
A AS ISSUED (1625)
21MX E-SERIES FIRMWARE ACCESORY BOARD (FAB)
13304A
5061-1334
D-5061-1339-51
HEWLETT PACKARD
CMAR 12
CMAR 11
CMAR 10
CMAR 9
CMAR 8
CMAR 7
CMAR 6
CMAR 5
CMAR 4
CMAR 3
CMAR 2
CMAR 1
CMAR Ø
CMAR 13
ECSEN
BSEN
GND
ROM Ø
ROM 23

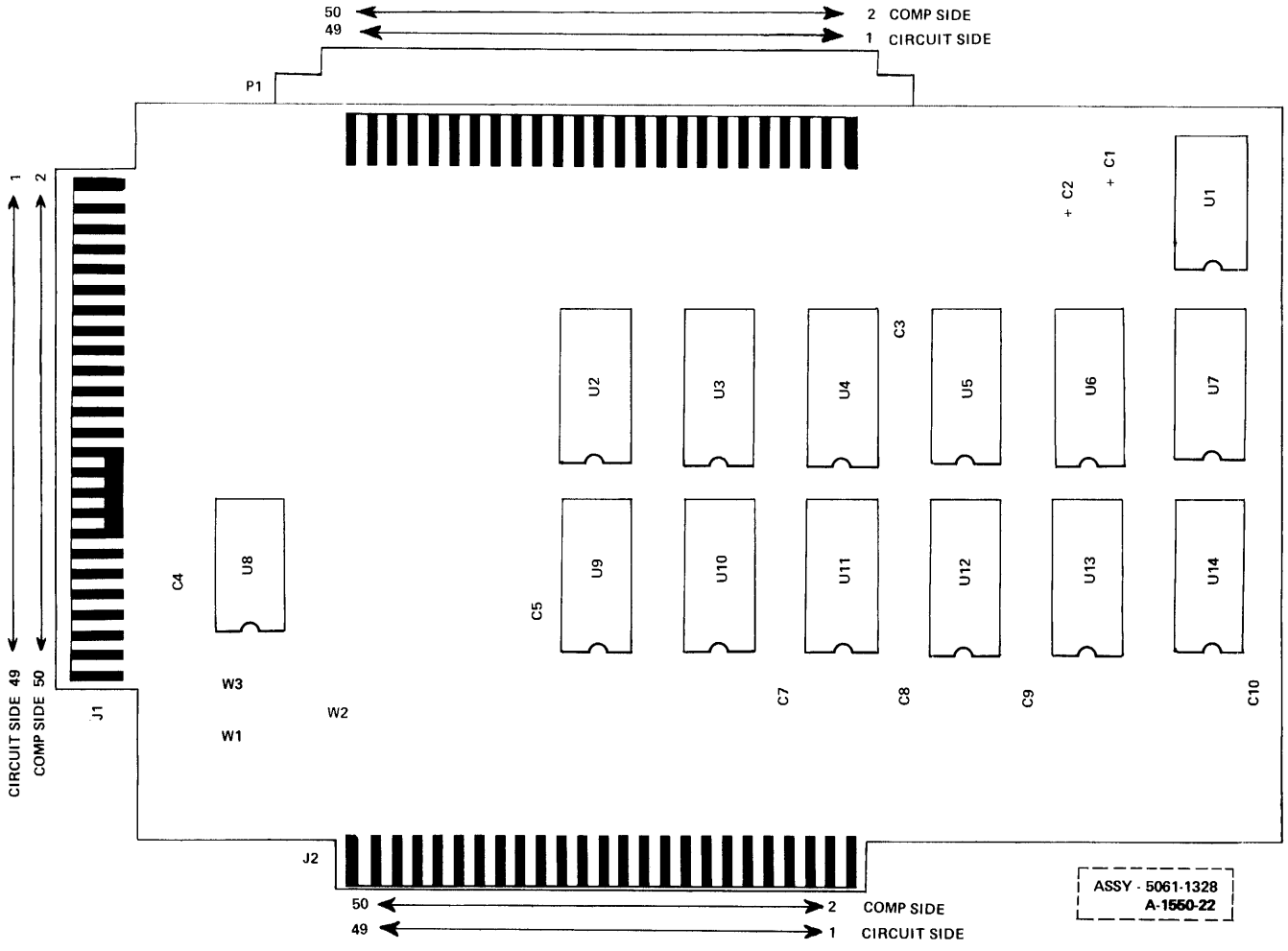


4K ROM Base-Set Assembly
5060-8400

4K ROM Base-Set Assembly Parts List (5060-8400)

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
01	C3,5,6,9	CAP 0.1UF		0150-0121		U	4	
01	C1,2,4,7	CAP .01UF		0160-2055		U	4	
00	C8	CAP 10UF 10%		0180-0374		D	1	
00	U6	4K ROM		1816-0910		U	1	
00	U4	4K ROM		1816-0911		U	1	
00	U2	4K ROM		1816-0912		U	1	
01	U1	IC ROM BIPOLAR		1816-0921		U	1	
01	U3	IC ROM BIPOLAR		1816-0922		U	1	
01	U5	IC ROM BIPOLAR		1816-0923		U	1	
00	U8,9	DM8097N		1820-1049		U	2	
00	U7	IC SN74S138N		1820-1240		U	1	
		LABEL-USA		7120-6830		L	1	
00	W1,2	WIRE JUMPERS		8159-0005		D	2	
		BOARD-ETCHED		5080-9759		W	1	


D-5060-8400-52
ADDED 2 HEX BUFFERS 1820-1049
ERROR CORRECTED.
NOTES:
1. +5V AND COMMON RETURN PROVIDED ON RC ASSY THR I MOUNTING STAND-OFFS.
2. CONNECTOR PINS NOT IN USE:
J1-19,16,28,38,40
J2-19,20,25,26
P1-19,20,25,26
3. REV A WAS SIZE "C" WITHOUT (2) 1820-1049
4K SIG ROM BD
PCA TITLE SCHEMATIC
HEWLETT PACKARD
NEXT ASSEMBLY 21MX
5060-8400
PART NUMBER
D-5060-8400-52
SHEET 1 OF 1



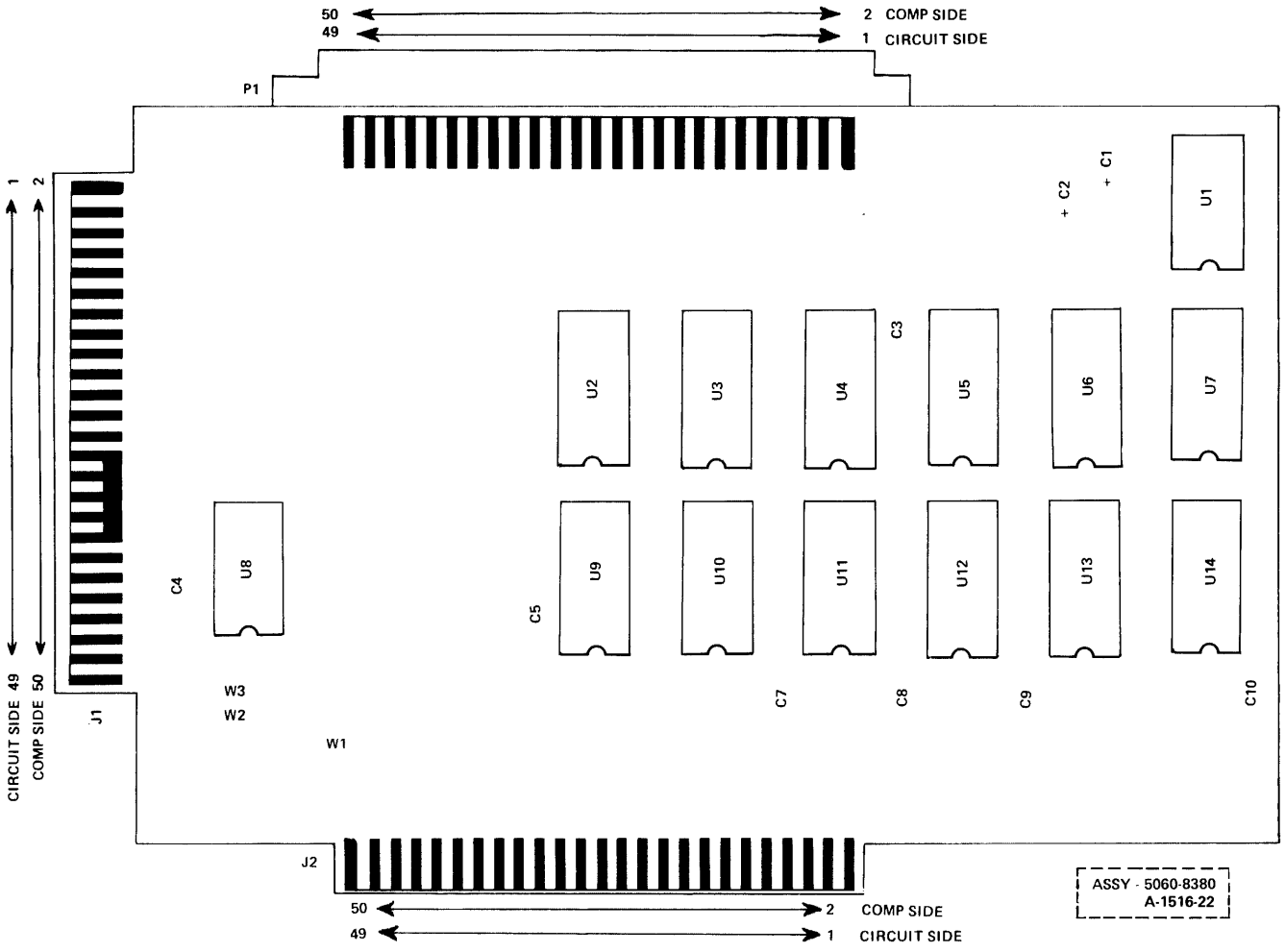
Fast FORTRAN Processor I Assembly
5061-1328

Fast FORTRAN Processor I Assembly Parts List (5061-1328) Sht. 1 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	C1,4	CAP 0.1UF		0150-0121		U	2	
01	C3,5,7-10	CAP .01UF		0160-2055		U	6	
00	C2	CAP 10UF 10%		0180-0374		D	1	
		STAND-OFF		0380-0058		U	3	
		CONN PC2X25.100S		1251-3106		U	1	
		IC HPROM-1024-5		1816-0015		3	12	
01	NOTE:							
03	QUANTITIES OF PROMS							
05	LISTED ABOVE ARE							
07	THOSE REQUIRED TO							
09	MAKE ROMS							
00	U3	IC ROM 4X256		1816-0429		3	1	
00	U4	IC ROM 4X256		1816-0430		3	1	
00	U5	IC ROM 4X256		1816-0431		3	1	
00	U2	IC ROM 4X256		1816-0432		3	1	
00	U6	IC ROM 4X256		1816-0433		3	1	
00	U7	IC ROM 4X256		1816-0434		3	1	
00	U13	I.C. ROM 4X256		1816-0630		3	1	
00	U12	IC ROM 4X256		1816-0851		3	1	
00	U10	IC ROM 4X256		1816-0852		3	1	
00	U11	IC ROM 4X256		1816-0853		3	1	
		IC ROM 4X256		1816-0854		3	1	

Fast FORTRAN Processor I Assembly Parts List (5061-1328) Sht. 2 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	U9			1816-0854				
00	U14	IC ROM 4X256		1816-0855		3	1	
00	U1	IC SN74H20N		1820-0373		U	1	
00	U8	IC SN74H04N		1820-0424		U	1	
		LKWSHR 6 HFL		2190-0006		U	3	
		SCR #6-32X.312L		2360-0115		U	3	
		WSHR #6 SS		3050-0228		U	3	
		LABEL-USA		7120-6830		L	1	
		WIRE JUMPERS		8159-0005		D	3	



Fast FORTRAN Processor II Assembly
5060-8380

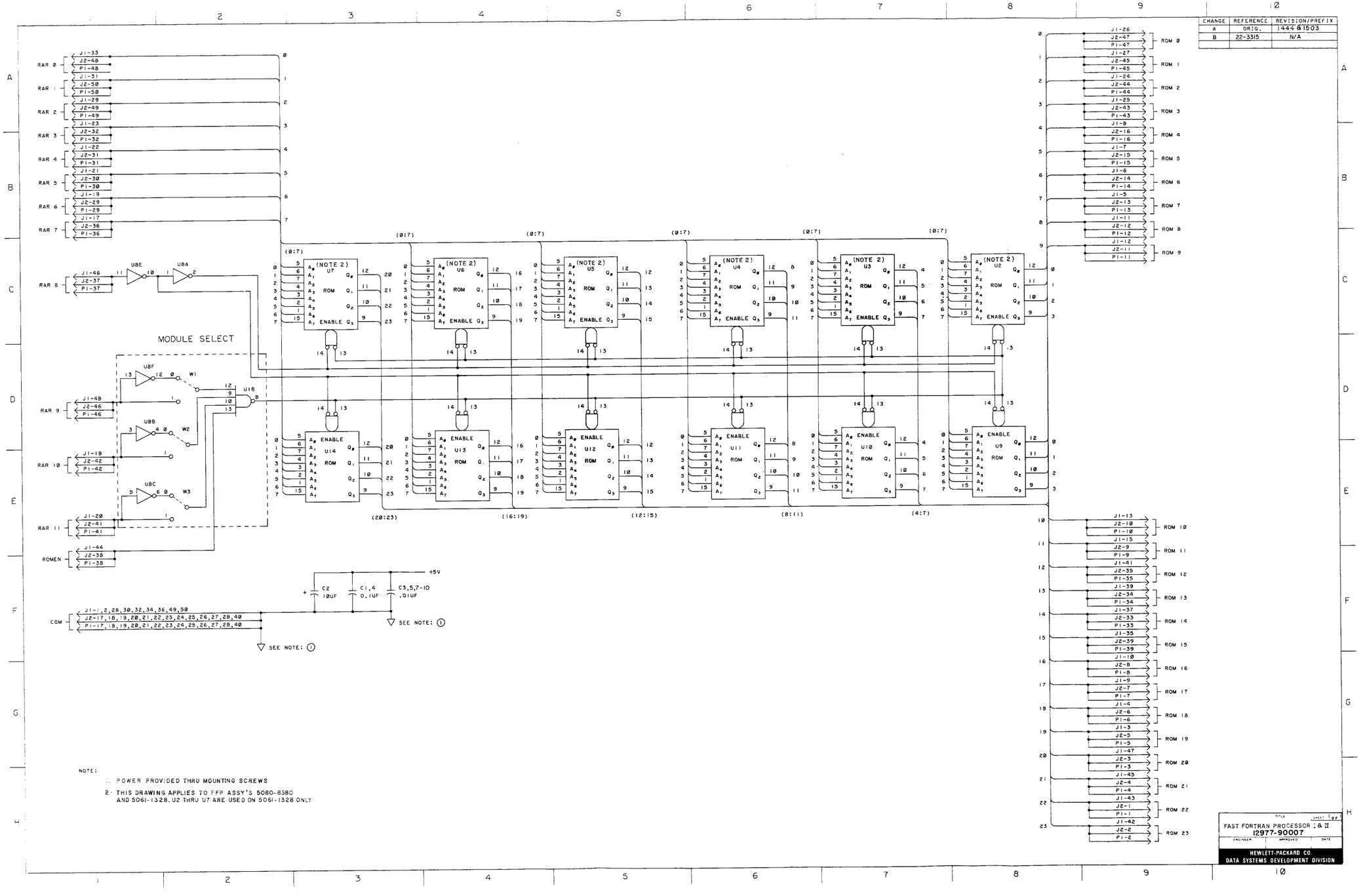
Fast FORTRAN Processor II Assembly Parts List (5060-8380) Sht 1 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
		CAP 0.1UF		0150-0121		U	2	
00	C1,4							
		CAP .01UF		0160-2055		U	6	
01	C3,5,7-10							
		CAP 10UF 10%		0180-0374		D	1	
00	C2							
		STAND-OFF		0380-0058		U	3	
		CONN PC2X25.100S		1251-3106		U	1	
00	J1							
		IC HPROM-1024-5		1816-0015		3	12	
01	NOTE:							
03	QUANTITIES OF							
05	PROMS LISTED							
07	ABOVE ARE THOSE							
09	REQUIRED TO							
11	MAKE ROMS							
		I.C. ROM 4X256		1816-0401		3	1	
00	U2							
		I.C. ROM 4X256		1816-0402		3	1	
00	U3							
		I.C. ROM 4X256		1816-0403		3	1	
00	U4							
		I.C. ROM 4X256		1816-0404		3	1	
00	U5							
		I.C. ROM 4X256		1816-0405		3	1	
00	U6							
		I.C. ROM 4X256		1816-0406		3	1	
00	U7							
		I.C. ROM 4X256		1816-0617		3	1	
00	U14							
		I.C. ROM 4X256		1816-0618		3	1	
00	U13							
		I.C. ROM 4X256		1816-0619		3	1	
00	U12							
		I.C. ROM 4X256		1816-0620		3	1	
00	U11							

Fast FORTRAN Processor II Assembly Parts List (5060-8380) Sht. 2 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
00	U10	I.C. ROM 4X256		1816-0621		3	1	
00	U9	I.C. ROM 4X256		1816-0622		3	1	
00	U1	IC SN74H20N		1820-0373		U	1	
00	U8	IC SN74H04N		1820-0424		U	1	
		LKWSHR 6 HEL		2190-0006		U	3	
		SCR #6-32X.312L		2360-0115		U	3	
		WSHR #6 SS		3050-0228		U	3	
		LABEL-USA		7120-6830		L	1	
00	W1-3	WIRE JUMPERS		8159-0005		D	3	

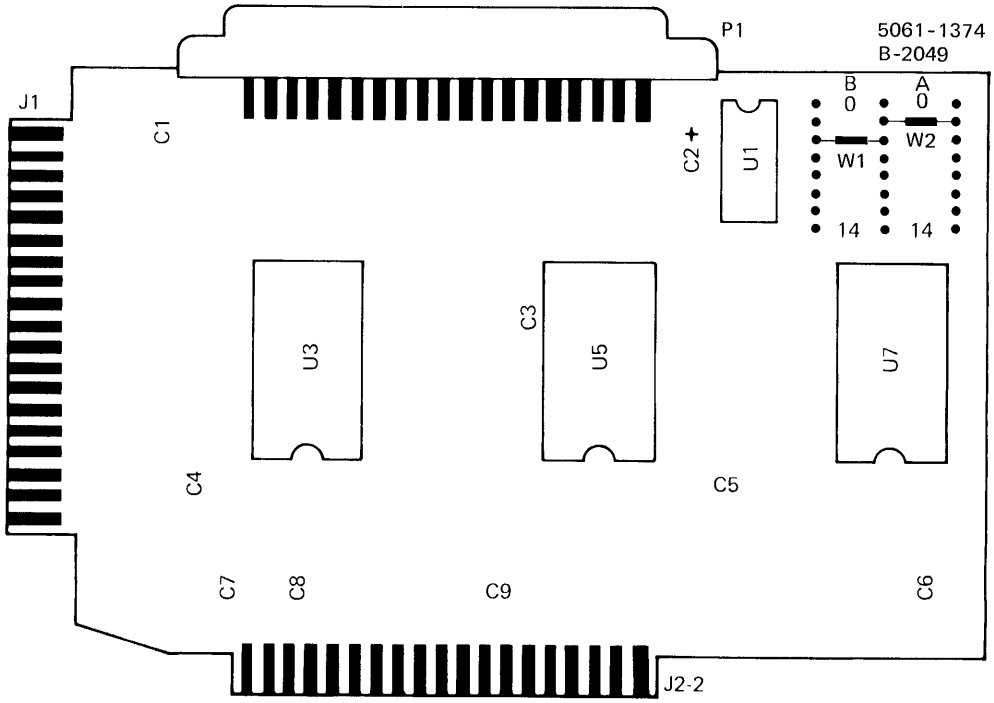
CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	1444 &1503
B	22-3315	N/A



NOTE:

1. POWER PROVIDED THRU MOUNTING SCREWS
2. THIS DRAWING APPLIES TO FFP ASSY'S 5060-8380 AND 5061-1328. U2 THRU U7 ARE USED ON 5061-1328 ONLY

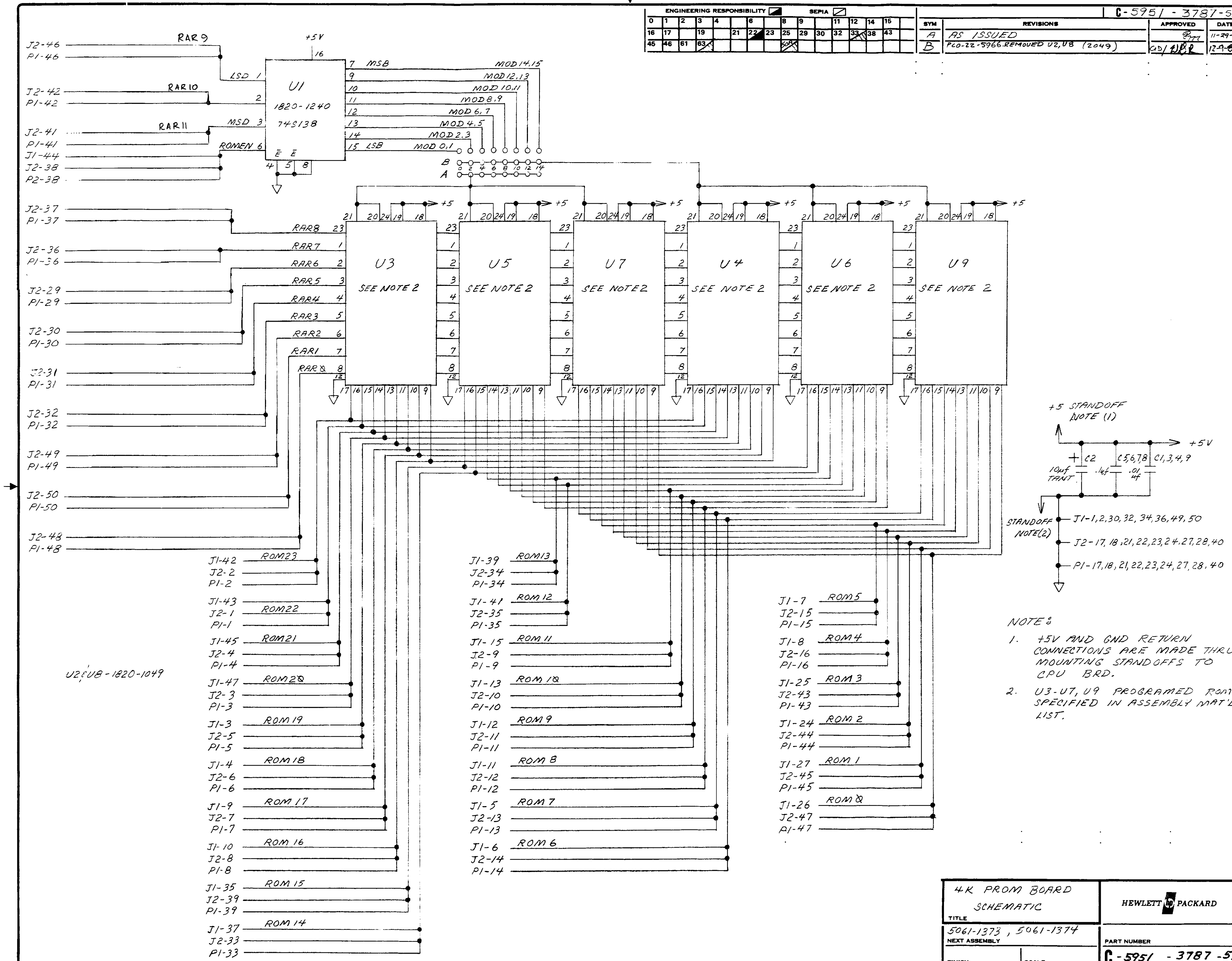
TITLE: FAST FORTRAN PROCESSOR I & II
12977-90007
SHEET 1 OF 1
ENGINEER | APPROVED | DATE
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION



12976B DMI (only) Assembly
5061-1374

12976B DMI (only) Assembly Parts List (5061-1374)

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
01	C5-8	CAP 0.1UF		0150-0121		U	4	
01	C1,3,4,9	CAP .01UF		0160-2055		U	4	
01	C2	CAP 10UF 10%		0180-0374		D	1	
01	P1	CONN PC2X25.100S		1251-3106		U	1	
01	U1	IC SN74S138N		1820-1240		U	1	
01	W1,2	WIRE JUMPERS		8159-0005		D	2	
		BOARD-ETCHED		5080-9758		W	1	
01	U7	PROM DMI 0-7		5090-0574		3	1	
01	U5	PROM DMI 8-15		5090-0575		3	1	
01	U3	PROM DMI 16-23		5090-0576		3	1	



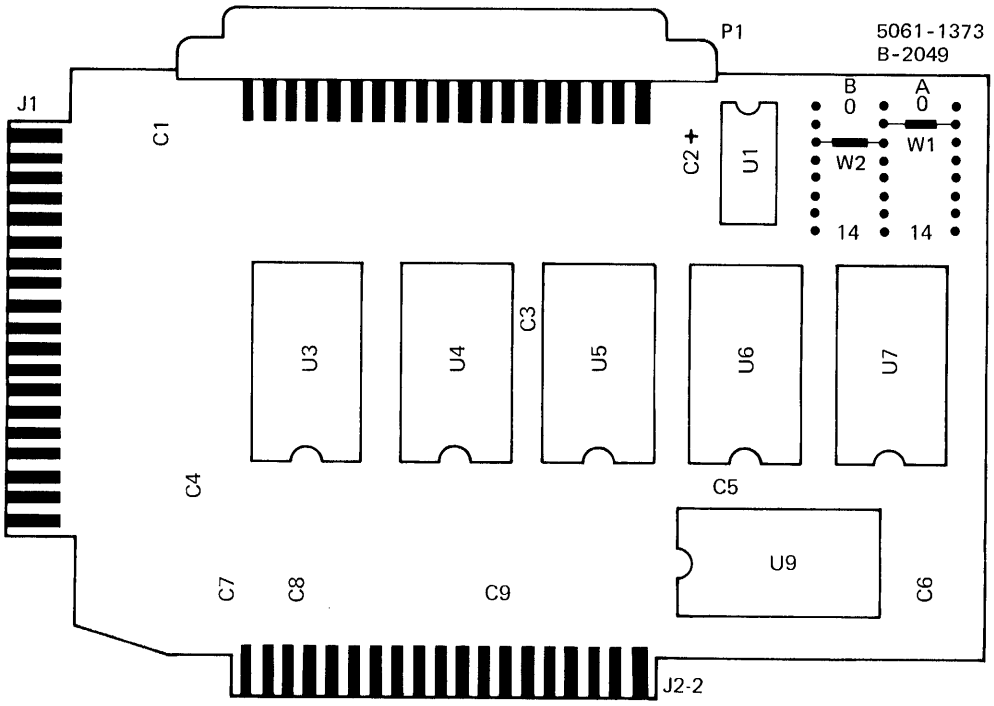
C-5951 - 3787-51
ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
A AS ISSUED 11-29-77
B PCO-22-5966 REMOVED U2,U8 (2049)
U1
1820-1240
74S138
+5V
RAR9
RAR10
RAR11
LSD
MSD
ROMEN
MSB
LSB
MOD 14,15
MOD 12,13
MOD 10,11
MOD 8,9
MOD 6,7
MOD 4,5
MOD 2,3
MOD 0,1
U3
U5
U7
U4
U6
U9
SEE NOTE 2
RAR8
RAR7
RAR6
RAR5
RAR4
RAR3
RAR2
RAR1
RAR0
J2-46
P1-46
J2-42
P1-42
J2-41
P1-41
J1-44
J2-38
P2-38
J2-37
P1-37
J2-36
P1-36
J2-29
P1-29
J2-30
P1-30
J2-31
P1-31
J2-32
P1-32
J2-49
P1-49
J2-50
P1-50
J2-48
P1-48
J1-42 J2-2 P1-2 ROM23
J1-43 J2-1 P1-1 ROM22
J1-45 J2-4 P1-4 ROM21
J1-47 J2-3 P1-3 ROM20
J1-3 J2-5 P1-5 ROM19
J1-4 J2-6 P1-6 ROM18
J1-9 J2-7 P1-7 ROM17
J1-10 J2-8 P1-8 ROM16
J1-35 J2-39 P1-39 ROM15
J1-37 J2-33 P1-33 ROM14
J1-39 J2-34 P1-34 ROM13
J1-41 J2-35 P1-35 ROM12
J1-15 J2-9 P1-9 ROM11
J1-13 J2-10 P1-10 ROM10
J1-12 J2-11 P1-11 ROM9
J1-11 J2-12 P1-12 ROM8
J1-5 J2-13 P1-13 ROM7
J1-6 J2-14 P1-14 ROM6
J1-7 J2-15 P1-15 ROM5
J1-8 J2-16 P1-16 ROM4
J1-25 J2-43 P1-43 ROM3
J1-24 J2-44 P1-44 ROM2
J1-27 J2-45 P1-45 ROM1
J1-26 J2-47 P1-47 ROM0
U2,U8 - 1820-1049
+5 STANDOFF NOTE (1)
+5V
C2
C5,6,7,8
C1,3,4,9
10uf TANT
.1uf
.01 uf
STANDOFF NOTE(2)
J1-1,2,30,32,34,36,49,50
J2-17,18,21,22,23,24,27,28,40
P1-17,18,21,22,23,24,27,28,40

NOTES:

1. +5V AND GND RETURN CONNECTIONS ARE MADE THRU MOUNTING STANDOFFS TO CPU BRD.
2. U3-U7, U9 PROGRAMED ROM SPECIFIED IN ASSEMBLY MAT'L LIST.

TITLE: 4K PROM BOARD SCHEMATIC	HEWLETT PACKARD
NEXT ASSEMBLY: 5061-1373, 5061-1374	PART NUMBER: C-5951 - 3787 -51
FINISH / SCALE	SHEET OF

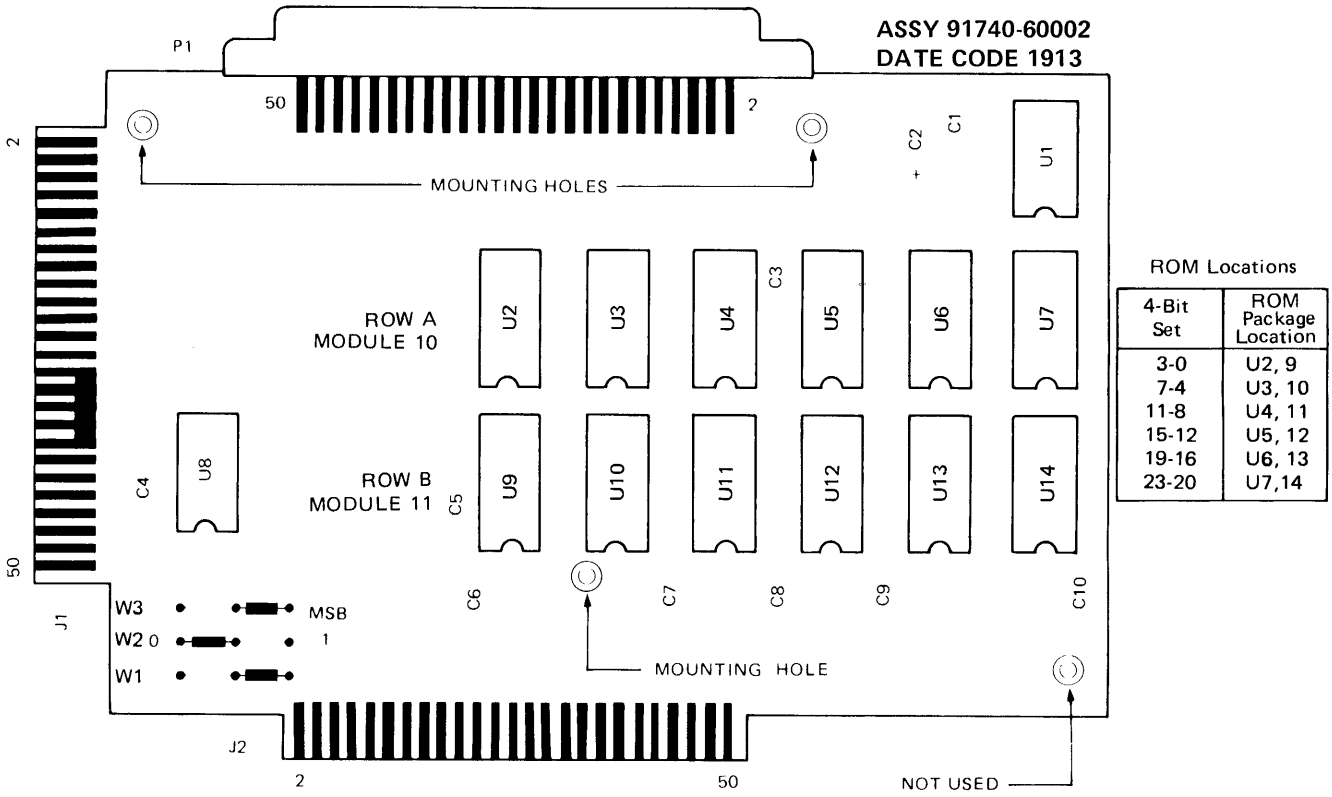
STOCK NO. 9280-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT



12977B DMI FPP Assembly
5061-1373

12977B DMI and FPP Assembly Parts List (5061-1373)

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
01	C5-8	CAP 0.1UF		0150-0121		U	4	
01	C1,3,4,9	CAP .01UF		0160-2055		U	4	
01	C2	CAP 10UF 10%		0180-0374		D	1	
01	P1	CONN PC2X25.100S		1251-3106		U	1	
01	U1	IC SN74S138N		1820-1240		U	1	
01	W1,2	WIRE JUMPERS		8159-0005		D	2	
		BOARD-ETCHED		5080-9758		W	1	
01	U7	PROM DMI 0-7		5090-0574		3	1	
01	U5	PROM DMI 8-15		5090-0575		3	1	
01	U3	PROM DMI 16-23		5090-0576		3	1	
01	U9	PROM FFP 0-7		5090-0577		3	1	
01	U6	PROM FFP 8-15		5090-0578		3	1	
01	U4	PROM FFP 16-23		5090-0579		3	1	



ROM Locations

4-Bit Set	ROM Package Location
3-0	U2, 9
7-4	U3, 10
11-8	U4, 11
15-12	U5, 12
19-16	U6, 13
23-20	U7,14

91740A DS/1000 M-Series ROM Assembly
91740-60002

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
01								
01								
03								
05								
		CAP 0.1UF		0150-0121			2	
01	C1,4,							
		CAP .01UF		0160-2055			7	
01	C3,5-10							
		CAP 10UF 10%		0180-0374			1	
01	C2							
		SOCKET 16 DIP LO		1200-0482			12	
01	U2-7,9-14							
		CONN PC2X25.100S		1251-3106			1	
01	J1							
		IC SN74H20N		1820-0373			1	
01	U1							
		IC SN74LS04N		1820-1199			1	
01	U8							
		WIRE JUMPERS		8159-0005			3	
01	W1-3							
		BOARD-ETCHED		5080-9740			1	
		1K ROM #1		91740-80052			1	
01	U2							
		1K ROM #2		91740-80053			1	
01	U3							
		1K ROM #3		91740-80054			1	
01	U4							
		1K ROM #4		91740-80055			1	
01	U5							
		1K ROM #5		91740-80056			1	
01	U6							
		1K ROM #6		91740-80057			1	
01	U7							
		1K ROM #7		91740-80058			1	
01	U9							
		1K ROM #8		91740-80059			1	
01	U10							

91740A DS/1000 M-Series ROM Assembly Parts List (91740-60002) Sht. 2 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER	UM
01	U11	1K ROM #9		91740-80060		3	1	
01	U12	1K ROM #10		91740-80061		3	1	
01	U13	1K ROM #11		91740-80062		3	1	
01	U14	1K ROM #12		91740-80063		3	1	