HP 12892A
MEMORY PROTECT

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

CONTENTS

THEORY OF OPERATION

1.0 INTRODUCTION

This Document provides the theory of operation for the 12892 Memory Protect/Parity option for the 2108 and 2112 computers. Discussion is conducted on the functional block, programming, and detailed operation levels. Block diagrams, generalized logic diagrams, and timing diagrams are used to show operation. Understanding of this document is essential when performing maintenance or trouble shooting on the 12892 option.

2.0 GENERAL DESCRIPTION

The following paragraphs describe the basic block diagram and define signals which interface with other computer system components.

2.1 Basic Block Diagram

Refer to Figure 1 for the following discussions.

2.1.1 Indirect Level Logic

This logic consists primarily of a counter which generates a signal to allow normal I/O interrupts in the CPU during indirect addressing routines, after three levels of indirection.

2.1.2 Parity Error Logic

This block of logic is used to enable and disable the 12892 option to interrupt on occurrence of a parity error. When a parity error occurs, bit 15 of the Violation Register is set high by this logic.

2.1.3 Memory and I/O Violation Detection Logic

This block consists of the logic necessary to determine if an I/O instruction has been fetched into the Instruction Register in the CPU, what bounds to allow on protected memory, and whether a reference to protected memory is imminent.

2.1.4 Interrupt and Control Logic

This block receives and decodes timing signals and I/O commands from the CPU and controls the other logical blocks. It also controls generation and handling of interrupts.

2.1.5 Violation Register

The Violation Register is loaded from the M-Bus with the address of the current instruction. When a 12892 option interrupt condition is imminent, it is disabled, saving this address. Occurrence of a parity error at any time will load it with the offending address.

2.2 Interface Signal Definitions

This section describes the main signals which interface the 12892 option board to other elements of the computer. Standard busses and I/O signals are not included. The reader is referred to the signal definitions and cross-references for the 2108A and 2112A for signals not included here. All signals are TTL compatible, ground true unless otherwise specified.

2.2.1 Input Signals

$\overline{\text{FTCH}}$ "Fetch". From the microinstruction Special field on the CPU. Indicates that an instruction has been fetched and that its address is present on the M-Bus. Causes resetting of violation detect logic and indirect counter, and loads the Violation Register.

$\overline{\text{HLTPE}}$ "Halt on Parity Error". From the parity option switch on the CPU. Indicates the CPU is set to halt on parity errors, and disables parity interrupts. Remains in one state until switch is manually changed.

$\overline{\text{INCI}}$ "Increment indirect counter". From the microinstruction Special field on the CPU. Signals another level of indirect to the indirect level logic. Occurs during one unfrozen P5 period.

$\overline{\text{IOGSP}}$ "I/O group special". From the microinstruction Special field on the CPU. Indicates that the I/O group signals will be enabled on the next T2 period. Lasts one T-period plus the number of T-periods to the nearest T2 (freeze time): 1 to 5 T-periods in length.

$\overline{\text{IRSTF}}$ "Instruction Register Store, freezable". From micro-instruction store field on CPU. Indicates that data

is being loaded into the Instruction Register on the CPU, and is currently present on the S-BUS. Used to set up error-detection logic for the current instruction. Lasts one T-period, broken up by freeze time.

$\overline{\text{MEV}}$ "Memory Expansion Violation". Generated by Memory Management Unit (MMU). Indicates violation of protected memory in that unit. Occurs during P5 of imminent violation in the MEU.

$\overline{\text{MPCK}}$ "Memory Protect Check". From microinstruction Special field on the CPU. Causes check for possible protected memory bounds violation. Occurs for one T period plus freeze time, if any.

$\overline{\text{PE}}$ "Parity Error". From the Memory controller. Indicates occurrence of parity error during memory reference. Consists of a pulse generated when data is valid during a Read operation.

$\overline{\text{DMAFRZ}}$ "DMA freeze condition". From the DMA board. Indicates that DMA is using the S-BUS and the CPU is frozen. Prevents error-checking the S-Bus until the CPU has control of it again.

2.2.2 Output Signals

$\overline{\text{CTL5}}$ "Control 5". Signal to Memory Management to show state of control flip-flop.

$\overline{\text{FLG5}}$ "Flag 5". Signal to CPU indicating state of Flag flip-flop. Used to disable the I/O priority chain and to generate a Special interrupt request.

$\overline{\text{MPCND}}$ "Memory Protect Conditional". Signal to Memory Management Unit. Indicates a memory protect check is in progress so the MEU can check for violations.

$\overline{\text{MPINTON}}$ "Memory Protect interrupt on". Signal to CPU. Indicates more than three levels of indirection have occurred, and enables normal I/O interrups to occur during further indirect levels.

$\overline{\text{MPV}}$ "Memory Protect Violation". Generated when the control is set and violations other than parity errors occur. Prevents CPU or Memory from altering protected memory or registers and disables I/O signals.

$\overline{\text{RESPE}}$ "Reset parity error". Signal to CPU which clears the parity error light on servicing of a 12892 option interrupt request.

SKF "Skip flag". Positive true. True when the skip condition is met for a SFS5 or SFC5 instruction. Responds to state of the Memory Expansion Flag flip flop (whether violation occurred in the Memory Management Unit).

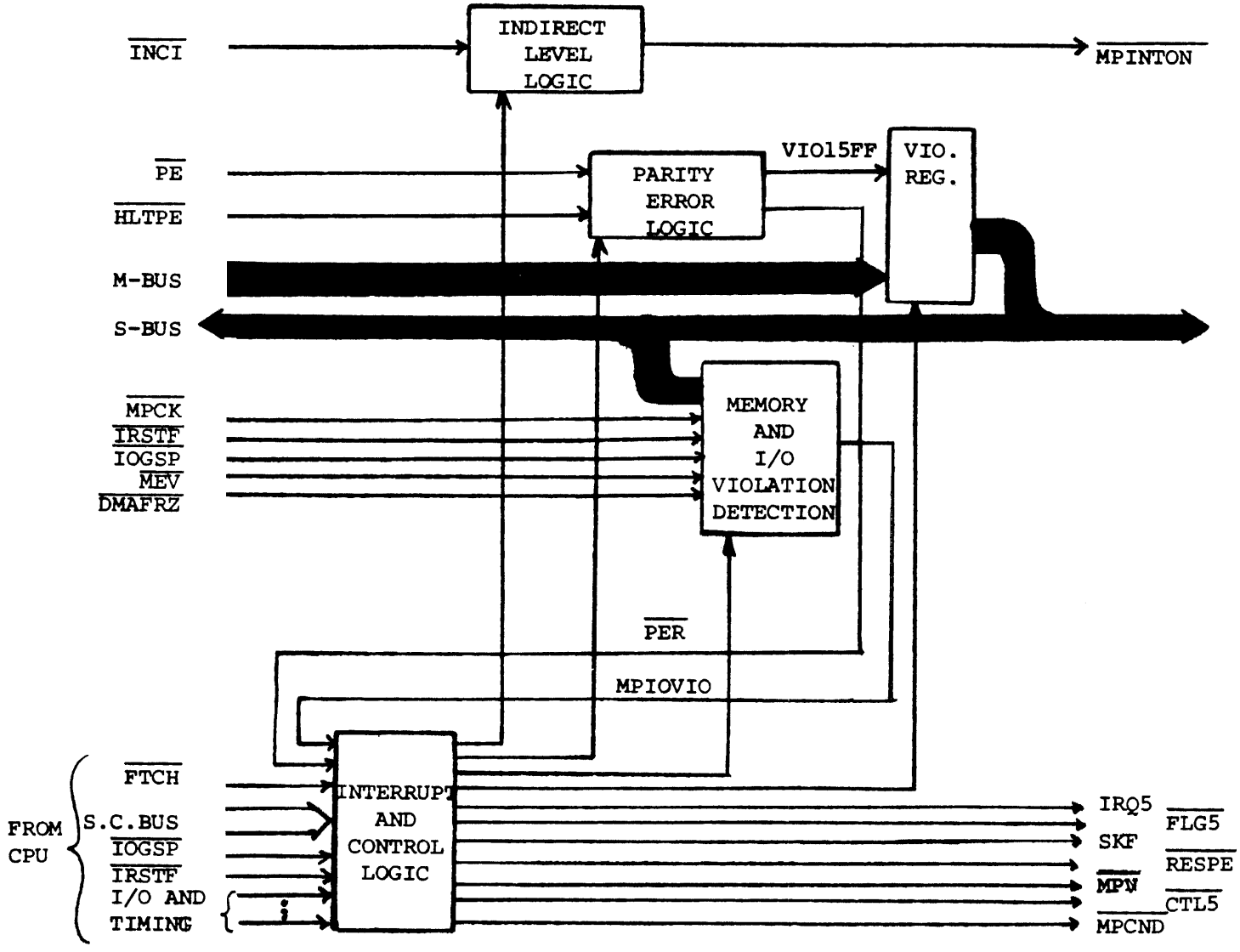


Figure 1

12892 Option Block Diagram

3.0 PROGRAMMING

The 12892 option interfaces with the CPU as a standard I/O device, except with regard to interrupt generation and handling. It is accessed as select code 5 in the I/O system. It performs the function described below.

3.1 Memory Protect Feature

This feature prevents certain instructions from altering memory below a programmed fence, and from jumping into protected memory. The check for possible violations is initiated by a microcode instruction field, so operation of this feature is very instruction-dependent. The programmer should consult the microprogramming manual and the specifications for the extra firmware packages installed in his computer to determine the extent of memory protection for his available instructions. The following discussions apply to Base Set and Extended Arithmetic Unit instructions.

3.1.1 Feature Programming

Memory Protection is enabled by a STC 5 instruction. It is disabled at power-up or by pressing the Preset button in the HALT mode, or by executing a trap cell instruction during an interrupt which is a Halt or a non-I/O instruction.

3.1.2 Feature Operation

If Memory Protection is enabled, and the interrupt system is enabled by a previous STFØ command, then an interrupt to trap cell 5 will be generated if any of the following instructions attempt to access protected memory:

a) ISZ
b) JSB
c) STA
d) STB
e) DST
f) JMP
g) Any other instruction, not in the base set, which provides memory protection.

NOTE

The interrupt system should always be enabled before enabling Memory Protection. If the interrupt system is off and Memory Protect is on and a violation occurs the CPU will permanently freeze and can recover only by going to reset.

3.1.3 Protection Boundaries

The upper address bound of protected memory is loaded from the A or B register into the Fence Register in the 12892 option by an OTA5/OTB5 command. Memory addresses below this Fence are protected.

The lower address bound depends on the instruction being executed. For any instruction with a JMP format in the Instruction Register at the time of a Memory Protect Check in microcode, the lower bound of protection is address Ø (the A-register). For all other instructions, the lower bound is address 2. Addresses equal to or above the lower bound are protected.

3.1.4 Indirect Addressing

Indirect addressing is permitted through protected memory for protected instructions, but the final effective address must be in unprotected memory.

3.1.5 Obtaining Violation Address

After a Memory Protect interrupt has occurred, the address of the violating Instruction may be obtained by a LIA5/LIB5 command. If a parity error occurs after the Memory Protect violation, the address loaded by LIA5/LIB5 will be that of the parity error. BIT 15 is low if the address was related to Memory Protection.

3.1.6 Memory Expansion Unit Memory Protection

The reader is referred to the Memory Expansion Unit (MEU) specifications for programming Memory Protect for that option. The 12892 option generates interrupts when notified by the MEU that a violation has occurred.

3.2 I/O Violation Feature

This feature provides protection of the system from illegal I/O instructions by causing an interrupt when an illegal I/O instruction is attempted.

3.2.1 Feature Programming

I/O Protection is enabled and disabled simultaneous with Memory Protection.

3.2.2 Feature Operation

The definition of an illegal I/O instruction is controlled by jumper W1. Instructions referencing select code 1 (front panel display register or Overflow flip-flop) are always legal. The jumper positions have the following meanings:

W1-A: All other I/O instructions are illegal.

W1-B: Only Halt instructions are illegal.

If this feature is enabled, and the interrupt system is enabled by a previous STFO, an interrupt to location 5 is generated if an illegal I/O instruction is attempted. Whether or not the interrupt system is enabled, the illegal instruction is treated as a NOP.

3.2.3 Obtaining Violating Address

After an interrupt occurs, the address of the violating instruction may be obtained by a LIA5/LIB5 instruction. Bit 15 will be low. Parity errors occurring subsequent to a violating I/O instruction will cause the address of the parity error plus bit 15 high to be loaded into the Violation Register.

3.3 Indirect Level Logic

Each time a level of indirect addressing is executed in the base set routines, the Indirect Counter on the 12892 option is incremented, until the third level. Then any pending interrupts are allowed to cause termination of indirect addressing, resetting of the P-counter to the start of the current instruction, and servicing of the interrupt before attempting the indirect-addressing instruction again. This prevents indirect addressing from holding off critical interrupt requests.

3.4 Parity Error Interrupt Feature

If the HALT/INTERRUPT feature is switch-selected on the CPU, the Parity Error Logic is enabled on the 12892 option, and the priority chain is high to the 12892 option board, then a parity error will cause an interrupt to trap cell 5. This will occur whether or not the interrupt system has been enabled by a previous STFØ command.

3.4.1 Feature Programming

This feature is enabled by the following:

a) STF5 instruction

b) Power turn-on

c) Pressing the PRESET button in the Halt mode.

The following occurrences disable the Parity Interrupt feature:

a) A memory parity error occurs during a Read operation.

b) A CLF5 command is performed.

c) The Halt-on-Parity option is switch-selected on the CPU.

3.4.2 Obtaining the Error Address

After occurrence of a parity error interrupt, the address on the M-Bus at the time of the parity error may be obtained by a LIA5/LIB5 instruction. BIT 15 will be a one.

4.0 DETAILED OPERATION

This section contains a detailed theory of operation for the 12892 Memory Protect Option. The reader should refer to the detailed schematic for this option, as well as the figures and diagrams referred to in this discussion. IC pack numbers are given in parentheses.

4.1 Indirect Level Logic

This consists of the two J-K flip-flops IND1FF and IND2FF (U92) and their associated logic. Refer to Figures 2 and 3. The flip-flops form a simple counter, clocked by $\overline{\text{INCI}}$, which occurs at P5 (freezable) of a microinstruction which specifies INCI in its Special field. This occurs in the indirect addressing routine. The counter increments are shown in Figure 2, at each occurrence of $\overline{\text{INCI}}$. $\overline{\text{MPINTON}}$ will go low until the counter is reset by $\overline{\text{FTCH}}$ at the next instruction fetch, or by IAK. This insures that each instruction, including interrupt trap cells, is allowed no more than 3 levels of indirect before checking for interrupts. MPINTON directly sets the Interrupt Enable flip-flop (INTENFF) on the CPU, allowing normal interrupts to be sensed during indirect addressing.

4.2 Parity Error Logic

This logic consists of the Parity Enable flip-flop (PARENFF), Violation Register 15 flip-flop (VIO15FF), and their associated gates. Refer to Figure 4.

4.2.1 Parity Enable Flip-Flop

A STF5 or POPIO will cause this flip-flop (U96A) to be reset on the next P5, setting $\overline{\text{PARENFF}}$ high. If $\overline{\text{HLTPE}}$ is low (HALT on Parity option), then $\overline{\text{PARENFF}}$ will be set low on the next P5. $\overline{\text{PARENFF}}$ will oscillate if STF5 or POPIO occur simultaneously with $\overline{\text{HLTPE}}$. But $\overline{\text{HLTPE}}$ will set $\overline{\text{PARENFF}}$ low on the next P5. The parity interrupt feature is enabled when $\overline{\text{PARENFF}}$ is high.

4.2.2 Violation Register 15 Flip-Flop

This flip-flop (U86A) is set low at the same time that $\overline{\text{PARENFF}}$ is set high, and is set high immediately on occurrence of a parity error if the priority chain is intact to the 12892 option (PRH5 is high).

4.2.3 Parity Error Interrupts

The $\overline{\text{PER}}$ signal initiates an interrupt if a parity error occurs, PRH5 is high, and $\overline{\text{PARENFF}}$ is high. $\overline{\text{PER}}$ will perform the following actions:

a) Direct-set $\overline{\text{PARENFF}}$ low, disabling future parity interrupts.

b) Set VIO15FF high, indicating occurrence of a parity error.

c) Set the 12892 option flag buffer in the interrupt logic.

d) Clock the contents of the M-Bus into the Violation Register.

e) Direct-reset EVRFF←Ø to prevent further clocking of the VIOLATION REGISTER.

$\overline{\text{FLG5}}$ and IRQ5 will be generated, and the interrupt will be serviced regardless of the state of the interrupt system (enabled by STFØ). See Section 4.4 for discussion of interrupts.

4.3 Memory Protect and I/O Violation Detect Logic

This logic consists of buffers, a comparator, flip-flops, the Fence Register, and associated logic necessary to decode the various violation conditions. Refer to Figure 6.

4.3.1 Fence Register and Comparator

An OTA5/OTB5 instruction will cause generation of IOO and SEL5 (select code 5) signals, which will load the buffered contents of the S-BUS into the Fence Register (U14, U56). The Fence Register and buffered S-Bus are inputs to the comparator logic (U34, U12, U54, U46, U44) which constantly performs the subtraction "S-BUS MINUS FENCE". ADR CARRY is high if the Fence is greater than the S-Bus. Thus, if an address is present on the S-Bus, ADR CARRY indicates if it is below the upper bound of protected memory. If an indirect address (bit 15 high) is on the S-Bus, it will be compared as being above the fence, and hence will not cause ADR CARRY to be high.

4.3.2 Protected Memory Lower Bounds

The lower bound of protected memory is determined by the presence or absence of a JMP instruction in the IR on the CPU. U11A and U65C cause setting high of the JUMP flip-flop (U96). ($\overline{\text{JMPFF}}$ goes low) if a JMP instruction is present on the S-Bus when a STORE into the IR is performed (IRSTF). $\overline{\text{JMPFF}}$ and U22, 42 and U52

decode violation of the lower bounds of protected memory, the output of U52 is high if the instruction is a JMP, or if the S-BUS is not Ø or 1. If either of these conditions is true, then if ADRCARRY is high, a violation condition is present.

4.3.3 Memory Protect Violation Detection

The 4-input NAND gate U11B decodes memory violation conditions. One microinstruction before a STORE into memory is initiated, the memory address is placed into the S-Bus, and MPCK is specified in the Special field. MPCK is then sent to the 12892 option. The address is checked for violation by the logic of sections 4.3.1 and 4.3.2 above. If there is a violation, then during the next P5, $\overline{\text{MEMVIO}}$ (U31) is low.

$$\overline{\text{MEMVIO}} = \text{BMPCK} \cdot \text{P5NF} \cdot \text{ADRCARRY} \cdot (\overline{\text{ADRØ} + 1} + \overline{\text{JMPFF}})$$

4.3.4 Memory Management Violation Logic

The Memory Management package has its own protection logic. It is sent information from the 12892 option to allow it to perform this function. $\overline{\text{CTL5}}$ notifies Memory Management of the state of the memory protect feature. $\overline{\text{MPCND}} = \text{BMPCK} \cdot \overline{(\text{ADRØ} + 1 + \overline{\text{JMPFF}})}$, which is low if a STORE address is not below the lower bound of protected memory. $\overline{\text{MEV}}$ is sent by Memory Management at P5 if a violation occurs there. The MEFLAG flip-flop (MEFLGFF) is set high on occurrence of $\overline{\text{MEV}}$ with setting of the Flag Buffer. It is reset whenever CNTRLFF is SET, and is tested with SFS5 and SFC5 commands (U103).

4.3.5 I/O Violation Logic

If at occurrence of $\overline{\text{IRSTF}}$ the S-Bus contains a HALT instruction, as decoded by gate U21A, then at the following P5, the Halt instruction flip-flop will be set (HLTIRFF will go high). It will be reset on the next $\overline{\text{IRSTF}}$. Also during an $\overline{\text{IRSTF}}$, the low-order six bits of the S-Bus are decoded by U32B, U32C, and U65B. If they decode to a value of $Ø1_8$, then I/O Select Code 1 flip-flop is set on P5 ($\overline{\text{IOSEL1FF}}$ goes low).

$\overline{\text{IOGSP}}$ is low at the start of execution of I/O instructions, and comes from the Special field of microcode. If $\overline{\text{HLTIRFF}}$ or IOSEL1FF

is low during IOGSP, then an illegal I/O instruction is being performed (HALT, or Select CODE ≠ 1). U76C and U52D decode I/O violations ($\overline{\text{IOVIO}}$). $\overline{\text{IOVIO}}$ is low during P5 of IOGSP for violations.

U84C and U61C detect attempted execution of a HALT. $\overline{\text{HLTVIO}}$ is low during P5 of $\overline{\text{IOGSP}}$ if HLTIRFF is high.

4.3.6 Violation Detection

U73A and W1 send a high pulse to the Interrupt Logic during P5 if any violating condition is met. Jumper W1 selects whether any I/O violation, or just HALTS are considered illegal I/O instructions, so the output of U73 is high during $\overline{\text{MEMVIO}}$ or $\overline{\text{MEV}}$ or either $\overline{\text{IOVIO}}$ or $\overline{\text{HLTVIO}}$.

4.4 I/O Interrupt and Control Logic

This part of the 12892 option consists of I/O signal buffers, I/O command decoding logic, and interrupt generation and response logic.

4.4.1 I/O Priority

The 12892 option occupies select code 5 in the I/O system. Hence, it has higher priority than any device except power fail. Priority chaining is not done on the 12892 board, but on the CPU in order to maintain it in the absence of the option.

On the CPU (refer to Figure 5), IEN5 is high to the 12892 option if the interrupt system is enabled. If power fail control is set ($\overline{\text{CONT4FF}}$ low), PRH5 is high and the priority chain is enabled. When the FLAG is set on the 12892 board, $\overline{\text{FLG5}}$ is low, which goes to the CPU to disable the priority chain to higher select code devices.

4.4.2 Parity Error Interrupt Generation

Two methods of interrupt requesting are performed. Parity errors generate different requests than other violations. Refer to Figure 7. Parity errors cause setting of the Flag Buffer flip-flop in U95 whether or not the interrupt system is enabled. Hence, parity errors will result in an I/O interrupt whether or not the system is enabled by STFØ.

When $\overline{PE}$ occurs, and $\overline{PARENFF}$ and PRH5 are high, then $\overline{PER}$ goes low, setting FLGBFF. At the next T2 period, the FLAG (FLAGFF) is set, and $\overline{FLG5}$ goes low. $\overline{FLG5}$ generates a special interrupt request in the CPU and disables the priority to other devices. So at conclusion of the current instruction, the interrupt will be serviced, whether IRQ has been generated or not. At the next T5 (SIR), IRQFF goes high. IRQFF goes high each T5 and low each T2 until the interrupt is acknowledged. NOTE that $\overline{FLG5}$ goes low to request a special interrupt early (T2) to provide parity error interrupts preferential servicing. IRQ5 need not be high until T6, when it is needed to load the Central Interrupt Register on the CPU.

Note that if a CLF5 instruction begins the fetch phase before $\overline{FLG5}$ goes low, then CLF5 will reset the Flag and Flag Buffer, and prevent the interrupt request, unless CNTRLFF is high, which would result in an I/O violation.

4.4.3 Memory Protect and I/O Interrupt Generation

Refer to Figures 7, 8, 10 and 11 for the following discussion.

Most of the time, Memory Protect and I/O violations interrupt before the next machine language instruction has entered the fetch cycle. However, if MPCK occurs at T2 or T3, and the next microinstruction specifies a return to the fetch routine, then there is not enough time to generate IRQ5 and $\overline{FLG5}$ by the time the CPU is ready to read the CIR. To overcome this problem,

if the CPU reads Ø from the CIR, then it will go back and read it again, allowing time for IRQ5 to be asserted. If any other I/O device sends its IRQ before MPIOVIO can set $\overline{\text{FLG5}}$, then servicing of the Memory Protect violation interrupt will be postponed until the first opportunity it has to interrupt again. Unless the I/O interrupt routine performs a CLF5 command, there is no danger in postponing the Memory Protect interrupt servicing in this manner. The violating program will not be allowed to perform illegal machine operations in any event.

If the Control flip-flop CNTRLFF, is set, then when MPIOVIO goes high, the output of gate U84B direct-sets the MPV flip-flop. (Refer to Figure 7.) $\overline{\text{MPV}}$ goes to the CPU and the Memory Controller to perform the following functions:

a. Inhibit alteration of the Program Counter and S-register on the CPU.
b. Inhibit storing into the memory address specified in the M-register of the CPU. DMA may store into protected memory.
c. Clear the I/O Group Enable flip-flop on the CPU, to inhibit I/O signals from the CPU.
d. If IEN5 and PRH5 are asserted, generate a Special Interrupt Request (refer to Figure 8). This allows MPV interrupts to occur before the next instruction is fetched.

MPV is returned to high state by either of two occurrences:

a. IAK: An interrupt is being serviced, so protection from illegal operations is not required any longer.
b. FETCH: This would not occur with $\overline{\text{MPV}}$ low, unless the interrupt system was not enabled, or the computer was in the Halt mode. In either case, the next instruction is to be allowed to execute freely until an illegal operation is attempted.

If MPIOVIO, CNTRLFF, IEN5, and PRH5 are all high, then the Flag Buffer, FLGBFF, is set high. FLAGFF is set on the next T2, which sends $\overline{\text{FLG5}}$ to the CPU to disable the priority chain. As long as FLAGFF is set, IRQ5 will be high only during T5 and T6 until the interrupt is granted. When IAK occurs and IRQ5 is asserted, the FLAGFF and FLAGBFF are cleared, and IRQ5 will no longer occur.

4.4.4 Interrupt Handling

When the CPU services a Memory Protect, Parity, or I/O interrupt, IAK is high during the last half of T6. IAK performs the following functions (refer to Figures 7, 9).

a. In conjunction with IRQ5, direct-clears the Flag and Flag Buffer flip-flops
b. In conjunction with IRQ5, sends a low level on $\overline{\text{RESPE}}$ to the CPU to reset the Parity Error LED on the front panel.
c. Resets $\overline{\text{MPV}}$ high at the end of P5
d. Unconditionally sets the Interrupt flip-flop (INT1FF) on P5, indicating occurrence of any interrupt (Figure 9).
e. Clears the Indirect Counter.

The Interrupt flip-flop (INT1FF, U94), Interrupt 2 flip-flop (INT2FF, U94) and the control flip-flop (CNTRLFF) and their associated logic (Figure 9) determine enabling and disabling of the Memory Protect features. Recall that Memory and I/O Protection are to be disabled on occurrence of any interrupt, unless the interrupt trap cell contains an I/O instruction other than HALT.

Refer to Figures 9, 12, 13 for the following discussion. Unconditionally, INT1FF is set high at the trailing edge of P5 during IAK. If CNTRLFF is already low, then at the following T2, INT1FF is set low again, preventing CNTRLFF from being set high, except by a succeeding STC5 instruction.

If CNTRLFF is high when INT1FF is high, then at the next T5, CNTRLFF is set low, disabling the Memory Protect and I/O Protect features. If $\overline{\text{IOGSP}}$ does not go low by T2 following CNTRLFF going low, then there was no I/O instruction in the trap cell, and INT1FF is set low, and CNTRLFF is left cleared.

However, if there is an I/O instruction in the trap cell, then $\overline{\text{IOGSP}}$ will be low at T2, then INT1FF will be set high at the end of T2 and INT1FF will go low if the instruction is not a HALT. One T-period later, CNTRLFF will be set high. The second Interrupt flip-flop, INT2FF, introduces a delay prior to setting of CNTRLFF to allow unprotected execution of the trap cell instruction.

If IRQ5 is not generated by the time the CPU sends IAK and no other I/O device is interrupting, then the CIR becomes Ø. Interrupt microcode tests for this, and attempts to load the CIR again if it is Ø. By this time, IRQ5 will be present, and the interrupt will be serviced. If INT1FF is high upon receiving IAK, it is due to this condition. So this condition direct-sets CNTRLFF again. This recreates the initial interrupt conditions described in the first two paragraphs above. The sequence will proceed normally from here (Figures 12, 13, case 2).

4.5 Violation Register

The Violation Register (Figure 14) monitors the M-Bus (15 bits). When a parity error occurs, $\overline{\text{PER}}$ clocks the M-Bus into the Violation Register, which will then contain the address of the parity error.

An STC5 instruction causes setting of the Enable Violation Register flip-flop (EVRFF), U72. As long as EVRFF is high, the Violation Register is clocked during $\overline{\text{FTCH}}$, while the address of the current instruction is on the M-Bus. When any violation causes setting of FLGBFF, EVRFF is set low, locking the offending address into the Violation Register (unless clocked by a subsequent parity error).

EVRFF may not be re-enabled until after the current violation interrupt has been serviced. ($\overline{\text{FLG5}}$ must be high before STC5 will re-enable the EVRFF.)

The Violation Register is buffered onto the S-Bus during an LI*5 or MI*5 instruction. VIOl5FF is used as the high order bit to indicate occurrence of a parity error.

4.6 Power-On or Preset

If power is being turned on, or the Preset button is pressed in the HALT mode, the following actions occur:

a. $\overline{\text{IOSEL1FF}}$ is set high (reset state)
b. $\overline{\text{JMPFF}}$ is set high (reset state)
c. $\overline{\text{PARENFF}}$ is set high, enabling parity error logic
d. VIOl5FF is set low (reset state)
e. EVRFF is set high (allow clocking of Violation Register)
f. INTlFF is set low (reset state)
g. INT2FF is set low (reset state)

i. FLGBFF, FLAGFF, IRQFF, CNTRLFF are set low (Memory Protect and I/O protect shut off)
j. MEFLGFF is set low (reset state)
k. HLTIRFF is set low (reset state)
l. MPV flip-flop is set low (reset state, $\overline{\text{MPV}}$ high).

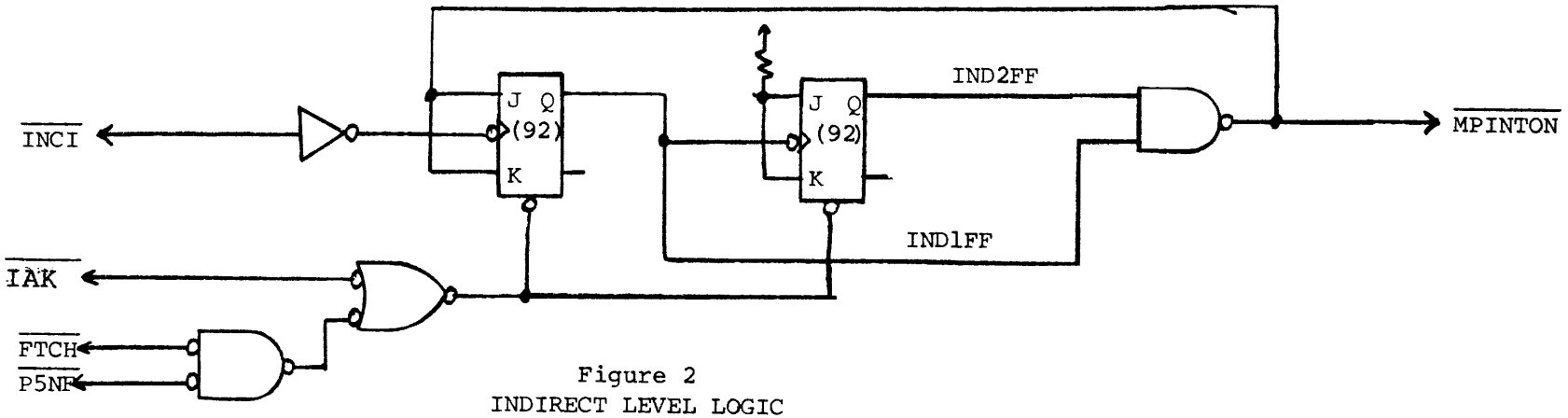


Figure 2
INDIRECT LEVEL LOGIC

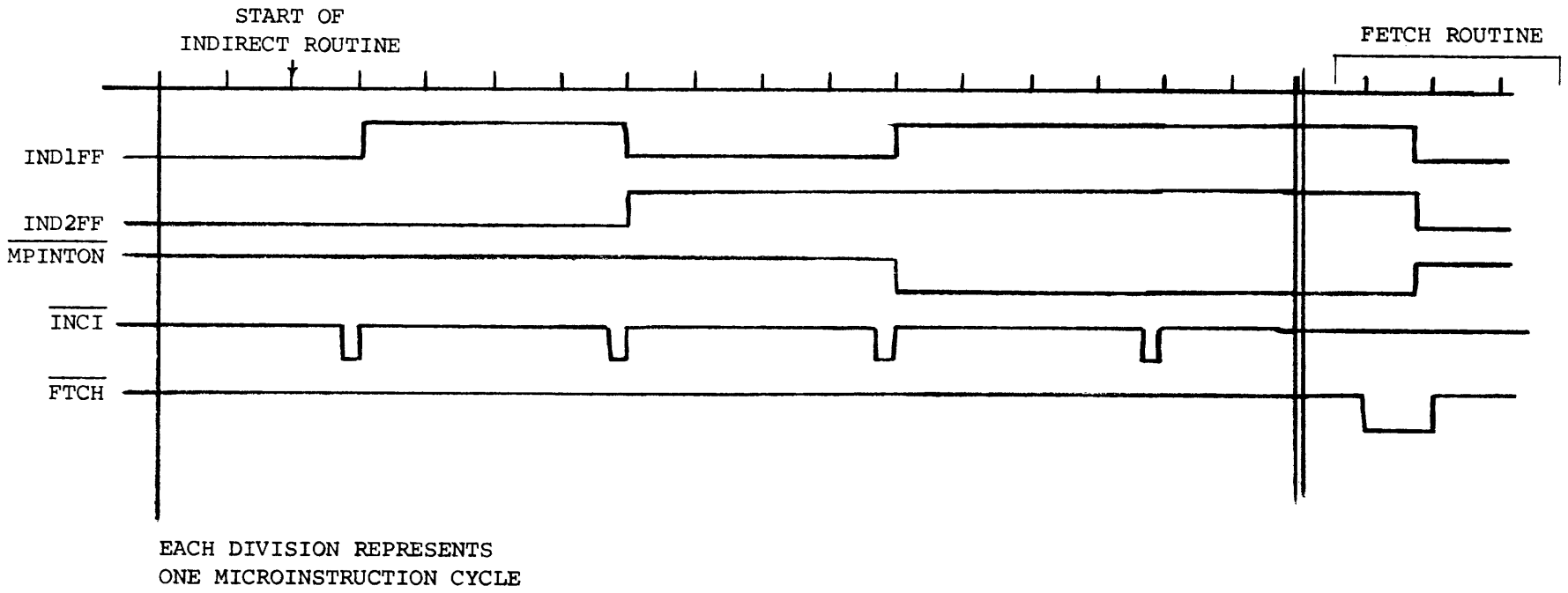


Figure 3
INDIRECT LOGIC TIMING
DURING MULTIPLE (4 LEVELS) INDIRECTS

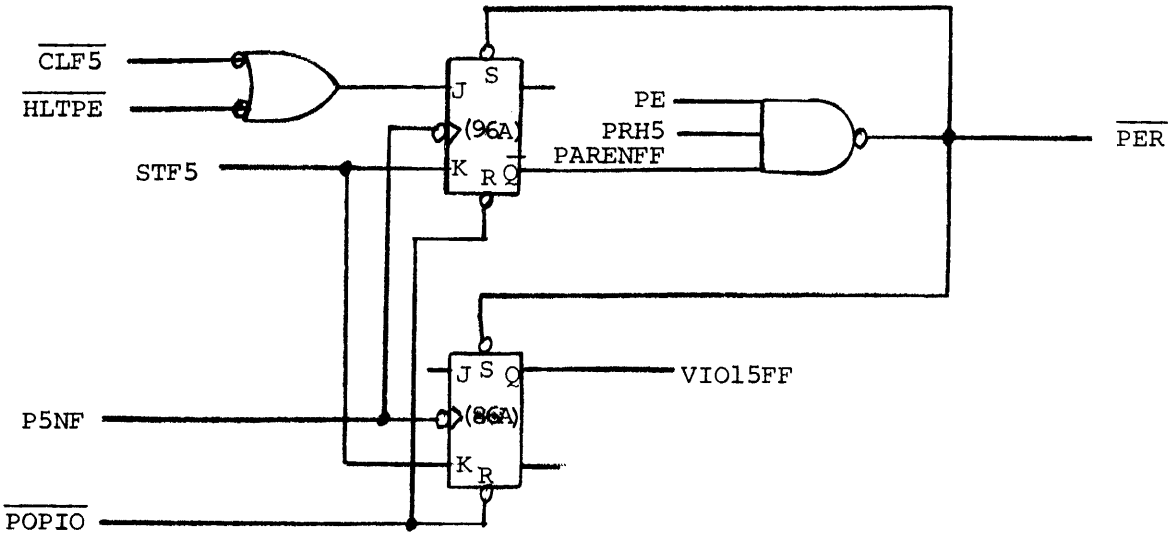


Figure 4
PARITY ERROR LOGIC

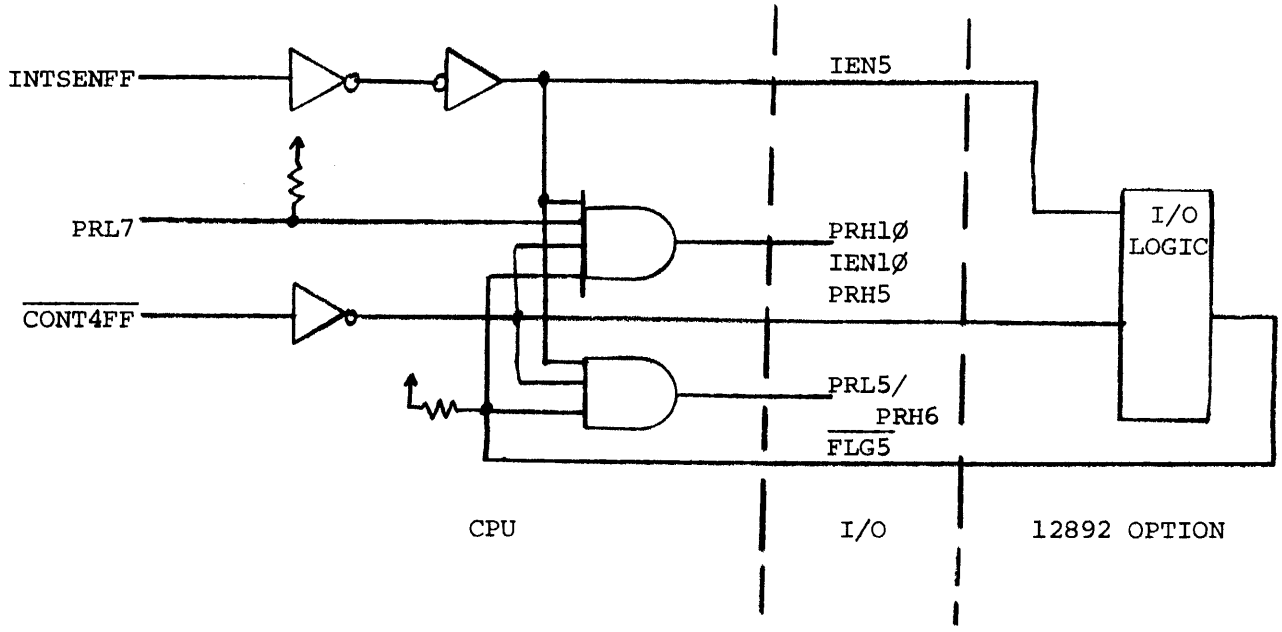


Figure 5
PRIORITY CHAIN LOGIC
INVOLVING THE 12892 OPTION

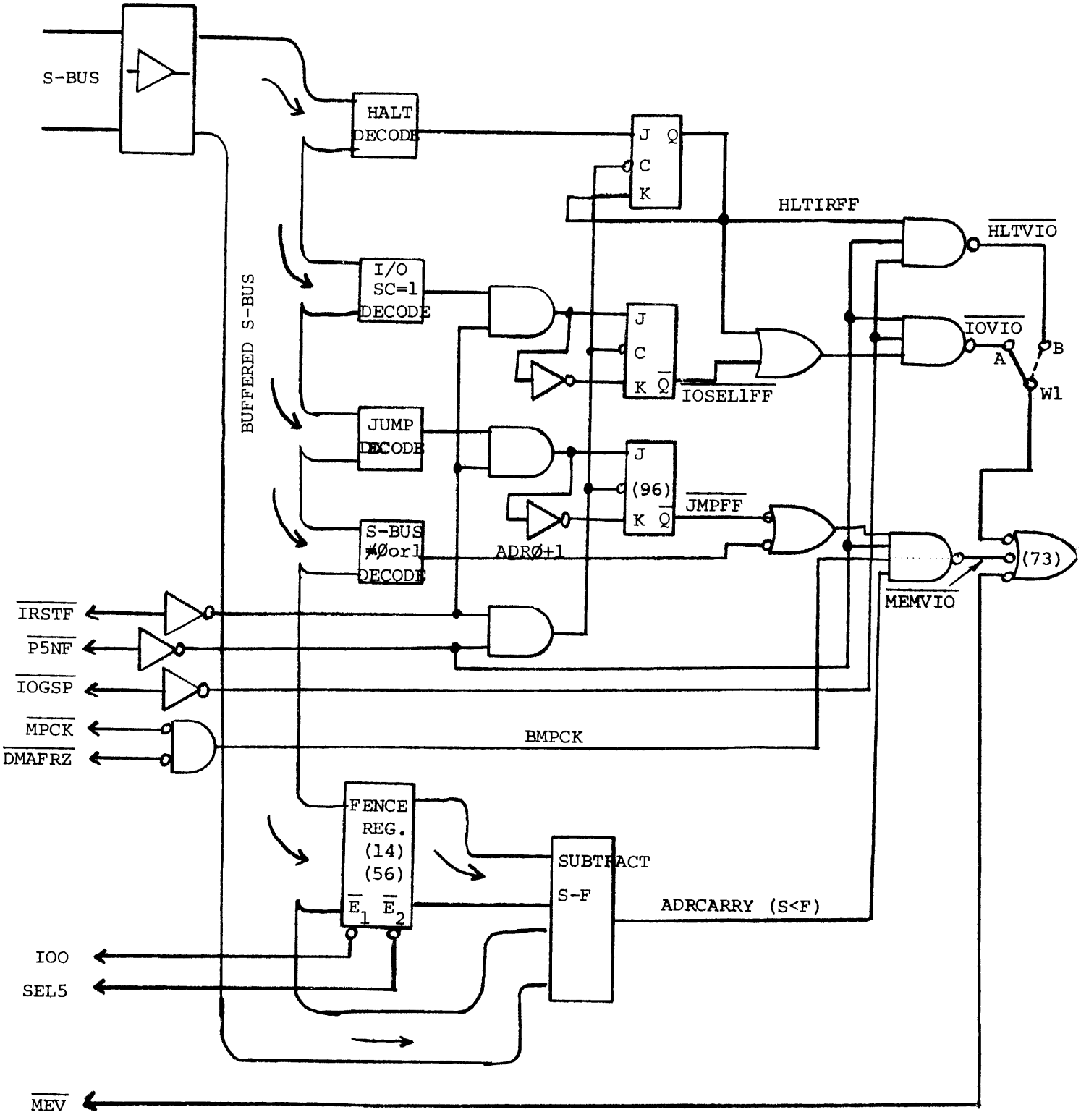


Figure 6
VIOLATION DETECT LOGIC

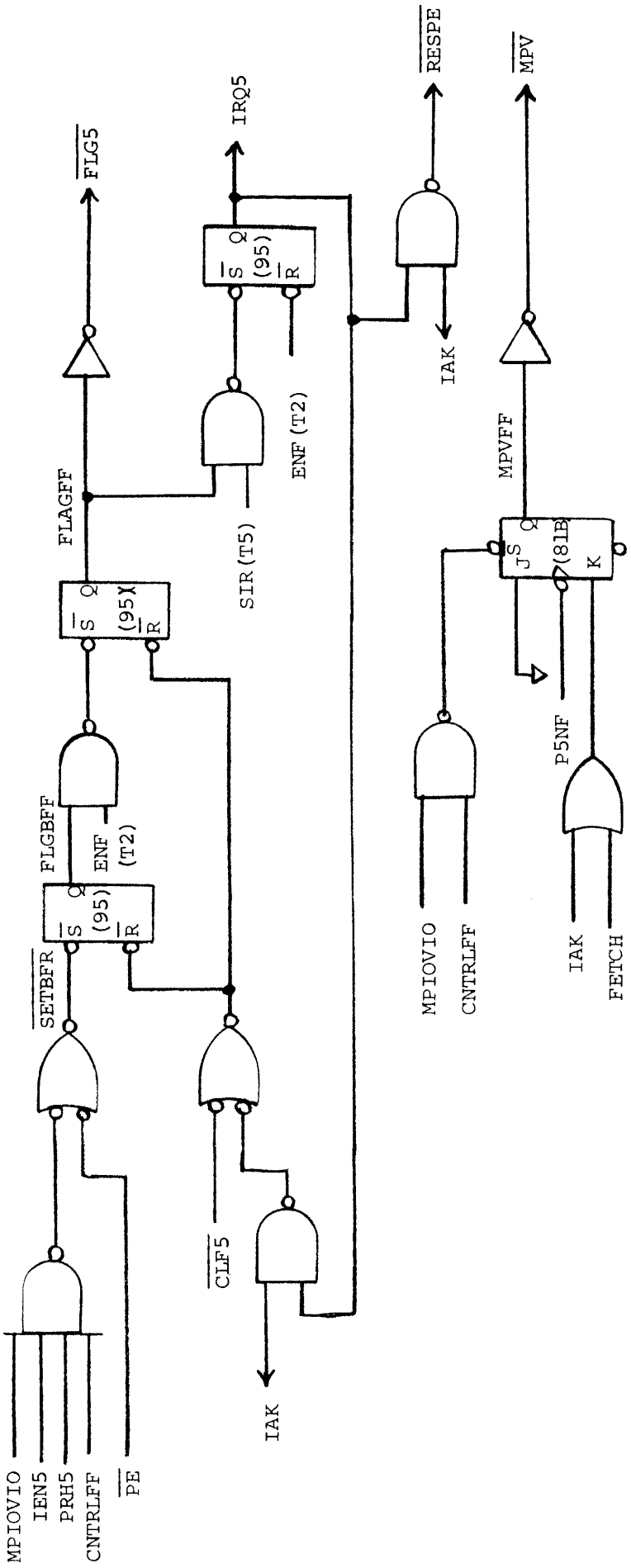


Figure 7
INTERRUPT AND MPV LOGIC

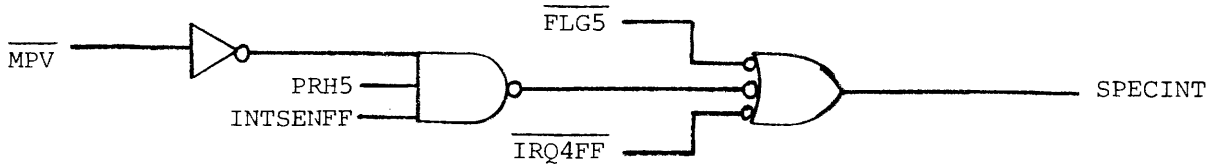


Figure 8
SPECIAL INTERRUPT LOGIC ON THE CPU

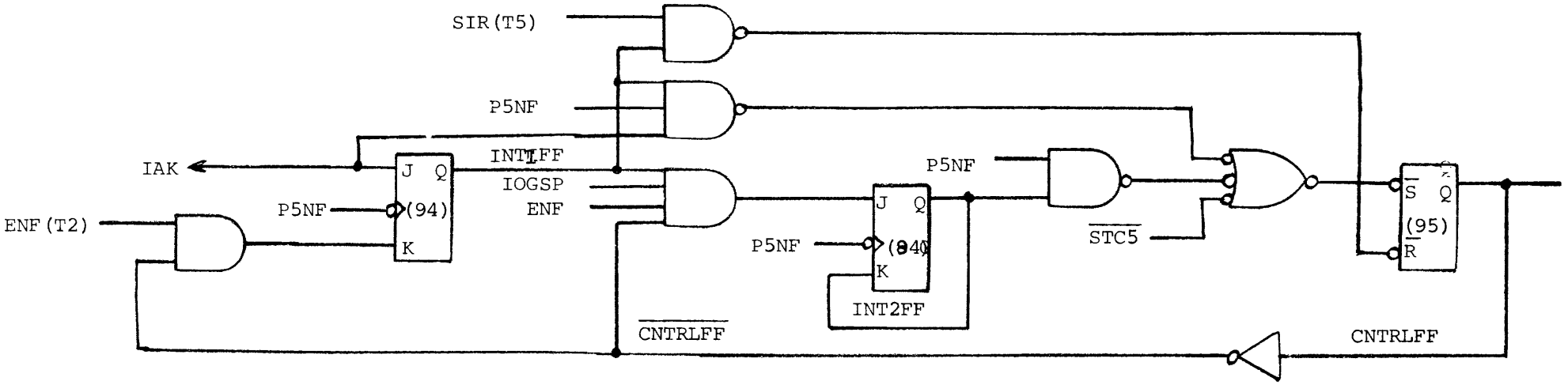
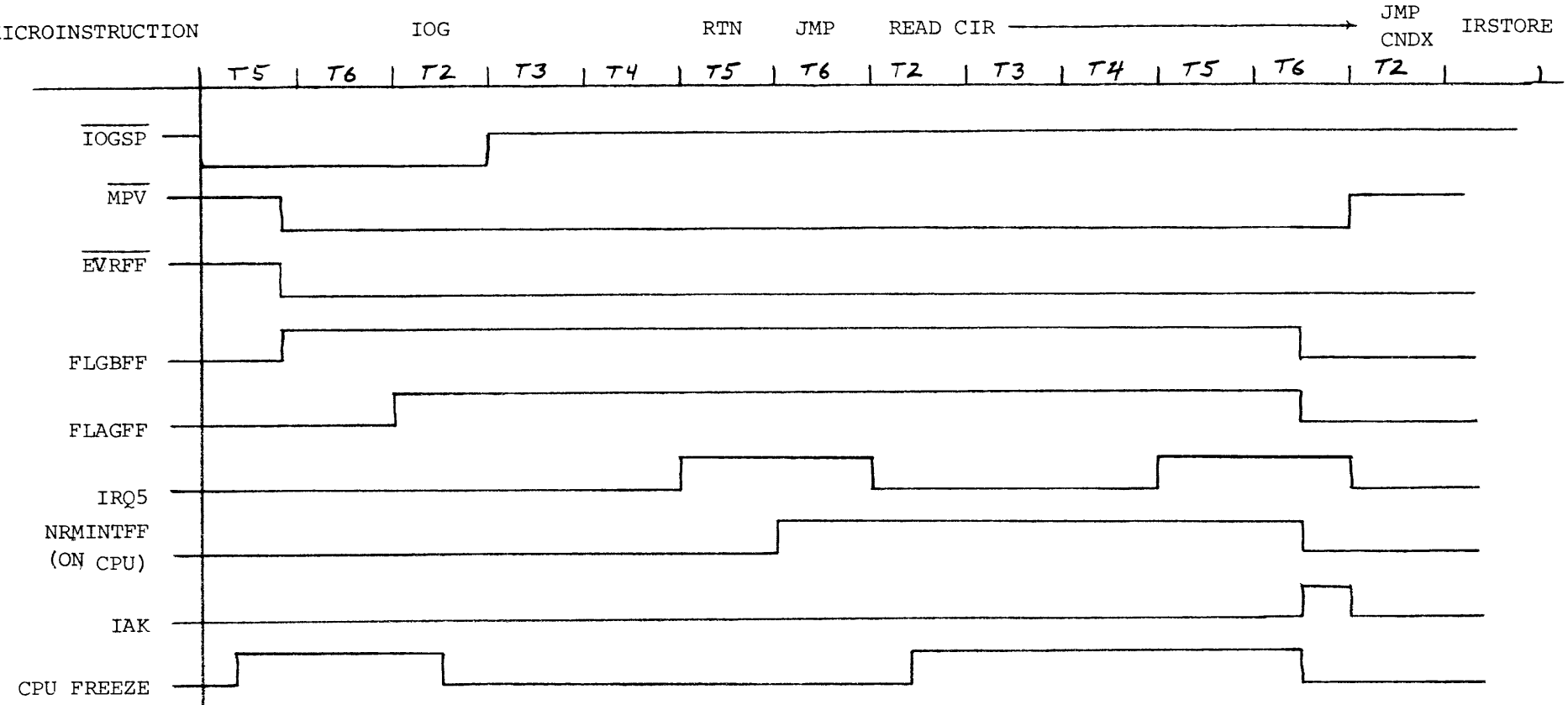
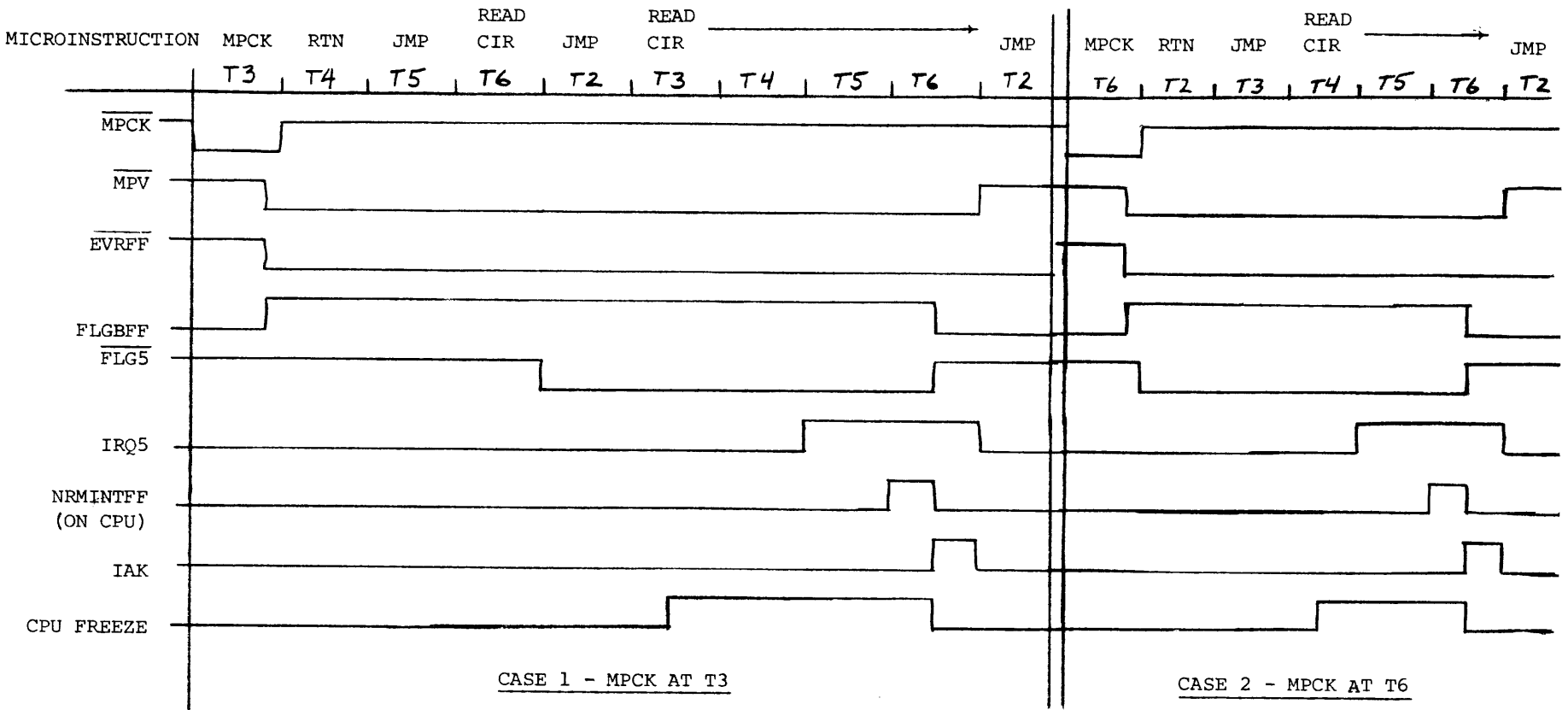


Figure 9
INTERRUPT RESPONSE LOGIC



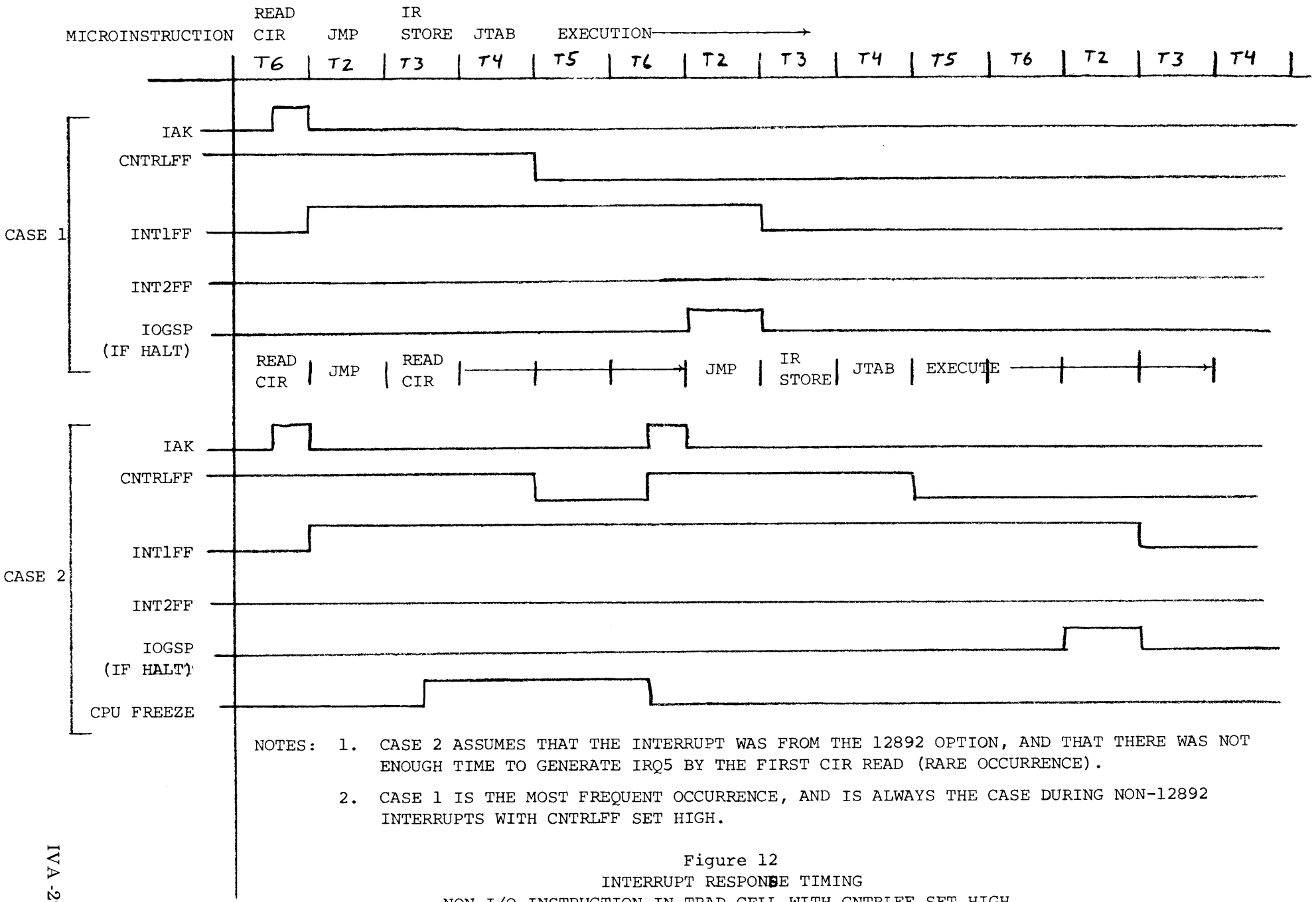
NOTES:
1. IOGSP COULD BE ASSERTED AT ANY T-PERIOD. THE CPU FREEZES UNTIL T2.
2. REFER TO BASE SET MICROCODE FOR ELABORATION OF INSTRUCTION SEQUENCE.
3. IT IS ASSUMED CNTRLFF, IEN5, AND PRH5 ARE ALL HIGH.

Figure 10
INTERRUPT TIMING FOR I/O VIOLATIONS



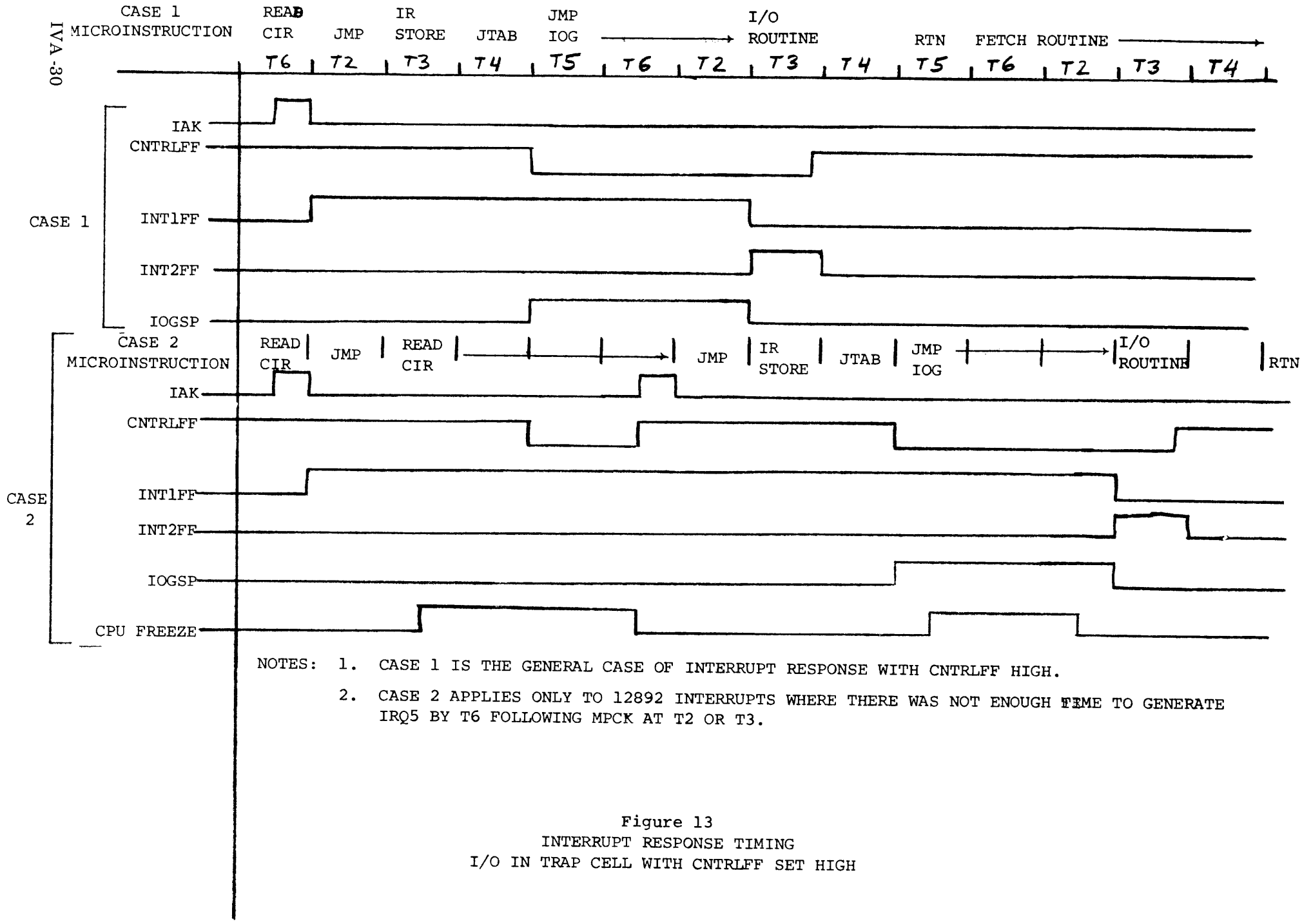
NOTES:
1. WHEN $\overline{\text{MPCK}}$ OCCURS AT T3, THERE IS NOT ENOUGH TIME TO GENERATE IRQ5 BY THE TIME IT IS EXPECTED AT T6.
2. $\overline{\text{MPCK}}$ MAY OCCUR AT ANY T-PERIOD.
3. THE EXAMPLES ABOVE ARE TYPICAL. EXACT TIMING DOES DEPEND ON THE PARTICULAR INSTRUCTION.

Figure 11
INTERRUPT TIMING FOR FENCE VIOLATIONS DURING A ST* INSTRUCTION



NOTES:
1. CASE 2 ASSUMES THAT THE INTERRUPT WAS FROM THE 12892 OPTION, AND THAT THERE WAS NOT ENOUGH TIME TO GENERATE IRQ5 BY THE FIRST CIR READ (RARE OCCURRENCE).
2. CASE 1 IS THE MOST FREQUENT OCCURRENCE, AND IS ALWAYS THE CASE DURING NON-12892 INTERRUPTS WITH CNTRLFF SET HIGH.

Figure 12
INTERRUPT RESPONSE TIMING
NON-I/O INSTRUCTION IN TRAP CELL WITH CNTRLFF SET HIGH



NOTES:
1. CASE 1 IS THE GENERAL CASE OF INTERRUPT RESPONSE WITH CNTRLFF HIGH.
2. CASE 2 APPLIES ONLY TO 12892 INTERRUPTS WHERE THERE WAS NOT ENOUGH TIME TO GENERATE IRQ5 BY T6 FOLLOWING MPCK AT T2 OR T3.

Figure 13
INTERRUPT RESPONSE TIMING
I/O IN TRAP CELL WITH CNTRLFF SET HIGH

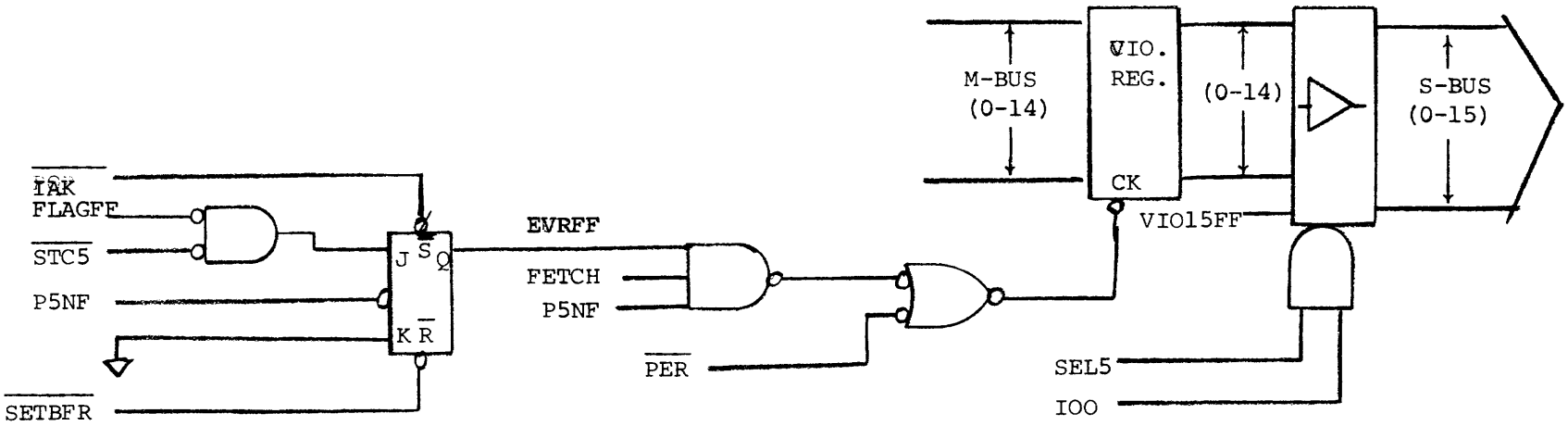
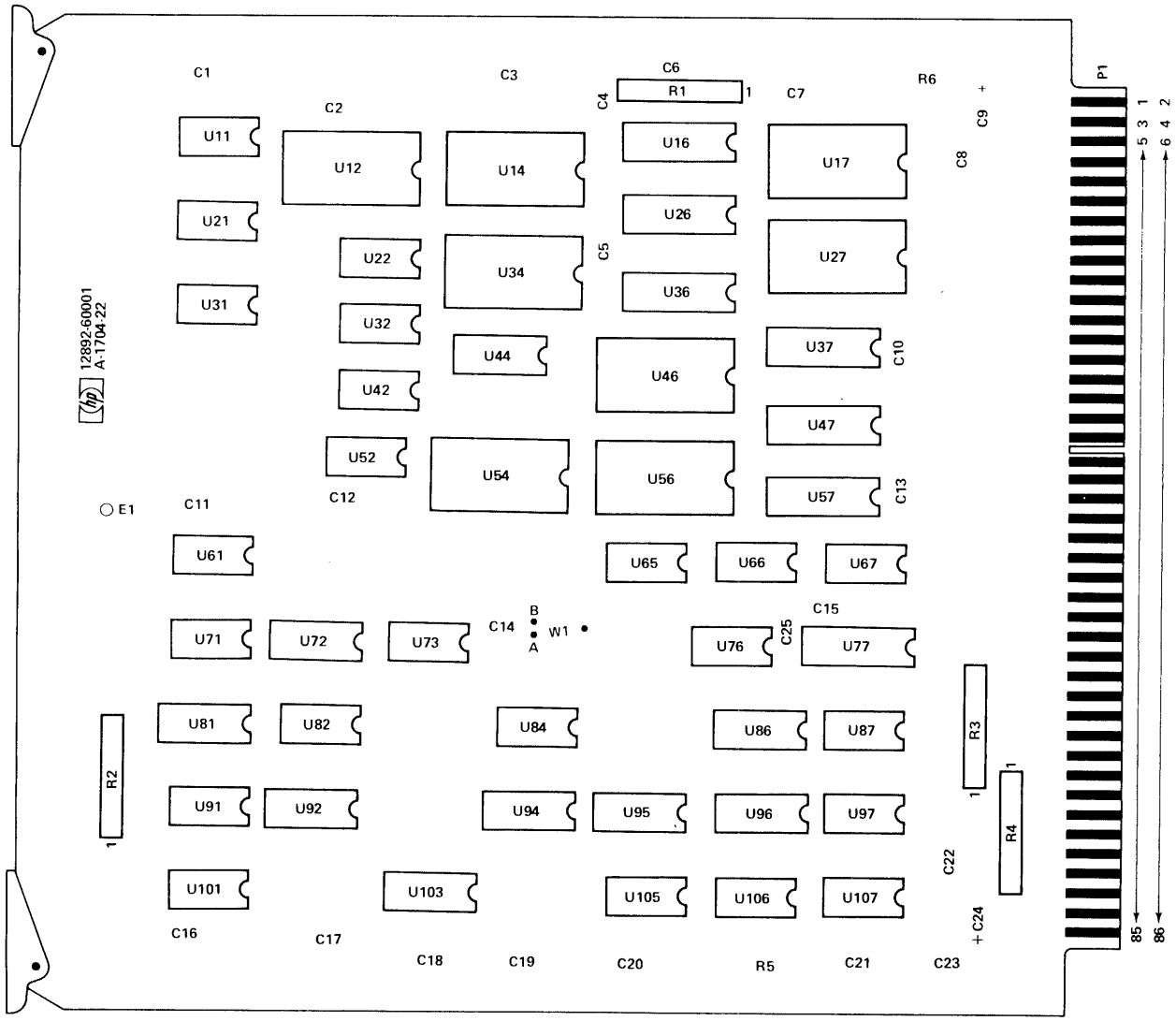


Figure 14

VIOLATION REGISTER LOGIC



12892A Memory Protect Assembly
12892-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
1	DIV.50			7			
3	DIV.33			7			
5	DIV.63			7			
	C4,5,10,13	CAP 0.1UF		0150-0121		U	4
	C1-3,6-8,11,12,14-23	CAP .01UF		0160-2055		U	18
	C25	CAP 820PF 5%		0160-3539		U	1
	C9,24	CAP 10UF 10%		0180-0374		U	2
	E1	STUD SOLDER TERM		0360-0294		U	1
	R5	RES 1K 1%.125		0757-0280		U	1
	R6	RES 1.5K 1%.125		0757-0427		U	1
		PIN GRV .062X.25		1480-0116		U	2
	R3,4	RES NET 7X1.5K		1810-0020		U	2
	R1,2	RES NET 7X1K		1810-0030		U	2
	U61,65,91,106	IC MC3001P		1820-0141		U	4
	U52	IC MC3003P		1820-0205		U	1
	U66	IC SN7402N		1820-0328		U	1
	U82,87,101	IC SN74H00N		1820-0370		U	3
	U32,67	IC SN74H10N		1820-0371		U	2
	U105	IC SN74H20N		1820-0373		U	1
	U11	IC SN74H21N		1820-0374		U	1
	U21,22,42	IC SN74H30N		1820-0375		U	3
	U71,107	IC SN74H04N		1820-0424		U	2
	U12,34,46,54	IC SN74181N		1820-0606		U	4
	U44	IC SN74182N		1820-0611		U	1
	U95	IC 9314PC		1820-0626		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
	U84	IC SN74S00N		1820-0681		U	1
	1U31,97	IC SN74S04N		1820-0683		U	2
	1U73,76	IC SN74S10N		1820-0685		U	2
	1U72,81,86,92,94,3 96	IC SN74H106N		1820-0715		U	6
	1U14,17,27,56	IC 9308PC		1820-0742		U	4
	1U16,37	IC HP147A		1820-0755		U	2
	1U26,57	IC HP106A		1820-0759		U	2
	1U36,47,77	IC HP106B		1820-0760		U	3
	U103	IC 8T13B		1820-1080		U	1
	W1	WIRE JUMPERS		8159-0005		U	1
		EXTRACTOR-PC		5040-6001		W	1
		EXTRACTOR-BLACK		5040-6068		W	1
		BOARD-ETCHED		12892-80001		W	1

REV	REF.	SERIES/PREFIX	DWGS AFFECTED
A	ORIG	1409	ALL
B	22-2288	1430	ALL
C	ERRATA	NA	ALL
D	22-3010	1548	-53
E	22-3345	1632	52,53
F	22-3806	1764	-53

DWG	REVISION
-51	B C
-52	B C E
-53	B C D E F

(A16) BSB (Ø:15)

+5V P1-39,40 +5V
C4,5,10,13 .1 C9 10.0 C1-3,6-8,11, 12,14-21 .01
COM P1-1,2,85,86 COM
C24 10.0 C22,23 .01
-2V P1-47,48 -2V

U14 DUAL 4-BIT LATCH
ENABLE 2,14 3,15
CLEAR 1,13

ADDRESS REGISTERS

SEL5 (E25)
BIOO (E23)

R1G 1K +5V

U56 DUAL 4-BIT LATCH
CLEAR 1,13
ENABLE 3,15 2,14

U12 FUNCTION GENERATOR
U34 FUNCTION GENERATOR
U46 FUNCTION GENERATOR
U54 FUNCTION GENERATOR
CARRY IN
MODE
CARRY OUT
A=B
CP
CG

ADR CARRY (F18)

VIOLATION DETECTION LOGIC

U44 CARRY GENERATOR

R1F 1K +5V

INCI P1-76
U107C
U92A IND1 FF
R2A 1K +5V
U92B IND2 FF
U82C
(C25) BPSB
(E25) FETCH
U101C
(C23) IAK
U91A

P1-18 MPINTON

NOTES:
1. UNLESS SPECIFIED OTHERWISE:
ALL RESISTANCES ARE IN OHMS
ALL CAPACITANCES ARE IN MICROFARADS

THIS SCHEMATIC DIAGRAM CONSISTS OF 3 SHEETS, DWG. NOS. 12892-60001-51 THRU 12892-60001-53.

MEMORY PROTECT
12892-60001-51
SHEET 1 of 1
ENGINEER | APPROVED | DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

REV	REFERENCE
B	22-2288
C	ERRATA
E	22-3345

SB (0:15)

SB0 P1-71
SB1 P1-64
SB2 P1-58
SB3 P1-53
SB4 P1-49
SB5 P1-45
SB6 P1-39
SB7 P1-35
SB8 P1-31
SB9 P1-27
SB10 P1-23
SB11 P1-19
SB12 P1-15
SB13 P1-11
SB14 P1-7
SB15 P1-3

(0:15) BSB (A4)

U26, U57, U36, U47 — ENABLE

R1D, R1E, R1A — 1K — +5V

$\overline{PE}$ P1-59
$\overline{HLTPE}$ P1-17
$\overline{IRSTF}$ P1-25
IO1 P1-63
$\overline{MPCK}$ P1-56
$\overline{DMAFRZ}$ P1-10

-2V — R3D 1.5K — U65A

R6 1.5K +5V

VIOLATION REGISTERS

MB0 P1-72
MB1 P1-61
MB2 P1-54
MB3 P1-52
MB4 P1-50
MB5 P1-46
MB6 P1-42
MB7 P1-37
MB8 P1-32
MB9 P1-28
MB10 P1-24
MB11 P1-20
MB12 P1-16
MB13 P1-12
MB14 P1-8

U27 — DUAL 4-BIT LATCH — ENABLE / CLEAR

R1B 1K +5V

U17 — DUAL 4-BIT LATCH — ENABLE / CLEAR

VIO15FF (B18)

U16, U37 — ENABLE

SEL5 (E25)

(E25) FETCH

(F28) $\overline{STC5}$
(C27) FLAG FF
U66C
EVR FF U72A — SET BFR
U73B
U91B
$\overline{PER}$ (D24)

(C25)
(C25) BP5C
(F25) STF5
VIO REG 15 U86A
VIO15FF (F14)

R1C 1K +5V
(F26) $\overline{CLF5}$
U76B
U97A
PAR ENA U96A
U76A
(D23) PRH5

$\overline{POPIO1}$ (E23)

R2F 1K +5V
HALT INSTR U81B
$\overline{HLTIRFF}$ (B25)
$\overline{POPIO2}$ (F28)

(B25) BP5A
U71C
U21A
U71D
U61A

R2G 1K +5V
JMP FF U96B
IOSEL FF U86B
U65C
U65B
U107F
U71A
U32C
U32B
U66B
U107B
U61B
U11A

(B25) IOGSP
U61C
U84C
U52D
U76C
$\overline{MEV}$ (F23)
U73A
MPIOVIO (C23)
(C25)BP5B
(D8) ADR CARRY
U11B
U31C
$\overline{MEMVIO}$

U22
U52C
U84A
P1-5 $\overline{MPCND}$
U42

THIS SCHEMATIC DIAGRAM CONSISTS OF 3 SHEETS, DWG. NOS. 12892-60001-51 THRU 12892-60001-53. SEE DWG. NO. 12892-60001-51 FOR REVISION STATUS OF ENTIRE DWG. SET.

MEMORY PROTECT — SHEET 1 OF 3
12892-60001-52
ENGINEER | APPROVED | DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

REV	REFERENCE
B	22-2288
C	ERRATA
D	22-3010
E	22-3345
F	22-3806

INTERRUPT LOGIC

THIS SCHEMATIC DIAGRAM CONSISTS OF 3 SHEETS, DWG. NOS. 12892-60001-51 THRU 12892-60001-53. SEE DWG. NO. 12892-60001-51 FOR REVISION STATUS OF ENTIRE DWG. SET.

MEMORY PROTECT
12892-60001-53
SHEET 1 of 1

ENGINEER | APPROVED | DATE

HEWLETT PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

HP 12892B
MEMORY PROTECT

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

CONTENTS

12892B MEMORY PROTECT OPTION
THEORY OF OPERATION

1.0 INTRODUCTION

This Document provides the theory of operation for the 12892B Memory Protect/Parity option for the 21MX computers. Discussion is conducted on the functional block, programming, and detailed operation levels. Block diagrams, generalized logic diagrams, and timing diagrams are used to show operation. Understanding of this document is essential when performing maintenance or trouble shooting on the 12892B option.

2.0 GENERAL DESCRIPTION

The following paragraphs describe the basic block diagram and define signals which interface with other computer system components.

2.1 Basic Block Diagram

Refer to Figure 1 for the following discussions.

2.1.1 Indirect Level Logic

This logic consists primarily of a counter which generates a signal to allow normal I/O interrupts in the CPU during indirect addressing routines, after three levels of indirection.

2.1.2 Parity Error Logic

This block of logic is used to enable and disable the 12892B option to interrupt on occurrence of a parity error. When a parity error occurs, bit 15 of the Violation Register is set high by this logic.

2.1.3 Memory and I/O Violation Detection Logic

This block consists of the logic necessary to determine if an I/O instruction has been fetched into the Instruction Register in the CPU, what bounds to allow on protected memory, and whether a reference to protected memory is imminent.

2.1.4 Interrupt and Control Logic

This block receives and decodes timing signals and I/o commands from the CPU and controls the other logical blocks. It also controls generation and handling of interrupts.

2.1.5 Memory Protect Violation Register

The Memory Protect Violation Register is loaded from the M-Bus with the address of the current instruction. When a 12892B option interrupt condition is imminent, it is disabled, saving this address.

2.1.6 Parity Violation Register

The Parity Violation Register is loaded from the M-Bus on the trailing edge of every memory read command. The occurance of a parity error inhibits subsequent clocking of this register.

2.2 Interface Signal Definitions

This section describes the main signals which interface the 12892B option board to other elements of the computer. Standard busses and I/O signals are not included. All signals are TTL compatible, ground true unless otherwise specified.

2.2.1 Input Signals

$\overline{\text{FTCH}}$ "Fetch". From the microinstruction Special field on the CPU. Indicates that an instruction has been fetched and that its address is present on the M-Bus. Causes resetting of violation detect logic and indirect counter, and loads the Memory Protect Violation Register.

$\overline{\text{HLTPE}}$ "Halt on Parity Error". From the parity option switch on the CPU. Indicates the CPU is set to halt on parity errors, and disables parity interrupts. Remains in one state until switch is manually changed.

$\overline{\text{INCI}}$ "Increment indirect counter". From the microinstruction Special field on the CPU. Signals another level of indirect to the indirect level logic. Occurs during one unfrozen P5 period.

$\overline{\text{IOGSP}}$ "I/O group special". From the microinstruction Special field on the CPU. Indicates that the I/O group signals will be enabled on the next T2 period. Lasts one T-period plus the number of T-periods to the nearest T2 (freeze time): 1 to 5 T-periods in length.

$\overline{\text{IRSTF}}$ "Instruction Register Store, freezable". From microinstruction store field on CPU. Indicates that data is being loaded into the Instruction Register on the CPU, and is currently present on the S-BUS. Used to set up error-detection logic for the current instruction. Lasts one T-period, broken up by freeze time.

$\overline{\text{MEV}}$ "Memory Expansion Violation". Generated by Memory Management Unit (MMU). Indicates violation of protected memory in that unit. Occurs during P4 of imminent violation in the MEU.

$\overline{\text{MPCK}}$ "Memory Protect Check". From microinstruction Special field on CPU. Causes check for possible protected memory bounds violation. Occurs for one T-period plus freeze time, if any.

$\overline{\text{PE}}$ "Parity Error". From the Memory Controller. Indicates occurrence of parity error during memory reference. Consists of a pulse generated when data is valid during a Read operation.

$\overline{\text{DMAFRZ}}$ "DMA freeze condition". From the DMA board. Indicates that DMA is using the S-BUS and the CPU is frozen. Prevents error-checking the S-Bus until the CPU has control of it again.

2.2.2 Output Signals

$\overline{\text{CTL5}}$ "Control 5". Signal to Memory Management to show state of control flip-flop.

$\overline{\text{FLG5}}$ "Flag 5". Signal to CPU indicating state of Flag flip-flop. Used to disable the I/O priority chain and to generate a Special interrupt request.

$\overline{\text{MPCND}}$ "Memory Protect Conditional". Signal to Memory Management Unit. Indicates a memory protect check is in progress so the MEU can check for violations.

$\overline{\text{MPINTON}}$ "Memory Protect interrupt on". Signal to CPU. Indicates more than three levels of indirection have occurred, and enables normal I/O interrupts to occur during further indirect levels.

$\overline{\text{MPV}}$ "Memory Protect Violation". Generated when the control is set and violations other than parity errors occur. Prevents CPU from altering protected memory or registers and disables I/O signals.

$\overline{\text{RESPE}}$ "Reset parity error". Signal to CPU which clears the parity error light on servicing of a 12892B option interrupt request.

$\overline{\text{SKF}}$ "Skip flag". Positive true. True when the skip condition is met for a SFS5 or SFC5 instruction. Responds to state of the Memory Expansion Flag flip flop (whether violation occurred in the Memory Management Unit).

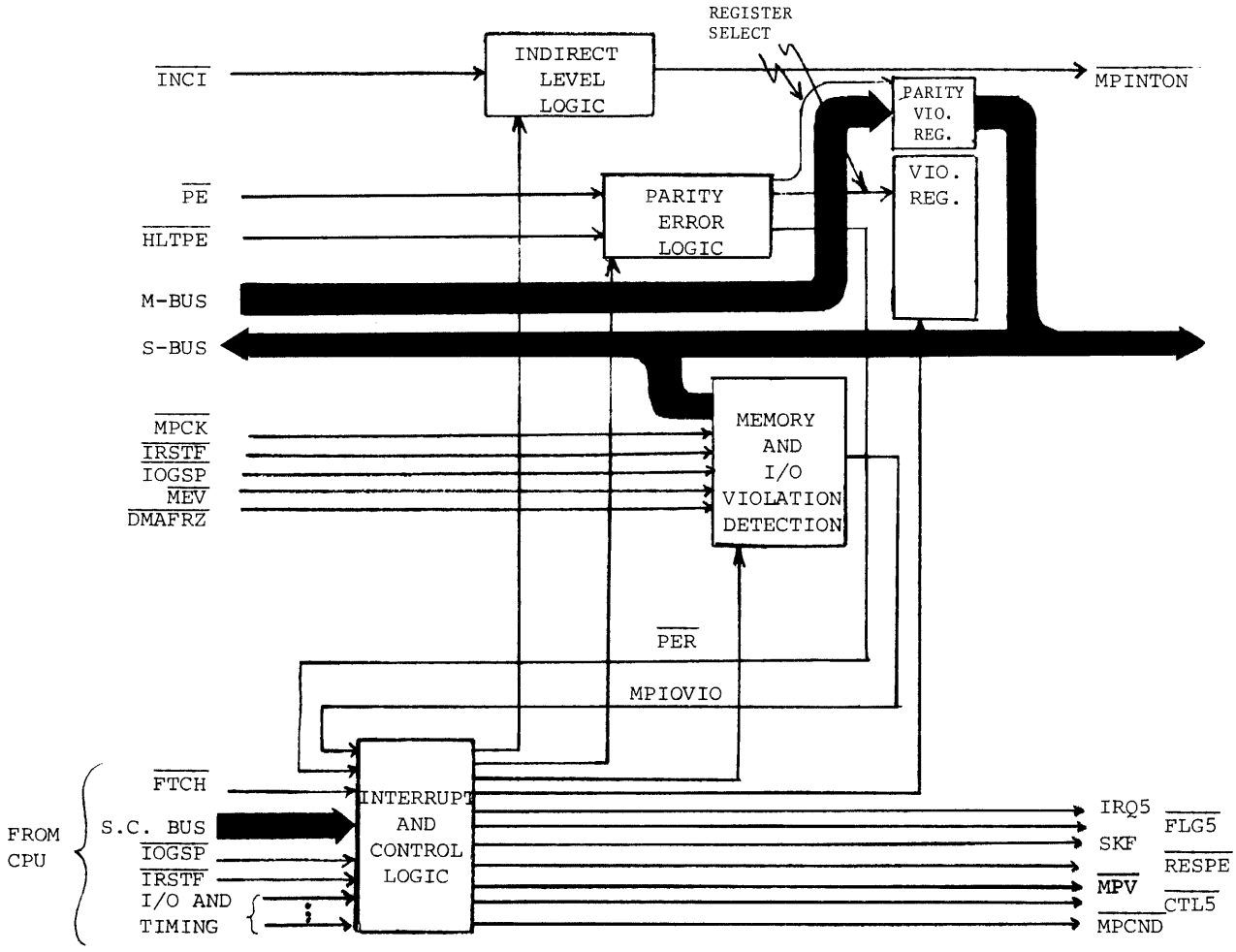


Figure 1

12892 Option Block Diagram

3.0 PROGRAMMING

The 12892B option interfaces with the CPU as a standard I/O device, except with regard to interrupt generation and handling. It is accessed as select code 5 in the I/O system. It performs the function described below.

3.1 Memory Protect Feature

This feature prevents certain instructions from altering memory below a programmed fence, and from jumping into protected memory. The check for possible violations is initiated by a microcode instruction field, so operation of this feature is very instruction dependent. The programmer should consult the microprogramming manual and the specifications for the extra firmware packages installed in his computer to determine the extent of memory protection for his available instructions. The following discussions apply to Base Set and Extended Arithmetic Unit Instructions.

3.1.1 Feature Programming

Memory Protection is enabled by a STC 5 instruction. It is disabled at power-up or by pressing the Preset button in the HALT mode, or by executing a trap cell instruction during an interrupt which is a Halt or a non-I/O instruction.

3.1.2 Feature Operation

If Memory Protection is enabled, and the interrupt system is enabled by a previous STF0 command, then an interrupt to trap cell 5 will be generated if any of the following instructions attempt to access protected memory:

a. ISZ
b. JSB
c. STA
d. STB
e. DST
f. JMP
g. Any other instruction, not in the base set, which provides memory protection.

The interrupt system must always be enabled before enabling Memory Protection. If the interrupt system is off and Memory Protect is on and a violation occurs the CPU will permanently freeze and can recover only by going to reset.

3.1.3 Protection Boundaries

The upper address bound of protected memory is loaded from the A or B register into the Fence Register in the 12892B option by an OTA5/OTB5 command. Memory addresses below this Fence are protected.

The lower address bound depends on the instruction being executed. For any instruction with a JSB format in the Instruction Register at the time of a memory protect check in microcode, the lower bound of protection is address 0 (the A-register). For all other instructions, the lower bound is address 2. Addresses equal to or above the lower bound are protected.

3.1.4 Indirect Addressing

Indirect addressing is permitted through protected memory for protected instructions, but the final effective address must be in unprotected memory.

3.1.5 Obtaining Violation Address

After a Memory Protect interrupt has occurred, the address of the violating Instruction may be obtained by a LIA5/LIB5 command. If a parity error occurs after the Memory Protect violation, the address loaded by LIA5/LIB5 will be that of the parity error. BIT 15 is low if the address was related to Memory Protection.

3.1.6 Memory Expansion Unit Memory Protection

The reader is referred to the Memory Expansion Unit (MEU) specifications for programming Memory Protect for that option. The 12892B option generates interrupts when notified by the MEU that a violation has occurred.

3.2 I/O Violation Feature

This feature provides protection of the system from illegal I/O instructions by causing an interrupt when an illegal I/O instruction is attempted.

3.2.1 Feature Programming

I/O protection is enabled and disabled simultaneous with Memory Protection.

3.2.2 Feature Operation

The definition of an illegal I/O instruction is controlled by jumper W7. Instructions referencing select code 1 (front panel display register or Overflow flip-flop) are always legal. The jumper positions have the following meanings:
W7-OUT: All other I/O instructions are illegal.
W7-IN: Only Halt instructions are illegal.
If this feature is enabled, and the interrupt system is enabled by a previous STF0, an interrupt to location 5 is generated if an illegal I/O instruction is attempted. Whether or not the interrupt system is enabled, the illegal instruction is treated as a NOP.

3.2.3 Obtaining Violating Address

After an interrupt occurs, the address of the violating instruction may be obtained from the memory protect violation register by a LIA5/LIB5 instruction. Bit 15 will be low. Parity errors occurring subsequent to a violating I/O instruction will cause the address of the parity error plus bit 15 high to be loaded into the Parity Violation Register.

3.3 Indirect Level Logic

Each time a level of indirect addressing is executed in the base set routines, the Indirect Counter on the 12892B option is incremented, until the third level. Then any pending interrupts are allowed to cause termination of indirect addressing, resetting of the P-counter to the start of the current instruction, and servicing of the interrupt before attempting the indirect addressing again. This prevents indirect addressing from holding off critical interrupt requests.

3.4 Parity Error Interrupt Feature

If the INTERRUPT/IGNORE feature is switch-selected on the CPU, the Parity Error Logic is enabled on the 12892B option, and the priority chain is high to the 12892B option board, then a parity error will cause an interrupt to trap cell 5. This interrupt will occur whether or not the interrupt system has been enabled (by a previous STF0). An LIA5/LIB5 will fetch the address of the parity error plus bit 15 high.

If the HALT ON PARITY feature is switch-selected on the CPU and jumper W3 is installed, no interrupt will be generated. An LIA5/LIB5 will return meaningless data. If jumper W3 is not installed, the 12892B will interrupt following the HALT if RUN is pressed before PRESET. If PRESET is not pressed an LIA5/LIB5 will fetch the address of the parity error with bit 15 high.

3.4.1 Feature Programming

This feature is enabled by the following:

a. STF5 instruction
b. Power turn-on
c. Pressing the PRESET button in the Halt mode.

The following occurrences disable the Parity Interrupt feature:

a. A memory parity error occurs during a Read operation.
b. A CLF5 command is performed.
c. The Halt-on-Parity option is switch-selected on the CPU and W3 installed.

3.4.2 Obtaining the Error Address

After occurrence of a parity error interrupt, the address on the M-Bus at the time of the parity error may be obtained by a LIA5/LIB5 instruction unless Halt-On-Parity selected and W3 installed. BIT 15 will be a one.

4.0 DETAILED OPERATION

This section contains a detailed theory of operation for the 12892B Memory Protect Option. The reader should refer to the detailed schematic for this option, as well as the figures and diagrams referred to in this discussion. IC pack numbers are given in parentheses.

4.1 Indirect Level Logic

This consists of the two J-K flip-flops ICA, ICB (U42), and their associated logic. Refer to Figures 2 and 3. The flip-flops form a simple counter, clocked by INCI, which occurs at P5 (M-Series) or P3 (E-Series) of a microinstruction which specifies INCI in its Special field. This occurs in the indirect addressing routine. The counter increments are shown in Figure 2, at each occurrence of INCI. When ICA=0 and ICB=1 the counter will not increment further, and MPINTON will go low until the counter is reset by FTCH at the next instruction fetch, or by IAK. This insures that each instruction, including interrupt trap cells, is allowed no more than 3 levels of indirect before checking for interrupts. MPINTON directly sets the Interrupt Enable flip-flop (INTENFF) on the CPU, allowing normal interrupts to be sensed during indirect addressing.

4.2 Parity Error Logic

This logic consists of the Parity Enable flip-flop (PARENFF), the Parity Error flip-flop (PARERRFF), the Parity Violation Register, and their associated gates.

4.2.1 Parity Enable flip-flop (PARENFF-U51B)

A STF5 or POPIO will set this flip-flop setting PARENFF (U51-9) high, enabling clocking of the parity violation register and parity interrupts.

A CLF5 or a Parity interrupt will reset PARENFF (U51-9) low, inhibiting parity violation register clocking.

4.2.2 Parity Error flip-flop (PARERRFF U51A)

A STC5 or POPIO will reset this flip-flop setting PARERRFF (U51-5) low, selecting the memory protect violation register on the next LIA5/LIB5.

A parity error will set this flip-flop causing PARERRFF (U51-5) to go high, selecting the parity violation register on the next LIA5/LIB5.

4.2.3 Parity Error Interrupts

The $\overline{PE}$ signal initiates an interrupt if a parity error occurs, PRH5 is high, PARENFF is high, and INTERRUPT/IGNORE is selected or HALT ON PARITY is selected and jumper W3 is not installed. $\overline{PE}$ will perform the following actions:

a. Direct set PARERRFF selecting Parity Violation register.
b. Reset PARENFF, disabling future parity interrupts.
c. Set the FLGBFRFF in the interrupt logic.
d. Reset EVRFF, preventing further clocking of the Memory Protect Violation register.

4.3 Memory Protect and I/O Violation Detect Logic

This logic consists of buffers, a comparator, flip-flops, the fence register, and associated logic necessary to decode the various violation conditions. Refer to Figure 6.

4.3.1 Fence Register and Comparator

An OTA5/OTB5 instruction will cause generation of IOO and SEL5 (select code 5) signals, which will load the buffered contents of the S-Bus into the Fence Register (U34, U74). The Fence Register and buffered S-Bus are inputs to the comparator logic (U24, U14, U54, U84, U44) which constantly performs the subtraction "M-BUS MINUS FENCE". MPCARRY is high if the fence is greater than the M-Bus. Thus, if an address is present on the M-Bus, MPCARRY indicates if it is below the upper bound of protected memory.

4.3.2 Protected Memory Lower Bounds

The lower bound of protected memory is determined by the presence or absence of a JMP instruction in the IR on the CPU. U86 causes setting low of the JUMP flip-flop (U93). U93-15 goes low if a JMP instruction is present on the S-Bus when a STORE into the IR is performed (IRSTF). U93-15, U94, and U83D decode violation of the lower bounds of protected memory, the output of U83D is high if the instruction is a JMP, or if the M-Bus is not 0 or 1. If either of these conditions is true, then if MPCARRY is high, a violation condition is present.

4.3.3 Memory Protect Violation Detection

U11A decodes memory violation conditions. One microinstruction before a STORE into memory is initiated, the memory address is placed on the S-Bus (M-Series only, the E-Series checks on the M-Bus) and MPCK is specified in the special field. $\overline{\text{MPCK}}$ is sent to the 12892B and the address is checked for a violation by the logic of sections 4.3.1 and 4.3.2 above. If there is a violation, then during the next P5, $\overline{\text{MPVIO}}$ (U11-12) is low.

4.3.4 Memory Management Violation Logic

The Memory Management package has its own protection logic. It is sent information from the 12892B to allow it to perform this function. $\overline{\text{CTL5}}$ notifies Memory Management of the state of the memory protect feature. $\overline{\text{MPCND}}$=MPCK • ($\overline{\text{A01}}$ + JMP) which is low if a STORE address is above the lower bound of protected memory. If Memory Management detects a violation, it will assert $\overline{\text{MEV}}$ at the next P4, setting the Memory Expansion Violation flip-flop (MEVFF U81B), and the FLGBFR flip-flop. MEVFF is reset by POPIO or STC5. The state of MEVFF may be tested with SFS5 and SFC5.

4.3.5 I/O Violation Logic

If at occurrence of $\overline{\text{IRSTF}}$ the S-Bus contains a HALT instruction, as decoded by gate U95, then at the following P5, the Halt instruction flip-flop will be set (U93-10 will go low). It will be reset on the next $\overline{\text{IRSTF}}$. Also during an $\overline{\text{IRSTF}}$, the low-order six bits of the S-Bus are decoded by U73D and U85. If they decode to a value of 01 octal, then I/O Select Code 1 flip-flop is set on P5 (u93-6 goes low).

$\overline{\text{IOGSP}}$ is low at the start of execution of I/O instructions, and comes from the special field of microcode. If U93-10 or U93-6 is low during IOGSP, then an illegal I/O instruction is being performed (HALT or select code $\neq$ 1). U92A and U32B decode I/O violations ($\overline{\text{IOVIO}}$). $\overline{\text{IOVIO}}$ is low during P5 of IOGSP for violations.

4.3.6 I/O Violation Detection

HALT instructions are always illegal. Jumper W7 selects the action to be taken for all other I/O instructions. If W7 is installed, I/O instructions to any select code are legal. With W7 out, only I/O instructions to select code 1 are permitted.

4.4 I/O Interrupt and Control Logic

This part of the 12892B option consists of I/O signal buffers, I/O command decoding logic, and interrupt generation and response logic.

4.4.1 I/O Priority

The 12892B option occupies select code 5 in the I/O system. Hence, it has higher priority than any device except power fail. Priority chaining is not done on the 12892B board, but on the CPU in order to maintain it in the absence of the option.

On the CPU (refer to Figure 5), IEN5 is high to the 12892B option if the interrupt system is enabled. If power fail control is set ($\overline{CONT4FF}$ low), PRH5 is high and the priority chain in enabled. When the FLAG is set on the 12892B board, $\overline{FLG5}$ is low, which goes to the CPU to disable the priority chain to higher select code devices.

4.4.2 Parity Error Interrupt Generation

Two methods of interrupt requesting are performed. Parity errors generate different requests than other violations. Refer to Figure 7. Parity errors cause setting of the Flag Buffer flip-flop in U81 whether or not the interrupt system is enabled. Hence, parity errors will result in an I/O interrupt whether or not the system is enabled by STF0.

If PARENFF, PRH5 and $\overline{HLTPE}$ are high and $\overline{PE}$ occurs, then U52-8 goes low, setting the PARERRFF and the FLGBFRFF. At the next ENF (T2) period, the FLGFF will set and $\overline{FLG5}$ will go low. $\overline{FLG5}$ generates a special interrupt request in the CPU and disables the priority to select codes 6 and above. At the next SIR (T5), the IRQFF will set asserting IRQ5 to the CPU. IRQFF will go high each T5 and low each T2 until the interrupt is acknowkedged Note that $\overline{FLG5}$ goes low to request a special interrupt early (T2) to provide parity error interrupts preferential servicing. IRQ5 need not be high until T6, when it is needed to load the Central Interrupt Register (CIR) on the CPU.

Note that if a CLF5 instruction begins the fetch phase before $\overline{FLG5}$ goes low, then CLF5 will reset the Flag and Flag Buffer, and prevent the interrupt request, unless CNTRLFF is high, which would result in an I/O violation.

4.4.3 Memory Protect and I/O Interrupt Generation

Refer to Figures 7, 8, 10, and 11 for the following discussion.

Most of the time, Memory Protect and I/O violations interrupt before the next machine language instruction has entered the fetch cycle. However, if MPCK occurs at T2 or T3, and the next microinstruction specifies a return to the fetch routine, then there is not enough time to generate IRQ5 and FLG5 by the time the CPU is ready to read the CIR. To overcome this problem if the CPU reads 0 from the CIR, then it will go back and read it again, allowing time for IRQ5 to be asserted. If any other I/O device sends its IRQ before MPIOVIO can set FLG5, then servicing of the Memory Protect violation interrupt will be postponed until the first opportunity it has to interrupt again. Unless the I/O interrupt routine performs a CLF5 command, there is no danger in postponing the Memory Protect interrupt servicing in this manner. The violating program will not be allowed to perform illegal machine operations in any event.

If the Control flip-flop (CNTRLFF), is set, then when MPIOVIO goes high, the output of gate U92D sets the MPV flip-flop on the next P5. (Refer to Figure 7). MPV goes to the CPU and the Memory Controller to perform the following functions:

a. Inhibit alteration of the Program Counter and S-register on the CPU.

b. Inhibit storing into the memory address specified in the M-register of the CPU. DMA may store into protected memory.

c. Clear the I/O Group Enable flip-flop on the CPU, to inhibit I/O signals from the CPU.

d. If IEN5 and PRH5 are asserted, generate a Special Interrupt Request (refer to Figure 8). This allows MPV interrupts to occur before the next instruction is fetched.

MPV is returned to the high state by IAK. An interrupt is being serviced, so protection from illegal operations is not required any longer.

If MPIOVIO, CNTRLFF, IEN5, and PRH5 are all high, then the Flag Buffer, FLGBFRFF, is set high. FLAGFF is set on the next T2, which sends FLG5 to the CPU to disable the priority chain. As long as FLAGFF is set, IRQ5 will be high only during T5 and T6 until the interrupt is granted. When IAK occurs and IRQ5 is asserted, the FLAGBFF is cleared, FLGFF clocked off at next T2, and IRQ5 will no longer occur.

4.4.4 Interrupt Handling

When the CPU services a Memory Protect, Parity, or I/O interrupt, IAK is high during the last half of T6. IAK performs the following functions (refer to Figures 7, 9).

a. In conjunction with IRQ5, clears the Flag Buffer flip-flop.

b. In conjunction with IRQ5, sends a low level on $\overline{\text{RESPE}}$ to the CPU to reset the Parity Error LED on the front panel.

c. Resets $\overline{\text{MPV}}$ high at P5.

d. Unconditionally sets the Interrupt flip-flop (INTPTFF) indicating occurence of any interrupt (Figure 9).

e. Clears the indirect counter.

The Interrupt flip-flop (INTPTFF, U31B) and the control flip-flop (CNTRLFF) and their associated logic (Figure 9) determine enabling and disabling of the Memory Protect features. Recall that Memory and I/O Protection are to be disabled on occurrence of any interrupt, unless the interrupt trap cell contains an I/O instruction other than HALT.

The interrupt flip-flop (INTPTFF) is set high during IAK if CTLFF is high. At P5, during IAK, the CTLFF is direct cleared disabling the Memory Protect and I/O Protect feature. If the trap cell contains an I/O instruction, IOGSP is asserted before the next FTCH and if the trap cell instruction is not a HLT, the CTLFF is set high at P5 during the IOGSP, thus re-enabling Memory Protect and I/O Protect features.

If the trap cell does not contain an I/O instruction (or it contains a HLT) the CTLFF remains low.

In either case, the next FTCH clears the INTPTFF preventing a subsequent IOGSP from setting the CTLFF.

4.5 Violation Registers

4.5.1 Parity Violation Register

The M-Bus is clocked into the PVR on the trailing edge of every READ (Read command from the CPU or DMA to memory) as long as the PARENFF (U51B) is set. When a parity error occurs, the PARENFF is reset inhibiting the PVR clock thus holding the address of the parity error in the PVR.

The PVR is buffered onto the S-Bus during an LI* 5 or MI* 5 instruction. Bit 15 of the PVR is always a one.

4.5.2 Memory Protect Violation Register

An STC5 instruction causes setting of the Enable Violation Register flip-flop (EVRFF), U33B. As long as EVRFF is high the Memory Protect Violation Register is clocked during FTCH, while the address of the current instruction is on the M-bus. When any violation causes setting of FLGBFF, EVRFF is set low locking the offending address into the violation register.

EVRFF may not be re-enabled until after the current violation interrupt has been serviced.

The MP Violation Register is buffered onto the S-Bus during an LI*5 or MI*5 instruction. Bit 15 of the MPVR is always a zero.

4.6 Power-On or Preset

If power is being turned on, or the Preset button is pressed in the HALT mode, the following actions occur:

a. $\overline{\text{IOSELIFF}}$ is set high (reset state)

b. $\overline{\text{JMPFF}}$ is set high (reset state)

c. $\overline{\text{PARENFF}}$ is set high, enabling parity error logic

d. EVRFF is set high (allow clocking of Violation Register)

e. INTPTFF is set low (reset state)

f. FLGBFF, FLAGFF, IRQFF, CNTRLFF are set low (Memory Protect and I/O protect shut off)

g. MEVFLGFF is set low (reset state)

h. $\overline{\text{HLTFF}}$ is set high (reset state)

i. MPV flip-flop is set low (reset state, $\overline{\text{MPV}}$ high).

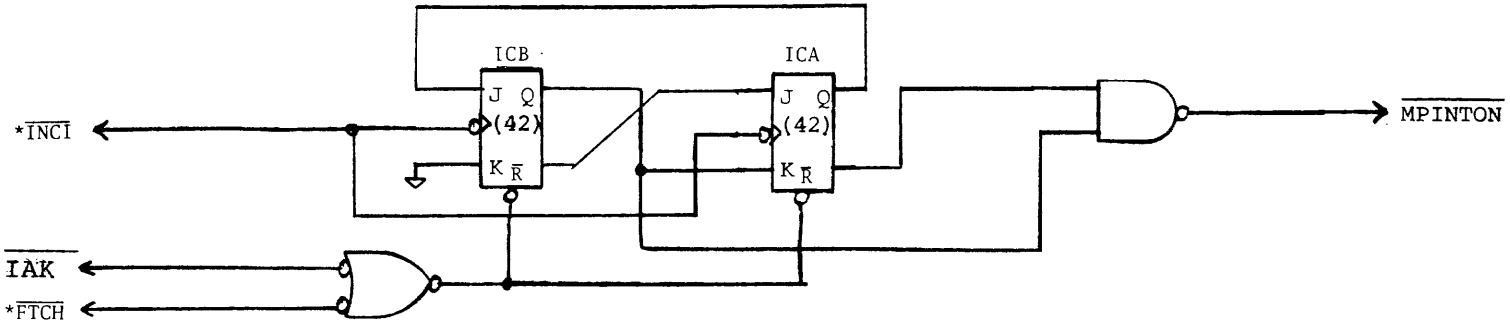
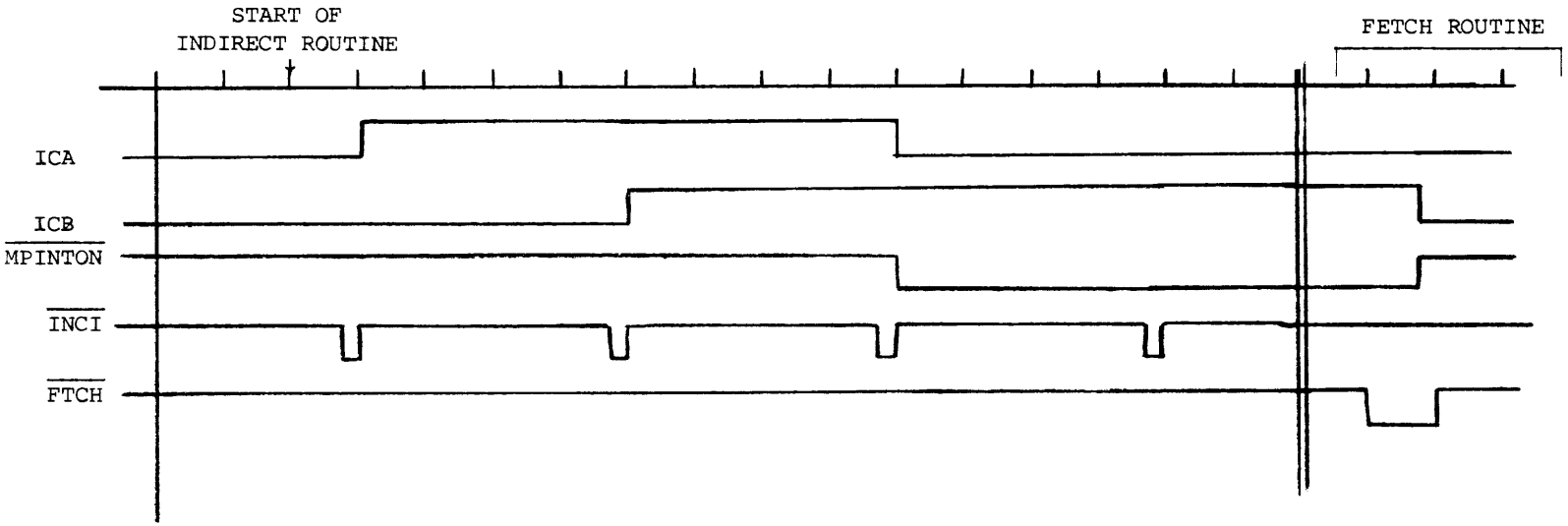


Figure 2
INDIRECT LEVEL LOGIC



EACH DIVISION REPRESENTS
ONE MICROINSTRUCTION CYCLE

*Occurs at P3 for E-Series or P5 M-Series

Figure 3
INDIRECT LOGIC TIMING
DURING MULTIPLE (4 LEVELS) INDIRECTS

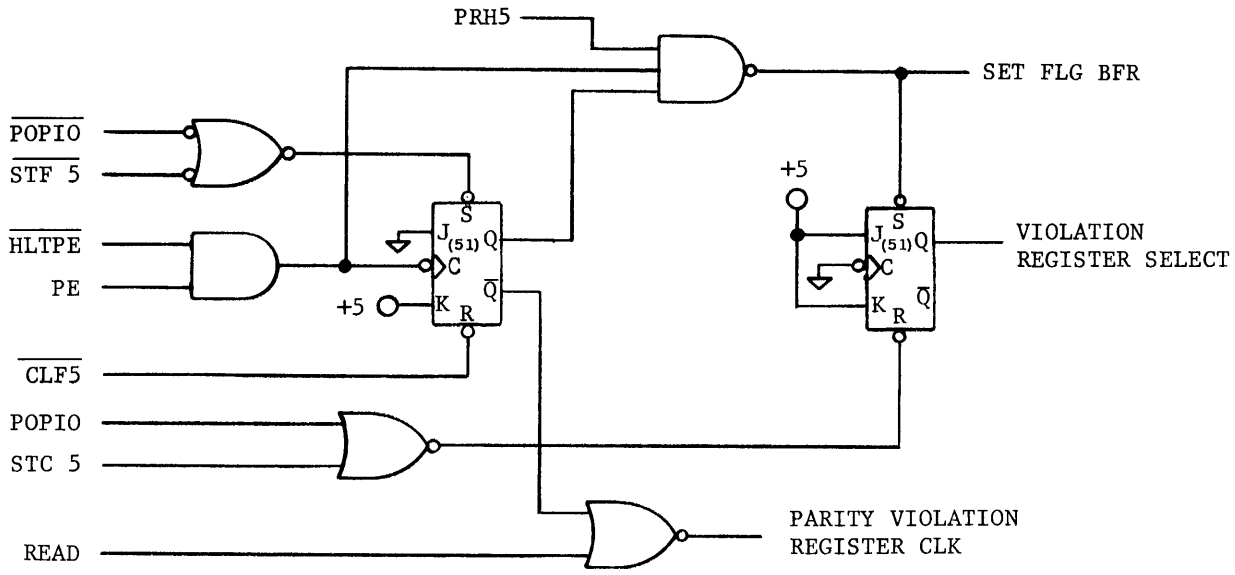


Figure 4

Parity Error Logic

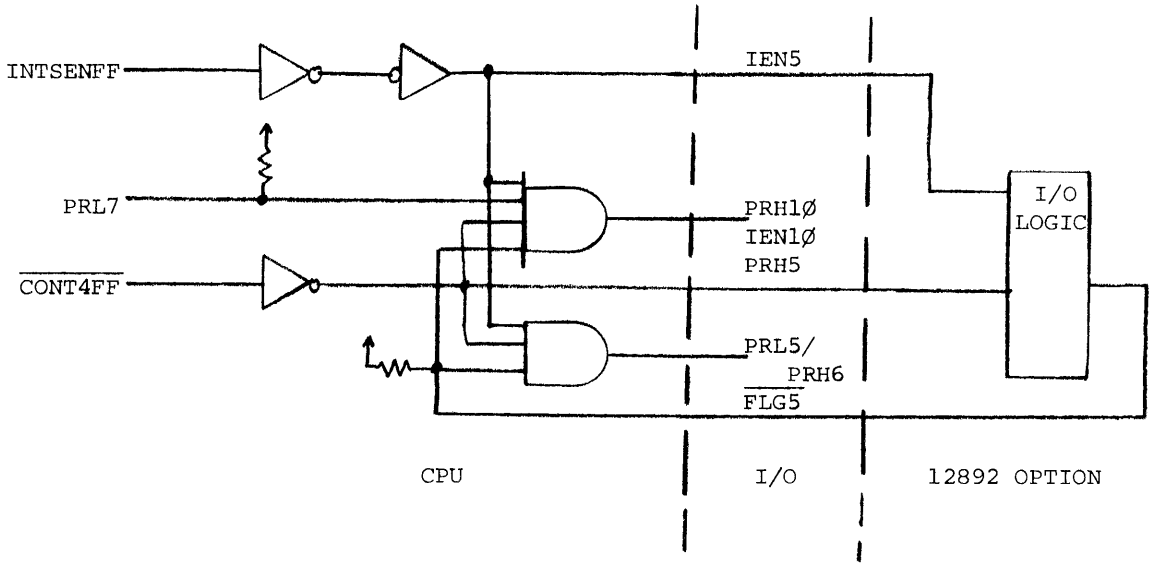


Figure 5
PRIORITY CHAIN LOGIC
INVOLVING THE 12892 OPTION

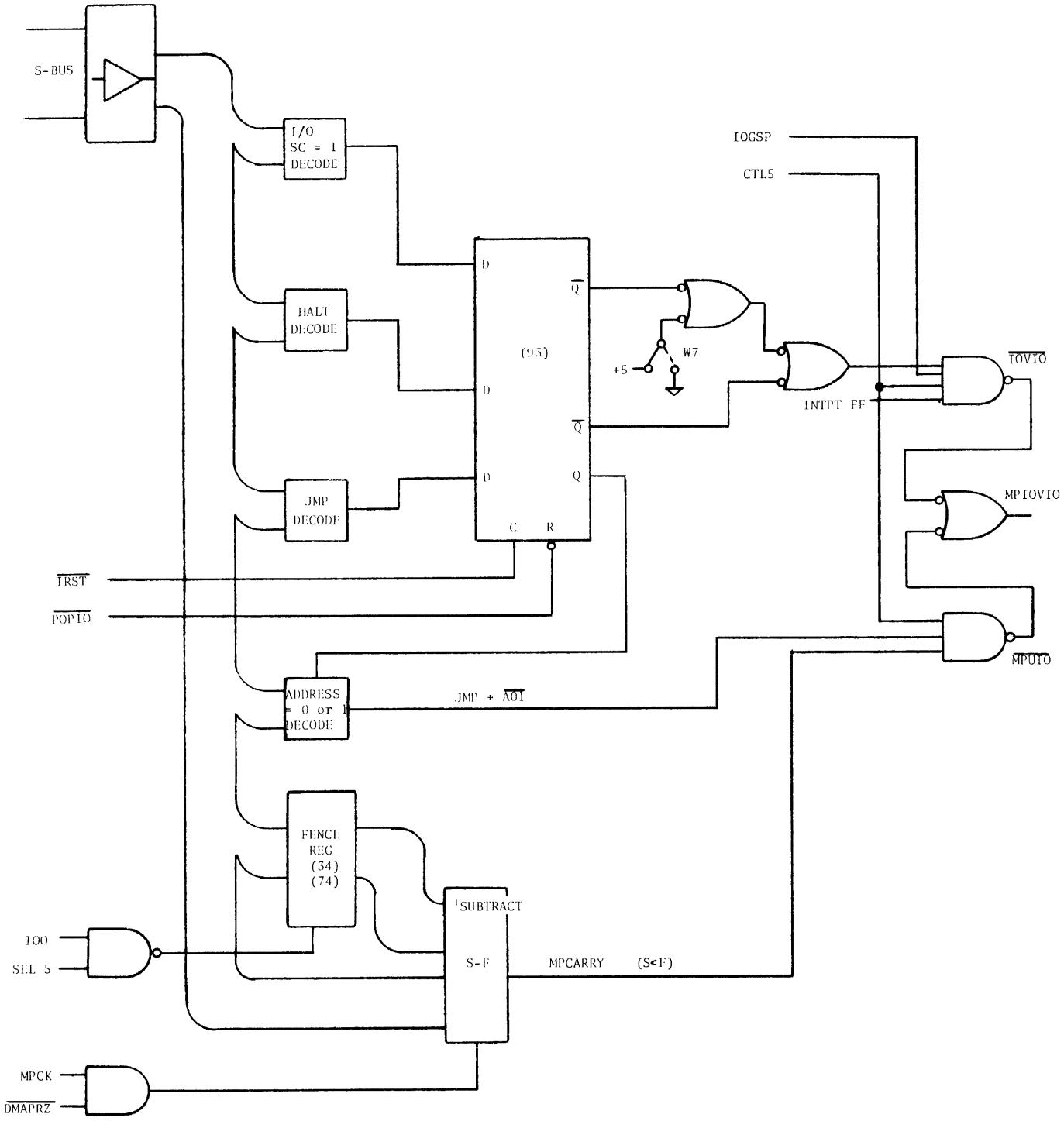


Figure 6

Violation Detection Logic

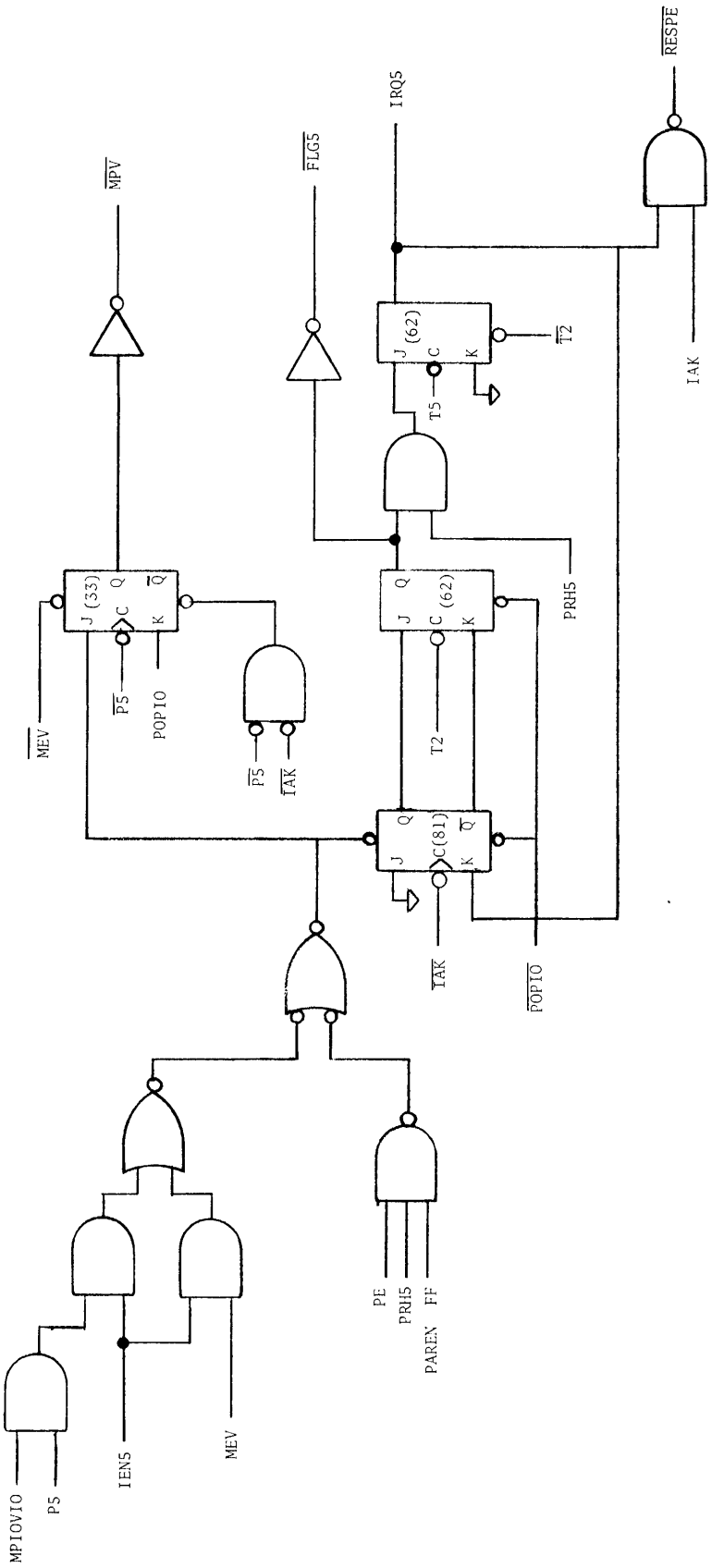


Figure 7

Interrupt and MPV Logic

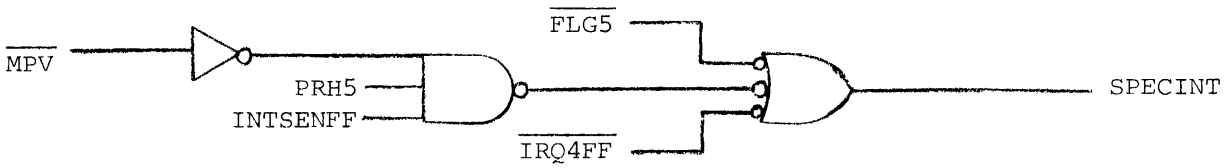


Figure 8
SPECIAL INTERRUPT LOGIC ON THE CPU

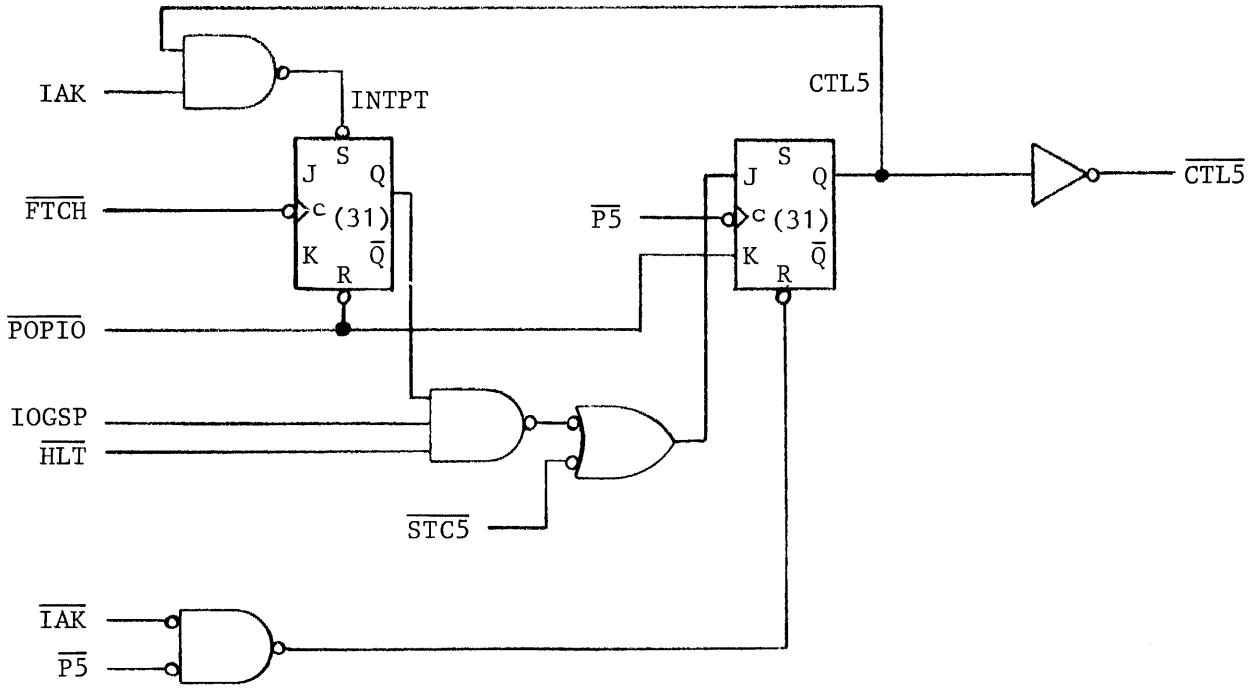


Figure 9

Interrupt Response Logic

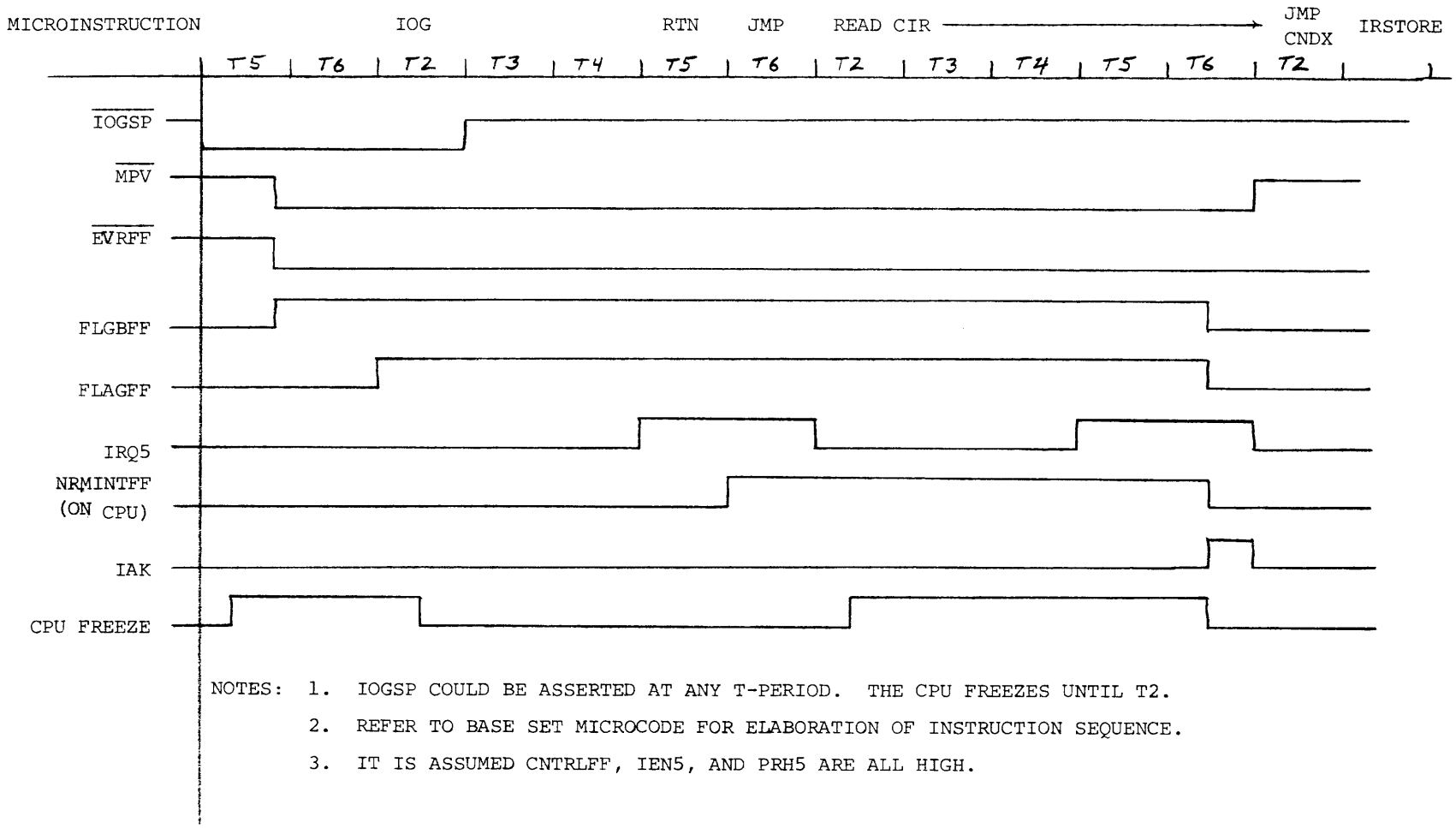
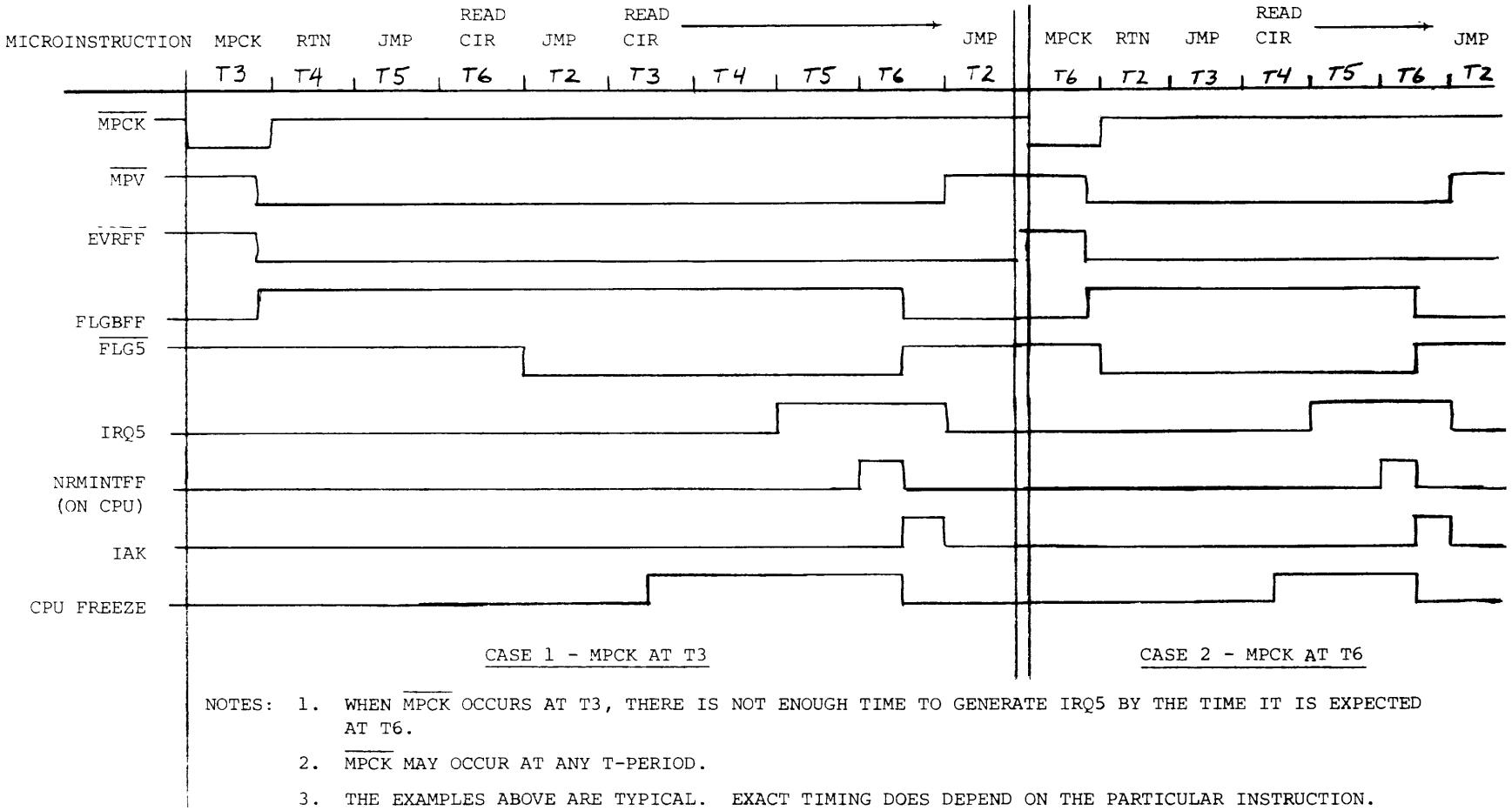


Figure 10
INTERRUPT TIMING FOR I/O VIOLATIONS



NOTES:
1. WHEN $\overline{\text{MPCK}}$ OCCURS AT T3, THERE IS NOT ENOUGH TIME TO GENERATE IRQ5 BY THE TIME IT IS EXPECTED AT T6.
2. $\overline{\text{MPCK}}$ MAY OCCUR AT ANY T-PERIOD.
3. THE EXAMPLES ABOVE ARE TYPICAL. EXACT TIMING DOES DEPEND ON THE PARTICULAR INSTRUCTION.

Figure 11
INTERRUPT TIMING FOR FENCE VIOLATIONS DURING A ST* INSTRUCTION

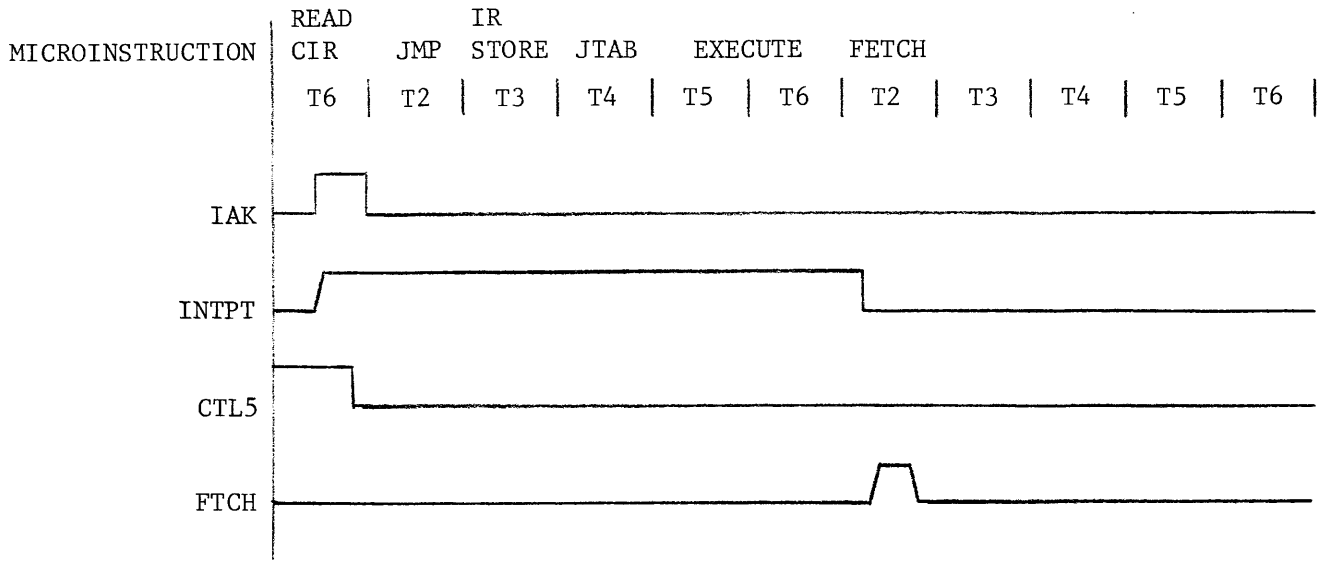


Figure 12 Non I/O Instruction in Trap Cell

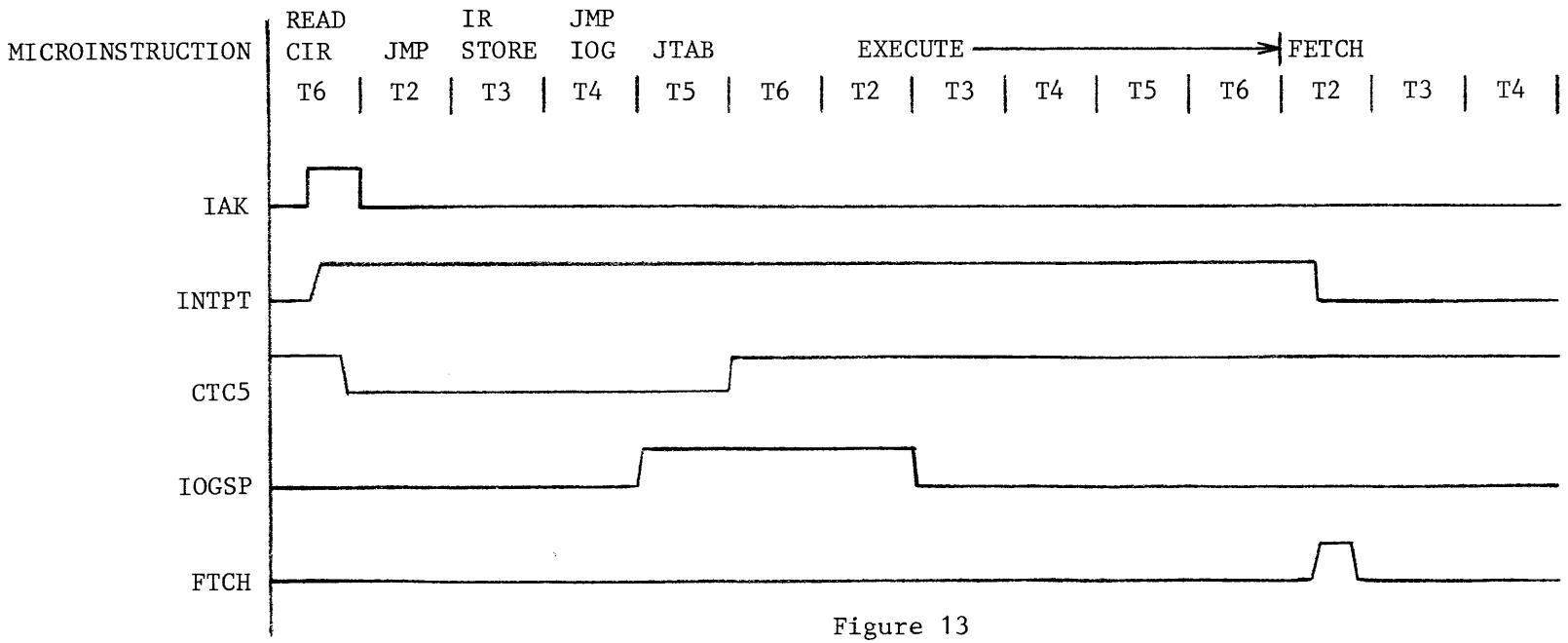


Figure 13
I/O Instruction in Trap Cell

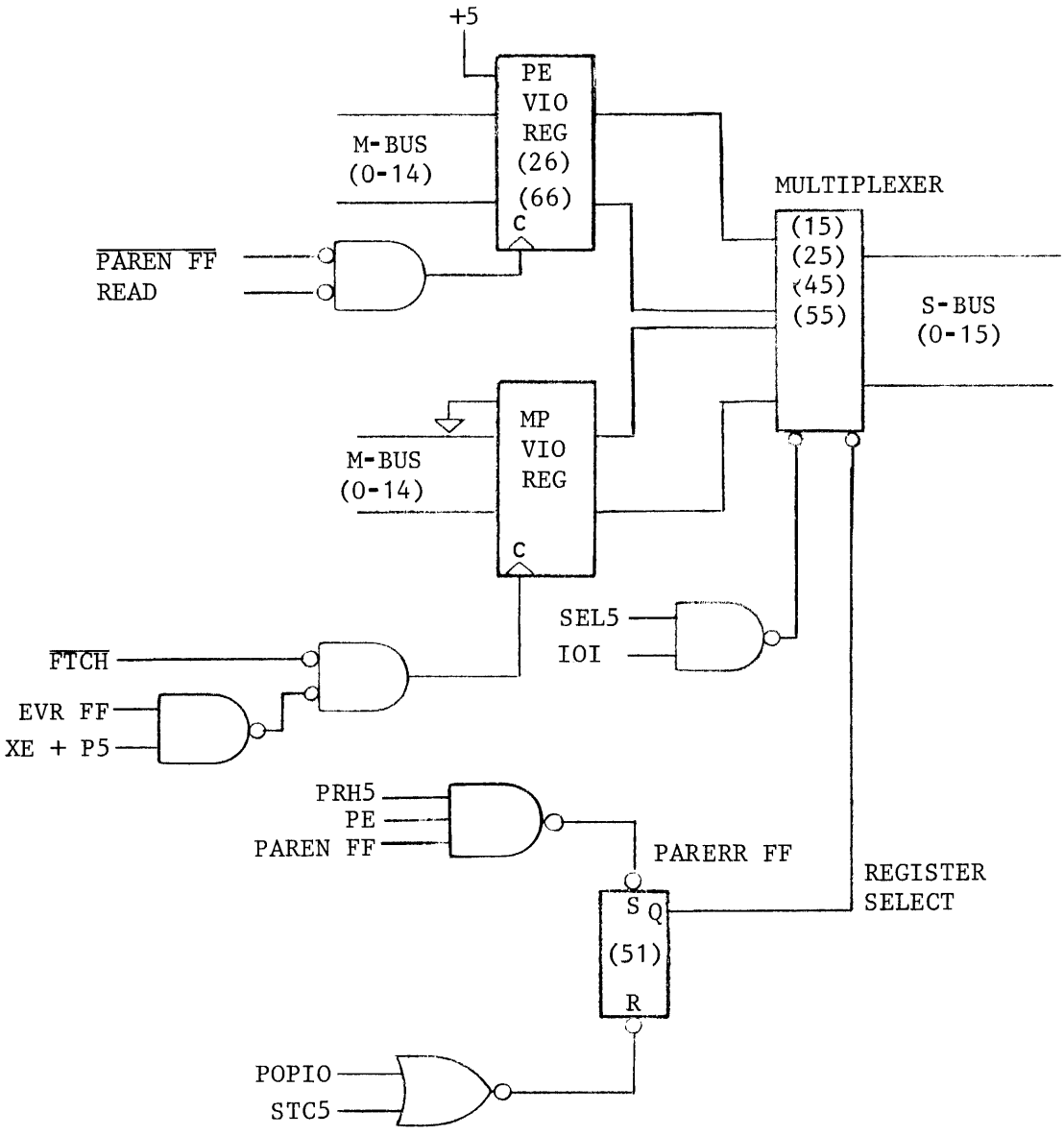
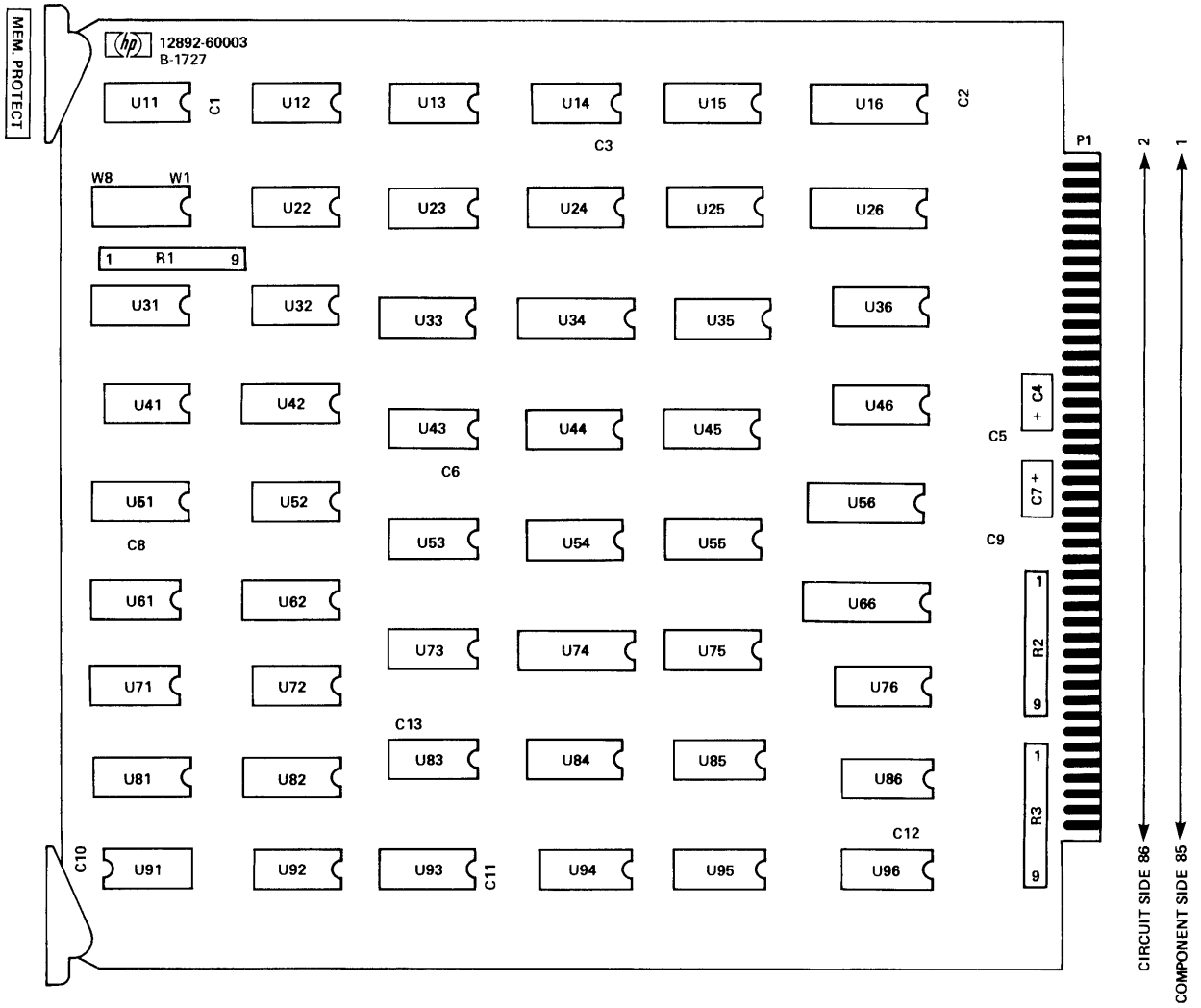


Figure 14
Violation Register Logic



12892B Memory Protect Assembly
12892-60003

12892B Memory Protect Assembly Parts List (12892-60003) Sht. 1 of 3

ITEM NO	REFERENCE DESIGNATOR FIRST SIX	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	C1-3,5,6,8-12	CAP .01UF		0160-2055		U	10
00	C13	CAP 820PF 5%		0160-3539		U	1
00	C4,7	CAP 15UF 10%		0180-1746		U	2
00	F1-3	STUD SOLDER TERM		0360-0474		U	3
		SOCKET 16 DIP LO		1200-0482		U	1
00	W4-6	JMPR PLUG .3"C-C		1258-0124		U	3
		PIN GRV .062X.25		1480-0116		U	2
00	R1-3	NETWORK-RES SIP		1810-0164		U	3
01	U33,51,81	IC SN74S112N		1820-0629		U	3
00	U53	IC SN74S00N		1820-0681		U	1
00	U43	IC SN74S04N		1820-0683		U	1
00	U11	IC SN74S10N		1820-0685		U	1
00	U14	IC SN74S64N		1820-0691		U	1
00	U82	IC 8T13B		1820-1080		U	1
00	U41	IC SN74S51N		1820-1158		U	1
00	U93	IC SN74S175N		1820-1191		U	1
01	U72,92	IC SN74LS00N		1820-1197		U	2
		IC SN74LS04N		1820-1199		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
				1820-1199			
00	U91						
		IC SN74LS08N		1820-1201		U	1
00	U71						
		IC SN74LS10N		1820-1202		U	1
00	U52						
		IC SN74LS11N		1820-1203		U	1
00	U22						
		IC SN74LS20N		1820-1204		U	1
00	U32						
		IC SN74LS30N		1820-1207		U	3
01	U85,94,95						
		IC SN74LS32N		1820-1208		U	1
00	U83						
		IC SN74LS112N		1820-1212		U	3
01	U31,42,62						
		IC SN74LS 55		1820-1284		U	1
00	U86						
		IC SN74S257N		1820-1301		U	4
01	U15,25,45,55						
		IC SN74S132N		1820-1307		U	1
00	U13						
		IC SN74S02N		1820-1322		U	2
01	U35,73						
		IC SN74S08N		1820-1367		U	3
01	U23,61,96						
		IC SN74LS85N		1820-1419		U	4
01	U24,44,54,84						
		IC SN74LS158N		1820-1428		U	4
01	U36,46,75,76						
		IC SN74S32N		1820-1449		U	1
00	U12						
		IC SN74273N		1820-1461		U	6
01 03	U16,26,34,56 66,74						
		LABEL-USA		7120-6830		L	1
		EXTRACTOR-PC		5040-6001		W	1

12892B Memory Protect Assembly Parts List (12892-60003) Sht. 3 of 3

ITEM NO	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP OPTION	LOC	QUANTITY PER
		EXTRACTOR-BLACK		5040-6068		W	1

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED (1621)	[illegible]	5/27/76
B	IAK-75 to U31 & U33-15 / U51-7 to U51-1 PER PRR E7AR	[illegible] / C.M.A	11/1/76
C	DATE CODE B-1644 thru 2458	GD	12/29/76
D	PCO-22-5806. ADD. C13, DATE CODE IS 1704	GD / [illegible]	2-8-77
E	PCO-22-6193. CIRCUIT CHG. DATE CODE IS 1727	GD / [illegible]	2-28-77

D-12892-60003-51

INDIRECT COUNTER

ICB ICA
0 0
0 1
1 0
1 1

XE ⇒ P45
XE ⇒ P3

INCI 76
IRSTF 25
FTCH 57
IAK 77
MPCR 56
JMP+A01 (F19)
MPCARRY (C20)
DMAFR2 10
IOGSP 66
HLT (G19)
SELI (F17)
STC 65
IENS 79
MEV 73
+5 39,99
GND 14,28,85,86
-2 47,48
SFS 62
SFC 82
STF 78
ENF 41
SIR 55
PRHS 81
HLTPE 17
PE 59
POPIO 74
IOO 67
CLF 80
IOI 63
READ 9
PSNF 84
SCB5 51
SCB4 34
SCB3 33
SCB1 24
SCB2 30
SCB0 22
IOG 68

SIRST (G18)
MX (A15)
IN=MX OUT=XE
"MX"
"HLTPE"
INTPT
CTL
MEVFLG
PSA
PSB
MPVIO
IOVIO
PAREN
PAR ERR
EVR
MPV
FLG BFR
FLG
IRQ
"INT"
"RME"
DMAFR2 • MPCK (A15)
JMP+A01
POPIO • STC5
T2
T5

18 MPINTON
13 CTL5
5 MPCND
2 MPVR (E11)
6 RME
14 MPV
29 FLG5
60 RESPE
83 IRQ5
75 SKF
2 POPIOA (G18)
2 PEFF (G14)
(G14) IOI5
2 PEVR (E11)

NOTE
W1, W2, U63, U64, U65
NOT ASSIGNED
ALL RESISTORS 4.7K

MEMORY PROTECT TITLE	HEWLETT PACKARD
NEXT ASSEMBLY 12892B	12892-60003 PART NUMBER
FINISH / SCALE	D-12892-60003-51 SHEET OF

STOCK NO. 5280-0004 PRINTED ON SEPO NO. 1030-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY																SEPIA
0	1	12	3	4		8		9	9		11	12	14	15		
16	17		19			21	23	26	29	30	32	34	38	43		
45	46	61	63			64										

D-12892-60003-52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED (1621)	[illegible]	5/27/76
B	DAK-PS to U31 & U33-15 / U51-7 to U51-1 PER PROCEAR	[illegible]	11/1/76
C	DATE CODE 8-1644 PER PCR 22-3628	[illegible]	12-28-76

P1

MB15 4
MB14 8
MB13 12
MB12 16
SB15 3
SB14 7
SB13 11
SB12 15
MB11 20
MB10 24
MB9 28
MB8 32
SB11 19
SB10 23
SB9 27
SB8 31
MB7 37
MB6 42
MB5 46
MB4 50
SB7 35
SB6 38
SB5 45
SB4 49
MB3 52
MB2 54
MB1 61
MB0 72
SB3 53
SB2 58
SB1 64
SB0 71

DMAFR2-MPCK (B9)
MX (B2)
U96 S08

U46 U36 U75 U74 U45 U55 U15 U25 LS157

U24 U44 U54 U74 U84 LS85

FENCE REGISTER
U34 74273

I005 (F3)
U14 S04
U48 S04
MPCARRY (C2)

FENCE < ADDRESS ⇒ ADDRESS < FENCE
A < B B < A

MEMORY PROTECT VIOLATION REGISTER
U16 74273
U56 74273
U26 74273
U66 74273
PARITY VIOLATION REGISTER

MPVR (C9)
PEVR (G9)
I015 (G9)
PEFF (F9)

U73 S02
U85 LS30
U94 LS30
U95 LS30
U83 LS32
JMP + A01 (C2)
U93 S175
U53 S00
SEL1 (D2)
HLT (C2)
R1-1
W7 "SEL1"
IN = PERMIT I/O TO ALL SELECT CODES
OUT = PERMIT I/O ONLY TO SELECT CODE 1

U49 JMP
U86 LS32
JSB
U96 S08
POFIOA (F9)
SIRST (A9)
R1-3
W5 "JSB"
IN = PERMIT JSB TO ϕ/1
OUT = INHIBIT JSB TO ϕ/1

NOTE
W1, W2, U63, U64, & U65 NOT ASSIGNED
ALL RESISTORS 4.7K

TITLE: MEMORY PROTECT	HEWLETT PACKARD
NEXT ASSEMBLY: 12892 B	PART NUMBER: 12892-60003
FINISH / SCALE	D-12892-60003-52
SHEET OF	

STOCK NO 9280-0004 PRINTED ON DIEPO NO 1030-10 CLEARPRINT FADEOUT