HONEYWELL EDP

GENERAL SYSTEM:

SERIES 200 PROGRAMMING

SUBJECT:

1410/7010 Liberation, The Virtually Automatic
Means Whereby Users of Competitive Systems
Can Obtain The Benefits of Third Generation
Series 200 Dimensional Data Processing. This
Bulletin Describes The Advantages of Libera-
tion Over Other Transition Methods, Supplies
The Supporting Theoretical Framework, and
Provides Comparison Data From Actual
Experience.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I
ADVANTAGES OF LIBERATION

Liberator is a proven Honeywell concept for elevating users of older systems to third-generation Series 200 dimensional data processing. Liberator provides fast, reliable, and low-cost transition from the 1410/7010 to a Series 200 environment consisting of a Model 1200, 2200, or 4200 running under control of the Operating System - Mod 2. The key to the success of Liberator is compatibility of hardware, software, data files, and operating environments within the larger framework of Series 200. The 1410/7010 user is freed from reprogramming, reconstructing files, redesigning systems, and retraining personnel. Many 1410/7010 source programs and control cards are acceptable to the Mod 2 Operating System as written. 1410/7010 Autocoder language is a fully compatible subset of Mod 2 assembly language. However, some hardware dissimilarities between the 1410/7010 and the Series 200 result in differences between Mod 2 assembly-language programs and 1410/7010 Autocoder programs. The Mod 2 Operating System includes a transition program, Easytran J, which automatically resolves hardware differences at the assembly-language level.

Liberated programs take full advantage of improved Series 200 hardware with a dramatic increase in throughput performance. For example, the Model 1200 executes 1410 programs 1.9 times as fast as the 1410. Model 2200 executes 1410 programs 2.8 times as fast as the 1410 and twice as fast as the System 360/40 could emulate the same programs. After a massive and laborious reprogramming effort to convert 1410 files and programs to 360/40 files and programs, the System 360 would execute the converted programs at approximately the same speed as Model 2200 executes the original programs. Model 4200 executes 7010 programs three times as fast as the 7010, and three times as fast as the System 360/50 could emulate the same programs. Model 4200 still executes the original 7010 programs about 1.4 times as fast as completely rewritten programs would run on the 360/50.

In addition to the increased throughput realized from faster Series 200 hardware, the design of the Operating System - Mod 2 enhances the efficiency of total system operation. The Mod 2 Operating System offers not only superior performance of the functions available in the 1410/7010 Operating System, but also many advanced capabilities not present in the 1410/7010 system. For example, the MGO system file in the 1410/7010 Operating System is constructed with 80-character records. In other words, for every 0.1 inch of data on tape there is 0.75 inch of wasted interrecord gap space. In the Mod 2 Operating System, the same file is constructed with

1600-character blocked records. This higher information density and the use of the Honeywell read-backward feature result in reduced file access time and correspondingly faster operation of the Mod 2 Operating System.

In addition, the Mod 2 Operating System offers third-generation data control facilities and multiprogramming capabilities for total and flexible utilization of the Series 200 processor and peripherals. Built into the advanced System Maintenance component of the Mod 2 Operating System is the ability to produce standard input tapes containing control cards, source programs, and object data. With this powerful feature, the Mod 2 user realizes the full potential of his third-generation operating system through the continuous processing of a stacked-job input stream. This feature eliminates most control-card handling by the operator and reduces setup time to an absolute minimum.

Thus liberation relocates the 1410/7010 user from a limited environment to the open-ended Series 200 with orderly growth potential in both hardware and software dimensions. This report first examines the factors responsible for the ease and simplicity of 1410/7010 liberation: in-depth hardware, software, data file, and operating environment compatibility and the Easytran J automatic transition program. Next, quantitative predictions of throughput performance are established for Models 1200, 2200 and 4200, and for System 360/40 and 360/50. Finally, statistics are recounted from an actual demonstration which verified the relative throughput predictions developed for the 1410, the Model 2200, and 1410 emulation on the 360/40.

SECTION II

EASY TRANSITION TO THE MOD 2 OPERATING SYSTEM

HARDWARE COMPATIBILITY

The 1200/2200/4200 instruction repertoire includes 110 of the 1410/7010 machine instructions in identical form. Only three 1410/7010 machine instructions are not available in Models 1200/2200/4200: CS, CS and Branch, and MCS. The Easytran J transition program automatically replaces each of these instructions with two or three in-line instructions. Note that the physical input/output instructions are not included in the 113 machine instructions considered above. The use of I/O operation codes is restricted in both the 1410/7010 Operating System and the Mod 2 Operating System, as all input/output operations are logically programmed through the resident input/output control systems.

DATA FILE COMPATIBILITY

The exact 1410/7010 magnetic tape file structure is acceptable to the Mod 2 Operating System. Data file compatibility includes:

1. Character codes
2. Record formats
3. Block formats
4. Tape-marking conventions
5. Structure, content, and handling conventions for tape labels.

SOFTWARE COMPATIBILITY

Autocoder

The entire 1410/7010 Operating System Autocoder assembly language is a fully compatible subset of the Mod 2 Operating System assembly language.

COBOL

The entire 1410/7010 Operating System COBOL compiler language is a fully compatible subset of the Mod 2 Operating System COBOL compiler language. All 1410/7010 COBOL programs compile under the Mod 2 Operating System without modification to a single source or control card, including the PROGRAM-ID card and the entire Environment Division.

Tape Sort

The entire 1410/7010 Operating System Tape Sort language and functions are a fully compatible subset of the Mod 2 Operating System Tape Sort language and functions. Control cards for

the 1410/7010 Tape Sort need not be changed to perform the identical sort/merge functions under the Mod 2 Operating System.

Basic Input/Output Control System (IOCS)

The 1410/7010 Operating System IOCS language and functions are a fully compatible subset of the Mod 2 Operating System input/output control language and functions.

Resident Monitor, Transitional Monitor, and Linkage Loader

The entire 1410/7010 Operating System Resident Monitor, Transitional Monitor, and Linkage Loader language and functions are a fully compatible subset of the Mod 2 Operating System Resident Monitor, Transitional Monitor, and Linkage Loader language and functions.

The performance of these components has been improved in the Mod 2 Operating System by a reduction in the number of control cards required, by optimum blocking of system files, and by extensive utilization of the magnetic tape read-backward feature. Both setup time and program access time are minimized.

EASYTRAN J TRANSITION PROGRAM

Four hardware dissimilarities between the 1410/7010 and the Series 200 introduce differences between 1410/7010 Autocoder programs and Mod 2 assembly-language programs, despite the complete compatibility of the two assembly languages. Easytran J automatically resolves these minor hardware differences, namely:

1. Addressing. The 1410/7010 uses decimal addressing digits and decimal address modification. Series 200 uses binary addressing digits and binary address modification. Address length is five characters in a 1410/7010 and four characters in a 1200/2200/4200. The addressing range in the 1410/7010 is 0 to 99999 (decimal). The addressing range of the 1200/2200/4200 is 0 to 262,144 (decimal).

2. Indexing. In a 1410/7010 address, indexing is indicated by B and A bits over the tens and hundreds positions of the address. In a 1200/2200/ 42000 address, indexing is indicated in the high-order five bits of the address. Because of the difference between decimal and binary addressing, index registers are loaded and modified differently in the 1410/7010 and the 1200/2200/4200. The 1410/7010 index registers are each five characters long and occupy memory locations 25 through 99 (decimal). The 1200/2200/4200 index registers are each four characters long and occupy memory locations 2 to 60 (decimal). Index register values in the 1410/7010 may be either positive or negative, and the sign may be reversed with an MLZS instruction. No sign bit is associated with index register values in the 1200/2200/4200.

3. Instruction Repertoire. Easytran J substitutes in-line code for the three 1410/7010 instructions not available in Models 1200/2200/4200. The MCS instruction is translated to two instructions: MLCWA, MCE. The CS instruction is translated to: MLCWA, CW. The CS and Branch instruction is translated to: MLCWA, CW, B.

4. Character Codes. Collating sequence for the 1410/7010 is external BCD. Collating sequence for the 1200/2200/4200 is internal binary.

Although the 1410/7010 and 1200/2200/4200 character codes are identical on magnetic tape, some characters are translated on input/output and have different internal equivalents.

Approximately ninety-five percent of all 1410/7010 Autocoder symbolic cards are translated directly to Mod 2 assembly language. The remaining five percent are flagged, Easytran J applies a default translation, and programmer hand-tailoring is sometimes indicated. An average of only one out of five flagged instructions actually requires hand-tailoring; the other flagged instructions require only verification of the default translation.

Easytran J includes an object-time package which is used by translated programs at execution time. The object-time package occupies only about 2,000 characters of memory, a fraction of the 25,000-byte overhead which is necessary for emulation on System 360. The Easytran J object-time package includes some routines and constants for binary/decimal conversion, masks for MCS operations, and constants for CS operations. Because the address lengths in a translated program have all been reduced from five to four characters, the total increase in object-program memory size is less than the 2K overhead.
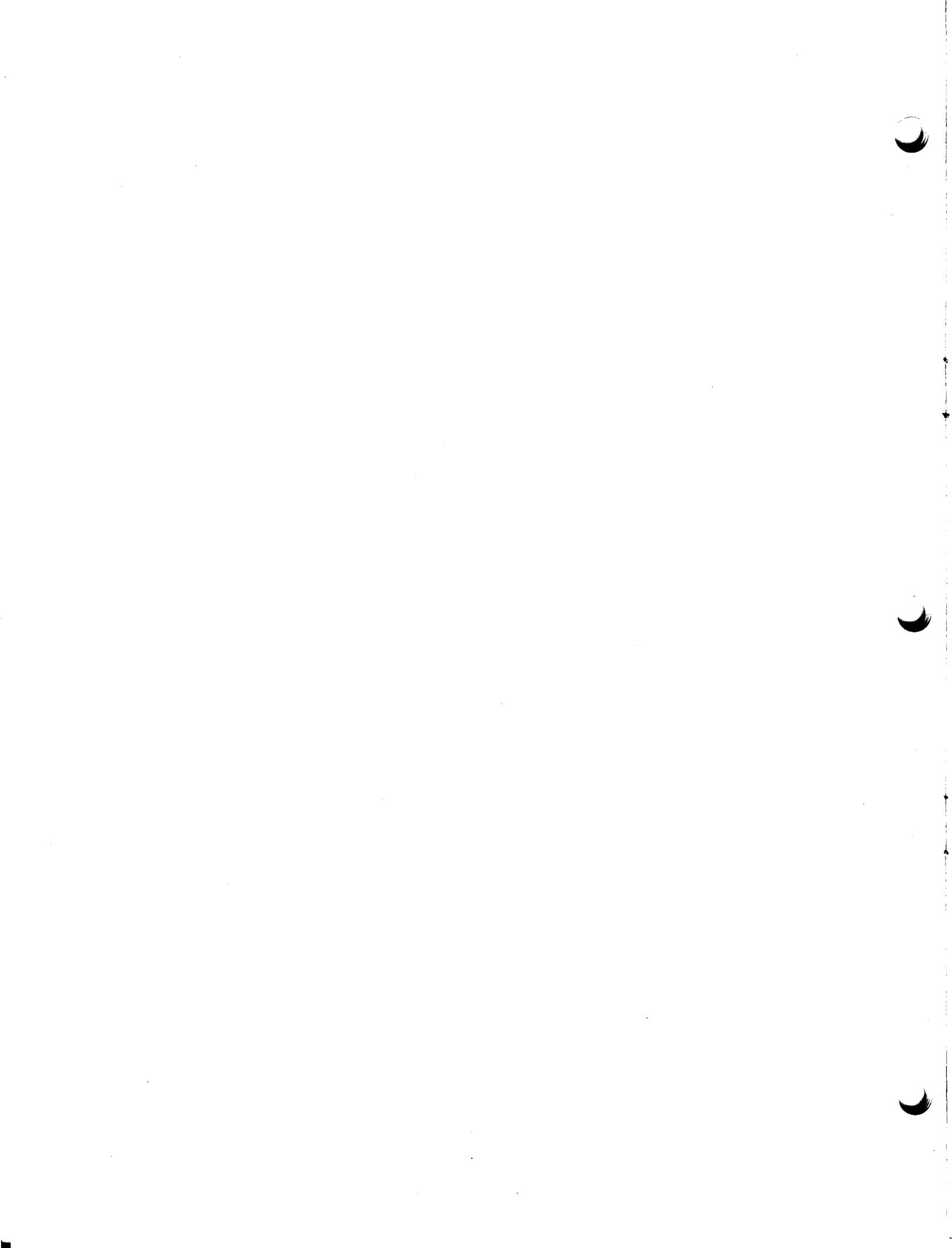
SECTION III

THROUGHPUT PERFORMANCE ANALYSIS

This analysis examines the relative throughput performance of the 1410, 7010, Models 1200/2200/4200, 360/40, and 360/50. Predictions of throughput performance are calculated on the basis of internal speeds, using an empirical ratio between internal and throughput speeds. This analytical method is invalid for peripherally limited programs but has been verified for the relevant high-speed, tape-oriented environments of the 1410/7010 and Mod 2 Operating Systems.

Table 3-1 shows the relative internal and throughput performance of the 1410, 7010, 1200, 2200, 4200, 360/40, and 360/50. The basis of comparison is the speed of the 1410. Thus, the internal performance column represents the number of times as fast as the 1410 that each processor performs the same internal operations. The throughput performance column represents the number of times as fast as the 1410 that each processor executes the same program.

Table 3-1. Internal and Throughput Performance

Processor	Internal Performance (Times as Fast as 1410)	Throughput Performance (Times as Fast as 1410)
1410 Execution	1	1
7010 Execution	3.5 (A)	2.5 (A)
1200 Execution	2.7 (E)	1.9 (*)
2200 Execution	4 (E)	2.8 (*)
4200 Execution	10.5 (E)	7.5 (*)
360/40 Emulation	2 (P)	1.4 (*)
360/50 Emulation	3 (P)	2.1 (*)
360/40 Execution	3.8 (E)	2.7 (*)
360/50 Execution	7.6 (E)	5.5 (*)

NOTES:
1. (A) = Experience Statistic
2. (P) = Published IBM Figure
3. (E) = Estimated from instruction timings
4. (*) = Calculated from 1410/7010 ratio of internal-to-throughput speeds.

The derivation of each number in the table is explained below, and the conclusions of the throughput analysis are summarized. An exhibit is presented which documents actual throughput performance for three 1410 programs which were liberated and executed on the Model 2200

and emulated on the 360/40. The results of this demonstration not only verify the data developed in Table 3-1 but also exceed the original prediction of the throughput advantage of the Model 2200.

INTERNAL PERFORMANCE

The internal performance figure for the 7010 relative to the 1410 (3.5 times as fast) is an experience statistic. As explained below, the internal and throughput experience figures for the 7010 give an internal-to-throughput ratio which is applied to the remaining internal performance figures to calculate throughput performance.

The internal performance figures for emulation on 360/40 and 360/50 relative to the 1410 are published IBM statistics from IBM System/360, Model 40 Emulation of the IBM 1410/7010 Data Processing Systems (Form C28-6563) and IBM System/360, Model 50 Emulation of the IBM 1410/7010 Data Processing Systems (Form C28-6568).

The internal performance figures for Models 1200/2200/4200 and for execution on 360/40 and 360/50 are estimates based on a detailed study of internal instruction timings. All 1410/7010 machine instruction timings and the corresponding 1200/2200/4200 timings are presented in Appendix A, which also includes timings for executing equivalent instructions on System 360. It should be noted that the statistics for execution on System 360 do not provide a rigorous comparison with the 1410/7010, because of total incompatibility in order structure between 1410/7010 and System 360. The emulation timings in Appendix A are based on the published ratios of 2 and 3 mentioned above, and are included for reference only. From the data in Appendix A, the statistical distribution of 1200, 2200, 4200, 360/40 (execution) and 360/50 (execution) instruction timings relative to the corresponding 1410 instruction timings are plotted in Figures 3-1 through 3-5. These graphs illustrate the internal performance figures given in Table 3-1.

THROUGHPUT PERFORMANCE

In the high-speed tape-oriented environments under consideration, throughput performance is directly related to internal performance. The throughput performance figure for the 7010 relative to the 1410 (2.5 times as fast) is an experience statistic. One example is the 1410/7010 Operating System COBOL compiler. Compile times are approximately 250 cards per minute on a tape 1410 and 600 cards per minute on a tape 7010, giving a 1410/7010 throughput ratio of 1 to 2.4. Another example is the 1410/7010 Operating System Autocoder Assembler, which assembles about 300 cards per minute on a tape 1410 and about 700 cards per minute on a tape 7010. Here the 1410/7010 throughput ratio is 1 to 2.33. Three calculations of sort timings, using the formulas in the IBM 1410/7010 Operating System Generalized Tape Sorting Program manual (Form C28-0354), give 1410/7010 throughput ratios of 1 to 2.8, 1 to 2.23, and 1 to 3.3.
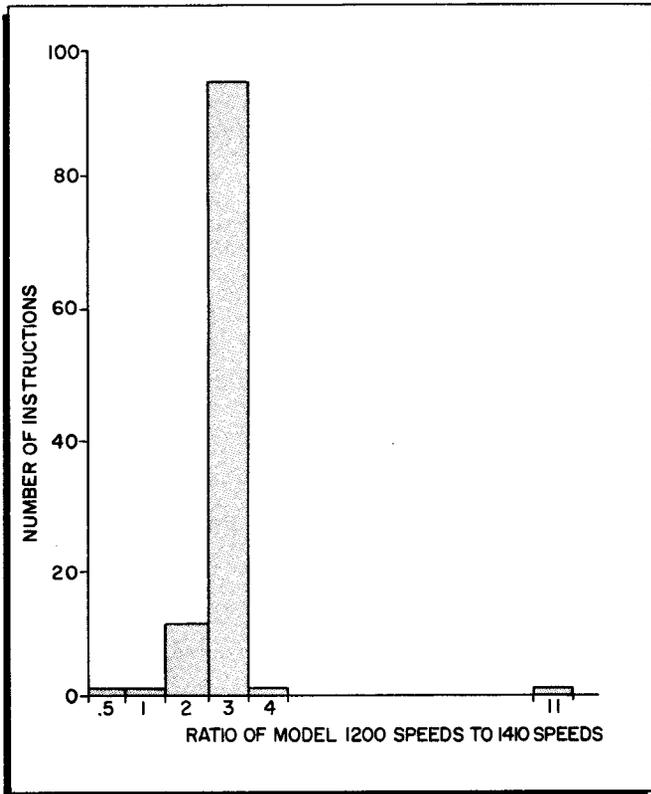
Figure 3-1. Comparison of Model 1200
and 1410 Instruction Timings
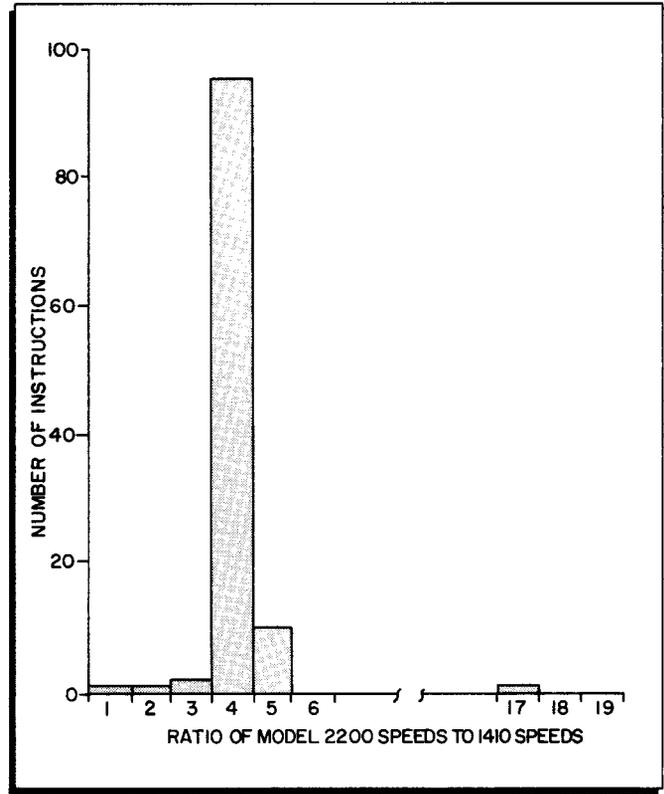
Figure 3-2. Comparison of Model 2200
and 1410 Instruction Timings
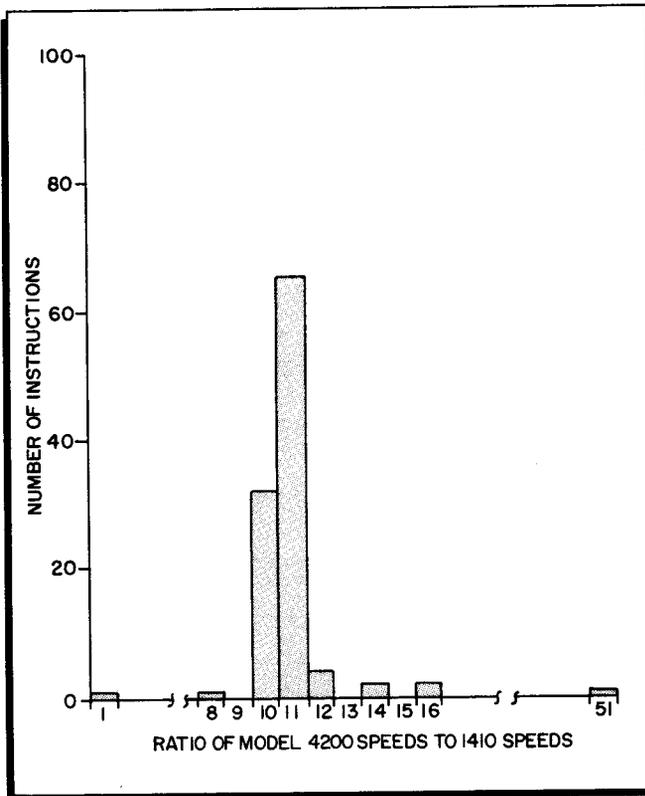
Figure 3-3. Comparison of Model 4200
and 1410 Instruction Timings
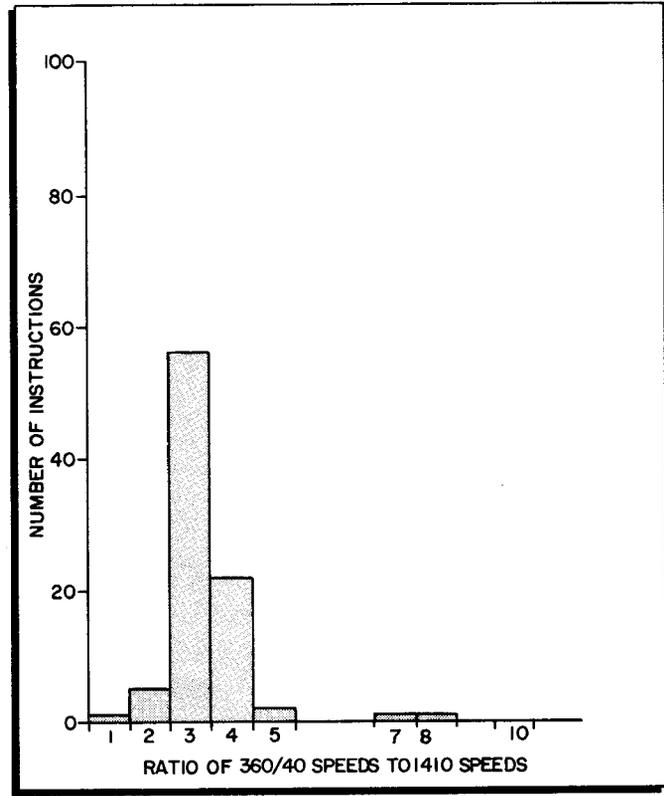
Figure 3-4. Comparison of 360/40 (Execution)
and 1410 Instruction Timings
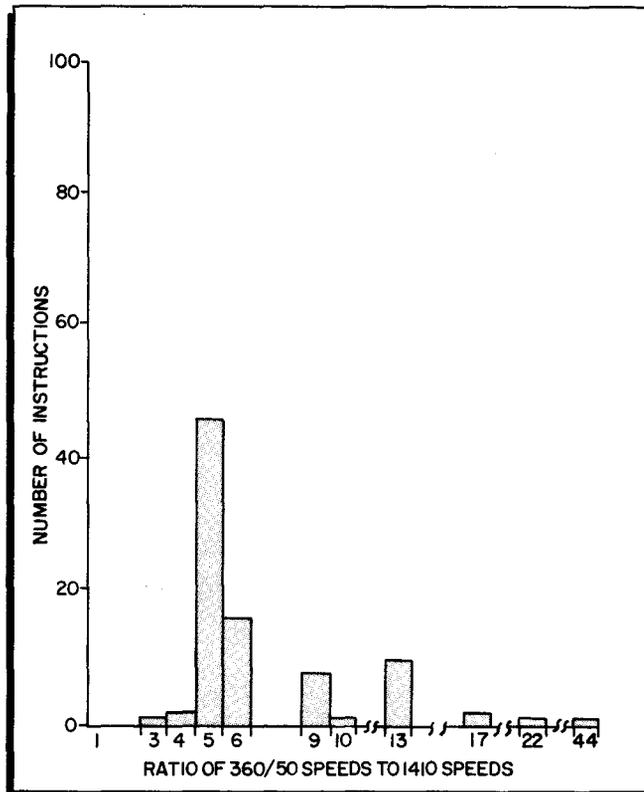
Figure 3-5. Comparison of 360/50
(Execution) and 1410 Instruction Timings

The experience statistics for internal performance and throughput performance of the 7010 relative to the 1410 establish an internal-to-throughput ratio of 3.5/2.5, or 1.4. This ratio is applied to the internal performance figures derived above to determine the throughput performance figures (relative to the 1410) in Table 3-1.

CONCLUSIONS

Referring to Table 3-1, approximate throughput predictions for high-speed tape-oriented environments are:

1. Model 1200 throughput performance should exceed 1410 performance by a factor of about 1.9.

2. Model 2200 throughput performance should exceed 1410 performance by a factor of roughly 2.8.

3. Model 2200 throughput performance should exceed emulation performance on the 360/40 by a factor of about two.

4. Model 2200 throughput performance should roughly equal the performance of the 360/40 running rewritten programs.

5. Model 4200 throughput performance should exceed 1410 performance by a factor of about 7.5.

6. Model 4200 throughput performance should exceed 7010 performance by a factor of roughly 3.

7. Model 4200 throughput performance should also exceed emulation performance on the 360/50 by a factor of about 3.

8. Model 4200 throughput performance should exceed the performance of the 360/50 running rewritten programs by a factor of about 1.4.

EXHIBIT: ACTUAL THROUGHPUT PERFORMANCES OF THE 1410, 2200, and EMULATION ON 360/40

For this demonstration, three 1410 Autocoder programs were run under the 1410/7010 Operating System on a tape-oriented 1410 equipped with the accelerator and two I/O channels. The same three programs were emulated on the System 360/40, and liberated and run under the Mod 2 Operating System on Model 2200. Program characteristics are summarized in Table 3-2. The observed running times are presented in Table 3-3.

Table 3-2. Program Characteristics for Throughput Demonstration

	Lines of Coding	Memory Required on 1410 (char.)	Memory Required on 2200 (char.)	Memory Required on 360/40 (bytes)	No. Modules	No. Phases	No. Files
Program #1	1483	40K	49K	65K	2	1	7
Program #2	1647	40K	49K	65K	3	1	4
Program #3	1875	40K	49K	65K	4	3	4

Table 3-3. Running Times in Throughput Demonstration

	Running Time on 1410 with Accelerator and Two I/O Channels	Running Time on S/360/40 Emulating 1410	Running Time on 2200-Mod 2 Operating System
Program #1	13.00 min.	8.55 min.	4.25 min.
Program #2	30.48 min.	20.67 min.	11.25 min.
Program #3	39.43 min.	30.00 min.	14.66 min.
Totals	82.91 min.	59.22 min.	30.16 min.

The results are:

1. Execution of liberated 1410 programs under the Mod 2 Operating System on Model 2200 was 1.96 times as fast as emulation of the original programs on the 360/40. The theory developed in the preceding section predicts that Model 2200 is twice as fast.

2. Program execution on Model 2200 was 2.74 times as fast as the 1410

with the accelerator and two I/O channels. This result actually surpasses
the predicted improvement factor of 2.8, as the 1410 with the accelerator
should itself demonstrate up to a 20 percent throughput increase over a
basic 1410.

SUMMARY QUESTIONS AND ANSWERS

1.   What are the advantages of transition to the Mod 2 Operating System from the

1410/7010 Operating System?

> *Reduced file-access time heightens the operating efficiency of
> the Mod 2 Operating System. Fewer control cards and the
> ability to produce standard system input tapes minimize setup
> time. In addition, the Mod 2 Operating System offers multipro-
> gramming capabilities and third-generation data control facilities.

2.   What characteristics of the Mod 2 Operating System and Models 1200/2200/4200

make 1410/7010 liberation virtually automatic?

> *Hardware compatibility, software compatibility, data file
> compatibility, operating environment compatibility, and
> the Easytran J transition program.

3.   Why is liberation to Series 200 superior to reprogramming for System/360?

> *Elimination of reprogramming, reconstructing files, and re-
> training personnel make 1410/7010 liberation both fast and inex-
> pensive.

4.   Why do liberated programs demonstrate improved throughput performance, com-

pared to corresponding 1410/7010 execution speeds and System 360 emulation

speeds?

> *Liberated programs take full advantage of third-generation
> Series 200 hardware with an immediate and dramatic increase
> in throughput. The theoretical analysis in Section III predicts
> that Model 2200 throughput performance should exceed the perform-
> ance of a basic 1410 by a factor of about 2.8 and should exceed
> 360/40 emulation performance by a factor of about 2. The actual
> performance demonstration documented in Section III shows that
> Model 2200 executed liberated 1410 programs 2.74 times as fast
> as a 1410 with two I/O channels and the accelerator and 1.96
> times as fast as emulation of the original programs on the
> 360/40.

5.   How does liberation support a 1410/7010 user's aspirations for future advance-

ments in data processing?

> *Liberation to Series 200 provides the means for orderly growth
> into more comprehensive and more advanced applications.

APPENDIX A

TABLE COMPARING 1410/7010, SERIES 200 AND SYSTEM 360

INSTRUCTION SIZES AND EXECUTION TIMES

A-2

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
A (1 field)	6	5	87.7	26.4	34	23	8.7	44	29	AP(6)	40.6	20
A (2 fields)	11	9	110.2	32.4	40	27	9.4	55	37	AP(6)	40.6	20
BAV	7	6	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BBE	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BCE	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BE	7	5	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BH	7	6	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BL	7	7	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BU	7	6	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BDV	7	6	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BZ	7	6	40.5	10.8	13.5	9	3.7	20	13	BC(4)	9.38	3.0
BW	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BWZ	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BWZ (A)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BWZ (AB)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BWZ (B)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BZN	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BZN (A)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BZN (AB)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
BZN (B)	12	10	69.7	19.2	22	15	5.7	35	23	2 Inst(8)	18.76	7.5
B	7	5	40.5	10.8	10	7	3.7	20	13	BC(4)	9.38	4.0

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
CS	6	N/A	256.5	91.2	N/A	N/A	N/A	128	85	N/A	N/A	N/A
CS (Branch)	11	N/A	279.0	97.2	N/A	N/A	N/A	140	93	N/A	N/A	N/A
CW (1 field)	6	5	45.0	16.0	13.5	9	4.2	22	15	N/A	N/A	N/A
CW (2 fields)	11	9	67.5	22.0	19	13	4.8	34	22	N/A	N/A	N/A
C	11	9	99	33.6	34	23	8.7	49	33	CLC(6)	29.68	15.25
D	11	9	2315.6	750.6	200	134	44.0	1162	772	DP(6)	308.48	52.74
H	1	1	4.5	4.8	8	5	4.2	2.3	1.5	N/A	N/A	N/A
H (Branch)	6	5	36.0	9.6	13.5	9	4.2	18	12	N/A	N/A	N/A
LE	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
LEH	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
LH	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
LL	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
LLE	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
LLH	12	10	396.0	134.4	146	97	38	198	132	N/A	N/A	N/A
MCE	11	9	110.25	43.6	39	26	10.5	2205	1543	ED(6)	43.06	22.28
MCS	11	N/A	144.0	32.4	N/A	N/A	N/A	2880	2016	N/A	N/A	N/A
MLCWS	12	10	69.7	22.4	22	15	6	35	23	MVC(6)	18.75	12.46
MLCWA	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MLCWB	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MLCW	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MLCS	12	10	69.7	22.4	22	15	6	35	23	MVC(6)	18.75	12.46
MLCA	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MLCB	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
MLC	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MLNWS	12	10	69.7	22.4	22	15	6	35	23	MVN(6)	19.38	13.96
MLNWA	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLNWB	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLNW	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLNS	12	10	69.7	22.4	22	15	6	35	23	MVN(6)	19.38	13.96
MLNA	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLNB	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLN	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MLWS	12	10	69.7	22.4	22	15	6	35	23	MVZ(6)	19.38	13.96
MLWA	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLWB	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLW	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZWS	12	10	69.7	22.4	22	15	6	35	23	MVZ(6)	19.38	13.96
MLZWA	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZWB	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZW	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZS	12	10	69.7	22.4	22	15	6	35	23	MVZ(6)	19.38	13.96
MLZA	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZB	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MLZ	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRCWG	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98

A-4

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
MRCWR	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRCWM	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRCW	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRCG	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRCR	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRCM	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRC	12	10	114.7	33.6	40	27	10	57	38	MVC(6)	28.75	16.98
MRNWG	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNWR	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNWM	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNW	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNG	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNR	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRNM	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRN	12	10	114.7	33.6	40	27	10	57	38	MVN(6)	34.38	20.48
MRWG	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRWR	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRWM	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRW	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRZWG	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRZWR	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRZWM	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48
MRZW	12	10	114.7	33.6	40	27	10	57	38	MVZ(6)	34.38	20.48

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
MRZG	12	10	114.7	33.6	40	27	10	57	38	MVZ (6)	34.38	20.48
MRZR	12	10	114.7	33.6	40	27	10	57	38	MVZ (6)	34.38	20.48
MRZM	12	10	114.7	33.6	40	27	10	57	38	MVZ (6)	34.38	20.48
MRZ	12	10	114.7	33.6	40	27	10	57	38	MVZ (6)	34.38	20.48
M	11	9	1051.6	366.6	300	200	100	525	350	MP	136.67	46.75
NOP	1	1	9.0	3.6	6	4	3.3	4.5	3	BC	9.38	3.0
SCNLS	12	10	69.7	22.4	22	15	6	35	23	N/A	N/A	N/A
SCNLA	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNLB	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNL	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNRG	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNRR	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNRM	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SCNR	12	10	114.7	33.6	40	27	10	57	38	N/A	N/A	N/A
SW (1 field)	6	5	45.0	16.0	13.5	9	4.2	22	15	N/A	N/A	N/A
SW (2 fields)	11	9	67.5	22.0	19	13	4.8	33	22	N/A	N/A	N/A
SAR	7	6	69.7	20.4	21	14	4.2	35	23	ST (4)	12.5	4.0
SBR	7	6	69.7	20.4	21	14	4.2	35	23	ST (4)	12.5	4.0
S (1 field)	6	5	87.7	26.4	34	23	8.7	43	29	SP (6)	40.6	20
S (2 fields)	11	9	110.2	32.4	40	27	9.4	55	37	SP (6)	40.6	20
ZA (1 field)	6	5	87.7	26.4	24	16	7.2	43	29	ZAP (6)	33.12	16.25

INSTRUCTION	1410/ 7010 Instr. Size (Chars)	1200/ 2200/ 4200 Instr. Size (Chars)	1410 Instr. Exec. Time (usec)	7010 Instr. Exec. Time (usec)	1200 Instr. Exec. Time (usec)	2200 Instr. Exec. Time (usec)	4200 Instr. Exec. Time (usec)	Approx. 360/40 Emulate Instr. Exec. Time (usec)	Approx. 360/50 Emulate Instr. Exec. Time (usec)	Equiv. 360 Inst. and Size in Bytes	Equiv. 360/40 Instr. Exec. Time (usec)	Equiv. 360/50 Instr. Exec. Time (usec)
ZA (2 fields)	11	9	110.2	32.4	30	20	7.8	55	37	ZAP(6)	33.12	16.25
ZS (1 field)	6	5	87.7	26.4	24	16	7.2	43	29	N/A	N/A	N/A
ZS (2 fields)	11	9	110.2	32.4	30	20	7.8	55	37	N/A	N/A	N/A
INDEXING/ ADDRESS			34.5	9.6	9	6	3	15	11	BASE REGISTER ADJUSTMENT (VARIABLE)		

NOTES:

1. All 1200/2200/4200 addresses are assumed to be four characters long.

2. All data fields are assumed to be five characters or digits long, except for the fixed one-character fields.

3. No floating or suppressing is included for edit timing.

4. Fifty characters are cleared for clear storage timing.

5. Five table arguments are compared for table lookup timing.

6. Five character arguments and functions are used for table lookup.

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: SERIES 200
1410/7010 LIBERATION CAPABILITY
REPORT
SOFTWARE BULLETIN

DATED: JUNE, 1966

FILE NO: 122.1405.002J.0-388

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____   DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

Cut . ng Line

Honeywell
ELECTRONIC DATA PROCESSING