PRELIMINARY

HITACHI

DK512S Winchester Disk Drive OEM Manual

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K 6600101	SHEET No.	REV NO	2
	1/80	95-10-4	

DK512S
WINCHESTER DISK DRIVE

K 6600101	SHEET No.	REV NO
	2/	'85

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REVISION RECORD

CODE AD: Addition, CH: Change, CR: Correction, DL: Deletion

No.	Revision	Page	Section	Subjects	Code
1	0→1	2-1	2	PRODUCT DESCRIPTION	CR
		2-3	2.4	Features	CR
		4-13	4.7.6(2)	READ GATE=BIT1	CR
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1. INTRODUCTION

1.1 Purpose

This manual is intended to familiarize Original Equipment Manufacturers (OEMs) with the Hitachi DK512S Winchester disk drives, and to enable OEMs to integrate the drives into their computer-based systems. The manual provides technical information needed by system designers, engineers, purchasing agents and quality-control personnel. A separate Service Manual describes installation, strapping, spare parts, and troubleshooting.

1.2 Manufacturer

The DK512S series disk drives are manufactured at the Odawara Works, a member of the Hitachi Computer Division. The Odawara Works also produces large disk drives, magnetic tape drives, optical character readers, mass storage units. Its first Winchester drives were delivered in 1976.

1.3 Quality Control

Production of the DK512S drives is highly automated, using robots and the latest technological advancements. The drives benefit from total vertical integration: heads, platters and electronics are all designed, manufactured and tested at the same facility, providing assurance of component compatibility. An elaborate quality control system assures that each drive satisfies all specifications.

1.4 Related Documents

The following documents are also applicable.

- Service Manual
- Schematic Diagrams : TBD
- Hitachi Technical Report on DK512S

2. PRODUCT DESCRIPTION

⚠ The Hitachi DK512S series disk drives are high-capacity 5.25-inch Winchester disk drives with a SMD Interface as well as DK512 with ESDI version.

The mechanics and electronics are similar to DK511 series disk drives, which are already being marketed, but these new drives feature larger storage capacities, and higher transfer and access speeds.

2.1 Models

The series includes three models, differing in the number of disks mounted on the spindle:

Model	Disks	Capacity (MBytes) (Unformatted)
DK512S-8	3	86.1
DK512S-12	4	120.6
DK512S-17	6	172.3

The unit is housed in an aluminum casting (see Figure 2-1). One casting accommodates all models.

2.2 Components

The DK512S disk drive includes the assemblies below and is delivered with the following documents attached. Sections 3.7 and 3.8 list the connectors and cables which the customer should prepare.

2.2.1 DK512S Disk Drive Unit

Figure 2-1 shows the DK512S disk drive unit.

The unit consists of:

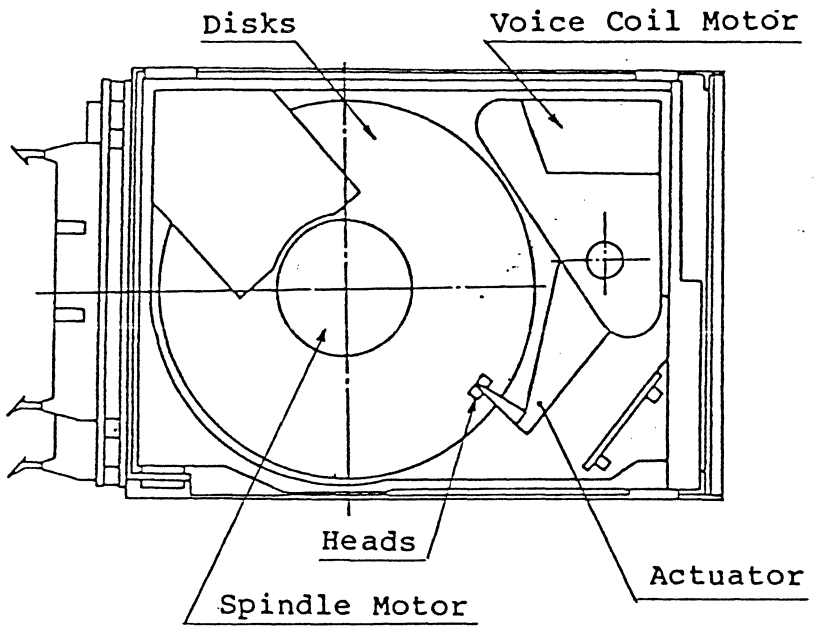
- Head and Disk Assembly (HDA)
- Mounting Frame and Shock Mounts
- Printed Circuit (PC) boards. These are mounted in the frame

2.2.2 OEM Manual, Service Manual and Schematic Diagrams

One set of these transparencies is delivered with the first lot of drives. When any modification is made, the corresponding transparency will be provided.

2.2.3 Test Report and Defect List

One set of the Test Report and the Defect List will be provided with each drive.



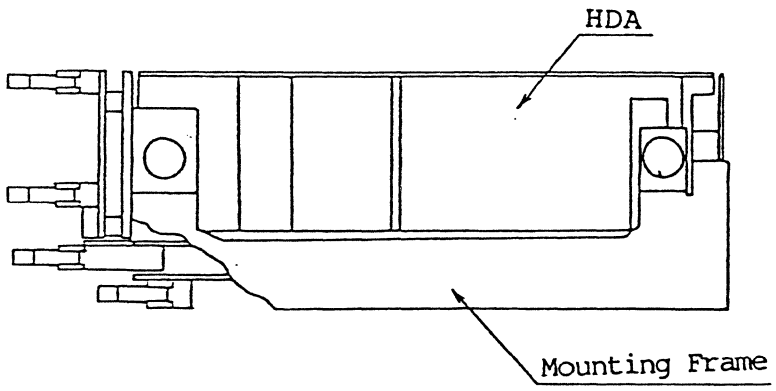


Figure 2-1 Structure of DK512S

K 6600101	SHEET No.	REV NO	0
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2.3 Options

- To be provided later.

2.4 Features

Hitachi drives are designed and manufactured for exceptional performance and high reliability. Each drive is given a lengthy burn-in, then tested at marginal conditions.

The principal features of the drives are summarized below:

- Large Capacity, Fast Data Transfer

  This is really a high performance disk drive with an exceptional maximum 172.3 Mbytes of capacity per drive and a fast 1.215 Mbytes/sec data transfer rate.

- Compact

  ⚠ It took Hitachi to put all of this capacity in a equivarent body size to a minifloppy disk drive.

- High-Speed Access

  ⚠ The DK512S offers 23 millisecond average access time thanks to positioning to heads by a microprocessor-controlled high performance rotary voice-coil actuator.

- Superior Reliability

  In-house manufacturing of all heads, disks and custom LSIs, plus strict testing throughout guarantees the highest drive reliability.

- Industry Standard Interface

  The SMD industry standard interface provides easy integration with a wide range of systems.

2.5 Specifications

Table 2-1 lists the complete specifications for DK512S models.

Table 2-1 Specifications

Model		DK512S -8	DK512S -12	DK512S -17
Total Capacity	(unformatted)	86.1 Mbytes	120.6 Mbytes	172.3 Mbytes
	(formatted)*	67.4 Mbytes	94.4 Mbytes	134.8 Mbytes
Capacity	per Track (unformatted)	20,944 bytes		
	per Track (formatted)*	16,384 bytes		
	per Sector (formatted)*	256 bytes		
Number of Sectors/Track		Selectable in one-byte increments		
Number of Disks		3	4	6
Number of Heads	Data Head	5	7	10
	Servo Head	1	1	1
Number of Cylinders		823		
Access Time (nominal)	Average	23 ms		
	Maximum	45 ms		
	Minimum	6 ms		
	Average Latency	8.6 ms		
Disk Speed		3,482 rpm ± 1%		
Data Transfer Rate		1,215 kbytes/sec		
Maximum Recording Density		18,500 bpi/925 tpi		
Recording Method		RLL 2-7		
Data Transfer Method with Controller		NRZ		
Startup Time		Approx. 25 seconds		
Power Requirements		+12V±5% 5.0 A (max.) 2.5 A (average) +5V±5% 3.0 A -12V±5%1A		
Dimensions	Height	82.5mm (3.25 in)		
	Width	146 mm (5.75 in)		
	Length	238 mm (9.37 in)		
Weight		Approx. 3.4Kg (7.5 lbs)		

6 = 15/16

(Cont'd)

*64 sectors/track

Table 2-1 Specifications (cont'd)

Model		DK512S -8	DK512S -12	DK512S -17
Interface	Type	SMD		
	Configurations	Daisy-Chain or Radial		
Acoustic noise		Max 50 dBA, except when start-up, stop and seek.		
Reliability	MTBF	20,000 POH, typical usage		
	Preventive Maintenance	Not required		
	MTTR	0.5 hrs		
	Start/Stop Operations	Up to 10,000		
	Component Design Life	5 years or 20,000 POH		
Error Rate (within 10 retrials)	Recoverable (soft)	1 per 10^{10} bits read		
	Unrecoverable (hard)	1 per 10^{13} bits read		
Seek Error Rate		1 per 10^{7} seeks		
Ambient	Altitude Operating Nonoperating	3,000 m (10,000 ft) max. 12,000 m (40,000 ft) max.		
	Temperature Operating Nonoperating Transporting/ storing Maximum Gradient	5° - 45°C (41° - 113°F) -20° - 50°C (-4° - 122°F) -40° - 60°C (-40°- 140°F) 10°C/hr. (18°F/hr.)		
	Relative Humidity Operating Nonoperating	8 - 80% (no condensation) 8 - 90% (no condensation)		
	Vibration Operating Nonoperating	0.25G max. 0.5G max.		
	Shock Operating Nonoperating	2G max. (10 msec,half sine wave) 20G max. (10 msec,half sine wave)		
	Air Cleanliness	No corrosive gas, salt, or metallic particulates.		
Media defects	Maximum number of defects per device	86	120	172
	Maximum number of defects per surface	40	40	40
	Defect Free Areas	Heads 0 and 1 on Cylinder 0		
	Logging	Each defect is identified in a written test report, and on the disk itself.		

2.6 Standards Observed

The DK512S drives will comply with the following standards:

UL 478
CSA 22.2-154
FCC Part 15, Class A (when mounted in a standard cabinet)
TÜV

2.7 Mechanical Construction

A durable casting provides a stable mounting for the spindle motor and supports the voice coil motor. The voice coil motor pivots on precision bearings, moving between the poles of a permanent magnet. The motor carries 6-11 heads (depending on the model), which are mounted in pairs on adjustable cast aluminum truss arms. The monolithic flying heads are housed in light-weight frames which have been computer-adjusted for optimum tension against the disks. Hall sensors measure the speed of the spindle motor.

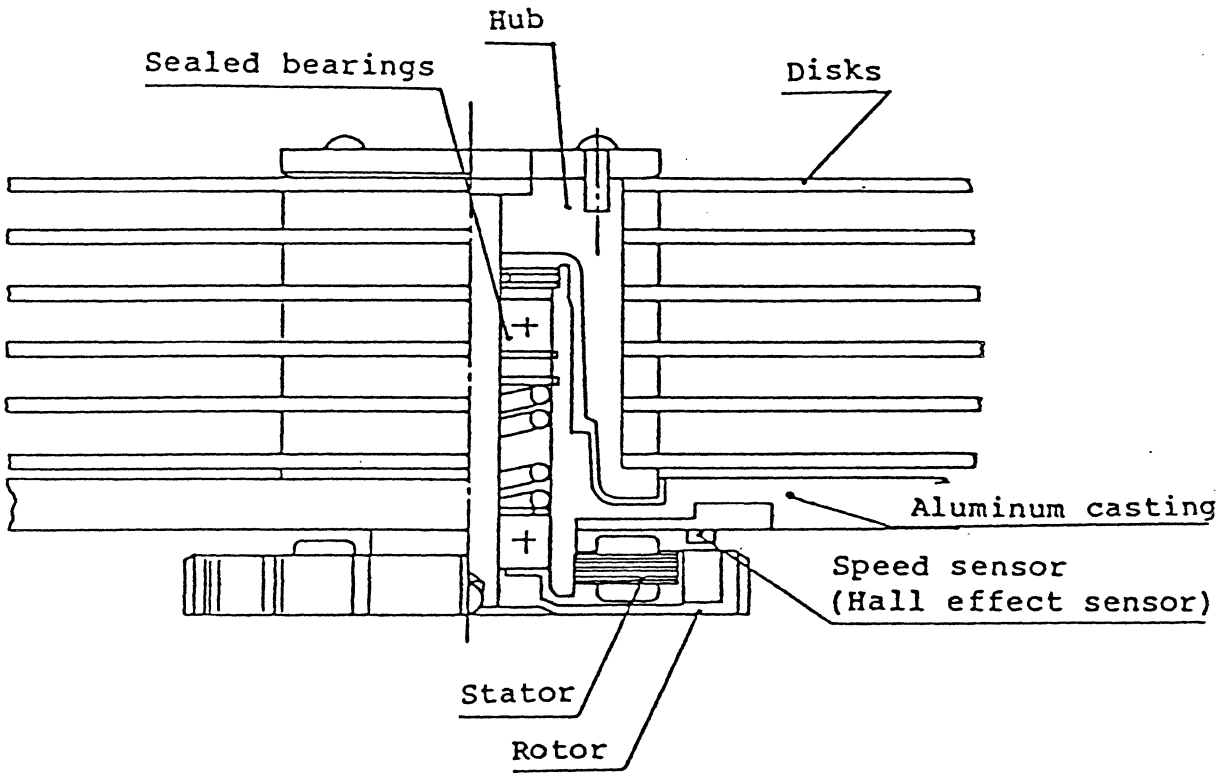


Figure 2-2. Spindle Motor

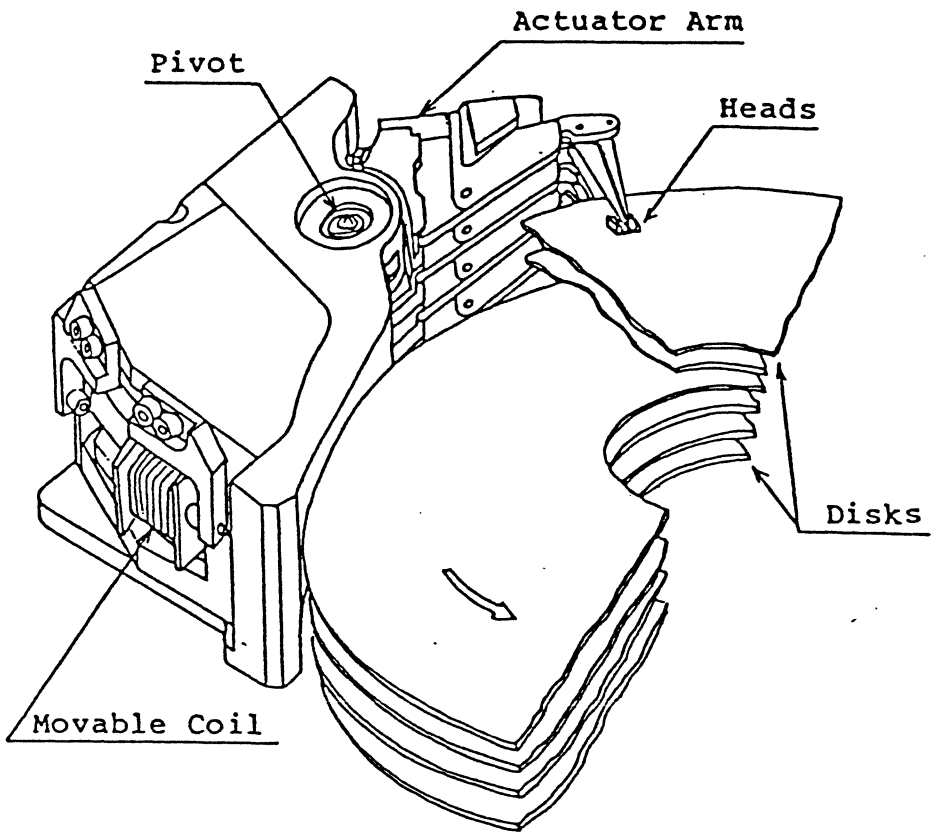


Figure 2-3 Actuator Arm Assembly

The disk platters are made with the aluminum substrates, which are turned with diamond tools to mirror finishes and parallel surfaces. Proprietary processes then produce uniform magnetic coatings. Every platter is tested and inspected at each step of production.

2.8 Electronics

The electronics assemblies are designed to insure high reliability and error-free operation. For example, no trimpots or DIP switches are used: strapping and adjustment are done with jumper plugs. Most of the semiconductors, including custom LSI chips, are made by Hitachi. Most resistors are metal film or are in networks.

Integrated circuits and transistors are soldered to the plated-through PC boards, thus eliminating socket problems. The boards have solder masks on each side, and white legends to identify each component. Power transistors are mounted on heat sinks, not directly on the PC boards. Power resistors are sealed in ceramic and are also mounted off the board. Low-level signal connectors are gold-plated.

2.9 Maintenance

No preventive maintenance is required. The HDA is sealed and must not be opened in the field. No mechanical or electrical adjustments at installation are required. When the DK512S PC assembly is changed, it is only necessary to reset the jumper plugs.
Major replaceable parts are the HDA, the Read/Write PC board, the Logical PC board, the Interface board, and the Analog PC board.

2.10 Daisy-Chain and Star Connections

The DK512S can be strapped to respond to 16 different device addresses, so that multiple drives can be addressed by the same controller, In the daisy-chain connection, a single control cable runs from drive to drive. This connection is used when the host addresses one drive at a time. In the star connection (also called a radial connection), a separate control cable connects each drive to the controller; this connection is used when the host addresses more than one drive at a time.

Both connections require data cables and power cables for each drive. All models can be connected in daisy-chain or star configurations.

2.11 Disk Basics

The spindle rotates at 3,482 rpm, creating air films over the surfaces of the disks, which balance the pressure of the flying heads and prevent the heads from touching the surfaces. When the disks stop, as when power is turned off, the heads come to rest in a safe area near the center of the disk. Close head-to-disk spacing requires that the disks be sealed in a clean environment.

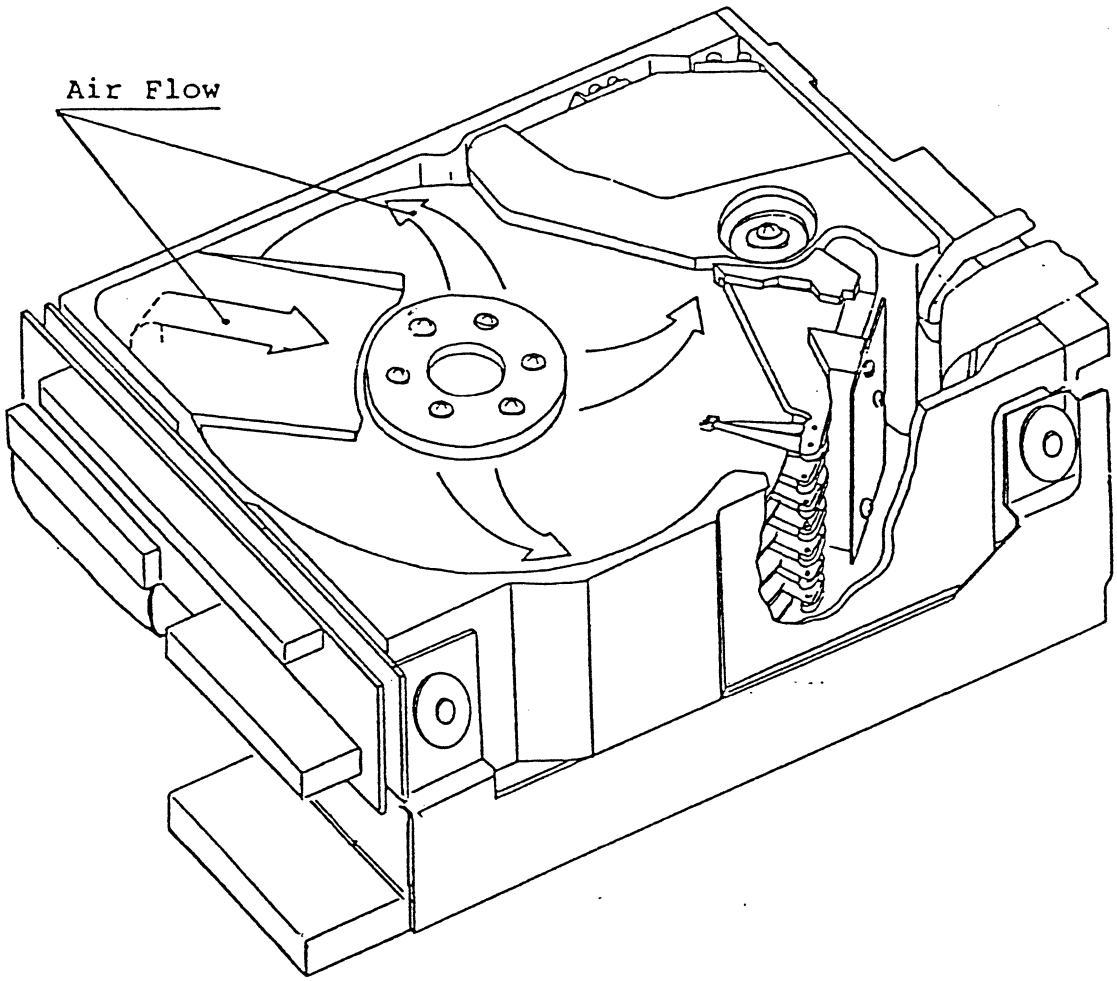


Figure 2-4 Air Circulation Inside Head and Disk Assembly

A positioning system for the voice coil motor moves the head assembly rapidly and accurately to the addressed cylinder. Since all heads are mechanically fastened together, they are positioned to the same cylinder, that is, to the same track on each surface. Cylinders are numbered from 0 at the periphery to 822 at the center.

Absolute cylinder position is established by the servo tracks, which are recorded at the factory on a dedicated surface, located at the top of the stack.
An elaborate feedback system centers the servo head in it's track.

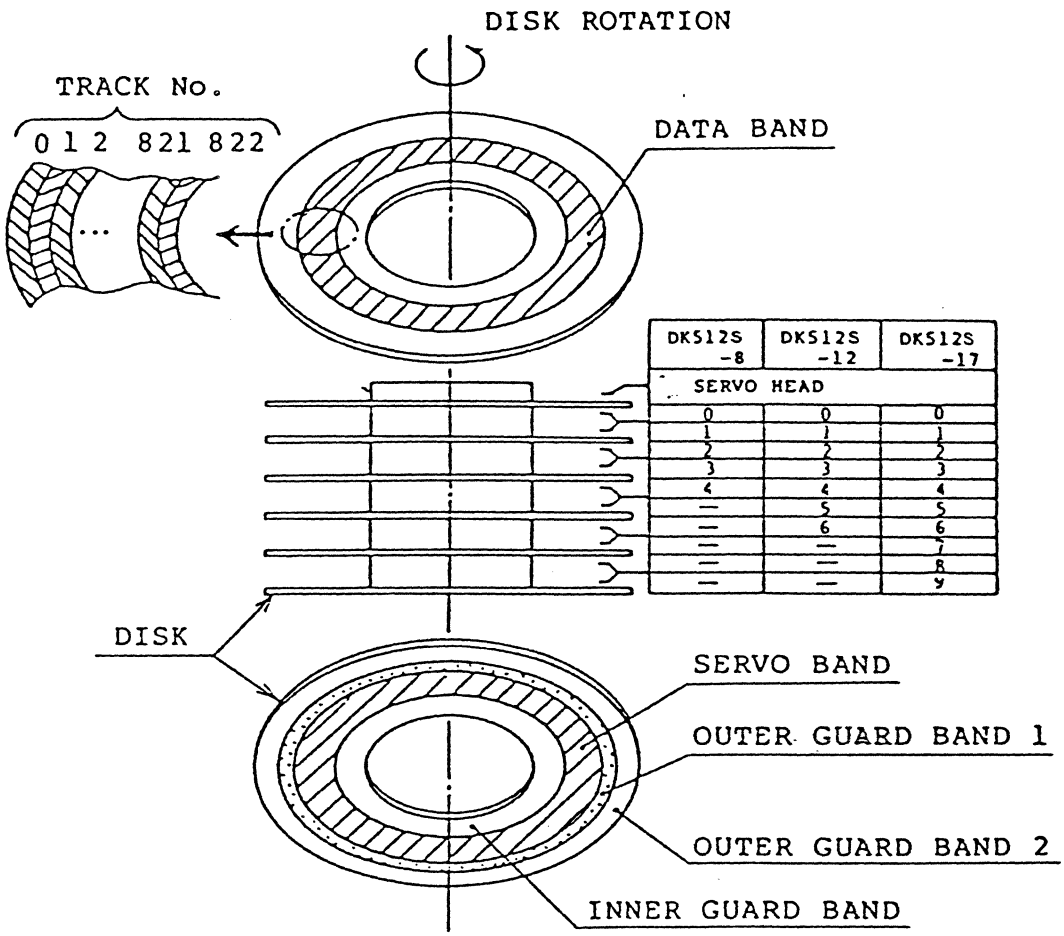


Figure 2-5 Head and Cylinder Address

An index signal and a precision clock are derived from the servo information. The index signal marks the beginning of a track or cylinder. The clock, a Phase Locked Oscillator (PLO), is a precision reference for writing data to the disk, and enables data to be formatted with shorter gaps between fields.

Disks are formatted by the OEM, depending on the intended application. Recommendations for a fixed sector format are provided in Chapter 5.

2.12 Power Supply

The drive requires +12 V DC, +5 V DC, and -12 V DC input. Figure 2-6 shows the derived voltages and representative circuits operated by each voltage.

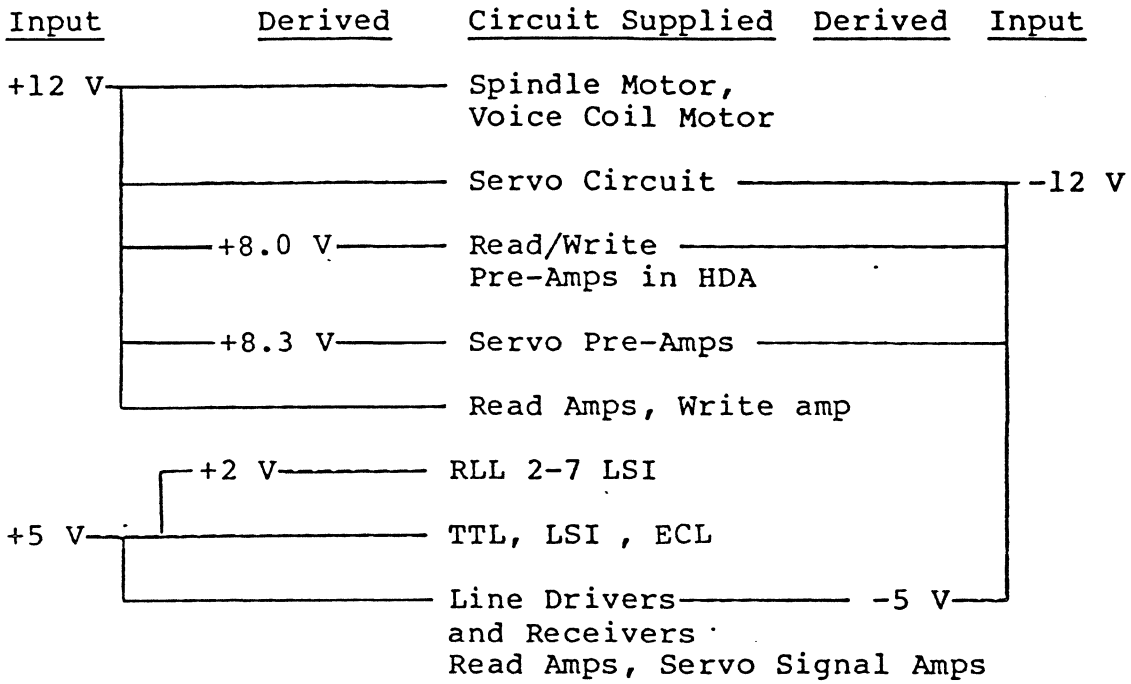


Figure 2-6 Voltage Utilization

2.13 SZ118B Read/Write PC Board

This PC board controls the drive's read and write operations. Mounted on this board are:

- Write driver
- READY Lamp (LED)
- Head select circuit
- Write fault sensor
- Read signal amplifier and AGC (Automatic Gain Control)
- Read signal equalizer amplifier

2.14 SZ144 Digital PC Board

This board controls digital operations such as interface control, seek control, servo control and read logic. Mounted on this board are:

-
- One-chip microprocesser
- Head velocity digital-to-analog converter
- Address mark detector
- R/W gate control
- Cylinder address register
- STATUS circuit
- PLO (Phase Locked Oscillator) for master clock
- VFO (Variable Frequency Oscillator) for READ DATA
- Read peak sense logic
- Write precompensation
- RLL 2-7 encoding and decoding (for writing to the disk)
- Servo logic
- Servo signal amplifier
- Position signal generator
- Sync pulse generator

2.15 SZ149 Analog PC Board

This board controls analog operations such as motor control, servo control and power supply. Mounted on this board are:

- Head positioning control
  - On-track signal sensor
  - Track crossing pulse generator
  - Absolute velocity signal generator
  - Velocity error signal generator
- Voice coil motor driver
- Voltage regulator (+2 V, -5 V)
- DC spindle motor control
- Low-voltage detector and power-on reset

2.16 SZ145 Interface PC Board

Mounted on this board are :

- Line drivers, receivers, and Termination networks

2.17 Microprocessor

A high-speed 64-pin CMOS one-chip microcomputer is employed. This has reduced remarkably the size of circuits. Its main functions are:

- Motor power-on sequence
- Positioning the heads at the addressed cylinder, using a fast seek algorithm
- Returning the heads to the zero cylinder during power-up and recalibration (RTZ)
- Spindle motor speed checking

3. PHYSICAL INTERFACE

3.1 Physical Description

The DK512S 5.25-inch disk drive is shown in the frontispiece and in Figure 3-1. Three cables (control, data, and power) plug in at one end of the DK512S PC assembly; connectors for cables to the Head and Disk Assembly (HDA) are at the other end where the Read/Write PC Board is attached, i.e., on the Front Panel side. The HDA is sealed in a contaminant-free atmosphere in its casting and is never to be opened in the field.

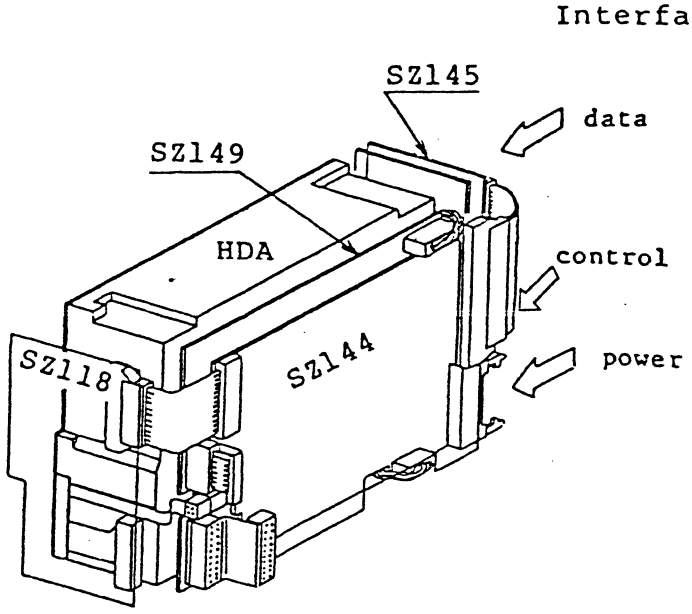
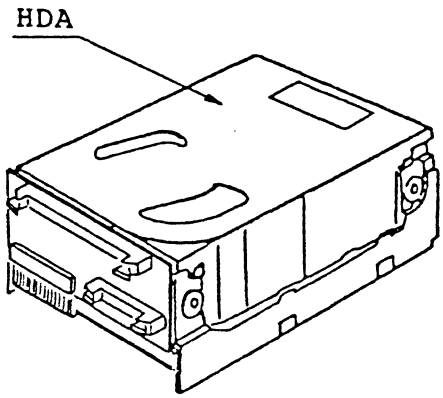
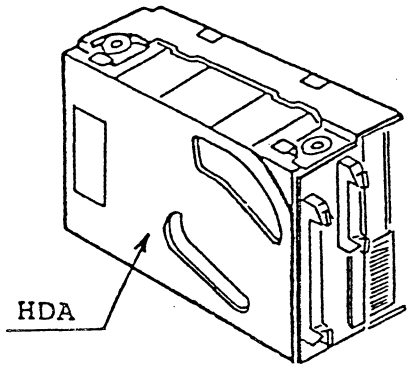


Figure 3-1 DK512S PC Boards and Interface Connectors

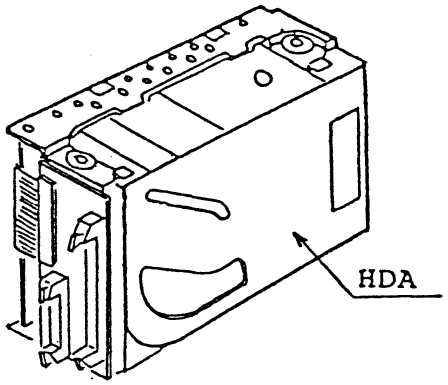
Figure 3-2 shows how the drive may be mounted either horizontally or vertically. Forced or natural air cooling may be used. When the drive is installed in a cabinet or box, forced air cooling is required. When no fan is used, the drive should be mounted so that the internal heat is conducted out completely and no outside heat affects the drive.



(a) Horizontal mounting



b) Vertical mounting-1



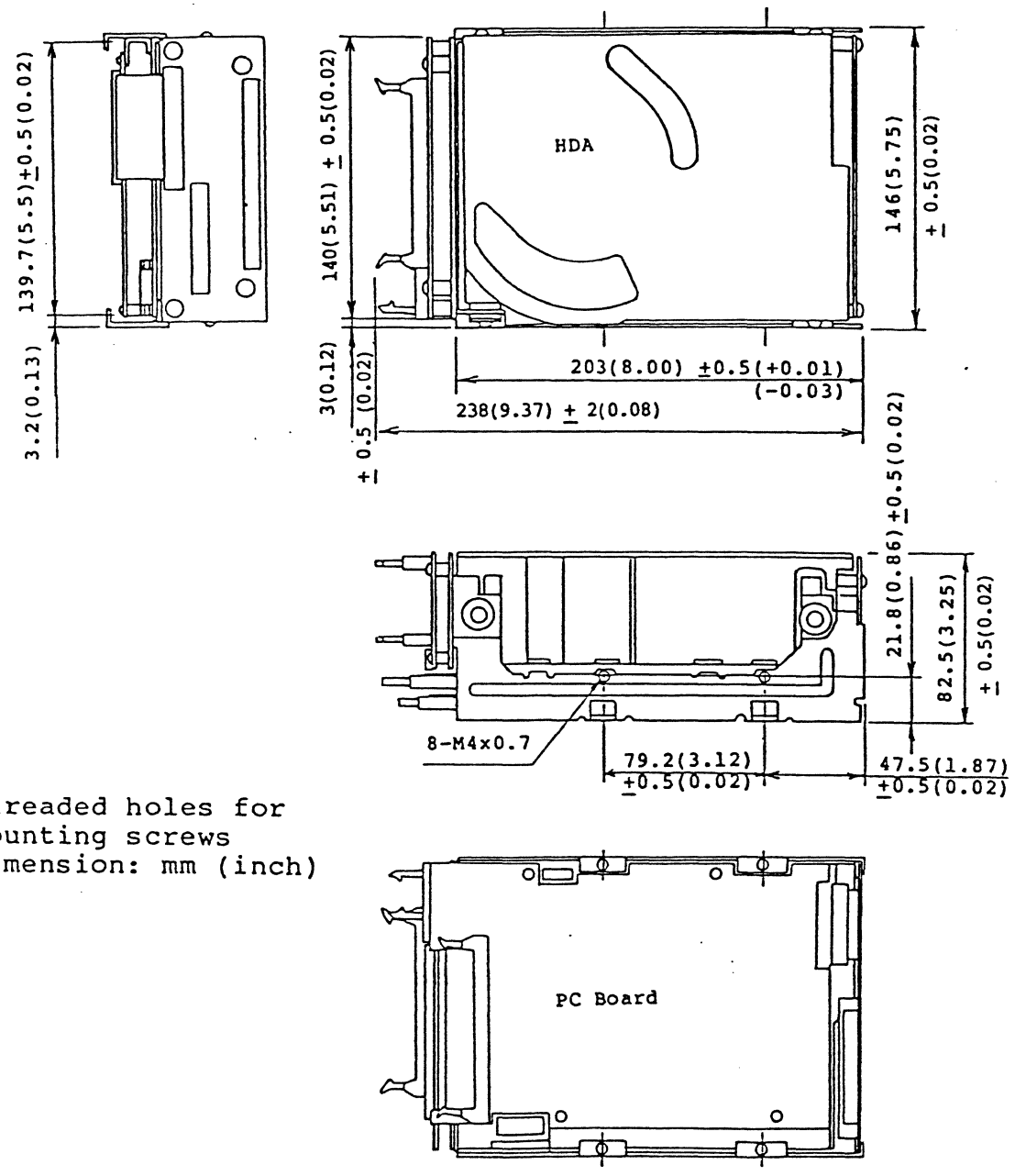
c) Vertical mounting-2

Figure 3-2 Mounting Positions

3.2 Mounting Requirements

The drive has 8 threaded holes for the mounting screws. Four screws are used, whether the drive is mounted horizontally or vertically. Be careful not to insert the mounting screws more than 5 mm (0.2 inch) into the drive. Figure 3-3 shows the DK512S mounting dimensions.

The guidelines in Section 3.2 should be observed by those responsible for mounting the DK512S in a system.



Threaded holes for mounting screws
Dimension: mm (inch)

Figure 3-3 DK512S Mounting Dimensions: Side and Top Views

3.2.1 Shock Mounts and Handling

Special precautions must be taken so that the drive is not jarred or bumped while it is off its shock mounts. When removed from the system, it must be placed on a urethane foam cushion. The drive should be installed in an accessible position for convenient removal and maintenance.

3.2.2 Metric Screws

Only metric screw threads and screws are used on the DK512. They are specified as:

M4x.7x8, where
- M = Metric
- 4 = basic major diameter, mm. Thus, a clearance hole would be approximately 4/25.4 = 0.157 inch.
- .7 = distance between threads, mm. Thus, this screw has 25.4/0.7 = 36.3 threads per inch.
- 8 = length, mm.

Metric screws must be used. There are no U.S. Standard screws, even in unusual sizes, that are interchangeable.

3.2.3 Air Flow

The DK512S disk drives are more reliable as the ambient temperature lowers. Air must pass over all sides of the HDA and between the boards. Select natural or forced cooling depending on its mounting conditions.

3.2.3.1 Forced Cooling

When the drive is mounted in a cabinet or box, a fan must be installed on the cabinet or box to force heated air out and take outside air in. Keep the internal temperature as close to the room temperature as possible. Figure 3-4 shows the forced air flow.

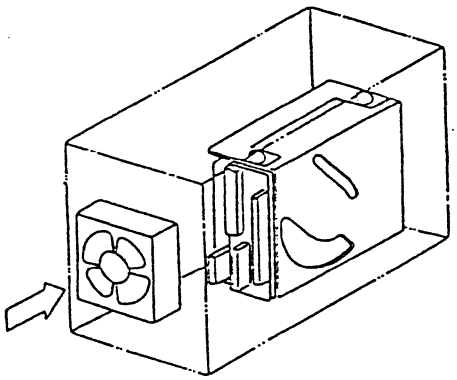


Figure 3-4 An Example of Forced Cooling

3.2.3.2 Natural Cooling

Natural cooling means that the drive is mounted so that no heated air remains anywhere in the devices, and that no outside heat affects the drive.

3.3 Interface Connectors

Control cable A, data cable B, and DC power cable C from the controller are connected to the drive at the following connectors:

- J1 for Control Cable A (P1)
- J2 for Data Cable B (P2)
- J3 for DC Power Cable C (P3)
- Ground Cable

Figure 3-5 shows the locations of these four connectors.

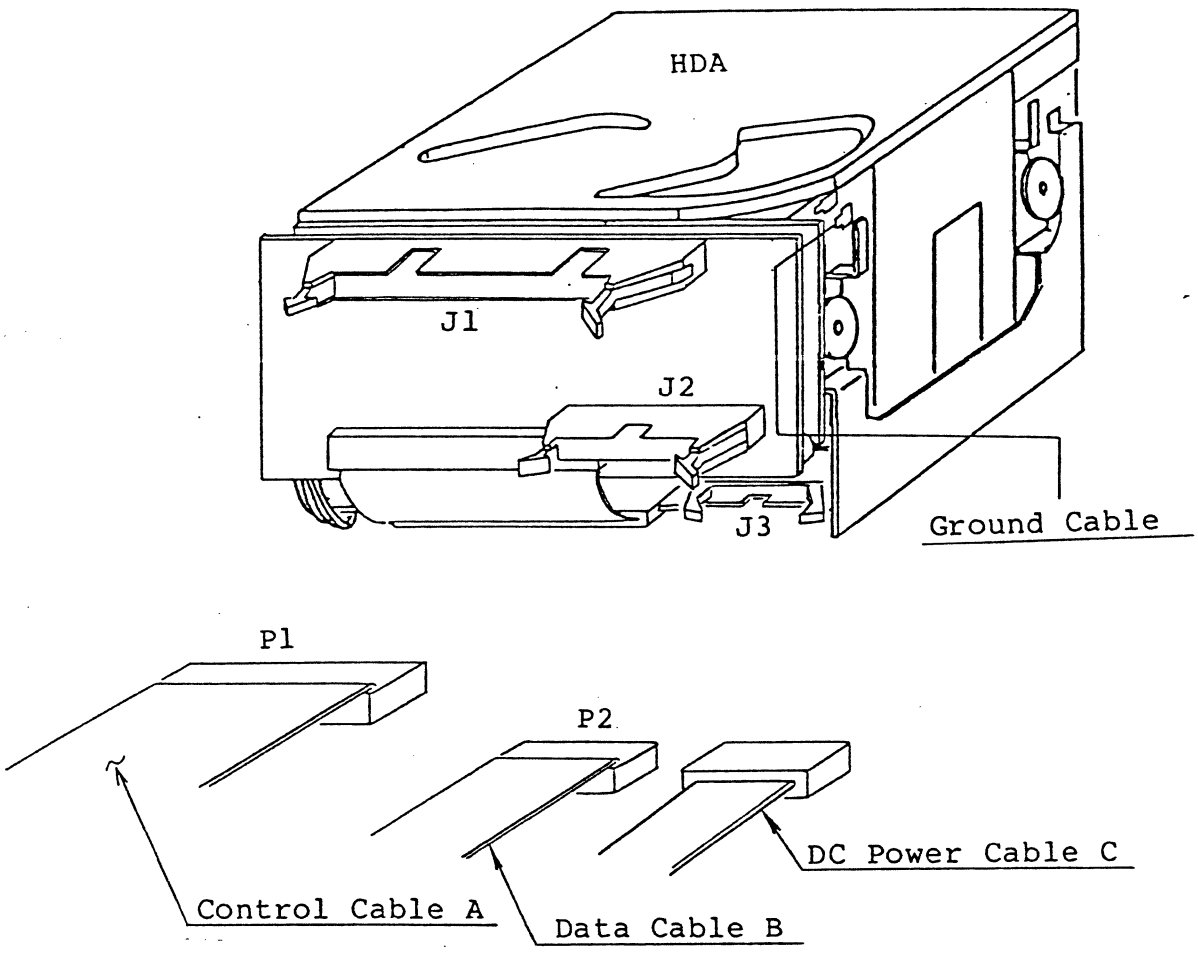


Figure 3-5 Cable Connector Locations

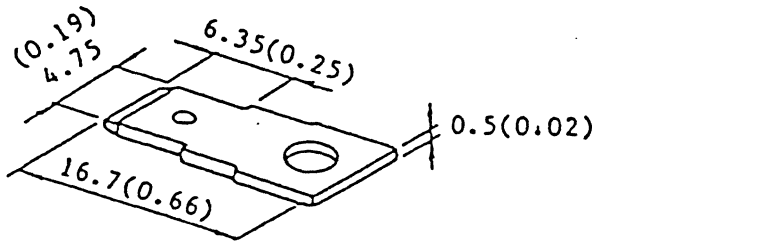


Figure 3-6 Ground Cable Connector

3.4 Control Cable A Pinout

Figure 3-7 shows the control cable A connector.

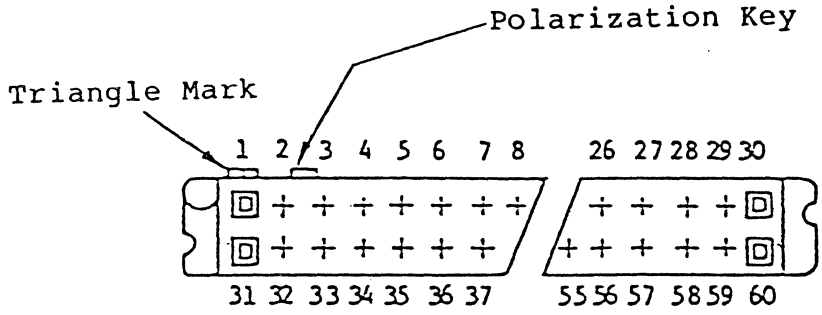


Figure 3-7 Control Cable A Connector

Table 3-1 lists the pinout for control cable A (for details, see Section 4.7, "Control Cable A Signal Descriptions"), and Table 3-2 shows the tag bus table (see Subsection 4.7.6, "TAG3"). Table 3-3 lists TAG4 and TAG5, Modes A, B and C. Table 3-4 shows DEVICE TYPEs for TAG4 and TAG5 (for details, see Subsection 4.7.9).

Table 3-1 Pinout for Control Cable A

Hitachi Signal Name	Source	Asserted-State Pin Polarity*	
		-	+
TAG1	CU	1	31
TAG2	CU	2	32
TAG3	CU	3	33
BIT0	CU	4	34
BIT1	CU	5	35
BIT2	CU	6	36
BIT3	CU	7	37
BIT4	CU	8	38
BIT5	CU	9	39
BIT6	CU	10	40
BIT7	CU	11	41
BIT8	CU	12	42
BIT9	CU	13	43
OPEN CABLE DETECTOR	CU	14	44
STATUS3 (FAULT)**	Drive	15	45
STATUS2 (SEEK ERROR)**	Drive	16	46
STATUS1 (ON CYLINDER)**	Drive	17	47
INDEX	Drive	18	48
STATUS0 (UNIT READY)**	Drive	19	49
STATUS5 (ADDRESS MARK FOUND)**	Drive	20	50
BUSY (Dual Port option only)	Drive	21	51
UNIT SELECT TAG	CU	22	52
UNIT SELECT 2^0	CU	23	53
UNIT SELECT 2^1	CU	24	54
SECTOR	Drive	25	55
UNIT SELECT 2^2	CU	26	56
UNIT SELECT 2^3 or TAG5#	CU	27	57
STATUS4 (WRITE PROTECTED)**	Drive	28	58
WR ENABLE##	CU	29	--
TAG4**	CU	30	60

Notes to Cable A Pinout

CU Control Unit

* All signals except WR ENABLE are differential. When the pins have the polarities shown, the signal is "asserted," that is, "true" or "one." When the signal is "negated," that is, "false" or "zero," the polarities are the reverse of those shown. The signals may also have high impedance in neither state.

** STATUS0-5 can be arranged to report additional status and error conditions by jumpering TAG4 and TAG5, as shown in Table 3-3. The signals in parentheses conform to the SMD standard, and are always available.

\# The function of pin 27 is set with a jumper plug; see Table 3-3.

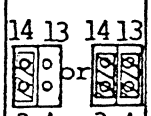
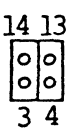
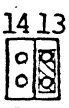
\#\# WR ENABLE is an added DK512S function. It may be enabled or disabled with a jumper plug.

Table 3-2 Tag Bus Table

		TAG1	TAG2	TAG3	UNIT SELECT TAG
		CYLINDER ADDRESS	HEAD ADDRESS	CONTROL SELECT	UNIT SELECT
BIT	0	CYLINDER ADDRESS 2^0	HEAD ADDRESS 2^0	WRITE GATE	–
	1	2^1	2^1	READ GATE	–
	2	2^2	2^2	SERVO OFFSET PLUS	–
	3	2^3	HEAD ADDRESS 2^3	SERVO OFFSET MINUS	–
	4	2^4	–	FAULT CLEAR	–
	5	2^5	–	AM EMABLE	–
	6	2^6	–	RTZ	–
	7	2^7	–	–	–
	8	2^8	–	–	–
	9	CYLINDER ADDRESS 2^9	–	RELEASE*	PRIORITY SELECT*

*Dual Port Option

⚠2 Table 3-3 TAG4 and TAG5, Modes A, B and C

MODE	A	B		C			
Jumper Plug MODE JP152							
TAG4	Don't care	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
TAG5	Don't care	Don't care	Don't care	FALSE	FALSE	TRUE	TRUE
STATUS0	UNIT READY	UNIT READY	SECTOR ADDRESS 1	UNIT READY	SECTOR ADDRESS 1	STATUS ERROR 1	DEVICE TYPE 1
1	ON CYLINDER	ON CYLINDER	2	ON CYLINDER	2	STATUS ERROR 2	2
2	SEEK ERROR	SEEK ERROR	4	SEEK ERROR	4	WRITE ERROR 1	4
3	FAULT	FAULT	8	FAULT	8	WRITE ERORR 2	8
4	WRITE PRO-TECTED	WRITE PRO-TECTED	16	WRITE PRO-TECTED	16	WRITE ERROR 3	16
STATUS5	ADDRESS MARK FOUND	ADDRESS MARK FOUND	SECTOR ADDRESS 32	ADDRESS MARK FOUND	SECTOR ADDRESS 32	SELECT ERROR 1	DEVICE TYPE 32

Note: STATUS0 - STATUS5 in this table are valid 200 ns after TAG4 and TAG5 change to a new condition. The signals are unstable for a short time after power is turned on. As shipped, JP is installed (Mode C).

Table 3-4 DEVICE TYPE Table for TAG4 and TAG5 True

STATUS( )	5	4	3	2	1	0
DEVICE TYPE( )	32	16	8	4	2	1
Drive Model Number:						
DK512S-8	0	0	0	0	0	1
DK512S-12	0	0	0	0	1	0
DK512S-17	0	0	0	1	0	0

1 = DEVICE TYPE asserted; 0 = DEVICE TYPE negated

3.5 Data Cable B Pinout

Figure 3-8 shows the data cable B connector; Table 3-5 lists the pinout for data cable B.

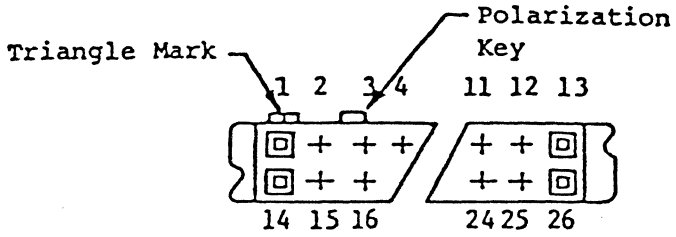


Figure 3-8 Data Cable B Connector

Table 3-5 Pinout for Data Cable B

Hitachi Signal Name	Source	Asserted-State Pin Polarity*		Shield
		-	+	
SERVO CLOCK	Drive	2	14	1
READ DATA	Drive	3	16	15
READ CLOCK	Drive	5	17	4
WRITE CLOCK	CU	6	19	18
WRITE DATA	CU	8	20	7
UNIT SELECTED	Drive	22	9	21
SEEK END	Drive	10	23	--
RPS INDEX	Drive	12	24	11
RPS SECTOR	Drive	13	26	25

Notes to Cable B Pinout

CU Control Unit.

* All lines are differential, terminated at the receiving end only. When the pins have the polarities shown, the signal is "asserted," that is, "true" or "one." When the signal is "negated," that is, "false" or "zero," the polarities are the reverse of those shown. The signals may also have high impedance in neither state.

3.6 Power Cable C Pinout

Figure 3- 9 shows the power cable C connector; Table 3-6 lists the pinout for power cable C.

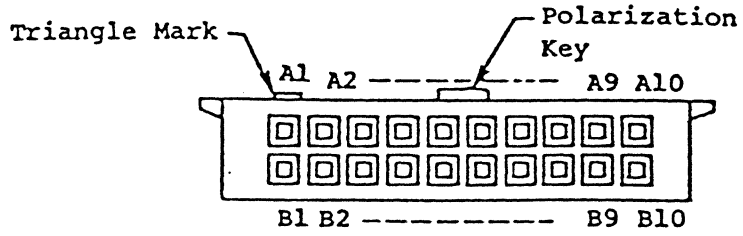


Figure 3-9 Power Cable C Connector

Table 3-6 Pinout for Power Cable C

Pin No.	Signal Name	Pin No.	Signal Name
A1	+12 V	B1	+12 V
A2	+12 V	B2	+12 V
A3	+12 V	B3	+12 V
A4	+12 V	B4	GND (+12 V)
A5	GND (+12 V)	B5	GND (+12 V)
A6	-12 V	B6	GND (-12 V)
A7	Not used	B7	GND (-12 V)
A8	GND (+5 V)	B8	GND (+5 V)
A9	+5 V	B9	GND (+5 V)
A10	+5 V	B10	+5 V

3.7 Connector Specifications for Cable Plugs

Table 3-7 lists connector specifications for cable plugs.

Table 3-7 Connector Specifications for Cable Plugs

Cable	Item	Mfr	Manufacturer's Part Number	Qty.
A Control	Mass termination connector*	3M	3334-6000	1
	Strain relief	3M	3448-3060	1
B Data	Mass termination connector*	3M	3339-6000	1
	Strain relief	3M	3448-3026	1
C Power	Connector	Japan Aeronautic Electronics	*PS-D4C20*	1
	Pin		*PS-SD-CINN-2N*	19
Ground	Faston Tab	AMP	62187-1 or 60711-1 or 170038-2	1

*The mass termination connector may be used either at the end of a cable (star connection), or in the middle of a cable (daisy-chain connection).

3.8 Cable Specifications

Table 3-8 shows cable specifications.

Table 3-8 Cable Specifications

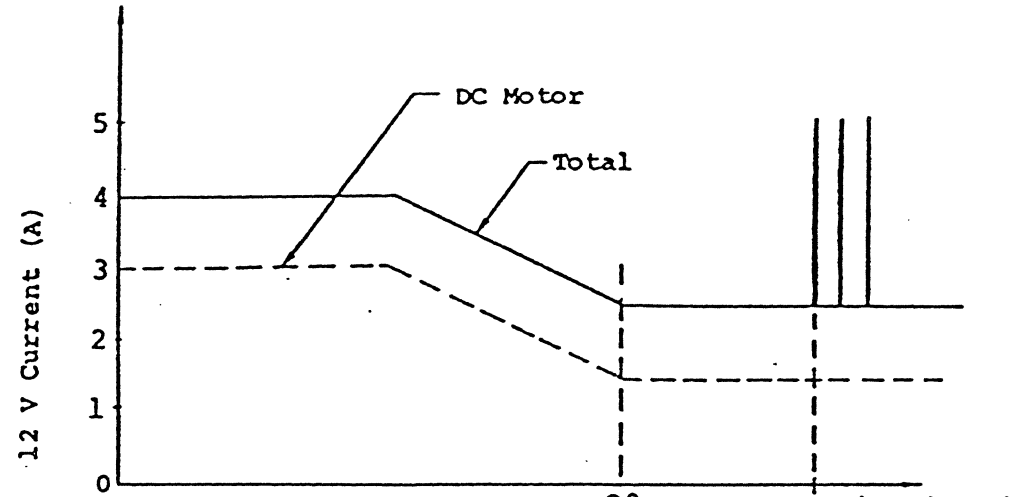
Cable	Item	Mfr	Manufacturer's Part Number	Length
A Control	Flat ribbon, 30 twisted-pairs, 28 AWG	Spectra-Strip	SS-455-248-60	30 m, max. (cumulative)
B Data	Flat ribbon, 26 conductor, with shield plane and drain wire. 0.05 in. spacing, 28 AWG.	3M	3476-26	15 m max, each cable
C Power	20 conductor, 22 AWG, maximum external dia. 0.06 in., each wire	--	--	3 m max, each cable
D Ground	Braid or equivalent, 20 AWG or larger	--	--	Min. possible

4. ELECTRICAL INTERFACE

4.1 DC Power Requirements

Figure 4-1 gives the +12 V DC requirements. The DC brushless motor requires a maximum current of 5.0 A at startup and has short peak current requirements during seek operations.

The drive requires also +5 V DC power of 3.0 A Max.



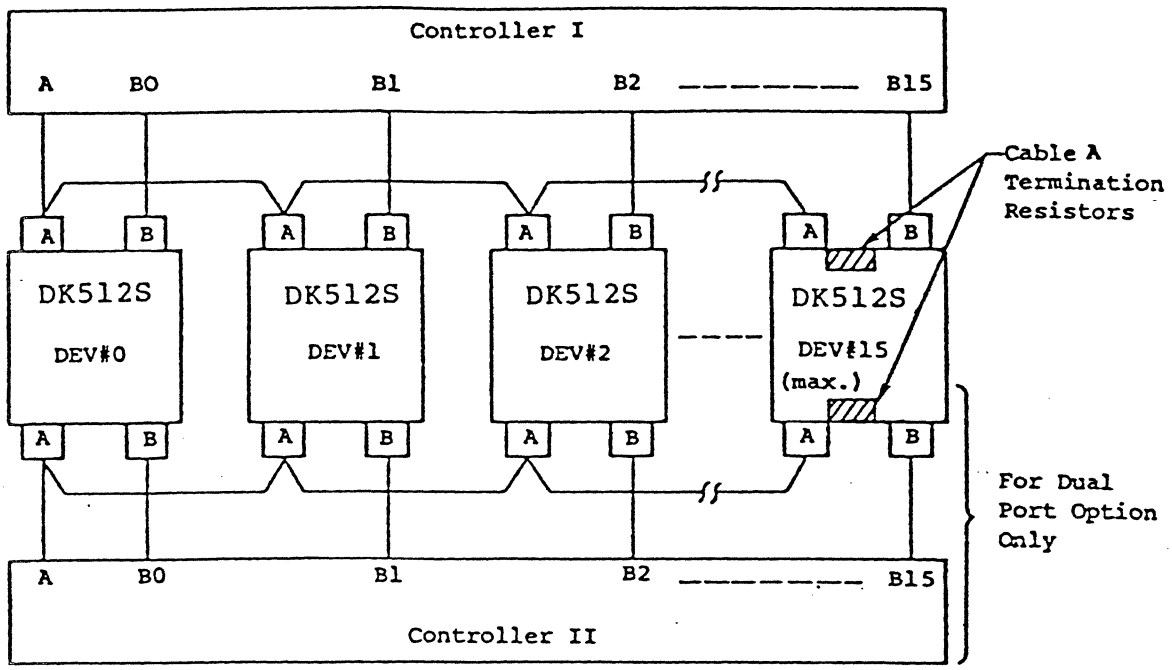
+12 V Power		(average)	
DC Motor	3.0 A max.	1.5 A	-
Other Equip.	1.0 A	1.0 A	-
Total	4.0 A max.	2.5 A	5.0 A max.

Figure 4-1 +12 V DC Power Requirements

Note that starting up two or more motors simultaneously results in a large current flow. To avoid this, wait at least 20 seconds before turning on the +12 V DC power for the second motor. All the devices become ready when the last device enters the READY state.

4.2 Daisy-Chain Connection

Figure 4-2 shows the daisy-chain connection.



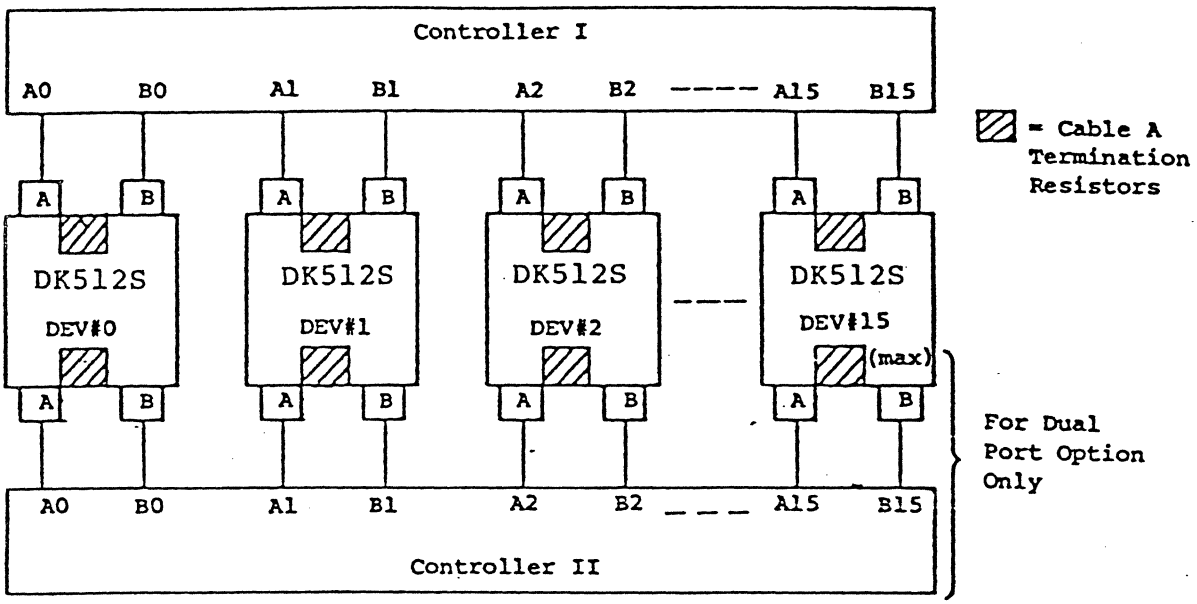
Notes

- The last device (only) in the daisy-chain must have termination networks on cable A. Plug-in termination networks are provided with each drive.
- Each drive has a separate cable B to each controller.
- Power and ground cables are not shown.

Figure 4-2 Daisy-Chain Connection

4.3 Star Connection

Figure 4-3 shows the star connection.



Notes

- Each control cable is terminated at its drive. Plug-in termination networks are provided with each drive.
- A separate data cable is required for each drive.
- Power and ground cables are not shown.

Figure 4-3 Star Connection

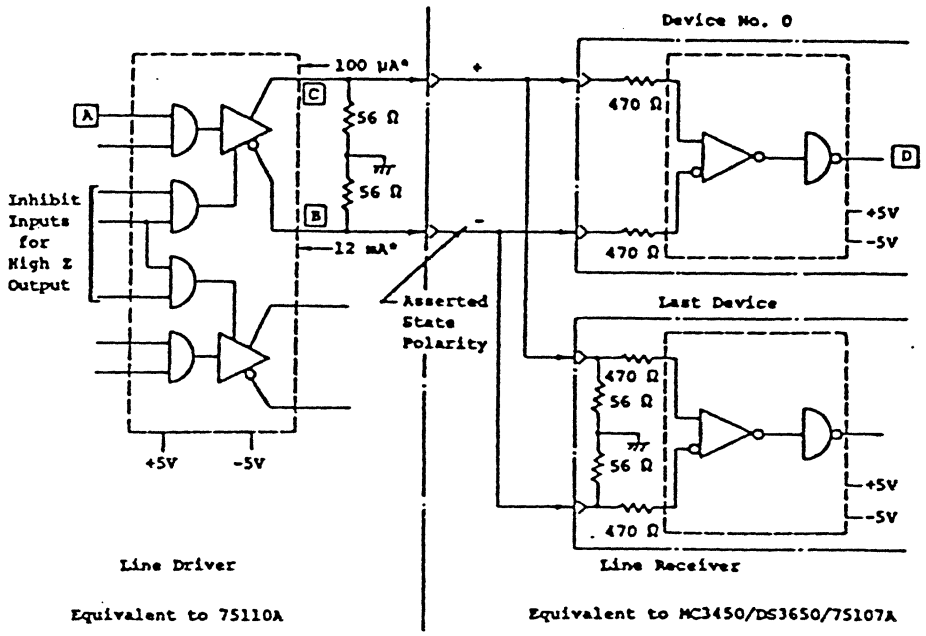
4.4 Control Cable A Transmitter and Receiver Circuits

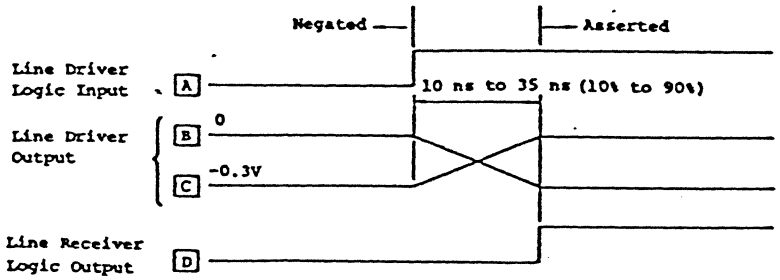
Figure 4-4 shows a single signal line in simplified form. The transmitter is a 75110A or equivalent integrated circuit line driver with a three-state differential output. Typical output is 12 mA, constant current. The receivers are 75107A or equivalent integrated circuit differential line receivers with 25 mV sensitivity. The integrated circuits are designed specifically for use in high-speed data transmission systems that use balanced, terminated transmission lines, such as the twisted pair cables used in the SMD interface. Since the system is balanced, noise induced on one line is also induced on the other, and appears as a common-mode signal to the receiver, which rejects it. The ground connection between the transmitter and receiver is not part of the circuit, so that transmission is not affected by circulating ground currents.

The drive output circuits are designed to drive transmission lines at their normal impedances. Control cable circuits are terminated at both ends, minimizing reflections. The low signal amplitudes and low line impedance also minimize crosstalk.

The output transistors are NPN, and sink current to -5 V. When the circuit is asserted, output B sinks current and output C has nearly zero current. When the circuit is negated, output C sinks current, and output B has nearly zero current. The resulting voltages are shown in the lower part of Figure 4-4.

When a drive is selected, its line drivers are on (carrying current), and data is transmitted by switching the output that sinks current. When a drive is not selected, its control cable transmitters are inhibited, and both outputs of the line drivers go to a high impedance state. This feature allows multiple transmitters to be connected to the same bus, as in daisy-chain configurations.



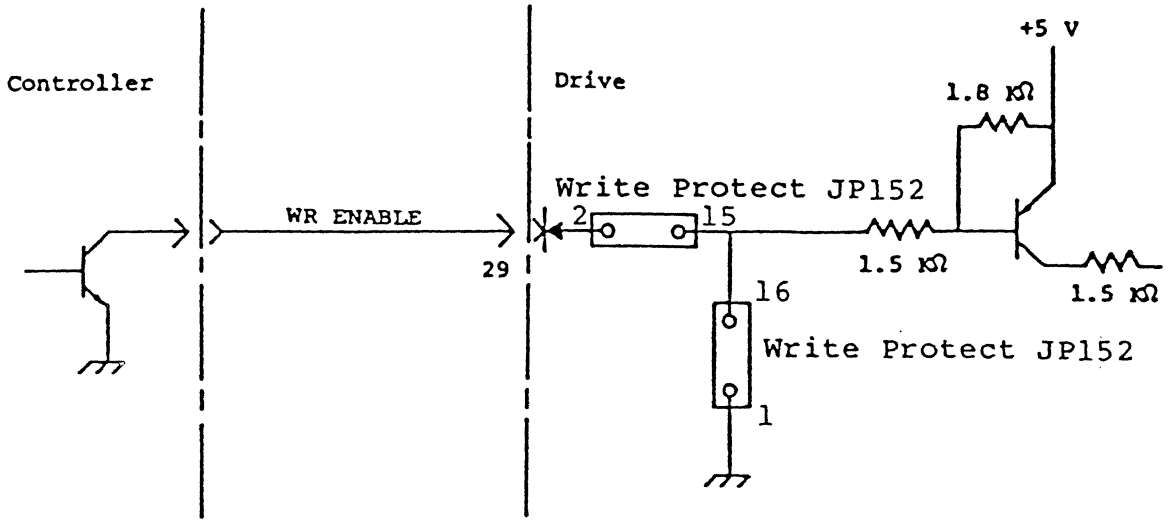


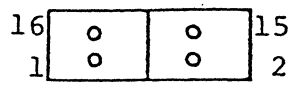
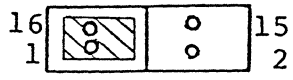
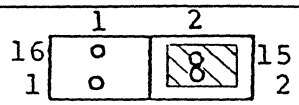
*Typical, Asserted State

Notes for control cable A circuit

- All resistors shown are ±5%, 0.1 W or more. This accuracy is required to maintain transmission balance.
- The receiver (drive end) of the OPEN CABLE DETECTOR has 10K pull-up resistors from each side of the line in order to bias it to the negated or false state. The source (controller end) must not be terminated. If more than eight drives are daisy-chained, the pull-up resistors must be 20K.
- The WR ENABLE circuit is not differential; see Figure 4-5 for the circuit.
- Transmission delay of the cable is about 1.5 ns/foot. Line receiver delay is 19 ns (typical).

Figure 4-4 Control Cable A Signal Transmission Circuit



Write Protect JP152	Description
	Drive is always read only.
	Drive is always read/write.
	Drive can be written to only when WR ENABLE is asserted.

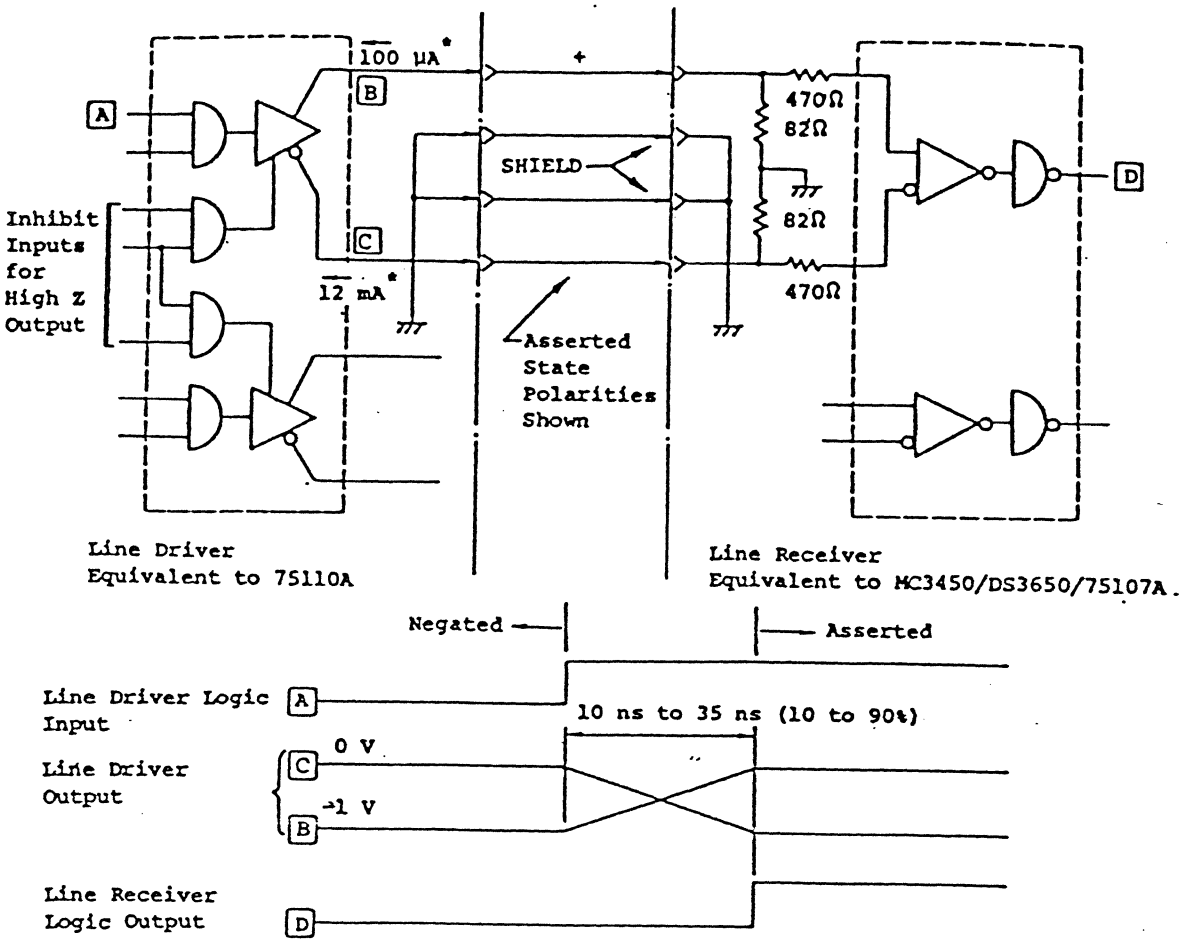
Notes

- WR ENABLE is asserted when pin 29 is 0 V, and negated when pin 29 is +.

Figure 4-5 WR ENABLE Circuit

4.5 Data Cable B Transmitter and Receiver Circuits

Figure 4-6 shows a simplified schematic of the data cable B signal circuits. The same integrated circuits are used as in the control cable, and the same description applies. The data cables are terminated only at the receiver end. The higher termination resistance results in a larger signal voltage at the receiver.



Notes

- All lines are differential, terminated at the receiver only.
- All resistors shown are ±5%, 0.1 W or more. This accuracy is required to keep transmission balance.
- Transmission delay of the cable is 1.5 ns/foot. Line receiver delay is 19 ns (typical).
- The receiver circuits (in the controller) for the UNIT SELECTED and SEEK END signals require bias networks, as shown in Figure 4-7. The networks bias the receivers to the negated or false state to prevent false status or interrupt signals if the power fails at the drive.

Figure 4-6 Schematic of Data Cable B Signal Transmission Circuit

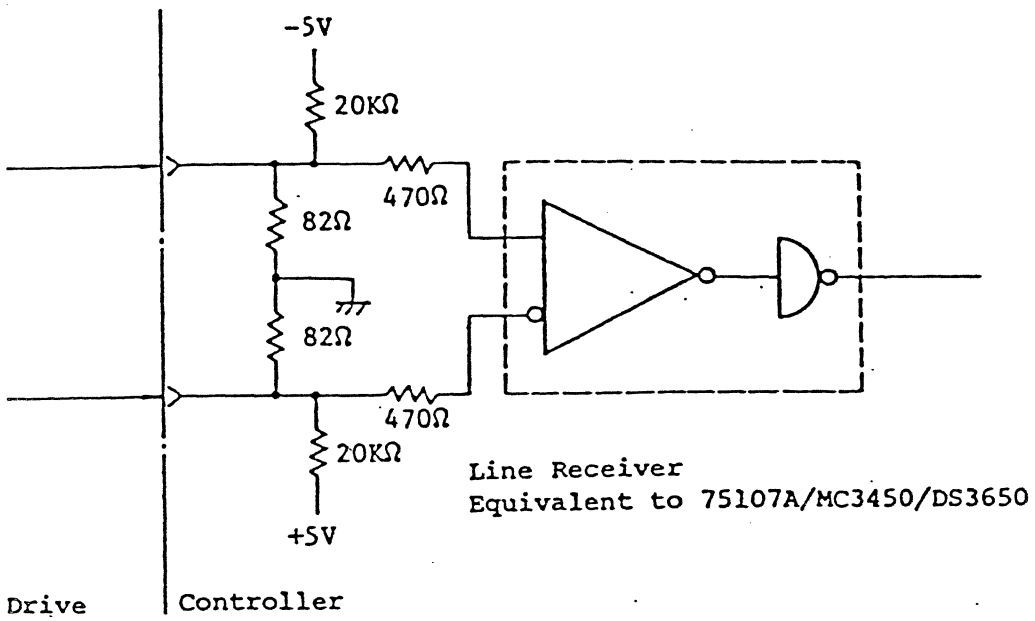


Figure 4-7 Bias Network for UNIT SELECTED and SEEK END Signals

4.6 Summary of Drive Operation

Figure 4-8 shows a typical sequence of operations and many of the timing relationships. First, the drive is selected, then the cylinder, finally the head. The desired sector is obtained by reading the sector addresses passing under the head. Each track has sync patterns and head scatter patterns. WRITE GATE is asserted and negated in designated places in these fields, producing write splices. The servo information keeps the heads on cylinder, and develops the clock for encoding and decoding the data.

4.7 Control Cable A Signal Descriptions

Table 3-2 above lists the control cable A signals and their sources.

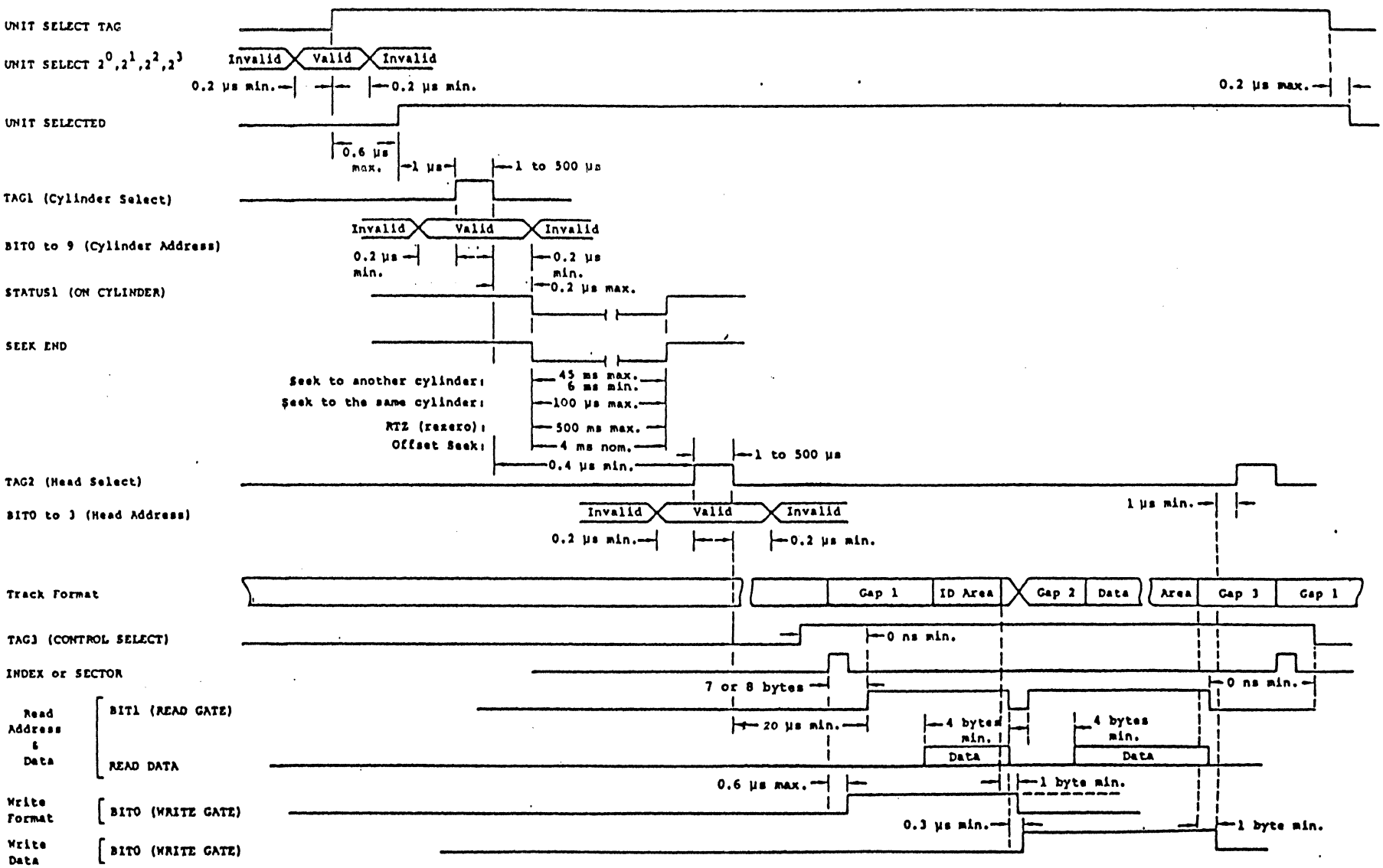


Figure 4-8 Timing Diagram, Fixed Format, Without Address Mark

4.7.1 UNIT SELECT 2^0, 2^1, 2^2, 2^3

To select a drive, the controller first places the binary drive address on these four lines. There are 2^4 (i.e., 16) unique addresses. Each drive on a control cable must have a different logical device number, or address, established with jumper plugs on the DK512S PC assembly. Another jumper plug changes the function of the control cable pair connected to pins 27 and 57 from UNIT SELECT 2^3 to TAG5. TAG5 provides additional functions, described in Subsection 4.7.9.

4.7.2 UNIT SELECT TAG

The leading edge of UNIT SELECT TAG selects the drive whose address corresponds to that set up on the UNIT SELECT lines. The drive remains selected until UNIT SELECT TAG is negated, regardless of the state of the UNIT SELECT lines.

When a drive is selected, it responds by asserting UNIT SELECTED (in data cable B). UNIT SELECTED remains asserted until the drive is deselected by negating UNIT SELECT TAG.

4.7.3 TAG1

To select a cylinder, the controller sets up the cylinder address on the 10 bus lines, BIT0-9, and strobes the address into the selected drive with TAG1. The drive must be ON CYLINDER and UNIT READY before the TAG1 strobe. If the cylinder address is invalid, SEEK ERROR is asserted. TAG1 must not be asserted while the drive is reading or writing. ON CYLINDER and SEEK END are always negated by the trailing edge of TAG1.

When changing cylinder addresses, TAG1 must not be asserted for at least one microsecond after WRITE GATE is negated.

4.7.4 STATUS1 (ON CYLINDER)

This signal is asserted when the servo has correctly positioned the head over a track. ON CYLINDER is momentarily negated while seeking to a new track. Typical times are shown in Figure 4-8. ON CYLINDER is negated within 200 ns of the trailing edge of TAG1 or the assertion of RTZ, SERVO OFFSET PLUS, or SERVO OFFSET MINUS.

4.7.5 TAG2

To select a head, the controller sets up the head address on the 10 binary bus lines, BIT0-9, and strobes the address into the selected drive with TAG2. UNIT READY must be asserted before the TAG2 strobe. TAG2 must not be asserted during a read or write operation.

When changing head addresses, TAG2 must not be asserted for at least one microsecond after WRITE GATE is negated. Assert TAG2 at least 20 microseconds before the beginning of the sector to be read or written to.

4.7.6 TAG3

This is an enable signal. When TAG3 is asserted, the BIT lines control operations in a selected drive. The combinations are shown in Table 3-2 above, and described below.

(1) WRITE GATE = BIT0

WRITE GATE causes the serialized data on the WRITE DATA line to be written to the disk (see Figure 4-9). If BIT5 is asserted at the same time, however, an address mark (AM) is written instead (see AM ENABLE in paragraph (6) below). If any BIT other than BIT5 is asserted with WRITE GATE, the result is undefined.

The following timing restrictions apply to WRITE GATE (see also Figures 4-10 and 4-11):

- During successive writes, as when formatting, WRITE GATE must be negated at least one microsecond between assertions.

- When writing after reading, WRITE GATE must not be asserted for at least 300 ns after READ GATE is negated.

- FAULT is asserted and prevents writing if WRITE GATE is asserted when UNIT READY, ON CYLINDER, SEEK END, or WRITE ENABLE is negated, or when SEEK ERROR, WRITE PROTECTED, SERVO OFFSET PLUS, SERVO OFFSET MINUS, or READ GATE is asserted.

- After WRITE GATE is negated, READ GATE must not be asserted for at least 20 microseconds. Do not assert TAG1, TAG2, or RTZ for at least one microsecond.

- After the desired data is written to the disk, one byte of dummy data must be written.

- The write driver turn-on time is approximately one byte. Account for this time when establishing the locations of splice areas.

Note: It is likely that the entire sector being written when FAULT is asserted will be invalid. The data will be lost, and must be rewritten.

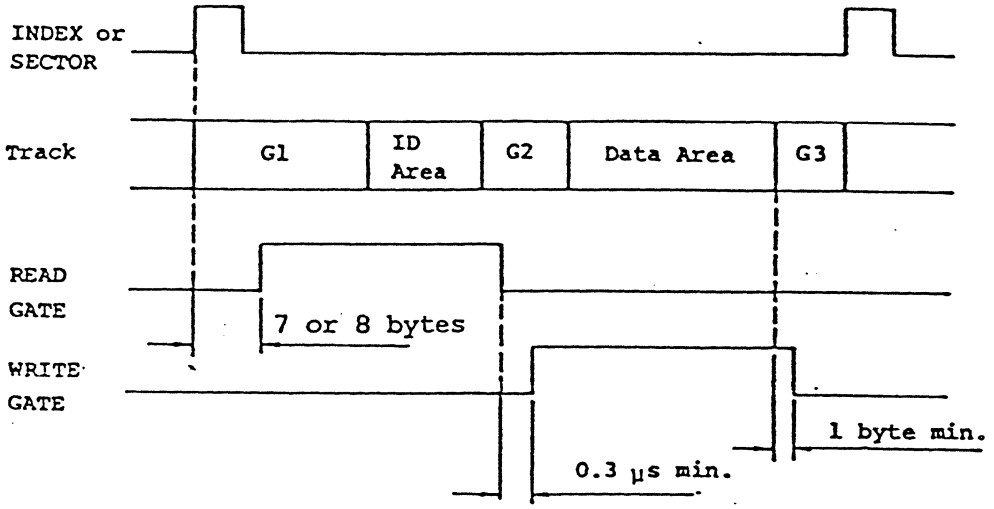
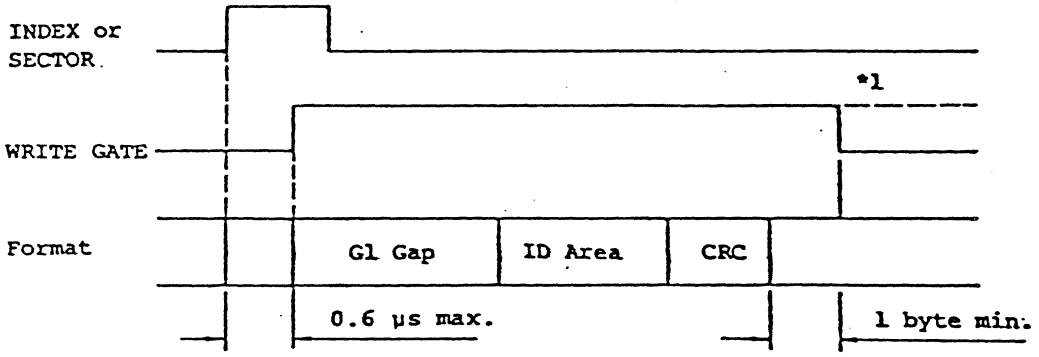


Figure 4-9 WRITE GATE Timing When Writing Data



*1. WRITE GATE may remain active for the portion indicated by "-----."

Figure 4-10 WRITE GATE Timing When Formatting

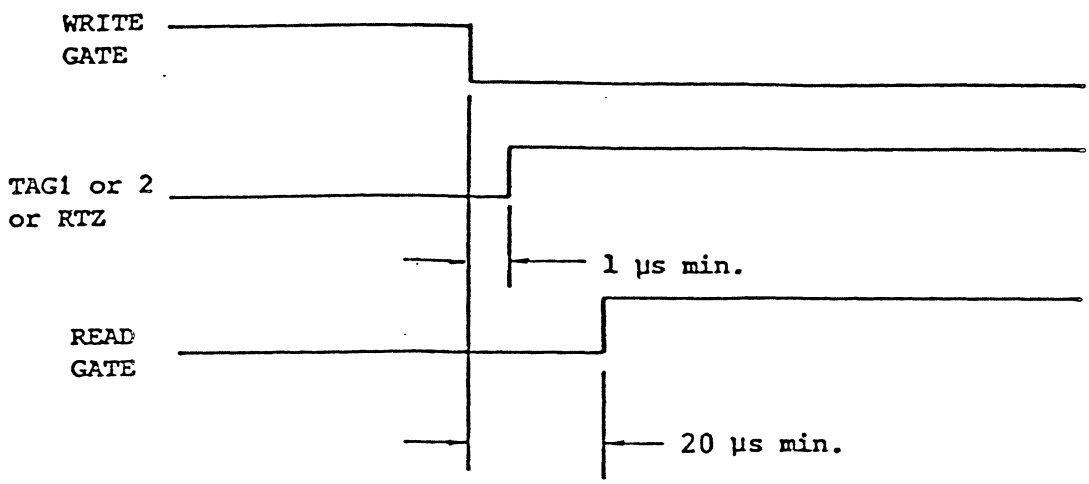


Figure 4-11 WRITE GATE Timing with TAG1, TAG2, RTZ, and READ GATE

(2) READ GATE = BIT1

READ GATE enables the read circuitry that decodes the serialized data written on the disk. The data is converted to NRZ format and transferred to the READ DATA line, which carries it to the controller.

If BIT5 is asserted at the same time as READ GATE, then AM ENABLE is true, and the drive searches the selected track for an address mark.

The following timing restrictions apply to READ GATE (see also Figures 4-8 and 4-12):

- ⚠ The characteristics of the drive circuit require a delay when changing heads. Data can be read without error with the new head 20 microseconds after the deselection of the other head: 5 microseconds to change the head, 15 microseconds to stabilize the read amplifier. READ GATE must not be asserted for 20 microseconds after the trailing edge of TAG2. Ignore the data for about 4 bytes after READ GATE is asserted.

- READ GATE must not be asserted for 20 microseconds after WRITE GATE is negated.

- READ GATE must be dropped prior to the write splice. Reassert READ GATE at least one bits after the write splice, with at least 10 bytes of zeros remaining of the 11 bytes of PLO SYNC.

While READ GATE is asserted, certain other BIT lines may be asserted: BIT5 (making AM ENABLE true), and either SERVO OFFSET PLUS or SERVO OFFSET MINUS. All other combinations are undefined.

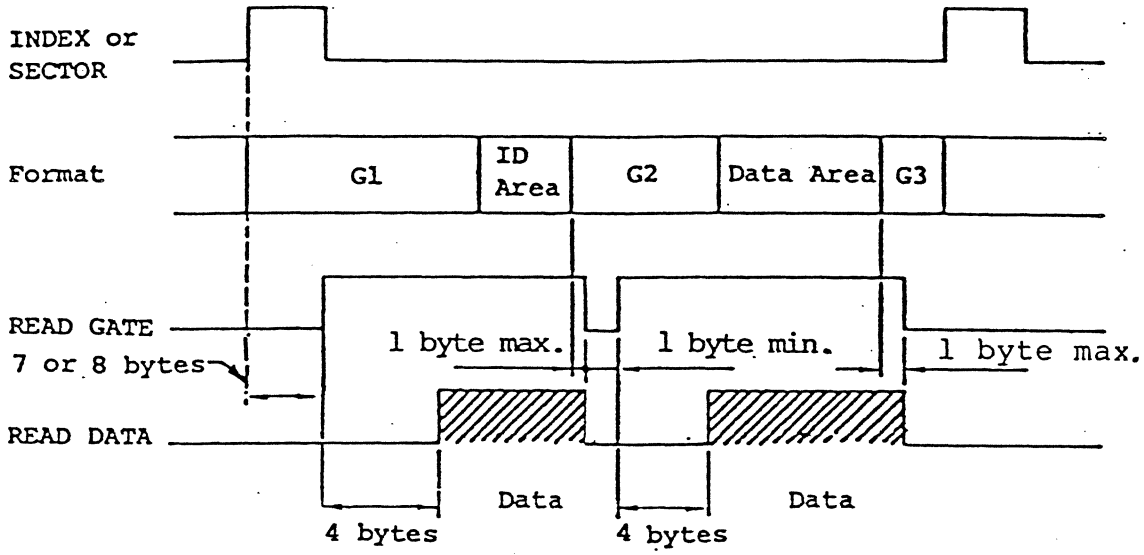


Figure 4-12 READ DATA Timing

(3) SERVO OFFSET PLUS = BIT2

This signal offsets the head by a fixed value toward the spindle if the head is located on an over cylinder, and offsets the head by a fixed value toward the outer edge of the disk if on an odd cylinder.

(4) SERVO OFFSET MINUS = BIT3

This signal offsets the head by a fixed value toward the outer edge of the disk if the head is located on an even cylinder, and offsets the head by a fixed value toward the spindle if on an add cylinder. Figure 4-13 shows SERVO OFFSET PLUS and SERVO OFFSET MINUS timing.

SERVO OFFSET PLUS and SERVO OFFSET MINUS are used when hard errors occur in reading data, i.e., errors that continue even on retries. If the errors are due to head misalignment, one of these signals may recover the data. The misalignment may be due to a temperature difference between the time of writing and reading, or other mechanical changes. Try both signals, if necessary; they will be most effective if the disk is formatted at normal temperatures.

SERVO OFFSET signals must not be asserted during a write; doing so causes FAULT to be asserted, and disables the write by negating WRITE GATE.

ON CYLINDER and SEEK END are negated by the leading edge of either OFFSET signal; they stay negated while the head seeks to its new position.

While either OFFSET signal is asserted, any combination of READ GATE, AM ENABLE and FAULT CLEAR may also be asserted. If any other BIT signals are asserted, the result is undefined.

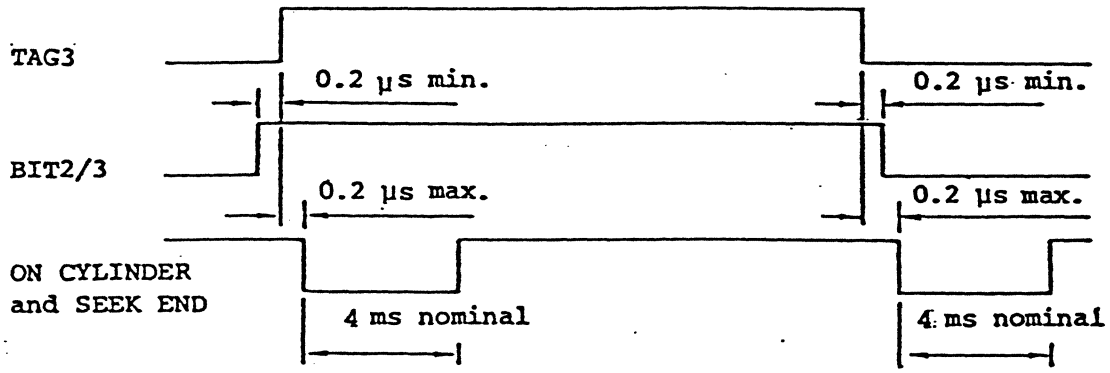


Figure 4-13 SERVO OFFSET PLUS and SERVO OFFSET MINUS Timing

(5) FAULT CLEAR = BIT4

This signal negates FAULT, providing that the fault condition no longer exists. RTZ may be asserted with FAULT CLEAR. Figure 4-14 shows FAULT CLEAR timing.

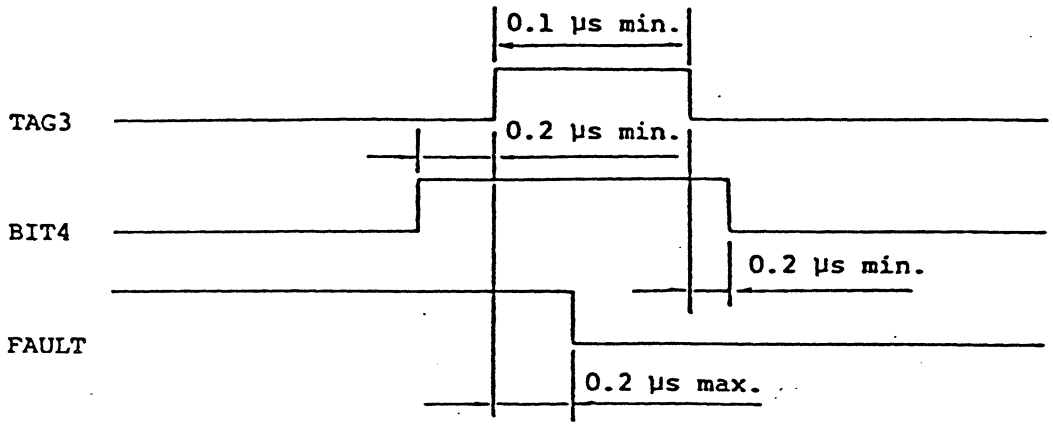


Figure 4-14 FAULT CLEAR Timing

(6) AM ENABLE = BIT5

The AM ENABLE command is used only with variable sector formats; it allows the controller to write and to find record boundaries on the disk. When AM ENABLE is asserted with WRITE GATE, the drive erases the data, thereby writing an address mark (AM). When AM ENABLE is asserted with READ GATE, the drive searches for three bytes of DC-erased data; when found, it asserts ADDRESS MARK FOUND. Figure 4-15 shows ADDRESS MARK timing.

Either OFFSET signal may be asserted while AM ENABLE is asserted; if other BIT signals are asserted, the result is undefined.

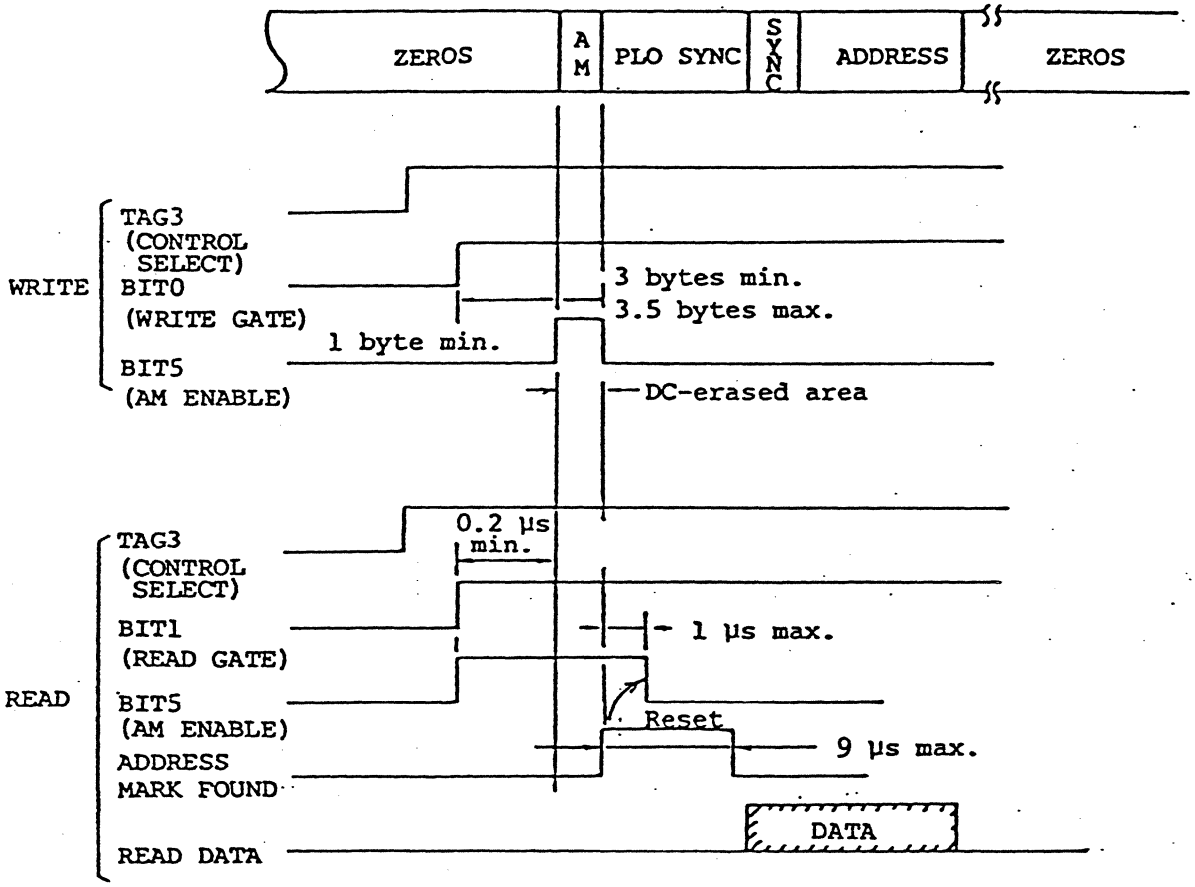


Figure 4-15 ADDRESS MARK Timing

(7) RTZ = BIT6

RTZ causes the drive to seek to track 0, select head 0, and reset SEEK ERROR. This requires about 0.5 seconds, much longer than a normal seek to track 0. RTZ should only be used to recalibrate the head positioner, as when a seek error occurs or an invalid ID sector is read. Figure 4-16 shows RTZ timing.

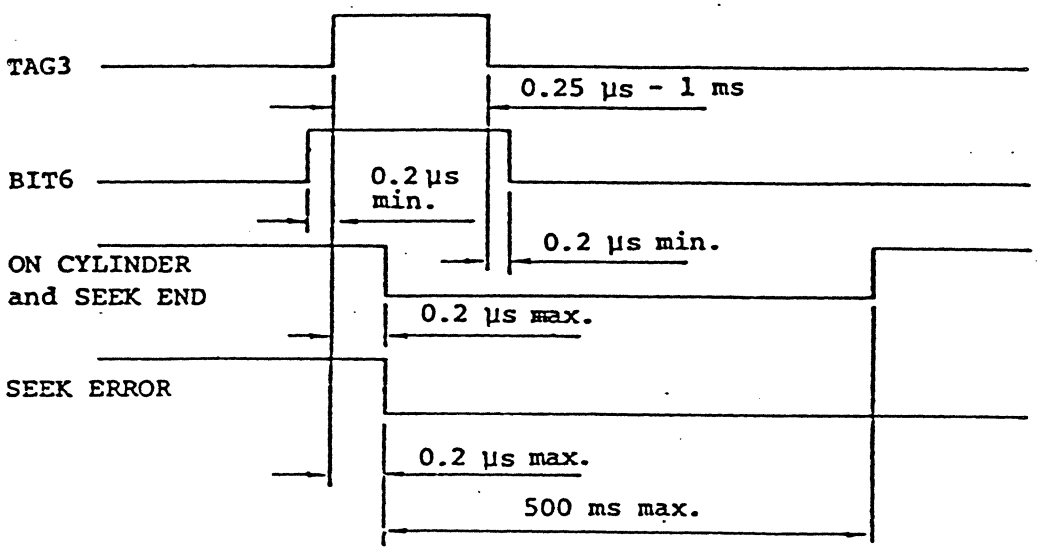


Figure 4-16 RTZ Timing

(8) RELEASE = BIT9

RELEASE is used only with the Dual Port Option.

4.7.7 INDEX

Assertion of this signal indicates that the reference point or index is passing under the heads. The pulse lasts 2.5 ±0.3 microseconds, and occurs once per disk revolution. Its leading edge is the leading edge of sector 0. To maintain timing integrity, INDEX is also asserted during a seek.

4.7.8 SECTOR

SECTOR is a one-byte pulse that marks the beginning of each sector except sector 0 (which is marked by INDEX). SECTOR is derived from INDEX and from the servo clock.

Each track is divided into 1-128 sectors, set by jumper plugs on the DK512S PC assembly.

Figure 4-17 shows both INDEX and SECTOR timing.

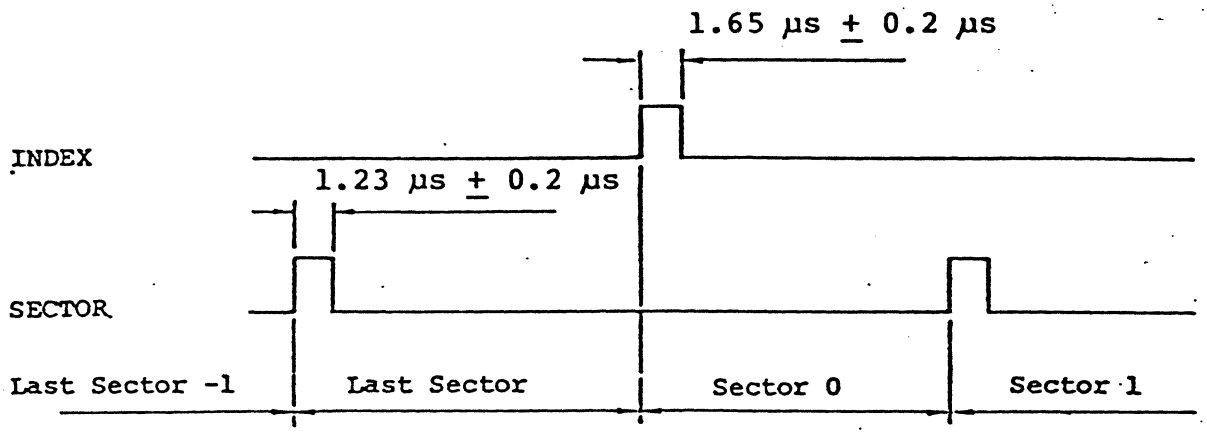


Figure 4-17 INDEX and SECTOR Timing

4.7.9 TAG4 and TAG5: Modes A, B, C

These signals are used in three different ways in the DK814S, depending on how the jumper plugs on the DK814S PC assembly are set. Table 3-3 above shows the signals available for each mode. The modes are described below, followed by descriptions of the signals. The extra signals are made available by using combinations of TAG4 and TAG5.

Mode A is compatible with the SMD standard and with many existing systems:

- Cable A pins 27 and 57 are used for UNIT SELECT 2^3, not TAG5. TAG4 is not used in the drive.
- Standard SMD status signals are provided by the drive.
- Sixteen drives may be addressed.

Mode B provides additional capability:

- Cable A pins 27 and 57 are used for UNIT SELECT 2^3, not TAG5. Pins 30 and 60 are used for the DK814S signal TAG4.
- When TAG4 is FALSE, the drive reports the standard SMD status signals.
- When TAG4 is TRUE, the six status lines report 2^6 (i.e., 64) different sector addresses as they pass under the head.
- Sixteen drives may be addressed.

Mode C adds additional error reporting capability, but with fewer drives:

- Cable A pins 27 and 57 are used for TAG5, not UNIT SELECT 2^3. Pins 30 and 60 are used for TAG4.
- When TAG4 and TAG5 are FALSE, the drive reports the standard SMD status signals.
- When TAG4 is FALSE and TAG5 is TRUE, the six status lines report six different error conditions.
- When TAG4 is TRUE and TAG5 is FALSE, the six status lines report 2^6 (i.e., 64) different sector addresses as they pass under the head.
- When TAG4 and TAG5 are both TRUE, the six status lines report the DEVICE TYPE.
- Eight drives may be addressed.

(1) UNIT READY (STATUS0) (Modes A, B, C)

When asserted, this status signal indicates that the drive is up to speed and ready to accept commands, that the head is positioned on a track after an initial seek, and that no fault exists.

The controller must continuously check this signal. When it is negated, the drive must not be commanded to seek, write, or read. Typically, UNIT READY recovers (is asserted) without intervention; the recalibration sequence should be executed at this time.

(2) ON CYLINDER (STATUS1) (Modes A, B, C)

When asserted, this status indicates that the heads are positioned on a cylinder. ON CYLINDER is negated within 200 ns by the trailing edge of TAG1, or by the leading edge of RTZ, or by the leading edge of either OFFSET. It remains negated during the seek, which takes:

- 45 ms (max.) for a typical seek to another track;
- 100 microseconds (max.) for a seek on the same track;
- 500 ms (max.) for an RTZ;
- 4 ms (nominal) for an offset seek.

(3) SEEK ERROR (STATUS2) (Modes A, B, C)

When asserted, this signal indicates that the drive is unable to complete a seek or to recalibrate within 500 ms, or that the heads have moved outside the recording boundaries to a guard band during a seek, or that an illegal cylinder address has been requested. SEEK ERROR is asserted within 100 microseconds of the trailing edge of TAG1 if a cylinder number is requested that is higher than the drive's specification. After the error condition has been corrected, SEEK ERROR may be reset by RTZ.

(4) FAULT (STATUS3) (Modes A, B, C)

When FAULT is asserted, one of the following errors has occurred: STATUS ERROR 1 or 2; WRITE ERROR 1, 2, or 3; SELECT ERROR. To prevent data loss, FAULT immediately inhibits WRITE GATE.

FAULT is latched in the drive. It is reset (negated) by FAULT CLEAR, RTZ, or power off/on, provided no fault remains.

(5) WRITE PROTECTED (STATUS4) (Modes A, B, C)

This status signal is continuously asserted if the drive is protected, i.e., read-only. A jumper plug on the DK814S PC assembly sets the drive either to read-only, or always read/write, or to respond to the WR ENABLE signal. Asserting WRITE GATE when WRITE PROTECTED is asserted causes FAULT to be asserted.

(6) ADDRESS MARK FOUND (STATUS5) (Modes A, B, C)

This status signal is used only with variable formats. The drive is instructed to search for a previously written address mark by asserting READ GATE and AM ENABLE. ADDRESS MARK FOUND is a pulse (9µs max pulse width) sent to the controller when the address mark is found on the specified track. The address mark is a 3-byte DC-erased area.

(7) SECTOR ADDRESS (Modes B, C)

SECTOR ADDRESS 1, 2, 4, 8, 16, 32 are status signals sourced at the drive, and are used in the fixed sector mode when the number of sectors per track is less than 64. The necessary TAG4 and TAG5 conditions to use these signals are shown in Table 3-4. SECTOR ADDRESS signals are negated by the leading edge of INDEX, then strobed by the leading edge of SECTOR to indicate the current sector address under the head.

(8) DEVICE TYPE (Mode C)

DEVICE TYPE 1, 2, 4, 8, 16, 32 are signals sourced at the drive, and are useful if different DK512S models are used in the same system. They allow the host to identify which model has been addressed. Table 3-5 gives the codes, which are set by jumper plugs on the DK512S PC assembly.

(9) STATUS ERROR 1 (STATUS0) (Mode C)

This status signal is asserted by the drive if it is commanded to read, write, or seek while UNIT READY is negated.

(10) STATUS ERROR 2 (STATUS1) (Mode C)

This status signal is asserted by the drive if it is commanded to read and write simultaneously, or if it is commanded to write during a seek.

(11) WRITE ERROR 1 (STATUS2) (Mode C)

An analog position signal is derived from the servo track and continuously monitored by the drive. WRITE ERROR 1 is asserted if an abnormal position is detected while writing, if INDEX is missed or detected too often, or if there is a ROM or RAM checksum error at initialization.

(12) WRITE ERROR 2 (STATUS3) (Mode C)

This status signal is asserted if the write amplifier cannot invert data bits while WRITE GATE is asserted, if no write current is detected in the head while WRITE GATE is asserted, or if write current is detected in the head while WRITE GATE is negated.

(13) WRITE ERROR 3 (STATUS4) (Mode C)

This status signal is asserted by the drive if it is instructed to write while write-protected. Write protection comes from the WR ENABLE signal and/or the write-protect jumper plugs on the DK512S PC assembly.

(14) SELECT ERROR (STATUS5) (Mode C)

This signal is asserted by the drive if two or more heads are selected simultaneously while READ GATE or WRITE GATE is asserted.

4.7.10 OPEN CABLE DETECTOR

This signal is used to prevent damage to data caused by interface disturbances that occur when controller power is going up or down. Negation of the signal disables the drive's line receivers and drivers: the drive does not respond to UNIT SELECT. During the entire time the controller's power is sequencing (up or down), the signal must be negated. The circuits must be designed so that removal of the cable disables the line receivers.

Note that the drive end is terminated, and is biased to the negated state.

4.7.11 BUSY

This signal is used only with the Dual Port Option.

4.7.12 WR ENABLE

⚠ WR ENABLE is special DK512S signal designed to protect data by write protecting the drive at appropriate times. The best protection is obtained by negating WR ENABLE whenever power is sequencing up or down, and when not writing. Jumper plugs on the DK512S PC assembly determine whether a drive responds to WR ENABLE.

4.8 Data Cable B Signal Descriptions

See Table 3-5 for a list of these signals and their sources.

4.8.1 UNIT SELECTED

This signal is asserted by the drive when it is selected, as described under UNIT SELECT and UNIT SELECT TAG. UNIT SELECTED is asserted within 0.6 microseconds of the leading edge of UNIT SELECT TAG.

4.8.2 SEEK END

This signal is the logical <or> of ON CYLINDER and SEEK ERROR, i.e., SEEK END = ON CYLINDER <or> SEEK ERROR.

4.8.3 SERVO CLOCK

The basic timing signal for the system, SERVO CLOCK is a 9.72 MHz clock, phase locked with the clock signal from the servo tracks on the disk, and available at all times.

4.8.4 WRITE CLOCK

WRITE CLOCK is developed in the controller by regenerating the drive's SERVO CLOCK. It must be synchronized to the NRZ write data since it is used by the drive to strobe the WRITE DATA line. It must be transmitted to the drive at least 250 ns prior to WRITE GATE.

4.8.5 WRITE DATA

This is the data transmitted to the drive for recording on the disk. Drive circuits convert it from NRZ format and write it on the disk in RLL 2-7 format. Figure 4-18 shows WRITE DATA and clock timing.

4.8.6 READ CLOCK

READ CLOCK is sourced at the drive, and is transmitted continuously. While READ GATE is negated, READ CLOCK is the SERVO CLOCK; when READ GATE is asserted, a variable frequency oscillator synchronizes READ CLOCK with the read data within 4 bytes. READ CLOCK is used by the controller to strobe the READ DATA.

4.8.7 READ DATA

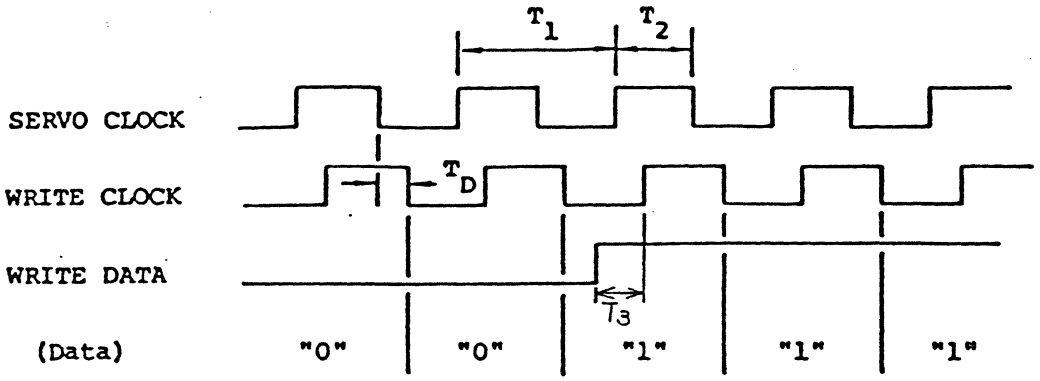
READ DATA is NRZ format data read from the disk and transmitted to the controller. It is synchronized with READ CLOCK. The data must be ignored for 4 bytes after READ GATE is asserted, the period required for READ CLOCK to synchronize. Figure 4-19 shows READ DATA and clock timing.

4.8.8 RPS INDEX

The RPS INDEX and RPS SECTOR signals on data cable B are identical to INDEX and SECTOR on control cable A, except that they are continuously available. (RPS means Rotational Position Sensing.)

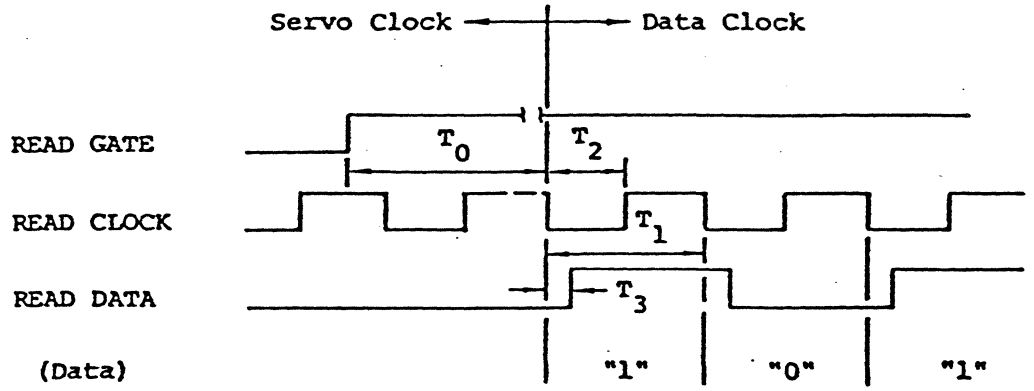
4.8.9 RPS SECTOR

See Subsection 4.8.8 above.



T_1 = 102.8 ns ± 8 ns
T_2 = (T_1/2) ± 10 ns
T_3 = $T_{1/2}$ ± 20 ns
$T_D \leq 2T_1$
T_4 = 102.8 ns ± 8 ns

Figure 4-18 WRITE DATA and Clock Timing



T_0 = Approx. 4 bytes
T_1 = 102.8 ns ± 10 ns
T_2 = T_1/2 ± 10 ns
T_3 = 0 ± 15 ns

Figure 4-19 READ DATA and Clock Timing

5. FORMATS

This chapter provides recommended track formats to be used when integrating the DK512S into a system. The DK512S is designed to use either a fixed sector or a variable sector format, and the drive may be jumpered for different numbers of bytes per sector, in 1-byte increments. Areas that must be set aside for write splices and synchronization are kept to a minimum, allowing the format to be adapted to a variety of special requirements.

There are 20,944 bytes per track. Suitable polynomials are given for these codes in Subsections 5.3.6 and 5.3.7.

5.1 Fixed Sector Format

Figure 5-1 shows a sample fixed sector format. Note the minimum number of synchronization bytes stated in the figure. They are required to synchronize the phase locked oscillator (PLO) with the data. The overhead (non-data bytes) shown in Figure 5-1 is 64 sectors per track. Given the desired data-bytes/ sector, the following calculation can be made:

$$\text{Number of sectors} = \frac{\text{Total bytes/track}}{\text{Total bytes/sector}} = \frac{20,944}{\text{Total bytes/sector}}$$

For example, 256 data-bytes/sector requires

$$\frac{20,944}{256+71} = 64 \text{ sectors/track} \quad \text{(truncate the remainder)}$$

and add one to the integer portion of "mumber of bytes per sector".

The efficiency of the scheme is $\frac{256 \times 64}{20,944} = 78.2\%$.

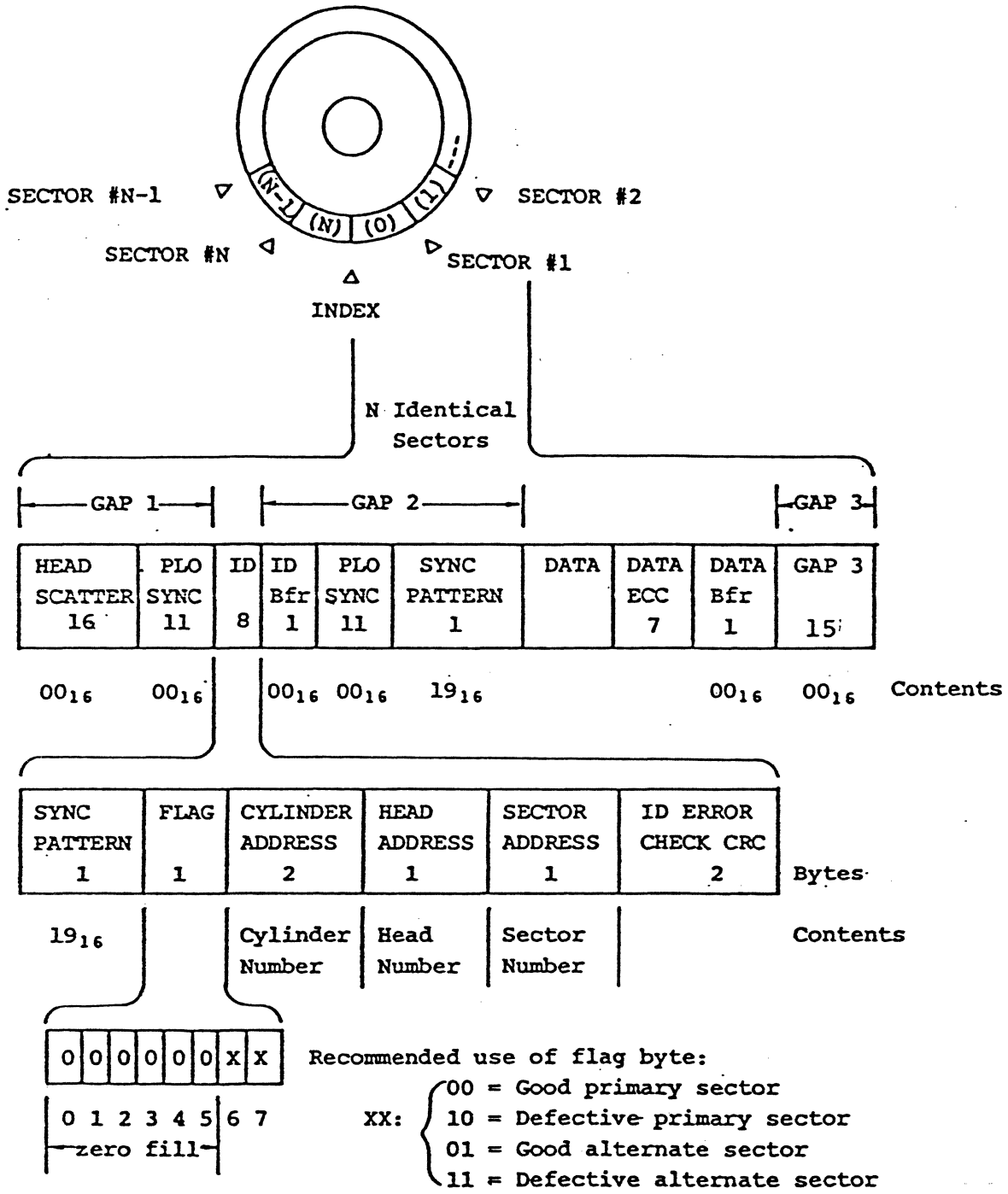


Figure 5-1 Fixed Sector Format (All Sectors Identical)

5.2 Variable Sector Format

An ADDRESS MARK identifies the beginning of each variable sector, and adds about 3 bytes to each sector. However, the HEAD SCATTER and GAP3 fields are required only once per track, so this format results in higher efficiency than fixed sector formats, in addition to allowing for variable length data fields.

Figure 5-2 gives a sample format. The minimum synchronization byte lengths stated in the figure must be observed. The data field size and the efficiency are calculated as follows:

$$\text{Data field} = \frac{\text{Total bytes/track-index loss}}{\text{Number of sectors/track}} - \text{(Non-data bytes)}$$

Example 1: Given 64 sectors/track:

$$\text{Data field} = \frac{20{,}944 - 31}{64} - 44 = 282 \text{ bytes}$$

$$\text{Track efficiency} = \frac{282 \times 64}{20{,}944} = 86.1\%$$

Example 2: Given 256 bytes/sector:

$$\text{Number of sectors} = \frac{20{,}944 - 31}{256 + 44} = 69 \text{ sectors/track}$$

$$\text{Track efficiency} = \frac{256 \times 69}{20{,}944} = 84.3\%$$

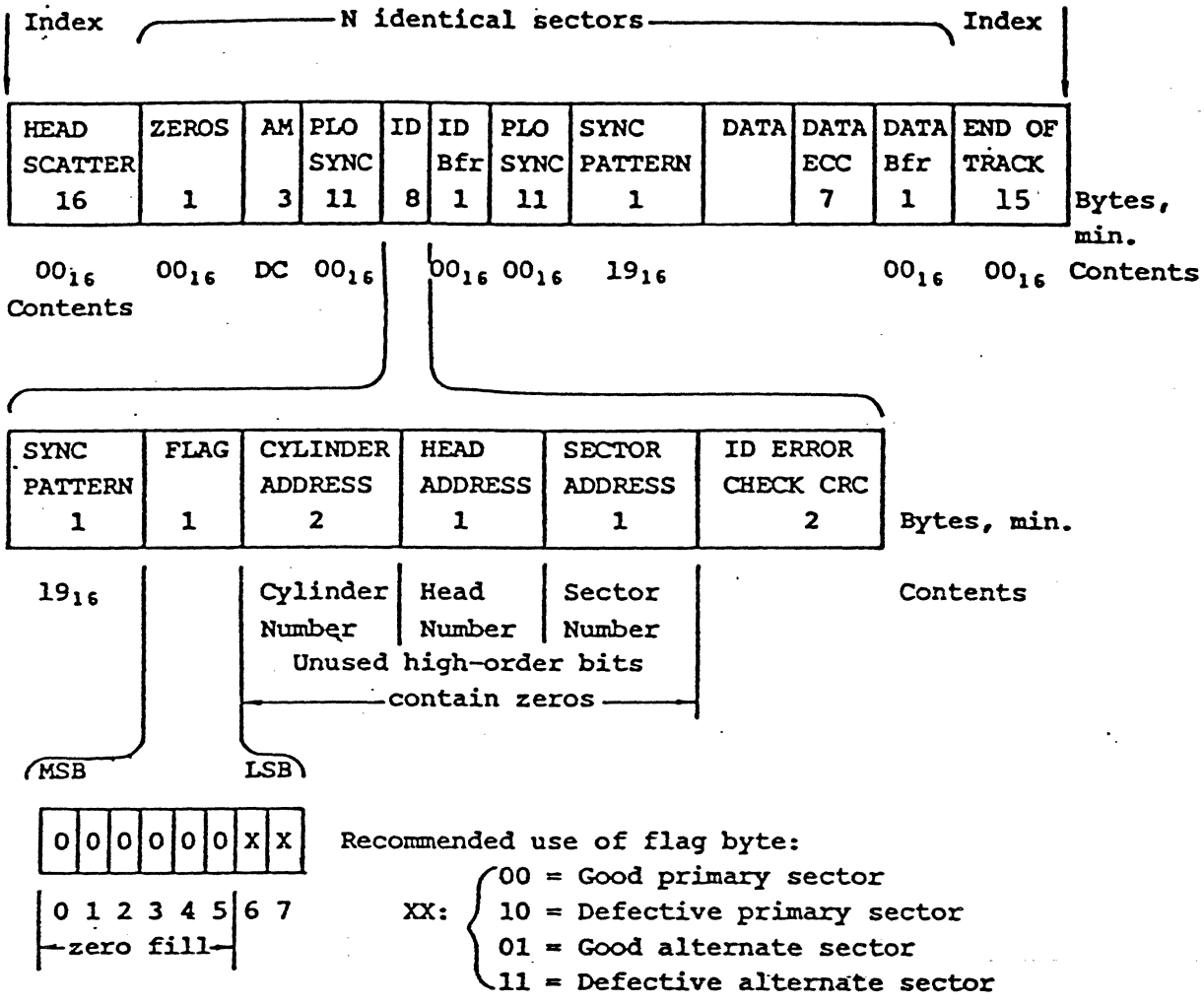


Figure 5-2 Variable Sector Format

5.3 Track Field Descriptions

The following provides additional information on the field lengths and field contents defined in Figures 5-1 and 5-2.

5.3.1 HEAD SCATTER

This field provides a start-of-record tolerance, allowing for mechanical and electrical variations. It is also used for the write splice, the point on the track where the drive changes from write to read.

5.3.2 ID Bfr (ID Buffer)

This field is the buffer for the ID area. There must be at least one byte of ID Bfr following the ID ERROR CHECK CRC.

5.3.3 PLO SYNC

In this field, read data is synchronized with the phase locked oscillator.

If the ID field has a media defect, it is recommended that 64 bytes or 00_{16} be added to the PLO SYNC field, and that the physical (primary) sector be abandoned. The logical (alternate) sector may be on one of the reserved tracks. The controller must keep track of the relationship between physical and logical addresses.

5.3.4 SYNC PATTERN

The field is filled with 1 bits to mark the beginning of an address or data area.

5.3.5 FLAG

The FLAG byte indicates whether the primary and alternate sectors are good or have media defects. This information may be used by the controller.

5.3.6 ID ERROR CHECK CRC Polynomial (2 bytes)

$X^{16} + X^{12} + X^5 + 1$, where the initial value is 00.

5.3.7 DATA ECC Polynomial (7 bytes)

$(X^{22} + 1)$ $(X^{11} + X^9 + X^7 + X^6 + X^5 + X + 1)$ $(X^{12} + X^{11} + X^{10} + X^9 + X^8 + X^7 + X^6 + X^5 + X^4 + X^3 + X^2 + X + 1)$ $(X^{11} + X^7 + X^6 + X + 1)$

5.3.8 DATA Bfr and GAP3

DATA Bfr is the buffer for the data area. There must be at least one byte of DATA Bfr following the DATA ECC. GAP3 must be a minimum of 15 bytes.

5.4 Bytes/Sector and Sectors/Track Selection

Selection is made with 14 jumper plugs on the DK512S PC assembly. Each plug represents a power of 2, from 2^0 (or 1) to 2^{13} (or 8192) bytes/sector, representing 1-byte increments. The Service Manual has detailed instructions.

The number of sectors is determined in either of the following ways:

(a) Given the number of bytes/sector:

Example: 579 bytes/sector are required:

$$\text{Number of sectors} = \frac{\text{Total bytes/track}}{\text{bytes/sector}} = \frac{20{,}944}{579}$$

$$= 36 \text{ sectors/track},$$

Each track will consist of 36 sectors of 579 bytes each and an additional sector of 100 bytes.

Install the following plugs:

SEC SW2^9		SEC SW2^6		SE SW2^1	
512	+	64	+	2	= 578

An extra count is added when the byte counter resets, giving the required 579 bytes/sector.

(b) Given the number of sectors/track:

Example: 32 sectors/track are required:

$$\text{Bytes/sector} = \frac{\text{Total bytes/track}}{\text{sectors/track}} = \frac{20{,}944}{32}$$

$$= 654 \text{ bytes}$$

Install the following plugs:

$$\underset{512}{\text{SEC SW2}^9} + \underset{128}{\text{SEC SW2}^7} + \underset{8}{\text{SEC SW2}^3} + \underset{4}{\text{SEC SW2}^2} + \underset{1}{\text{SEC SW2}^0} = 653$$

An extra count is added when the byte counter resets, giving the required 654 bytes/sector.

5.5 Media Defects and Logging

This section defines defects precisely, and gives the factory formats used to record them. Table 2-1 shows the allowable number of defects for each model.

Media defects are logged at the factory during a lengthy test which includes operation at low and high temperatures, low and high voltages, and worst-case seek algorithms. Media defect lengths and positions are written on the disk in a format that can be read with either fixed sector or variable sector controllers. In addition, a flaw map is included on the test data sheet shipped with each drive. For each defect, the flaw map lists the cylinder number, head number, number of bytes from index, and bit length.

5.5.1 Factory Standard External Format

To be provided later.

5.5.2 Defect Definitions

To be provided later.

5.6 Formatting Procedure

The following procedure is suggested for fixed sector formats:

1. Select the desired drive, cylinder, head, and sector.

2. Introduce a 5-microsecond delay between asserting TAG2 (HEAD SET) and the start of the search for the leading edge of SECTOR, so the drive can begin writing as soon as SECTOR is found.

3. Search for the leading edge of SECTOR.

4. When the leading edge of SECTOR is found, assert WRITE GATE and start writing zeros.

5. Write 27 bytes of zeros for the HEAD SCATTER and PLO SYNC fields.

6. Write a SYNC PATTERN (19_{16}), the cylinder, head, and sector addresses, and the ID ERROR CHECK CRC.

7. Write zeros for the ID Bfr and the PLO SYNC fields.

8. Write a SYNC PATTERN, a worst case DATA field, the DATA ECC, and a 1-byte DATA Buffer.

9. To format the next sector with the same head, write zeros in GAP3 to the next SECTOR pulse, and leave WRITE GATE asserted.

10. If WRITE GATE is negated, do not assert it again for one microsecond.

5-10 5.7 Data Control Timing

(a) Read Initialization Time

To initiate a read operation with a new head, a 20-microsecond delay is required: 5 microseconds for head change, 15 microseconds to stabilize the read amplifier.

(b) Write-to-Read Recovery Time

The transition from inactivating WRITE GATE to activating READ GATE requires at least 20 microseconds.

(c) Read-to-Write Recovery Time

The transition from inactivating READ GATE to activating WRITE GATE requires at least 0.5 microseconds.

(d) Write Gate Off Time

The controller must send at least one byte of dummy data following a correct write data(ID or DATA CHECH BYTE) before inactivating WRITE GATE.

(e) Write Driver Turn On Time

The write driver requires 0.8 microseconds or one-byte time to become enabled. The period is provided as a write splice.

6. HANDLING AND SHIPPING

6.1 Receiving

When shipped from the factory, the DK512S is double-packed in inner and outer cartons made of strong, two-ply corrugated cardboard. The drives and their inner cartons are cushioned on all sides by approximately two and one-half inches of urethane foam. This careful packaging protects the drive against shocks and vibrations during shipping.

Keep the original cartons for shipping individual drives that are not mounted in a cabinet. For storage, seal the drive in a heavy plastic bag with a desiccant, and keep it in the inner carton.

When a drive is brought from a cold warehouse or truck into a warmer area, let it warm up slowly so that water vapor does not condense in the HDA. Open the outer carton and remove it. Leave the drive in the inner carton for the length of time shown below so it can warm up to typical room temperature (to 77°F with 50% relative humidity).

Warehouse temperature	+32°F	+14°F	-4°F
Warm-up time	6 hrs	9 hrs	11 hrs

7.2 Handling

Before removing a drive from its inner carton or from its shock-resistant mounting, prepare a cushioned area to set the drive on. Use two or three inches of urethane foam covered with cardboard, such as the top cushion of the inner carton. This is especially important if the drive will be moved around on a cart. Lift the drive by both ends, and set it gently on the cushion.

Keep each test data report with its own drive, and make sure the serial number on the report matches the nameplate on the drive. Do not separate PC boards from their drives -- the factory has installed the correct assemblies for each model.

Before testing a drive, changing any jumper plugs, or formatting, make a back-up copy of the track defect data which has been written by the factory on each surface. When the data has been backed up, the jumper plugs may be reset, as described in the Service Manual.

6.3 Shipping

Drives can be shipped in the cabinets if the drives are securely installed on their shock-absorbing mounts. If cabinets with the drives mounted will be shipped by motor freight, the cabinets should be carefully packed in cushioned packages. Drives can also be shipped separately if they are packed in their original shipping cartons.

The following procedures should be taken:

1. Clean the drive.

2. Seal the drive in a heavy plastic bag with a desiccant, otherwise water vapor might condense.

3. Double pack the drive in the original inner and outer cartons, or equivalent ones that can protect the drive from shocks of 5G or more during shipment.

4. Put a "This Side Up" mark and a "Handle with Care" indication on the outer carton surfaces.

7.4 Cautions

- Do not apply any force to the plug-in parts during packing, unpacking, or shipping.

- Take care not to vibrate or shock the drive while handling it.

7. Connector for an External Control Panel

(1) The SZ144 PCB allows for connection of external control panel. At the edge of this PCB, there is a 16 pin connector.

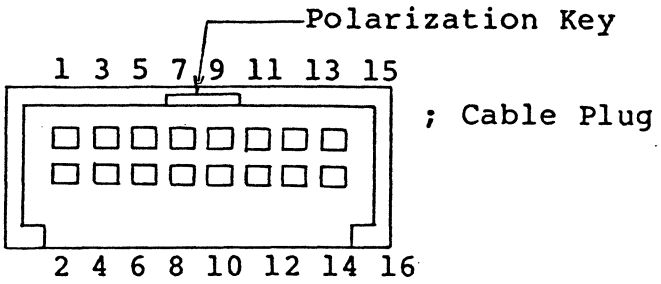


Figure 7-1 External Control Panel Connector

Table 7-1 Pinout for External Control Panel Connector

Pin. No.	Signal Name	Pin. No.	Signal Name
1	+5V	2	+5V
3	WPTK-N	4	GND
5	CLRFLT-N	6	GND
7	RDYL-N	8	FLTL-N
9	GND	10	WPTL-N
11	USLDL-N	12	PWRLDY-N
13	GND	14	GND
15	NOT USED	16	NOT USED

WPTK-N

- This switch signal inhibites the write operation.

- CLRELT-N
  This switch signal resets a Fault Status.

- PWRLDY-N
  This signal for LED is active when the power is turned on.

- RDYL-N
  This signal for LED is active when the drive is in Ready condition.

- FLTL-N
  This signal for LED is active when the drive is in Fault condition.

- WPTL-N
  This signal for LED is active when writing is inhibited.

- USLDL-N
  This signal for LED is active when the drive is selected.

(2) Connector Specification

Table 7-2 Lists connector specification for a cable plug.

Table 7-2 Connector Specification

Item	Mfr.	Manufacturer's Part. Number	Q'ty
Socket Housing (Double Row 16 pin)	AMP	280366	1
Socket Contact	AMP	181271-2	16

(3) Cable Specification

Table 7-3 Cable Specification

Item	Spec.
Cable for External control panel signal	AWG #32～28. (External dia, 1.64～1.22mm)

(4) Operator Circuit

Figure 7-2 Shows a circuit is simplifed form.

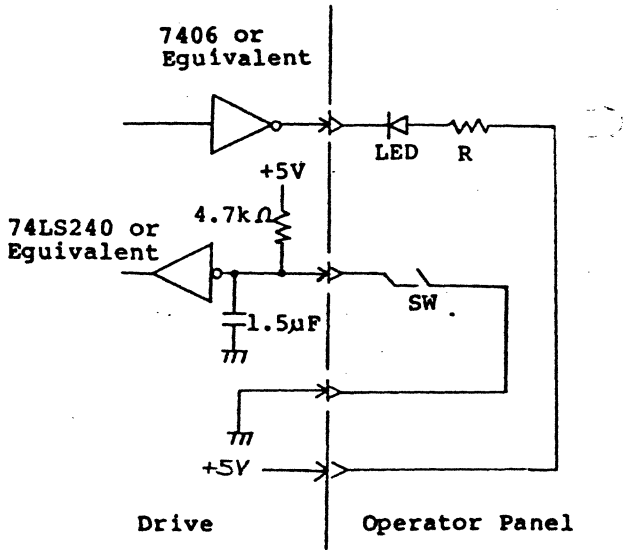


Figure 7-2 Operater Panel Circuit